Features

- **Voice Recorder/Player on a Chip**
- **On-board Flash Memory**
- **Low Voltage and Low Power Operation**
  - **2.4V to 3.3V**
  - **10 mA Active I_{CC} Current**
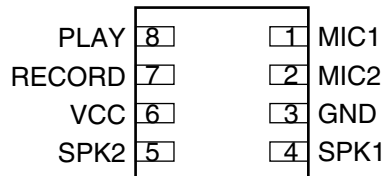 - **0.1 µA Standby I_{CC} Current**

Description

The AT72AV010 is a single-chip voice recorder/player with on-board nonvolatile memory. Output from a microphone is processed on-chip and stored in digital form in memory. Data from the memory is then processed and presented to a speaker for playback. Up to 20 seconds of voice can be stored in the 1-Mbit Flash memory at the nominal sampling frequency of 6.4 kHz. The device is available in a space saving 8-lead Leadless Array Package (LAP).

Pin Configuration

Pin Name	Function
MIC1	Microphone Inputs
MIC2	
GND	Ground
VCC	Power Supply
SPK1	Speaker Outputs
SPK2	
PLAY	Control Inputs
RECORD	

**8-lead Leadless Array
Bottom View**

PLAY	8		1	MIC1
RECORD	7		2	MIC2
VCC	6		3	GND
SPK2	5		4	SPK1

**Voice
Recorder/Player
IC**

AT72AV010

**Preliminary
Information**

Block Diagram

VCC
GND

Flash Memory

PLAY
RECORD

User Interface

Controller

System Clock

PWUP

CODEC

MIC1
MIC2

PREAMP

AAF

LPF

INTP

PWR AMP
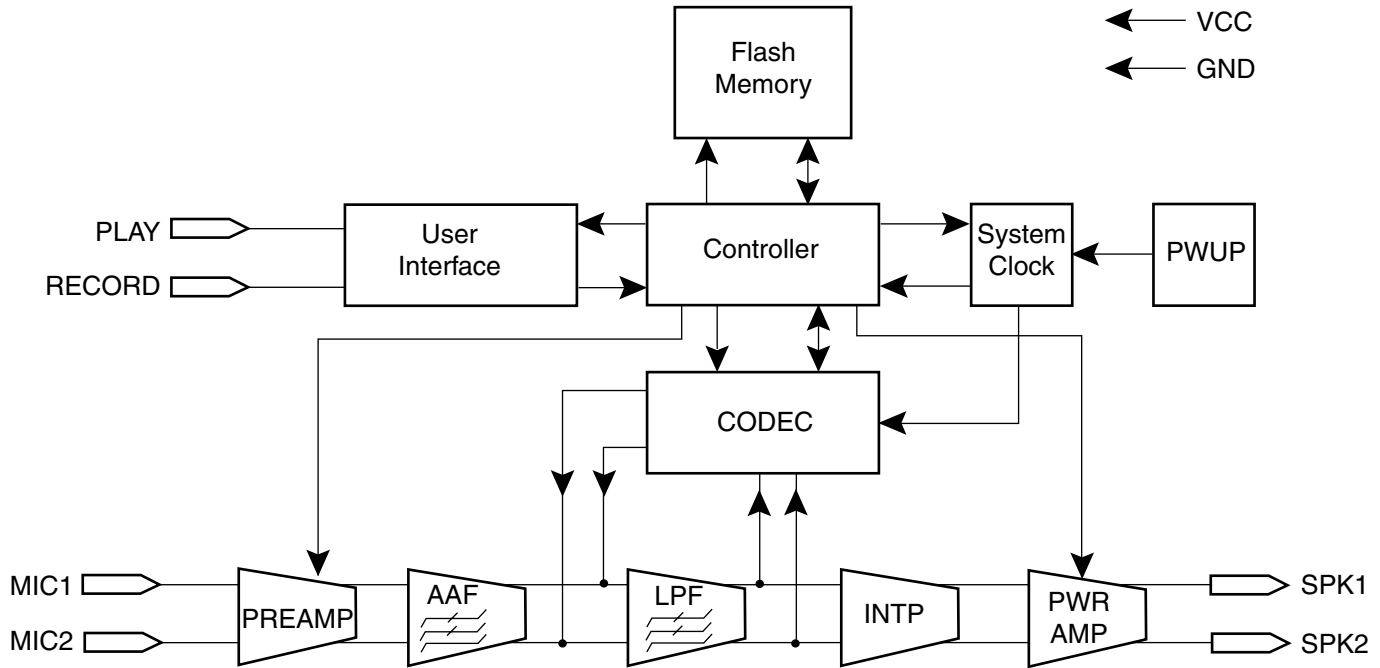
SPK1
SPK2

Device Operation

After connecting a microphone to the MIC1 and MIC2 inputs and a speaker to the SPK1 and SPK2 outputs, operation of the voice recorder is controlled by the PLAY and RECORD inputs.

With both PLAY and RECORD low, the AT72AV010 is in standby mode. Both control pins have on-chip pull-downs; i.e., they are normally low, unless pulled up to V_{CC} by external switches.

Taking PLAY high, while RECORD stays low starts playback. Playback continues either until the end of memory or until encountering empty memory.

A recording session is started by pulsing RECORD high, while PLAY is high. Following the low-to-high transition of RECORD, the entire memory is erased. Completion of the internally timed chip erase operation is signaled to the user by a short beep played through the speaker. Recording starts after the beep and continues until the entire memory is filled or until PLAY is taken low. If end of memory is reached during recording, then the beep is played again; signaling to the user that recording has stopped.

Recording can be initiated either during playback or after playback. Nevertheless, while waiting for a RECORD command, the device will draw more current than in standby and therefore PLAY should be taken low if no recording is imminent; this will save battery life.

To play back a fresh recording, PLAY must first be taken low and then high again.

Both PLAY and RECORD inputs are internally debounced for approximately 80 ms to avoid false command triggering. If RECORD is high while PLAY is low, the AT72AV010 enters a Direct Memory Access (DMA) mode; therefore this condition should be avoided in voice recorder (or player) applications; i.e., RECORD should be pulsed high only while PLAY is high.

Absolute Maximum Ratings*

Operating Temperature...0°C to +70°C

Storage Temperature .... -65°C to +150°C

Voltage on Any Pin
with Respect to Ground ....-1.0V to +4.0V

Maximum Operating Voltage 3.6V

DC Output Current... 50 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Capacitance[1]

Symbol	Parameter	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SPK)	8	pF	$V_{I/O} = V_{CC}/2$
C_{IN}	Input Capacitance (MIC)	6	pF	$V_{I/O} = VG$

Note: 1. This parameter is characterized and is not 100% tested.

DC Characteristics

V_{CC} = 2.4V to 3.3V T_A = 0°C - 70°C unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CC}	Supply Voltage		2.4		3.3	V
I_{REC}	Supply Current	Recording @ V_{CC} = 3.3V			10.0	mA
I_{PLY}	Supply Current	Playing @ V_{CC} = 3.3V (No Load)			10.0	mA
I_S	Standby Current	Play and Record Low		0.1		µA
I_{SINK}	Input Sink	On Play/Record Pins @ V_{CC}		30.0		µA

AC Characteristics

V_{CC} = 2.4V to 3.3V T_A = 0°C - 70°C unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_S	Sampling Frequency[1]		5.8	6.4	7	kHz
BW	Bandwidth[1]	f_S = 6.4			2.7	kHz
$\Delta f_S / f_S$	f_S Stability[1]	V_{CC} = 2.7V ± .3V			± 3	%
R_{MIC}	Input Impedance[2]	to VG		60		kΩ
A_{VREC}	Recording Gain[3]		17.5	28	38.5	dB
A_{VPLY}	Playback Gain[3]		4		7	
V_{OMPP}	Maximum Output Voltage[3]	Matching V_{CC}	3.2		5.6	V_{PP}
I_{OMP}	Maximum Output Current[3]		35	40	45	mA
V_{OS}	Output Offset[4]				100	mV
T_{HD}	Total Harmonic Distortion[5]	@ 1 kHz		1		%

Notes: 1. Sampling frequency is set at the factory to 6.4 kHz. Upper pass band limit tracks the sampling frequency, while the lower limit is determined by the time constant of the microphone connection, typically in the 100 - 200 Hz range.
2. The quiescent level of the MIC inputs is at virtual ground (VG). The VG is a level between GND and V_{CC}. The DC resistance between the MIC input and VG is typically 60 kΩ. The external microphone should be AC-coupled to the MIC input with 0.1 µF ceramic capacitors.
3. Recording gain is factory adjusted. The nominal recording gain is 28 dB, i.e., an Input signal of 32 mV_{PP} is amplified to the internal full scale voltage of 800 mV_{PP}. The gain can be adjusted up or down in steps of 1.5 dB, from a minimum gain of 17.5 dB to a maximum gain of 38.5 dB. Playback gain is also factory adjusted. The power amplifier amplifies the internal signal by 4, 5, 6 or 7. The quiescent output level is approximately halfway between GND and V_{CC}. To avoid clipping, the maximum output signal should be matched to the low end of the expected V_{CC} range. The recommended speaker impedance is 200Ω.
4. Output offset is measured by playing back a recorded input "short."
5. THD is typically better at lower recording gain.
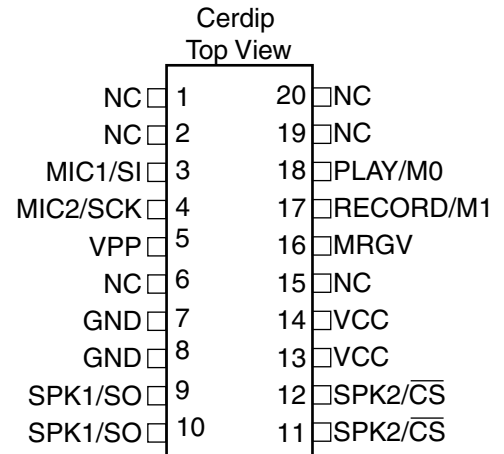
DMA Mode

A Direct Memory Access (DMA) mode is provided for test and development purposes.

The DMA mode is activated by taking the M1 (RECORD) input high, while keeping M0 (PLAY) low. This mode provides access to the internal Flash memory as well as to the parameter configuration register; therefore, the DMA mode should only be used after first consulting with the factory.

In DMA mode it is possible to digitally record pre-processed data which can then be played back through the speaker.

Pin Configuration in DMA Mode

Pin Name	Function
SI	Serial Data Input
$\overline{CS}$	Chip Select
SO	Serial Data Out
SCK	Serial Data Clock
VPP	High Voltage Supply
MRGV	Factory Use
M0	Control Inputs
M1	
NC	Not Connected

Cerdip
Top View

```
          ┌──────────┐
   NC ☐  1 │        20 │ ☐ NC
   NC ☐  2 │        19 │ ☐ NC
MIC1/SI ☐ 3 │        18 │ ☐ PLAY/M0
MIC2/SCK ☐ 4 │        17 │ ☐ RECORD/M1
  VPP ☐  5 │        16 │ ☐ MRGV
   NC ☐  6 │        15 │ ☐ NC
  GND ☐  7 │        14 │ ☐ VCC
  GND ☐  8 │        13 │ ☐ VCC
SPK1/SO ☐ 9 │        12 │ ☐ SPK2/CS̅
SPK1/SO ☐10 │        11 │ ☐ SPK2/CS̅
          └──────────┘
```

In DMA mode the 1-Mbit Flash memory can be erased, written and read by using SPI protocol type commands. Internal parameters such as pre-amp and power-amp gain, as well as sampling frequency can also be modified in DMA mode. Consult factory for details.

The two additional pins presented in the 20-pin Cerdip package are ignored in Audio mode; therefore, the 20-pin package can be used for development of Audio applications (as sockets are more readily available). A 12V supply is needed on VPP; this pin should not be connected in Audio applications. The MRGV pin is used in production for Margin testing and should not be connected in Audio applications. The DMA mode can be used in the 8-lead LAP as well, but write speed is 8 times slower in the absence of a high voltage on VPP.

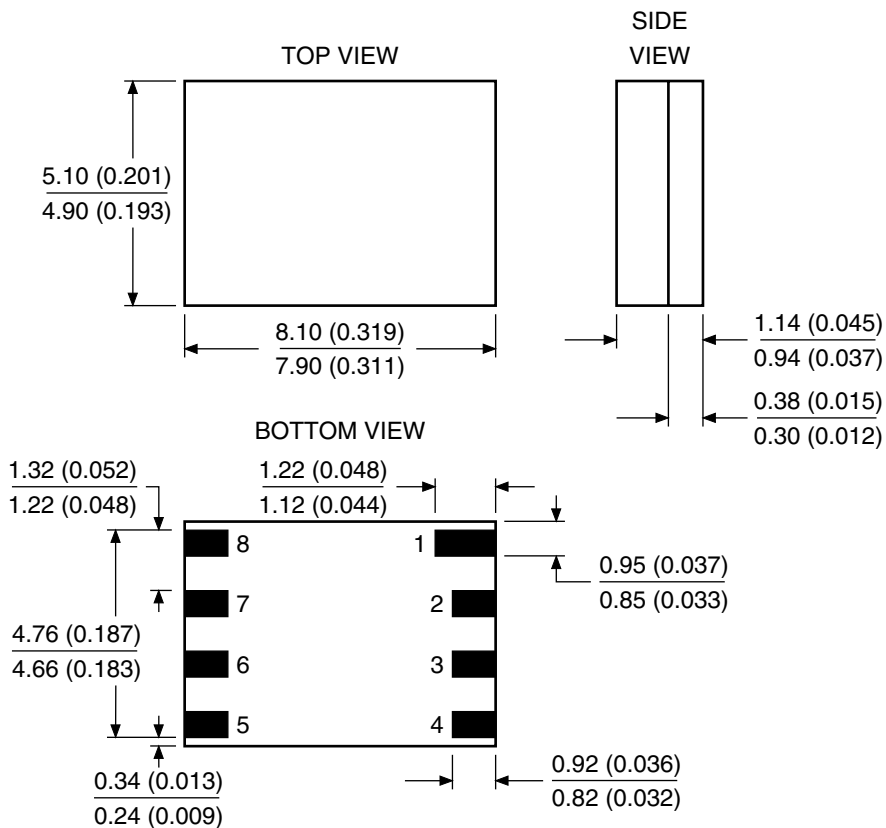## Bonding Information

Die Size: 3.6 x 3.9 mm
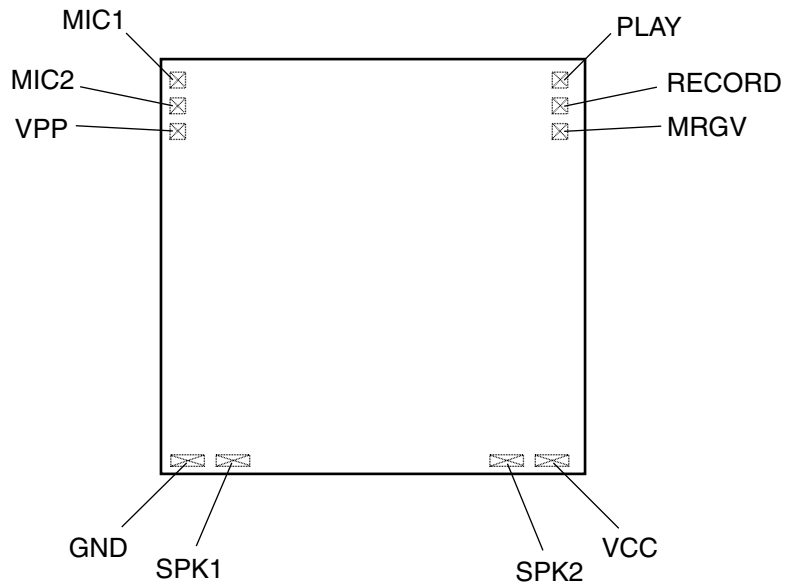
Packaging Information

8C1 – LAP

Dimensions in Millimeters and (Inches)*

*Controlling Dimension: Millimeters

SIDE
VIEW

TOP VIEW

$\dfrac{5.10\ (0.201)}{4.90\ (0.193)}$

$\dfrac{8.10\ (0.319)}{7.90\ (0.311)}$

$\dfrac{1.14\ (0.045)}{0.94\ (0.037)}$

$\dfrac{0.38\ (0.015)}{0.30\ (0.012)}$

BOTTOM VIEW

$\dfrac{1.32\ (0.052)}{1.22\ (0.048)}$

$\dfrac{1.22\ (0.048)}{1.12\ (0.044)}$

8   1

7   2

6   3

5   4

$\dfrac{0.95\ (0.037)}{0.85\ (0.033)}$

$\dfrac{4.76\ (0.187)}{4.66\ (0.183)}$

$\dfrac{0.34\ (0.013)}{0.24\ (0.009)}$

$\dfrac{0.92\ (0.036)}{0.82\ (0.032)}$

	TITLE	DRAWING NO.	REV.
ATMEL 2325 Orchard Parkway San Jose, CA 95131	**8C1**, 8-lead 0.300" Wide, Leadless Array Package (LAP)	8C1	A

20D3 – Cerdip

Dimensions in Millimeters and (Inches)*
MIL-STD-1835 D-8 CONFIG A (Glass-Sealed)

*Controlling Dimension: Inches

04/11/2001
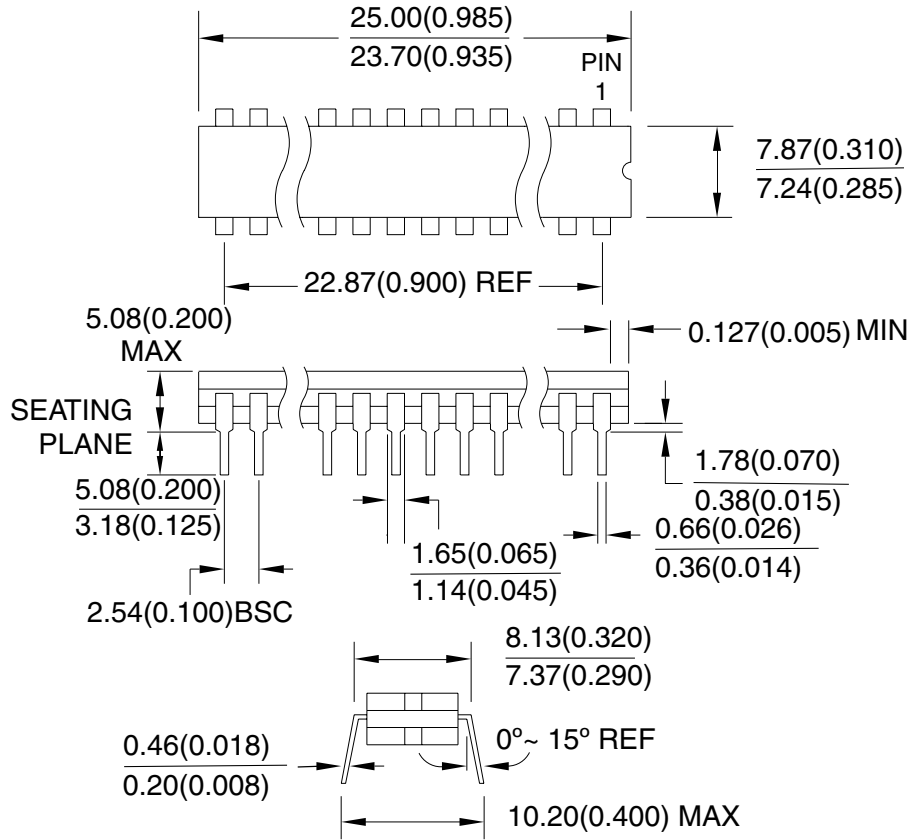
	TITLE	DRAWING NO.	REV.
Almel 2325 Orchard Parkway San Jose, CA 95131	**20D3**, 20-lead, 0.300" Wide. Non-windowed, Ceramic Dual Inline Package (Cerdip)	20D3	A

2469A–10/01

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