APPLICATION INFORMATION FOR ALL ChipCorder PRODUCTS

Introduction

THE TECHNOLOGY AND THE PRODUCTS

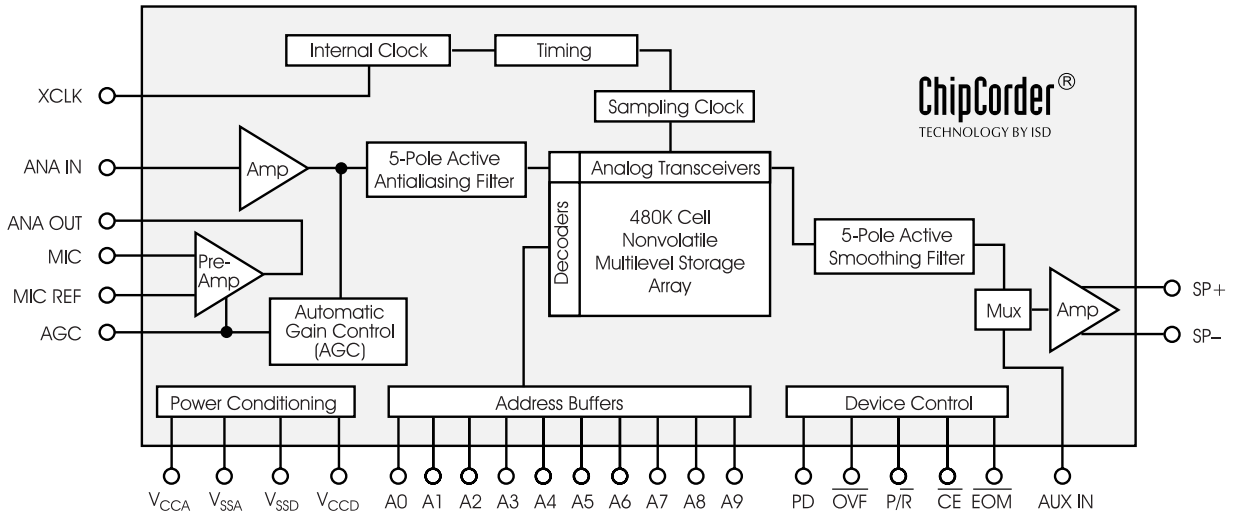
The ISD patented ChipCorder technology brings analog data into the semiconductor memory world. This "break through" EEPROM storage method allows analog data to be written directly into a single cell without A/D or D/A conversion. This results in:

- Increased density over equivalent digital methods
- Nonvolatile storage of analog data

Numerous schematics in the following sections show single-chip voice message systems. A block diagram of one family of ISD devices is shown in Figure 1. In this device, the external components (a microphone, loudspeaker, switches, a few resistors and capacitors, and a power source) are all that is required to build a complete voice record and playback system. All other functions (preamplifier, filters, AGC, power amplifier, control logic, and analog storage) are performed on-chip. This device, the ISD2500 and other products such as the ISD1100, ISD1200 and ISD1400 families emphasize simple push-button or parallel addressed microcontroller operation from a single 5-volt supply.

A new series of devices, starting with the ISD33000 family, emphasizes 3 volt operation and serial port control and may be tailored for specific markets. The ISD33000, for instance, does not have the on-chip microphone amplifier and speaker driver, allowing for a more cost-effective solution for those applications that already have those functions included elsewhere in the circuit.

Figure 1: ISD2560/75/90/120 Basic Block Diagram



OPERATIONAL OVERVIEW

During recording, the ISD device performs several stages of signal conditioning before the actual storage operation takes place.

For example, in those products with an included on-chip AGC, the first stages are composed of a preamplifier, amplifier and AGC blocks.

The preamplifier is connected to the microphone by a DC blocking capacitor that removes the DC component from the low level (2 to 20 mV) AC signal. Amplification is performed in two stages; initially by the input preamplifier and then by the fixed gain amplifier. The signal path is completed by connecting a capacitor between the ANA OUT and ANA IN pins.

Such an architecture allows system design flexibility, particularly for non-voice applications and also provides an additional pole for low frequency cutoff. The AGC circuit dynamically monitors the signal level at the amplifier output and sends a gain control voltage to the preamplifier. The preamplifier gain is automatically adjusted to maintain an optimum signal level into the filter. This gives the highest level of recorded signal while reducing clipping to a minimum.

The characteristic of the AGC circuit is described by two time constants; the attack time and the release time.

- Attack time is the time required by the AGC to reduce gain in response to an increasing input signal.
- Release time is the time constant of the gain increase in the presence of a decreasing signal.

The user can adjust both the attack and the release time by selecting values of the resistor and capacitor connected to the AGC pin. Certain default values will give optimum performance for normal speech; however, the accessibility of the resistance and the capacitance allows the user to tailor the AGC to his own particular needs. The 20 dB or so gain compression range on the preamplifier compensates for various microphone characteristics and also various levels of speech volume. The signal integrity is maintained. There is minimum clipping or other forms of distortion yet the dynamic signal range is increased by 20 dB.

All ISD devices next include a stage of signal conditioning performed by an input filter. As we will see later, the storage, although analog in nature, still employs sampling techniques. As a result the device requires an antialiasing filter to remove (or at least reduce to an insignificant level) input frequency components above half the sampling frequency. This is to satisfy the well-known Nyquist Criterion that applies to all sampled data systems.

Voice quality better than "telephone quality" (telephones cut off below 300 Hz) is achieved with a sampling frequency of 8 KHz. The high frequency cutoff of the low pass filter is then chosen to be 3.4 KHz, satisfying the Nyquist criterion, but still with a wide enough frequency band to allow for good quality voice reproduction. The filter is a continuous time, 5-pole low-pass filter with a roll-off of 40 dB per octave at 3.4 KHz.

Signal conditioning is now completed. The input waveform is then passed into the analog transceivers to be written into the Analog Storage Array. Samples are taken by the 8-KHz sample clock. These samples undergo a level shifting process to produce the high voltages required for the nonvolatile writing procedure, at the same time compensating for some of the practicalities related to Fowler-Nordheim tunneling. The sample clock is also used to increment the array decode so that the input samples are mapped sequentially into the array.

During playback, the recorded analog voltages are sequentially read from the storage array under control of the same sample clock, reconstructing the sampled waveform. The smoothing filter on the output path removes the sampling frequency component and the original waveform is restored.

The frequency of the sample clock affects record duration and quality. As the frequency increases the sound quality is improved, but, of course, the record duration is reduced. Conversely, a lower oscillator frequency gives increased duration at the cost of lower quality. The oscillator frequency

is trimmed to an accuracy better than 1% before the product leaves the factory. This is achieved by taking further advantage of the features of this technology. Trimming of oscillator components is done by programming nonvolatile trim bits that have been included on-chip.

The same process variables that affect the oscillator frequency also effect the filter cutoff frequency. When we trim the oscillator frequency, we also automatically trim the filter cutoff frequency.

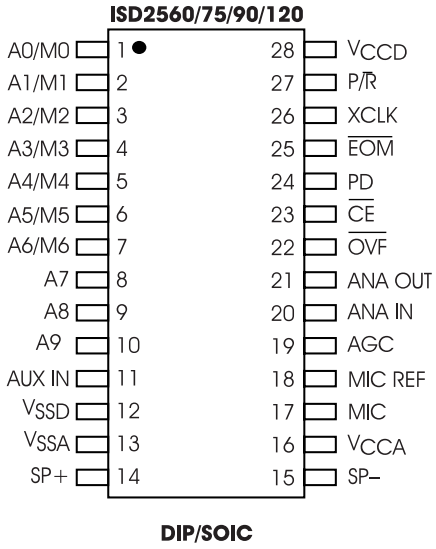
All ISD devices also include a smoothing filter connected to the output of the analog storage array. In devices without an on-chip speaker driver, this filter output is buffered and presented to an output pin.

Some ISD products include an on-chip speaker driver. In these devices, the output of the smoothing filter is connected through an analog multiplexer into the output power amplifier. Two output pins provide direct speaker drive capability of about 12.5 mW RMS (25 mW peak) into a 16 ohm speaker. This is enough to be clearly heard from the other side of a normal sized room. In some products the speaker driver is also available for system use via the AUX IN pin. From this input it can provide 50 mW RMS output.

The circuit design used in the ISD Series of devices results in the equivalent of 8 bits of storage in each EEPROM cell. Information is written into the cell in a closed loop fashion. A sample-and-hold circuit holds the data during the programming cycle and supplies the analog voltage to be stored to one input of a comparator. The other input to the comparator is the output of the storage cell itself. Electrons are pumped into the cell during multiple writes and the resulting stored level is fed back to the comparator.

When the comparator signals that the cell output voltage equals the level from the sample-and-hold, programming of that cell ceases. The minimum amount of charge injected into the cell during each write sets up system resolution. This is approximately 256 levels, which is equivalent to 8 bits of accuracy. Writing to the cell in this manner also eliminates cell to cell variations.

Figure 2: ISD2500 Pinout



The process used is based on the EEPROM floating gate technology. ISD guarantees 10 years of data retention but laboratory tests suggest that the typical data retention will be 100 years.