APPLICATION BRIEF 4 — EXTERNAL CLOCK DRIVE USING THE ISD1100, ISD1200 OR ISD1400

In the ISD1000A or ISD2500 device series, some customers experienced difficulties in switching from internal to external clock and back again. Particularly, any noise or spikes at the wrong time could convince the part it was in the external mode when there was no clock present. Then the device would cease to function, ignoring all inputs until the power was removed and reapplied.

The ISD1100, ISD1200, and ISD1400 series is designed so the device will not end up in a locked up state. This is accomplished by logic that automatically switches the device back to internal clock whenever the three pins, $\overline{REC}$, $\overline{PLAYL}$, and $\overline{PLAYE}$, are all HIGH. In this way, the device is always looking for command inputs with the internal clock if the external clock is off.

Table 4: External Clock Drive Frequencies

Device Part Number	Int. Osc. Freq. (KHz)	Ext. Drive Freq. (KHz)	Sample Rate (KHz)	Filter Pass Band (Hz)
ISD1016A	512.0	1,024.0	8.0	3400
ISD1020A	409.6	819.2	6.4	2700
ISD1110	409.6	819.2	6.4	2600
ISD1112	341.3	682.7	5.3	2200
ISD1210	409.6	819.2	6.4	2600
ISD1212	341.3	682.7	5.3	2200
ISD1416	512.0	1,024.0	8.0	3300
ISD1420	409.6	819.2	6.4	2600
ISD2532/60	512.0	1,024.0	8.0	3400
ISD2540/75	409.6	819.2	6.4	2700
ISD2548/90	341.3	682.7	5.3	2300
ISD2564/120	256.0	512.0	4.0	1700

Expressing this a different way, to use the external clock, one of the three inputs must be LOW. A recording is made by having an external clock present at the XCLK pin when $\overline{REC}$ goes LOW. The $\overline{PLAYL}$ input should be brought LOW simultaneously (or shortly after) with $\overline{REC}$. At the end of the recording $\overline{REC}$ is brought HIGH. This begins the "finish recording" process. Because the device continues to sample and record for the remaining portion of the row until it reaches an EOM location, $\overline{PLAYL}$ must be kept LOW for another 50 to 75 msec. This keeps the device in the external clock mode until everything is written to memory. If only $\overline{REC}$ is used there will be a short "chirp" or change in pitch at the very end of the recording.

Playback with the external clock requires that the $\overline{PLAYL}$ pin be used, not the $\overline{PLAYE}$. This is because the device will switch to external clock when $\overline{PLAYE}$ goes LOW but will immediately revert to the internal clock when $\overline{PLAYE}$ goes HIGH again.

For applications where one wants to vary the pitch of playback the $\overline{PLAYL}$ pin must be used for Playback. Another alternative is to record with the external clock and then use the internal clock and $\overline{PLAYE}$ for playing back the messages. This eliminates the need for external timing of the $\overline{PLAYL}$ signal in Playback.

NOTE *The ISD1100, ISD1200 and ISD1400 devices include a pull-down resistor to V_{SS} on the XCLK pin. This pull-down resistor is approximately 100 KΩ.*