

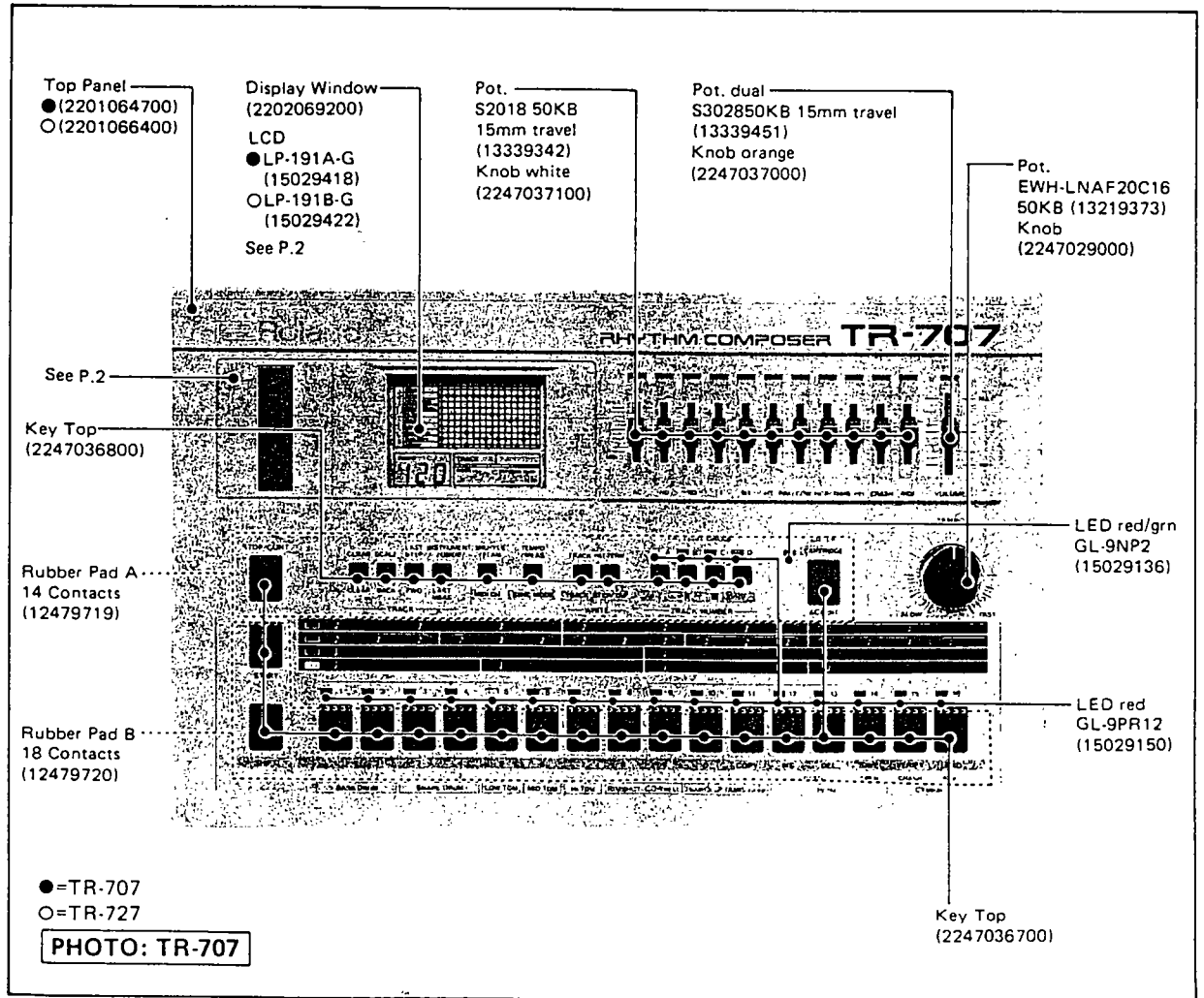
TR-707/727

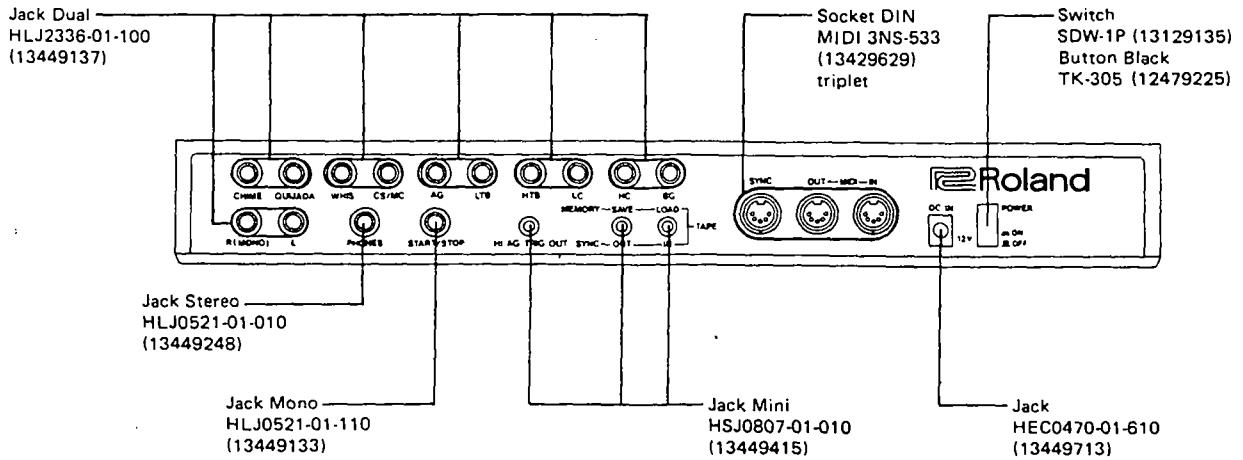
SERVICE NOTES

First Edition

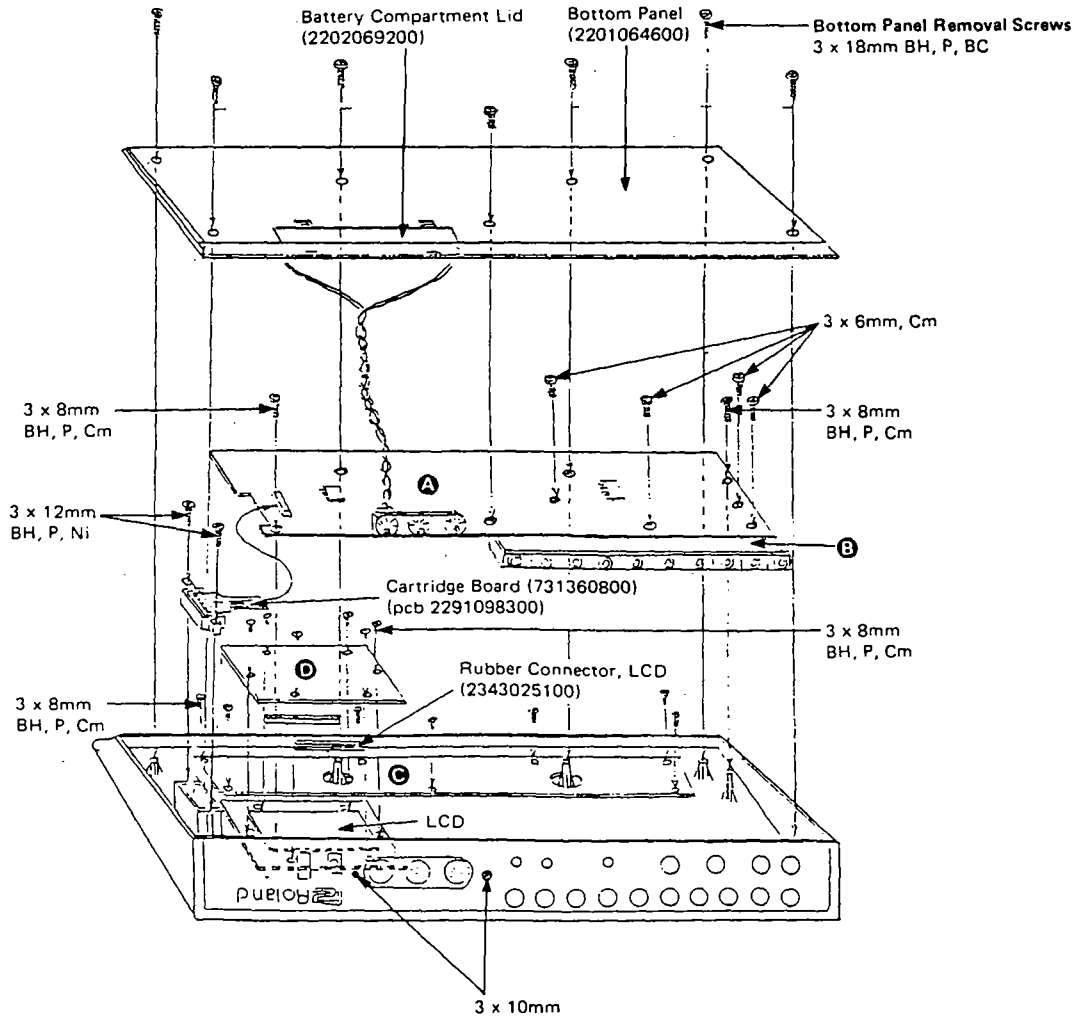
SPECIFICATIONS

Memory Capacity	: 64 Rhythm Patterns (16 x 4 Group)
Track	: 4 (1 to 4; continuous Maximum measures=998)
Step	: 1 to 16 steps/measure
Tempo	: ♩ = 38 to 250
Rear Panel	: Master Out (L,R/MONO) [8Vp-p, 1K Ω]
Trigger Out	: +5V, 20ms Pulse TR-707 Rim Shot TR-727 Hi Agogo
Sync In/Out (5P DIN)	: (1: Run/Stop, 2: GND, 3: Clock, 4: NC, 5: Continue)
Power Consumption	: 2.4 W
Dimensions	: 380 (W) x 73 (H) x 250 (D) mm 14-15/16" (W) x 2-7/8" (H) x 9-13/16" (D) in
Weight	: 1.5 kg/13 lb. 5 oz.
Accessories	: 12V AC Adaptor Connection Cord PJ-1
Options	: Memory Cartridge M-64C Pedal Switch DP-2

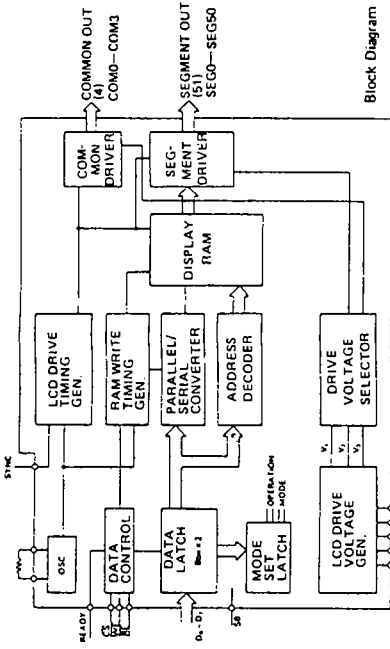




	TR-707	TR-727
A	Voicing Board (7313604000) (pcb 2291098102)	Voicing Board (7313804000) (pcb 2292018900)
B	Volume Board (7313605000) (pcb 2291098002)	Volume Board (7313805000) (pcb 2292019000)
C	Switch Board (7313606000) (pcb 2291097903)	
D	LCD Board (7313607000) (pcb 2291098203)	

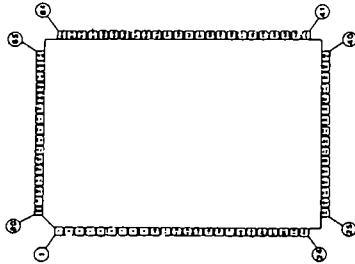


LCD Driver HD61602

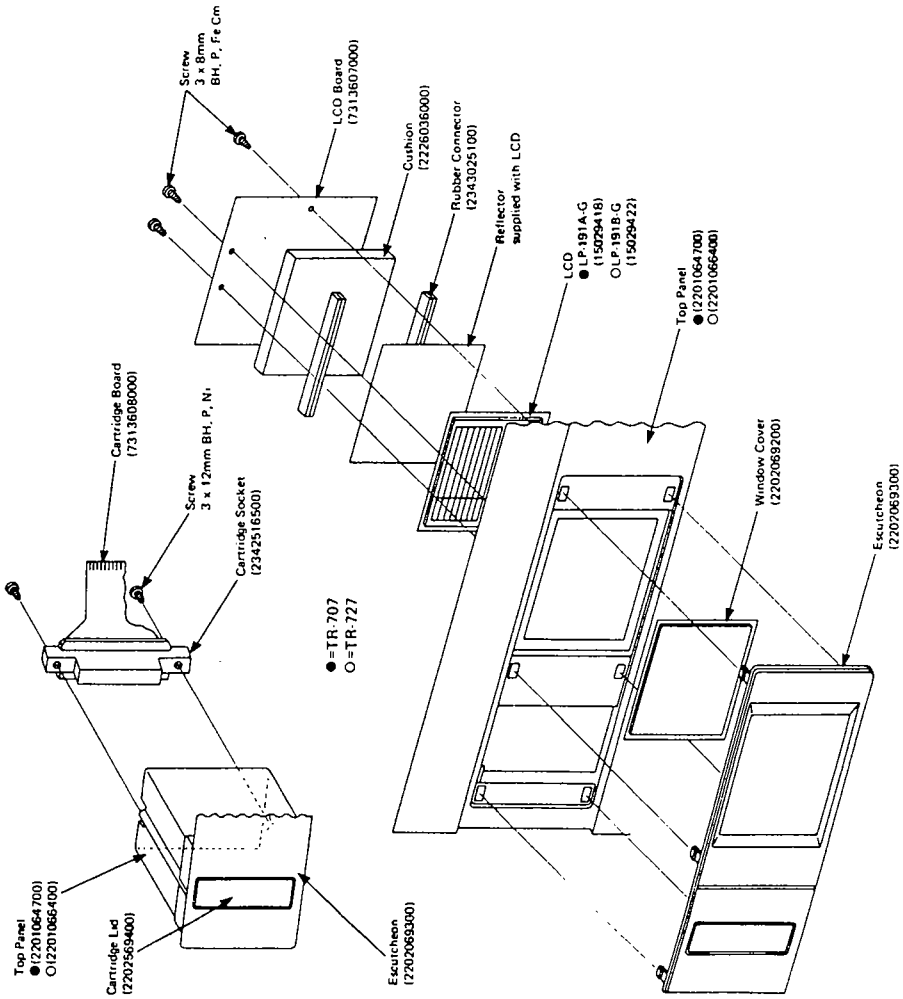


Block Diagram

Pin configuration
(Top View)



TERMINAL ASSIGNMENTS			
Pin No.	Pin Name	Pin No.	Pin Name
1	Pin	28	SEG19
2	REF10	29	SEG20
3	REF11	30	SEG21
4	REF12	31	SEG22
5	REF13	32	SEG23
6	REF14	33	SEG24
7	REF15	34	SEG25
8	REF16	35	SEG26
9	REF17	36	SEG27
10	REF18	37	SEG28
11	REF19	38	SEG29
12	REF20	39	SEG30
13	REF21	40	SEG31
14	REF22	41	SEG32
15	REF23	42	SEG33
16	REF24	43	SEG34
17	REF25	44	SEG35
18	REF26	45	SEG36
19	REF27	46	SEG37
20	REF28	47	SEG38
21	REF29	48	SEG39
22	REF30	49	SEG40
23	REF31	50	SEG41
24	REF32	51	SEG42
25	REF33	52	SEG43
26	REF34	53	SEG44
27	REF35	54	SEG45



PARTS LIST EXCLUSIVE PARTS

TR-707

CASING	I2201064700	Top Panel
PCB	I7313604000	Voicing Board (pcb 2291098102)
	I7313605000	Volume Board (pcb 2291098002)
LCD	I15029418	LCD LP-191A-G
IC		
Program ROM	HN4827128G-25	NMOS EPROM
	I15179720	(Ver.0 SH460100-504399)
		(Ver.1 SH504400-519599)
or		
	I15179660	HN613128PE95
		CHOS MASK ROM
or		
	I15179692	HN613128PG24
		CHOS MASK ROM
		(Ver.2 SH533100-up)
UPWARD COMPATIBILITY		
Ver.0		

In Pattern PLAY mode -- Selecting a pattern from different scale while repeating STOP and START or CONTINUE sometimes leads to Power-ON initialization.
ROMs of Ver. 1 always run the new pattern at the beginning of a measure.

Ver.1
When the unit is used as a Master -- Repeating of STOP and CONTINUE more than 30 times would cause Generation of a redundant MIDI clock SF8.
When the unit is used as a Slave -- Will miss a MIDI IN clock when STOP signal follows the Clock within 1ms.

MASK ROM of Ver.2 cures this problem.
For a replacement Ver.2 or up is recommendable.
上記コンパチの適用としてはバージョン番号の大きいPROMの使用が望ましい。

Sound ROM	I15179661	HN61256PC-71	CHOS MASK ROM
			BD1/2, SD1/2, LT, HT
	I15179662	HN61256PC-72	CHOS MASK ROM
			HT, Open/Closed H.H, Rim, Cow
			HCP, Tambourine
	I15179663	HN61256PC-73	CHOS MASK ROM
			Crash Cymbal 1
	I15179664	HN61256PC-74	CHOS MASK ROM
			Ride Cymbal

TR-727

CASING	I2201066400	Top Panel
PCB	I7313804000	Voicing Board (pcb 2292018900)
	I7313805000	Volume Board (pcb 2292019000)
LCD	I15029422	LCD LP-191B-G
IC		
Program ROM	I15179719	HN4827128G-25
		NMOS EPROM
Sound ROM	I15179694	HN61256PC-79
		CHOS mask ROM
		HI/LOW BONGO, HI CONGA
		LOW CONGA, HI TIMBALE

15179695	HN61256PC-80	CMOS mask ROM	LOW TIMBALE, AGOCO, CABASA
15179696	HN61256PC-81	MARACAS, WHISTLE	
15179697	HN61256PC-82	CMOS mask ROM	QULJADA
		CMOS mask ROM	STAR CHINE

COMMON PARTS

CASING	2201064600	Bottom Case	
	2202069100	Battery Cover	
	2202069200	Display Window	
	2202069300	LCD Escutcheon	
	2202569400	Cartridge Lid	
KNOB, BUTTON, KEY TOP	2247029000	Knob	TEPO
	2247036700	Key Top (large)	gray
		Key Top (small)	gray
	2247036800	Key Top (small)	gray
	2247037100	Knob	BD,SD,LT,HT,HT,UCH, RS/CB,HCP/TAMB,RIDE, CRASH
	2247037000	Knob	orange
	12479225	TK-305	black

PCB ASSY	7313606000	Switch Board	(pcb 2291097903)
	7313607000	LCD Board	(pcb 2291098203)
	7313608000	Cartridge Board	(pcb 2291098300)

COIL, TRANSFORMER	2244025000	S097744	Transformer
	12449229	FX08160RH15	Coil

SOCKET	13429629	HID1 3-NS-533	DIN
	13449713	HEC0470-01-610	AC adapter
	13449415	HSJ0807-01-010	mini
	13449248	HLJ0521-01-010	stereo
	13449133	HLJ0521-01-110	monoral
	13449137	HLJ2336-01-100	dual
	2342516500	PBR8-280-T01-S	cartridge

SWITCH	12479719	Rubber switch (Pad) A	14 contact upper row
	12479720	Rubber switch (Pad) B	18 contact lower row
	13129135	SDW-1P	POWER

POTENTIOMETER	13339342	S2018 50KB	slide 15mm travel
	13339451	S3028 50KB	dual slide 15mm travel
	13219373	EMH-LNAFZ0C16 50KB	TEPO
	13299136	RVF8P01-503 50KB	trimmer
	13299141	RVF8P01-204 200KB	trimmer

XTAL, CERAMIC RESONATOR	12389736	HC-18/U	4.0MHz Xtal
	12389735	CSA 1.6KH	1.6MHz ceramic resonator

IC	15229825	RD63H14PF	gate array
	15179200	HD6303XF	CPU
	15179340	HM6116LP-4	CMOS S RAM
	15219148	HD61602	LCD driver
	15159503	TC40H000P	H CMOS
	15159504	TC40H002P	H CMOS

15159505	TC40H004P	H CMOS	hex inverter
15159517	TC40H010P	H CMOS	triple 3-input NAND gate
15159506	TC40H138P	H CMOS	3-to-8 line decoder/demultiplexer
15159535	TC40H151P	H CMOS	1-of-8 data selector/multiplexer
15159511	TC40H174P	H CMOS	hex D-type flip flop
15159524	TC40H245P	H CMOS	octal bidirectional bus buffer
15159507	TC40H273P	H CMOS	octal D-type flip flop
15159530	TC40H367P	H CMOS	hex bus buffer
15159104	TC4011BP	CMOS	quad 2-input NAND gate
15159105	TC4013BP	CMOS	dual D-type flip flop
15159141	HD14040BP	CMOS	12-stage binary counter
15159113	HD14051BP	CMOS	single 8-channel multiplexer/demultiplexer
15159301	TC45208P	CMOS	dual binary up counter
15159303	HD45848P	CMOS	hex schmitt trigger
15189136	M5218L	Op amp	
15189154	TL064	FET Op amp	
15219147	UPC624C	D/A converter	
15199108FO	UA78M05UC	voltage regulator +5V	
15229712	PC900	photo coupler	
15149118	M54517P	transistor array	

MISCELLANEOUS

2217515300	Spring	RAM cartridge
2214531300	Shaft	RAM cartridge
2345014600	Plate	battery
22469117	Heat Sink MT-25-BS	(switch pcb)
2219049900	LED Holder	(LCD pcb)
13529117	Ceramic Capacitor	0.33uF
12559708	Fusing Resistor	FRN8 1/4WZ.7R
2225022801	Shield Cover	(Voicing pcb-Volume pcb)
2225022400	Shield	top panel

COMMERCIALLY AVAILABLE ACCESSORIES

12569105	Dry cell S04-3S	1.5V
12449538	12V AC adapter	(100V)
12449539	12V AC adapter	(117V)
12449540	12V AC adapter	(220V)
12449541	12V AC adapter	(240VA)
2343067500	Connection Cable LP-25	Australian

15129612	2SD1469-R	NPN
15129137	2SC2603-F	NPN
15129412	2SC1384-Q	NPN
15119125	2SA1115-F	PNP
15139101	2SK30ATH-Y	FET

15019126	1SS113T-77	diode
15019209T0	S-5500G	rectifier
15019667	RD-12EB1-T	12V zener
15029136	GL-9NF2	LED red/grn
15029150	GL-9PR12	LED red

13919133	BKM7LM502	D/A converter
13919103	RCSD8X103J	10K x 8
13919113	RCSD4X103J	10K x 4
13910107	RSD8X332J	3.3K x 8

13439256	5089-11A	11P (Switch pcb)
13439255	5089-13A	13P (Switch pcb)
13439253	5494-9C	9P (Voicing pcb)
13439252	5494-10C	10P (Voicing pcb)
13439254	5597-28APB	28P (Voicing pcb)
2343025100		rubber connector LCD

2341048000	13P	(LCD pcb)
2341047900	11P	(Voicing pcb)
2347015200	9P flat cable	(Volume pcb)
2347015300	10P flat cable	(Volume pcb)

WIRING ASSY	2341048000	13P	(LCD pcb)
	2341047900	11P	(Voicing pcb)
	2347015200	9P flat cable	(Volume pcb)
	2347015300	10P flat cable	(Volume pcb)

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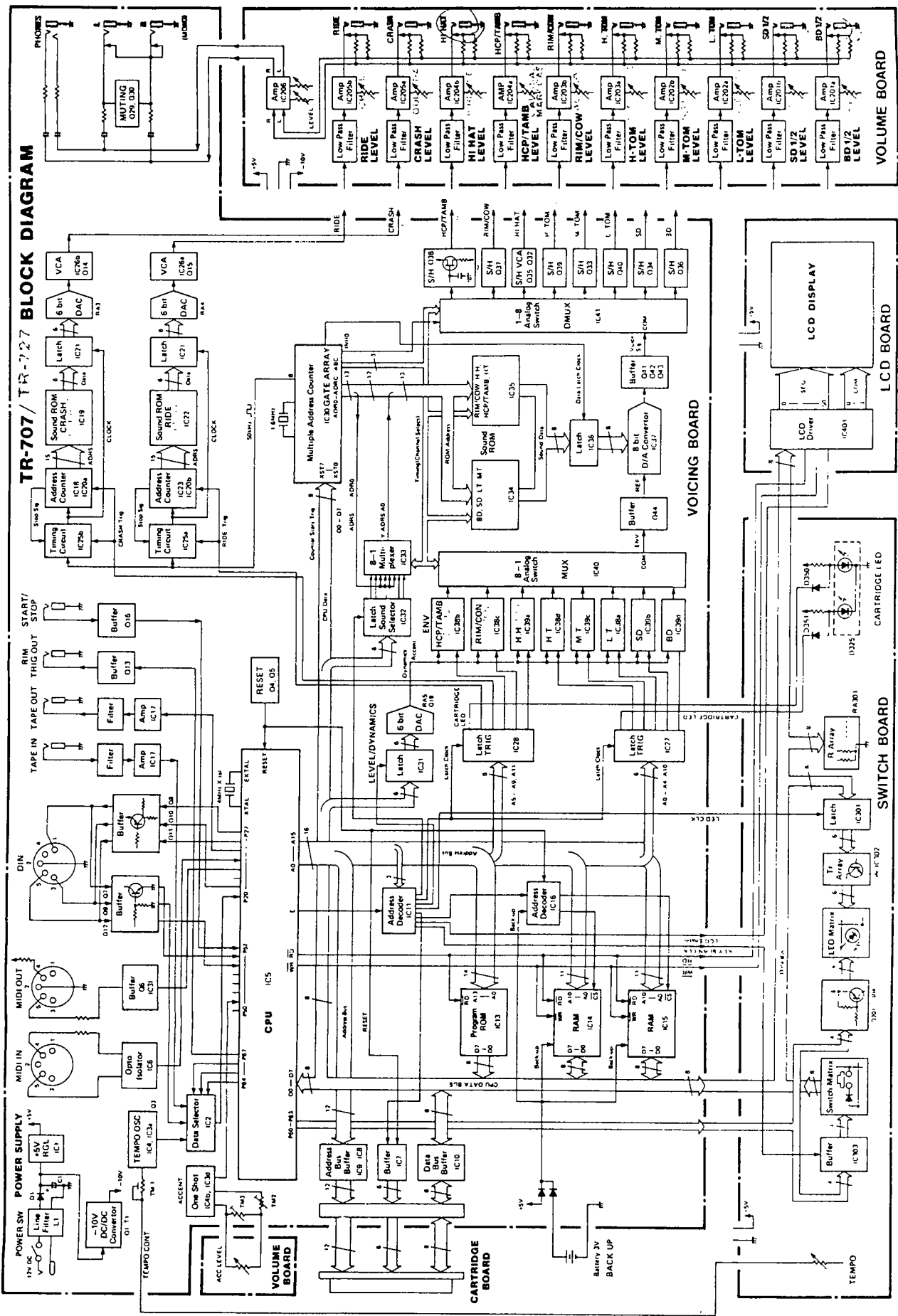
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TR-707 / TR-727 BLOCK DIAGRAM



CIRCUIT DESCRIPTIONS

TR-707 and TR-727 are designed based on the same circuit configuration, having more in common with each other. The differences between two models are sound data, component values in several audio stages and a couple of pin connections at IC30 of Voice board.

Both models derive all rhythm sounds from PCM-encoded samples of real sounds stored in ROM. Each waveform is stored either independently (e.g. CYMBAL) or together with another waveform as shown in Tables 1 and 2. Accordingly, sound reproducing circuits are classified into two: multiplex and single. The following description focuses on PCM sound reproduction system, taking TR-707 circuits as a representative.

回路解説

TR-707/727はROMにメモリされているPCM波形(サウンドデータ)を音源として利用しています。楽器の種類が異なる為一部に回路や定数の違いがあるものの、全体の回路構成は両機種に共通です。以下TR-707を例として説明します。

表1及び2から判る様に、IC34、IC35には複数音源のデータが、IC19、IC22には単一音源がメモリされています。従って、これら音源データの読み出しから再生までの過程もシングルフーズとマルチの二種類があります。

MULTIPLY SOUND PROCESSING

MULTIPLE ADDRESS COUNTERS

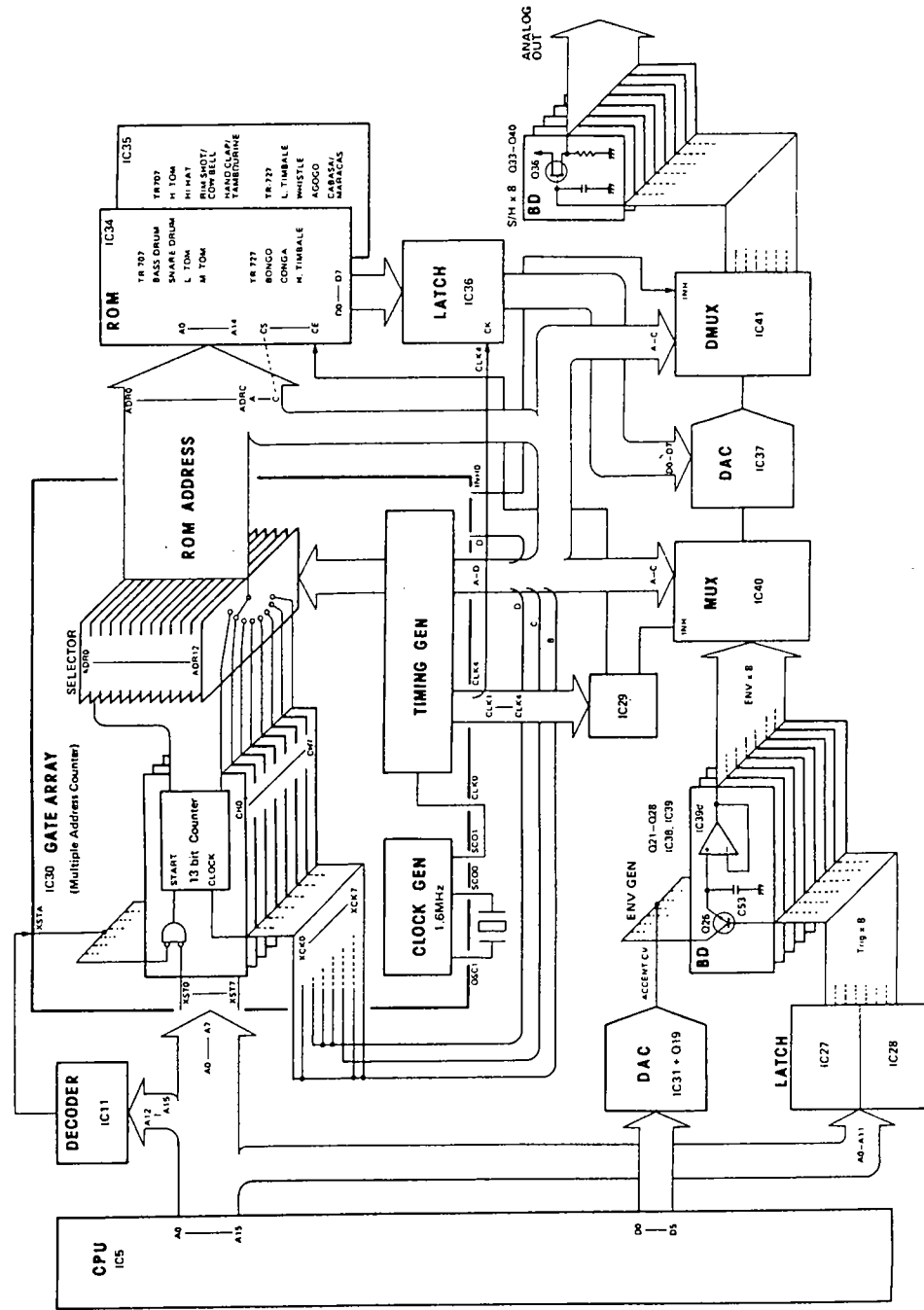
IC30 RD63H114 on Voicing Board is a custom-LSI (called Gate Array) designed for use in PCM-sound multi-rhythm systems. The LSI assumes the key role in the TR-707 sound system. It incorporates a master clock generator, timing generator and 8 13-bit address counters. The timing generator, not only supplies clocks to these counters for generating address bits, but also feeds peripheral circuits with various timing clocks to sync the entire system operation. Of these timing clocks, A, B and C together make a channel-select code for signaling the ROMs (ICs 34, 35), MUX IC40 and DMUX IC41 which voice is being addressed by an address counter in IC30.

マルチ音源

マルチアドレスカウンタ

多音源データをメモリしているROM (IC34、35)からのデータ読み出し、D/A変換、S/Hおよびその他の関連回路は、IC30 RD63H114はマルチ音源装置用に開発されたカスタムLSIである。内蔵のクロックおよびタイミング発生回路によりこれら外付回路を同期させるクロック信号を出力します。同期クロックのうちA、B、Cはボイス・チャンネルのセレクトコードを形成しますのの特長です。IC30はROM (IC34、35)内の各音源データのアドレスを次々と出力して行きますが、A、B、Cはこの音源アドレス(アドレス・カウンタのチャンネル番号)が出力されているかを、ROM以外のMUX IC40、DMUX IC41にも知らせます。(例SDの場合 A=1、B=0、C=0。次頁のタイミングチャート参照)

MULTIPLY SOUND SYSTEM BLOCK DIAGRAM



今 BASS DRUM1 (BD-1) が選択された状態で、リズムが走ったとすると、IC30にXST0 (チャンネル0スタート)とXSTA (XST0-7ハイネープル)が加わり、カウンタCH0は0000Hにリセットされた後XCK0Cに加えられて来るクロックBをカウンタとして行きます。この1.3ピルス・アドレスカウンタのカウント値は40μs毎にアドレス・セレクタによりADRO-ADRC端子に出力されて行きます。(次にもう一度XST0が加わらない場合、カウンタは最大値1FFFHに達するとストップしたままとなります。)

サウンドデータの読み出し

2.56KビットROM IC34, IC35のメモリー・ロケーションにアクセスするには、15ビットのアドレスが必要ですが、残りのMSB2ビットにはIC30のA, Bクロックが当てられます。クロックCは、どちらのROMIC7がアクセスするかを選ぶチップセレクタです。一方LSBAD R0は、音源によってはROMアドレスとして使用されません。例えば、BD-1とBD-2は同じROMのメモリアリアを共有しており、BD-1には鳴数のアドレスがBD-2には鳴数アドレスが割当てられています。(表1参照)。この為、BD-1の場合、ROMのA0には常に“0”がIC32, IC33を通じて加えられます(BD-2の場合は“1”)。

ROMから読み出されたサウンド・データは、IC37 (ラダー・ネットワーク内蔵) でアナログ電圧に変換され、リズム音源の一部(サンプリング波形)を再現しますが、振幅値は原音の値とは必ずしも一致しません。これはPCMの過程においてS/N比や分解能向上の処理が含まれている為です。再生音のエンベロープは、IC37の(4) REFに接続されたENV GENからの信号によって左右されます。

Now suppose that TR-707 is to run with BASS DRUM 1(BD-1) being selected, the CPU IC5 puts XST0 (CH0 start) and XSTA (XST0-XST7 enable) low, resetting counter 0, presenting it to the starting address 0000H and allowing it to count the clock pulse XCK0 from pin B in discrete steps. The counter continues counting until it increments up to 1FFFH and tops, there until the next trigger pulse is received. While counting, the contents (a group of 13 clock pulses) of the counter is transferred to address selector where it is read every 40μs and is presented along ports ADRO through ADRC-13 lower address bits.

ROM MEMORY READING

IC34 and IC35, 32,768 word by 8 bit ROM, require 15 address bits to access their memory locations. Clocks A and B from IC30 serve as MSBs while C indicates which one of two ROMs is to be selected—Chip Select. On the contrary, LSB ADRO is defeated when particular voice is selected: BD-1 and BD-2 share the same memory area with even addresses allocated to BD-1 and odd ones to BD-2 as shown in Table 1. With BD-1, data selector IC33 blocks ADRO and passes “0” data from IC32 onto AD of ROM IC35. With BD-2, IC33 selects “1”. With Low Tom, Mid Tom, Hi Tom or Hi Hat, ADRO is allowed to reach A0.

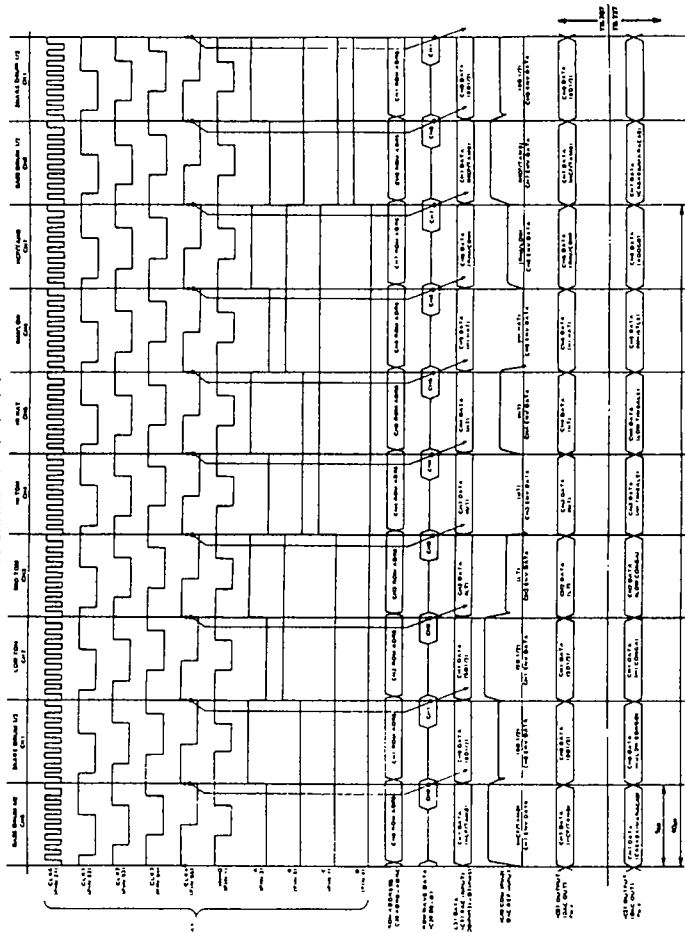
Each 8-bit memory location (PCM waveform data) in ROM is loaded into latch IC36 on the rising edge of CLK4. This 8-bit data is, if converted to analog equivalent by D/A converter IC37 as it is, not restored to its original amplitude. A certain technique is involved during PCM to improve S/N ratio, to have higher resolution, etc. A signal coming from Envelope Generator into (4) REF pin gives right tone contour to a continual PCM waveforms being decoded and converted to an analog sound.

TR-727 Sound Data ROM

IC No.	ROM	CE	CS	VOICE	MEMORY
IC34	M81328K71 (15179681)	N	L	Hi Bongo	2K - 1 ADRES 4K byte
				Mid Bongo	2K - 1 ADRES 4K byte
				Open Hi Conga	2K - 1 ADRES 4K byte
				Open Lo Conga	2K - 1 ADRES 4K byte
				Hi Timbale	2K - 1 ADRES 4K byte
				Whistle	2K - 1 ADRES 4K byte
IC35	M81328K40 (15179655)	N	N	Hi Tom	2K - 1 ADRES 4K byte
				Mid Tom	2K - 1 ADRES 4K byte
				Low Tom	2K - 1 ADRES 4K byte
				Hi Hat	2K - 1 ADRES 4K byte
				Hi Conga	2K - 1 ADRES 4K byte
				Hi Bongo	2K - 1 ADRES 4K byte

Table 1 表1

TIMING CHART タイミング・チャート



ENVELOPE GENERATOR

Data coming to latch IC31 is a combination of LEVEL and DYNAMICS (ACCENT). The value of LEVEL is always constant regardless of voice selected, while DYNAMICS varies with MIDI Velocity or ACCENT amount setting. Although LEVEL/DYNAMICS is connected to all 8 ENV GENERATORs it is allowed to enter only the transistor whose base-emitter junction, for example O26, is being forward biased by a TRIG from latch IC27 or IC28 at XSTA rate. O26 output is then connected by IC40 to (+) REF pin of IC37 every 40μs with its level decaying according to C53xR59 time constant as the successive BD-1 data are converted to analog voltages, giving a bass drum contour to the voice.

The DAC output is boosted at Q41 and Q42 conjunction and is channeled into the S/H which is designated by A BC code placed at IC41 select pins. As can be seen from the timing chart, the timing of envelope and D/A converting lag one slit behind the memory addressing. That is, BD-1 sound read from ROM with channel No. ABC=000 becomes an audible sound when channel No. is represented by ABC=100. This is because the data accessed on a positive going CLK4 with ABC=000 is latched into IC36 on the next CLK4 with ABC=100. Consequently, TRIG data to ICs 27 and 28, and LEVEL/DYNAMICS data to IC31 are made to delay one CLK4 cycle to keep pace with D/A conversion at IC37

エンベロープ・ジェネレータ

XSTA (XST0-7ハイネープル)はIC30のアドレスカウンタに加えられ、同時に、ラッチIC27, 28のCLKにも加えられ、BD-1が選択されている時には、ENV GENのQ26がTRIG・パルスによって導通し、LEVELとDYNAMICS(ACCENT)の混合された電圧がC53に充電されます。なお、LEVELの値はどの音源の場合でも常に一定です。また、LEVEL/DYNAMICS CVは8本全てのトランジスタに印加されますが、TRIG・パルスが現在加わっているトランジスタにのみ流入します。Q26の出力はIC39dを通り、IC40により時分割でD/AコンバータのREF端子へ送られて行きますが、裏面はC53xR59の時間定数に応じて減衰して行きます。時定数はBDのサウンド・データ全部がROMから読み出される時間より長くなる様に設定されています。

IC30のアドレス・カウンタのチャンネル番号とIC40/41のチャンネル番号が異なっています。これはROMのサウンド・データが、アキュムレタの時よりCLK4の1サイクル分遅れてIC36にラッチされ、D/A変換される為です。したがってTRIGおよびLEVEL/DYNAMICS・データもその分遅れて出力されます。

HI HAT

Output from Q35 has no distinction between closed hi hat and open hi hat and is given a particular waveshape (decay) at VCA Q22 and IC42 as OPEN/CLOSED select signal is applied on the base of Q21.

SINGLE SOUND PROCESSING

Each of CYMBAL voices (RIDE and CRASH) has dedicated sound ROM, address counter, D/A converter and envelope generator. The difference from Multiplex processing in circuit configuration is that envelope control is accomplished after the wave data becomes analog form. LEVEL/DYNAMICS (ACCENT CV) routed to Q18 emitter (CRASH) is charged into envelope capacitor C50 on a TRIG, giving a contour to CRASH sound passing through Q14.

TR-707 Sound ROM

IC NO.	ROM	CE	CS	VOICE	MEMORY
IC19	HN61256PC73 (15179663)	H	L	CRASH CYMBAL	32k byte
IC22	HN61256PC74 (15179664)	H	L	RIDE CYMBAL	32k byte

Hi Hat に対しては、もう一度エンベロープ回路(VCA-IC42a, Q32)が追加されており、クローズかオープンかによりディケイタイムを切替えています。

シングル音源

RIDE CYMBAL および CRASH CYMBAL は、それぞれ専用のアドレス・カウンタ、ROM および D/A コンバータを持っていますが動作原理はマルチ音源の場合と変わりません。ただし、エンベロープがD/A変換後VCAに加えられる点の違いがあります。

TR-727 Sound ROM

IC NO.	ROM	CE	CS	VOICE	MEMORY
IC19	HN61256PC81 (15179696)	H	L	QUIJADA	32k byte
IC22	HN61256PC82 (15179697)	H	L	STAR CHIME	32k byte

Table 2 表2

TESTING AND ADJUSTING

The built-in test program executes the following test and adjusting routines while in Test Mode.

RUNNING TEST PROGRAM

While holding down CLEAR and INSTRUMENT, switch the power ON. The unit is now in the test mode and the test program initiates test routines with TEST 1.

TEST 1. LED SEQUENTIAL LIGHTING

Upon entering test mode the program lights up LEDs, starting with MAIN KEY 1 through SCALE INDICATOR, PATTERN GROUP and CARTRIDGE (red and green alternately) and repeats.

Leave the LEDs lighting and go to TEST 2.

TEST 2. ALL LEDs AND LCD DOTS LIGHTING

Press ENTER and verify lighting of all LEDs and LCD dots.

Leave them lit and go to TEST 3.

TEST 3. SWITCHES AND ACCENT AMOUNT READING

Press ENTER. All LCD display will be cleared OFF. Referring to the illustration below, push numbered buttons 1-32 one by one and check for the lighting of corresponding dot on either Bass Drum (BonGo) or Snare Drum (Hi Conga) row on the display window.

Slide up or down ACCENT and verify that TEMPO MEASURE window reads 1 and 16 at the extremities of travel.

テストおよび調整

TR-707, TR-727 には回路機能チェックおよび調整用のプログラムが内蔵されています。このプログラムを走らせるにはテストモードに入る必要があります。

テストモード

CLEAR と INSTRUMENT ボタンを同時に押しながら電源をオンするとテストモードとなり、テスト 1 が自動的に実行されます。

テスト 1 LED 順次点灯

テストモードに入ると、メインキーの 1 から順次 LED が点灯して行きます。CARTRIDGE の LED は赤と緑が交互に点灯します。

LED の点灯はくり返されますが、そのままの状態でもテスト 2 へ進んで下さい。

テスト 2 LED および LCD 全点灯

ENTER を押します。全ての LED および LCD 上の全ドットが点灯する筈です。

そのままの状態でもテスト 3 へ進んで下さい。

テスト 3 スイッチおよびアクセントレベル読み込み

ENTER を押すと LCD のドットが消えます。パネル上のスイッチを押すと、右図に示す様に、対応した番号のドットが LCD の上に表示されます。

If not verified, go to ACCENT AMOUNT ADJUSTMENT below without exiting the test mode.

When all tests are satisfactory, turned the power off and on again to return to the normal operation mode (if necessary).

ACCENT AMOUNT ADJUSTMENT

This test must be carried out in the test mode and follow the tests above.

1. Set ACCENT at MIN and adjust TM2 of VOICING board for a transition point of "1" to/from "2" of TEMPO MEASURE display reading.
2. Set ACCENT at MAX and adjust TM3 for a transition point of "15" to/from "16" of TEMPO MEASURE display reading.

The unit will remain in the test mode until the power is turned OFF.

TEMPO CLOCK RATE ADJUSTMENT

This adjustment must be done in the normal operation mode.

1. Set TEMPO at FAST and adjust TM1 of VOICING board for 250 reading on TEMPO MEASURE window.

次に、アクセント（AC）つまみを上下させるとLCDのTEMPO/MEASURE部に数字が表示されます。MINの位置で"1"、MAXで"16"とならない場合は、次のアクセントレベル調整へ進んで下さい。

調整が不要で、通常モードに戻るには一旦電源をオフして下さい。

アクセントレベル調整

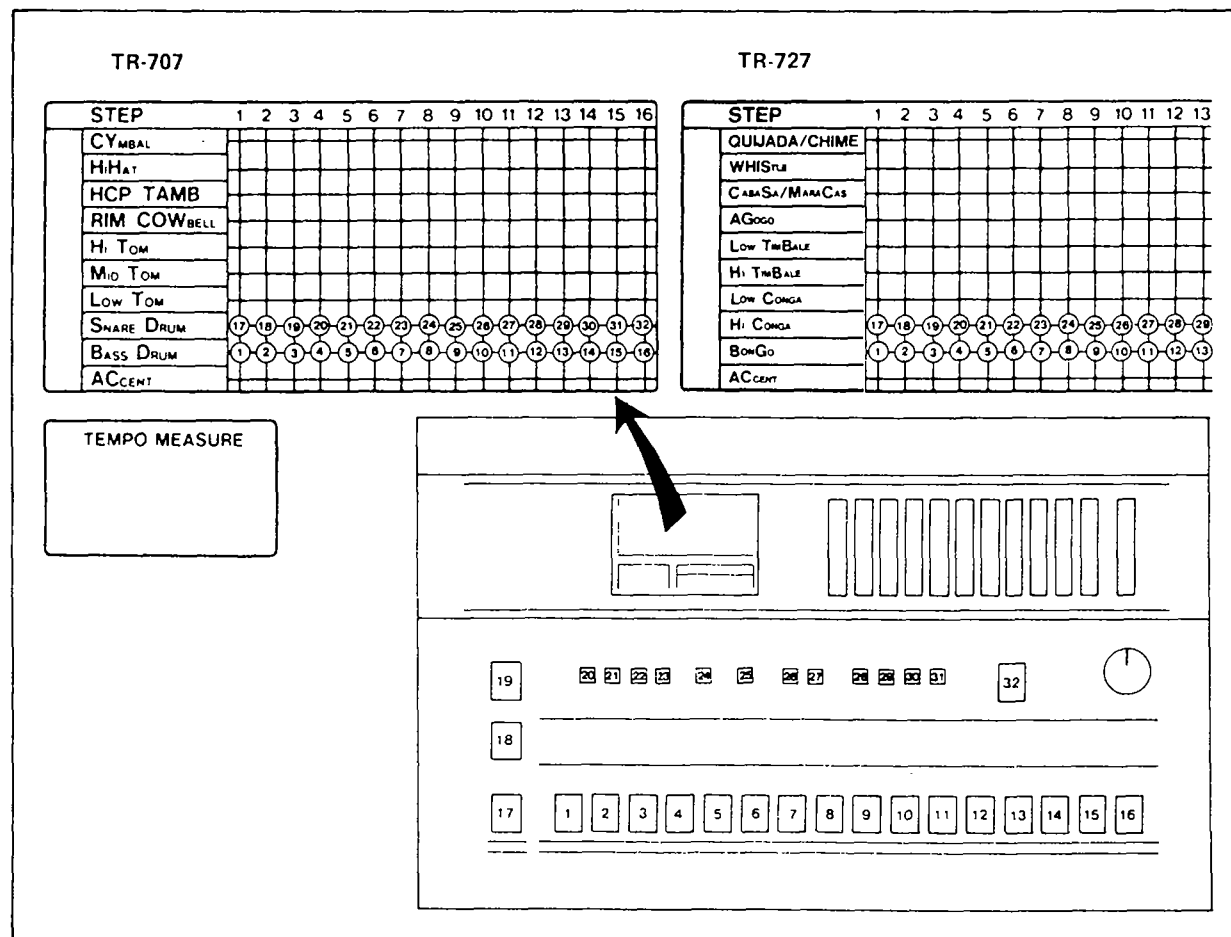
本調整はテストモードで行ないます。上記のテストの後で行なって下さい。

1. アクセント（AC）をMINにセットし、TM2（ボイシング基板）でTEMPO/MEASUREの表示が"1"か"2"になる臨界点に調整します。
2. ACをMAXにセットし、TM3で表示が"15"か"16"になる臨界点に調整します。

テンポ調整

本調整は通常モードで行ないます。テストモードになっている場合は、一度電源をオフして下さい。

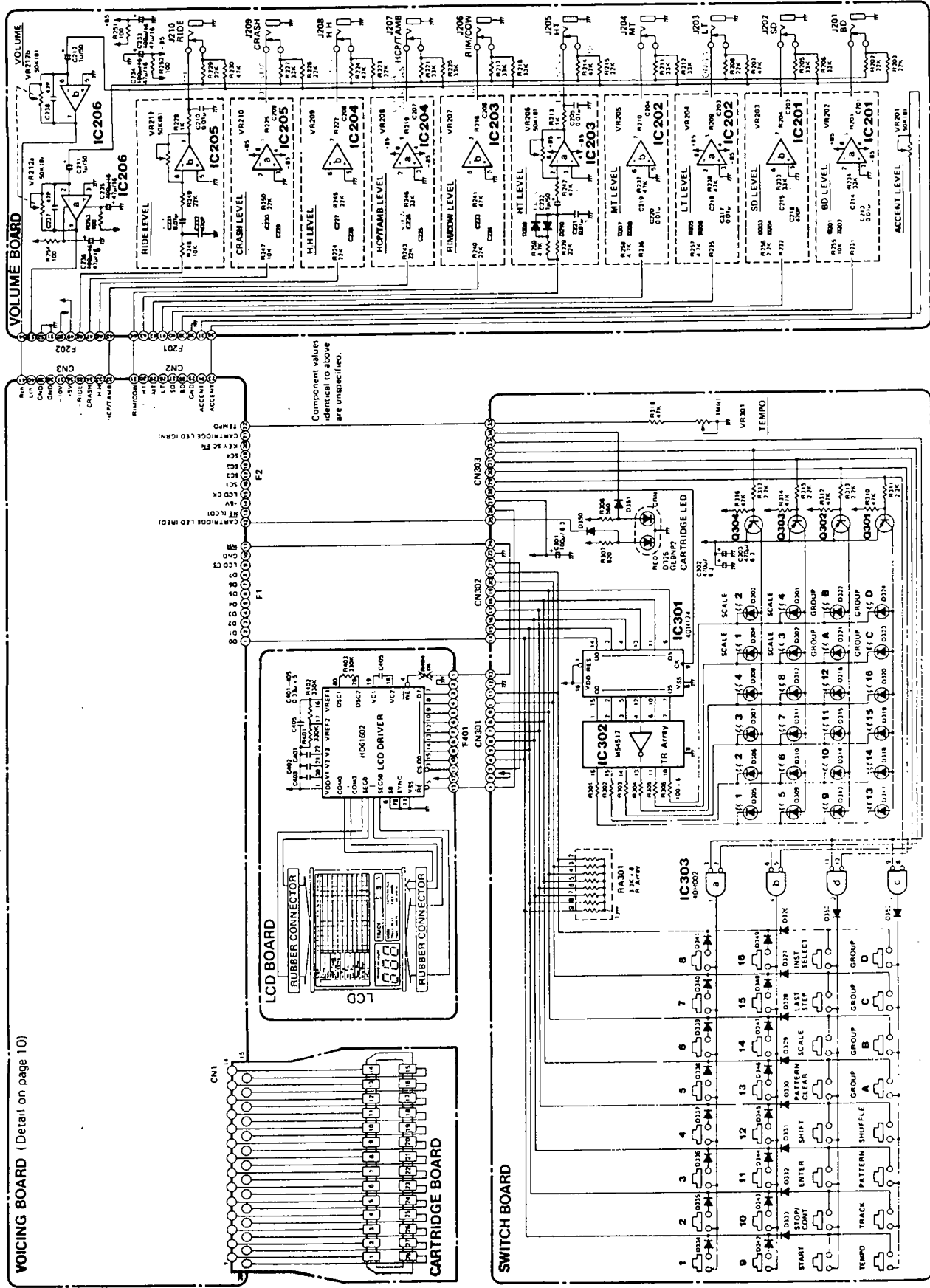
TEMPOをFASTにセットし、TM1（ボイシング基板）でTEMPO/MEASUREの表示が250になる様調整します。



2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39

TR-707/IR-727 GENERAL CIRCUIT DIAGRAM

VOICING BOARD (Detail on page 10)



MAIN KEY LED

VOLUME BOARD

TR-707 7313605000 (pcb 2291098002)

TR-727 7313805000 (pcb 2292019000)

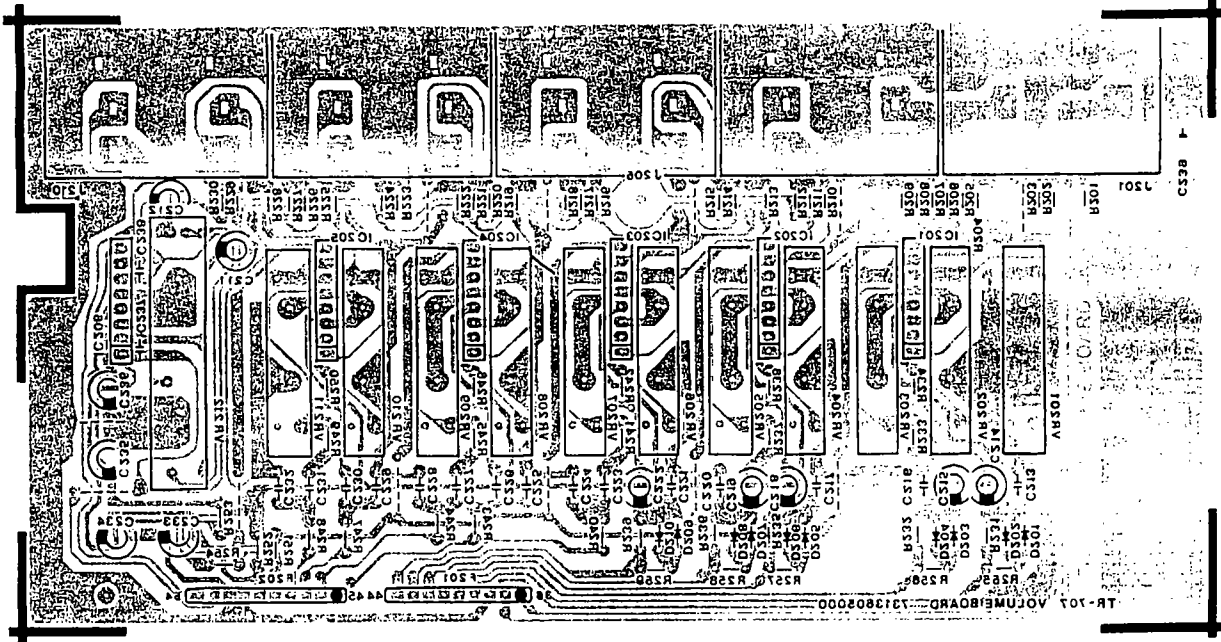
View from foil side

BELOW PCB LAYOUT For TR-707

TR-727's: identical to TR-707's except for those represented in red in the circuit diagram left.

下の基板図はTR-707用です。

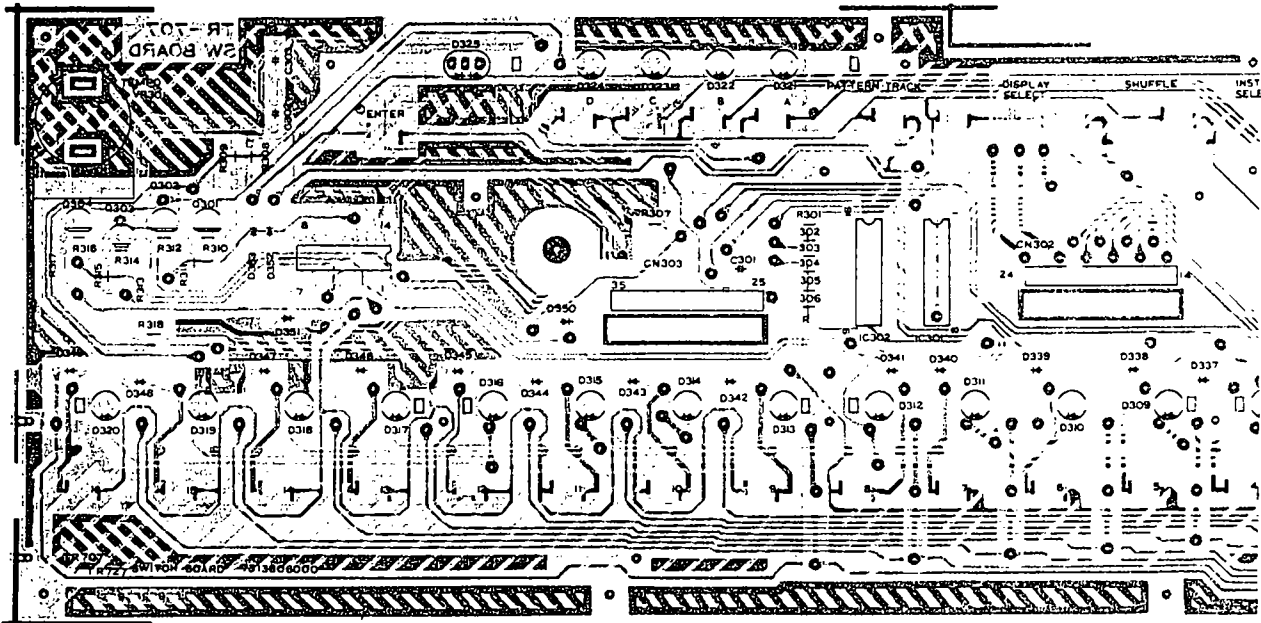
TR-727の場合は回路図の赤線表示に従って相違点を確認して下さい。



SWITCH BOARD

7313606000 (pcb 2291097903)

View from foil side



UT For TR-707

R-707's except for those represented in red
diagram left

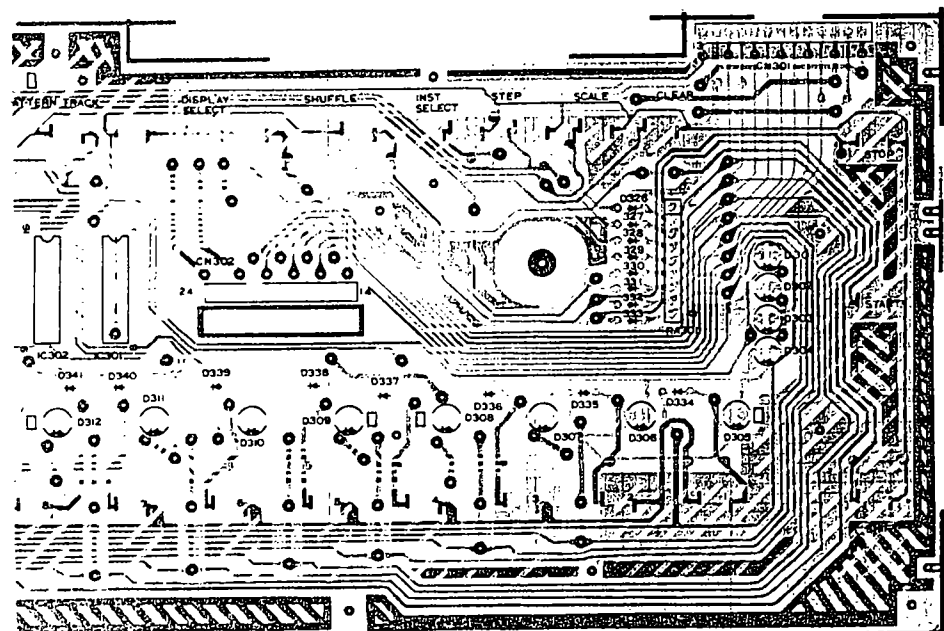
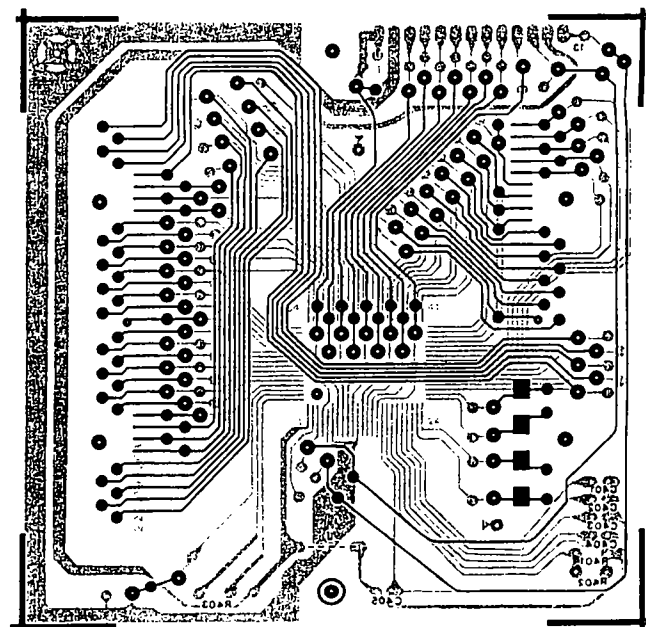
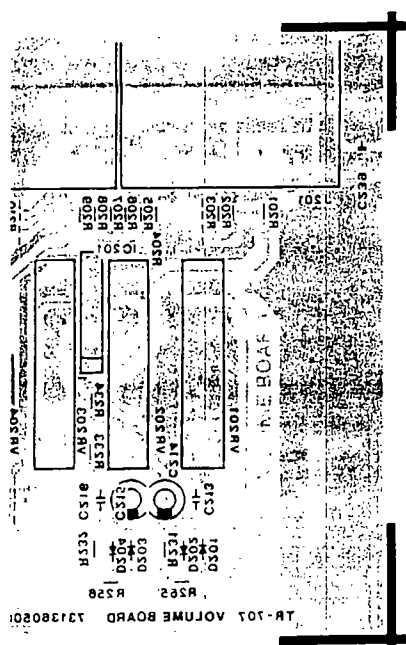
緑表示に従って相違点を確認して下さい。

LCD BOARD

7313607000

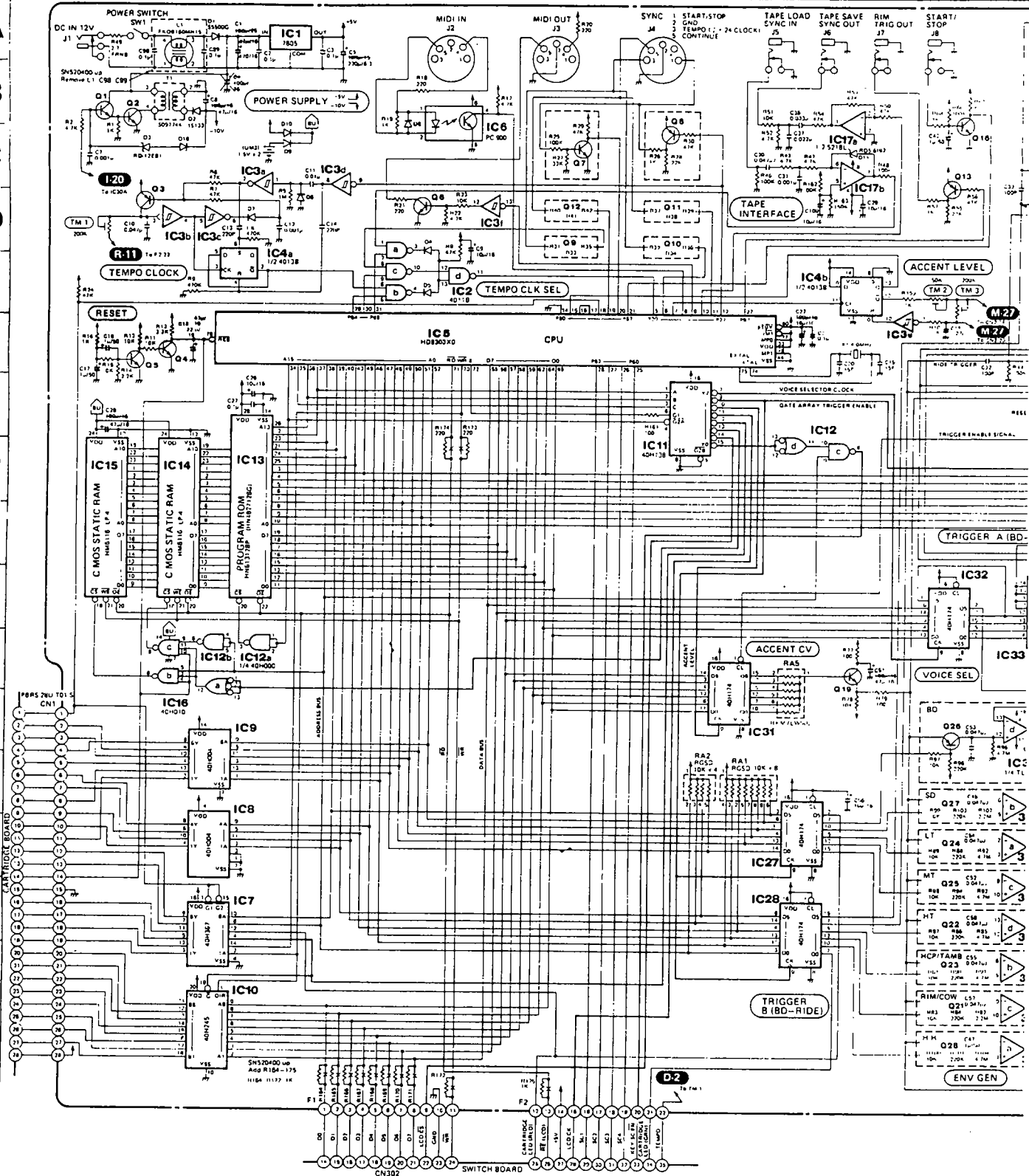
(pcb 2291098203)

View from foil side



1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

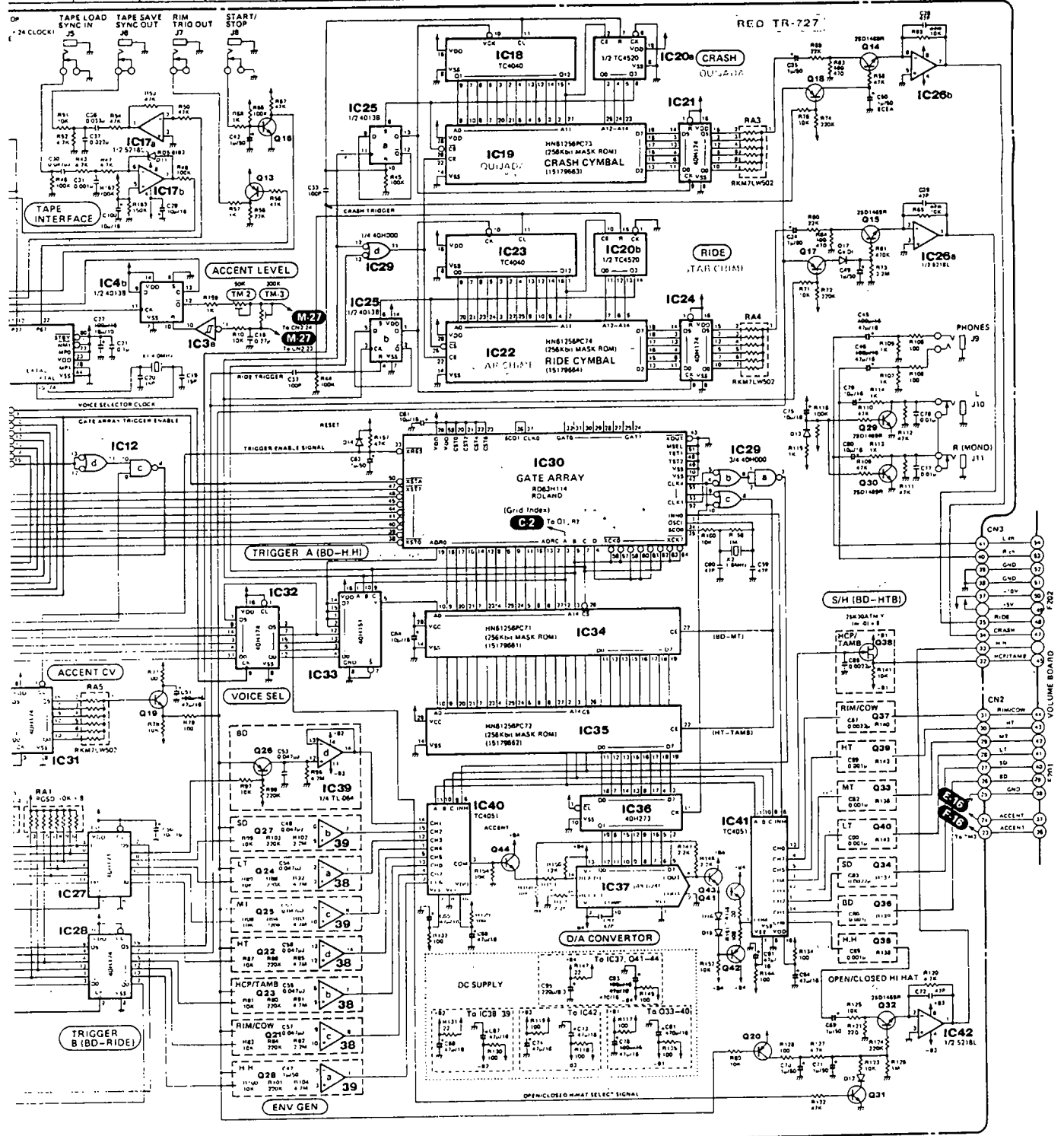
A
B
C
D
E
F
G
H
I
J
K
L
M
N
O
P
Q
R
S



CN302

SWITCH BOARD

12 13 14 15 16 17 18 19 20 21 22 23 24 26 27 28



VOICING BOARD

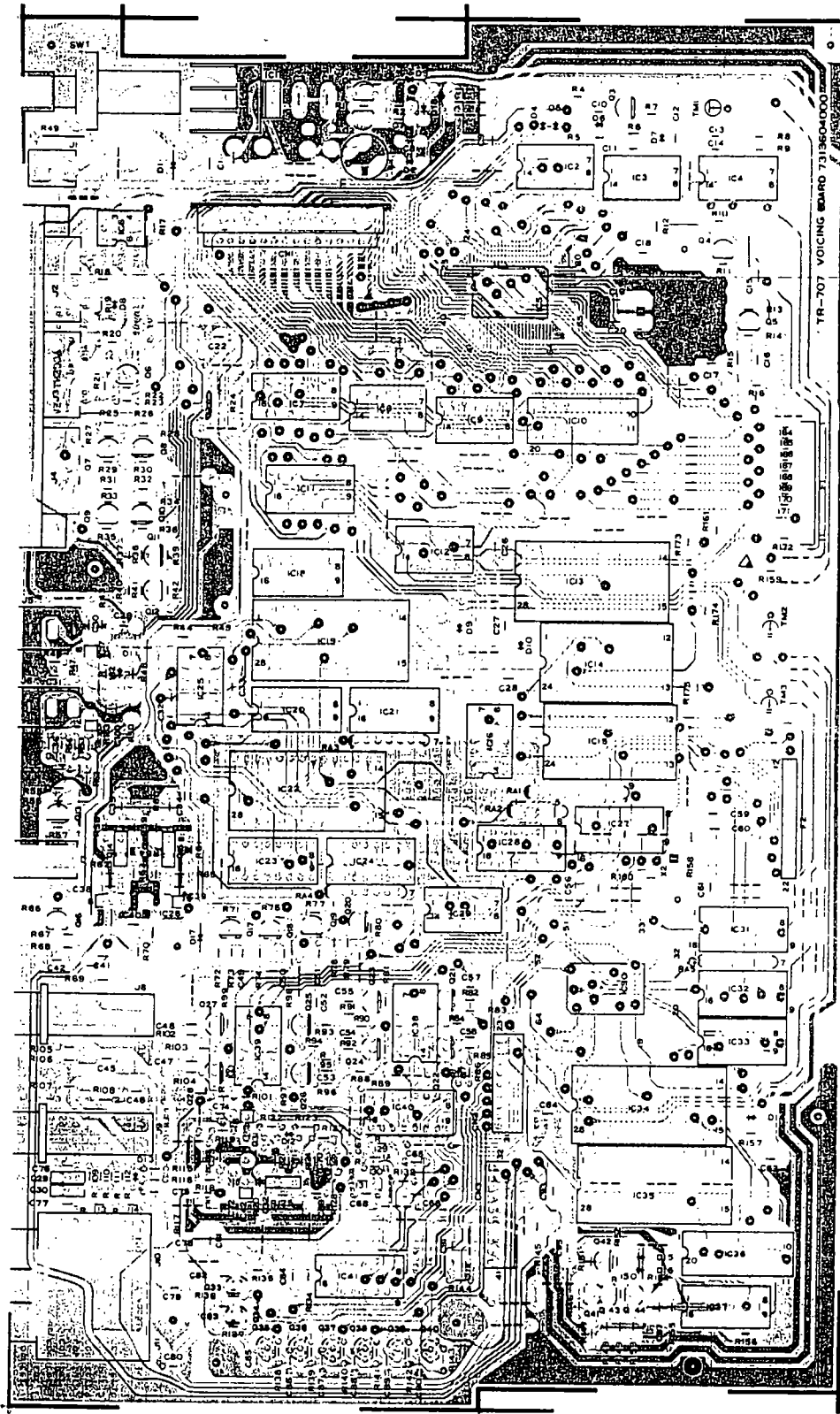
TR-707 7313604000 (pcb 2291098102)
TR-727 7313804000 (pcb 2292018900)

BELOW PCB LAYOUT For TR-707

TR-727's identical to TR-707's except for those represented in red in the circuit diagram left.

下の基盤図はTR-707用です。

TR-727の場合は同図の赤線表示に従って組立点を修正して下さい。

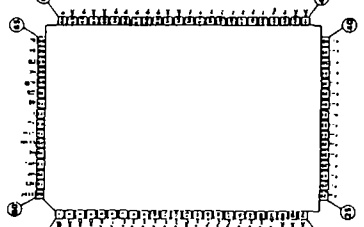


View from foil side

IC DATA

CPU HD6303X

Pin Configuration (Top View)

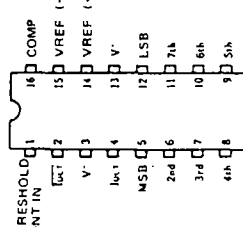


Port Assignment

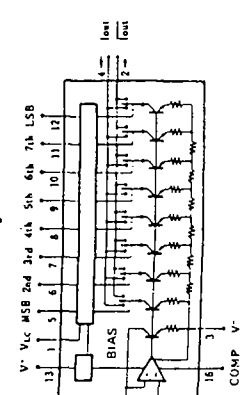
PIN NO.	PORT NAME	DESCRIPTION
1	NMI	Unused, pulled up +5V
2-4	NC	Unused, open
5	P20	Input, TEMPO CLOCK (DIN)
6	P21	output, TEMPO CLOCK (DIN)
7	P22	output, ACCEPT LEVEL input trigger for Internal ADC
8	P23	input, MIDI IN
9	P24	output, MIDI OUT
10	P25	output, COME SYNC (DIN)
11	P26	output, COME SYNC (DIN)
12	P27	output, START/STOP (DIN)
13	NC	Unused, open
14	P50	IRQ1 unused, pulled down
15	P51	input, ACCEPT LEVEL
16	P52	RR unused, pulled up +5V
17	P53	BALT unused, pulled up +5V
18	P54	RAM cartridge control
19	P55	input, COMT START (DIN IN)
20	P57	input, START/STOP (DIN IN)
21	NC	Unused, open
22-24	NC	Unused, scanning signal to LED and KEY
25-28	P60-P63	output, Internal TEMPO CLOCK
29	P64	output, Internal TEMPO CLOCK
30	P65	output, TAPE SYNC TEMPO CLOCK
31	P66	output, Trigger (RIM SHOT-TR-707)(BI ADOCO-TR-727)
32	P67	output, +5V power supply
33	Vcc	output, address A15---A19
34-40	A15-A9	output, address A8
41-42	NC	Unused, open
43	Vcc	output, address A7---A0
44	Vcc	output, open
45-52	A7-A0	data bus D7---D3
53-54	NC	Unused, open
55-59	D7-D3	data bus D2
60-61	NC	data bus D1---D0
62	D2	output, unused
63	NC	Unused, open
64-65	D1-D0	output, unused
66	BA	output, system clock 10MHz
67	LLR	terminal, Xtal
68	NC	Unused, open
69	W4	input, HCU mode setting pulled up +5V
70	W4	input, HCU mode setting pulled down CHD
71	W4	Unused, pulled up +5V (active low)
72	E	Unused, open
73	Vss	Unused, open
74	XTAL	terminal, Xtal or external system clock in
75	EXTAL	Unused, open
76	NC	Unused, open
77	MFO	input, HCU mode setting pulled up +5V
78	RES	input, HCU mode setting pulled down CHD
79	RES	input, HCU mode setting pulled up +5V (active low)
80	STRV	Unused, open

μPC624C

Pin Configuration (Top View)

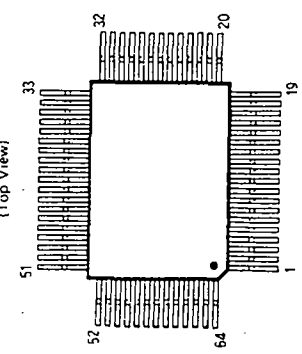


Block Diagram



GATE ARRAY RDS3H114

Pin Configuration (Top View)



PK name	PK name	PK name			
1	INH0	23	CS1 6	45	Y5T5
2	ADRC	24	GATE7	46	Y5T6
3	A	25	GATE6	47	Y5T7
4	0	26	VDD	48	Y5T1
5	B	27	GATE5	49	Y5T2
6	ADR7	28	GATE4	50	Y5T4
7	C	29	GATE3	51	WSEL
8	ADR6	30	GATE2	52	CLK1
9	ADR5	31	GATE1	53	CLK2
10	VSS	32	GATE0	54	CLK3
11	ADR9	33	YRES	55	CLK4
12	ADR8	34	OSC	56	YCK0
13	ADR8	35	SC00	57	YCK1
14	ADR4	36	SC01	58	VDD
15	ADR3	37	CLK0	59	YCK2
16	ADR4	38	Y5T0	60	YCK3
17	ADR2	39	Y5T1	61	YCK4
18	ADR1	40	Y5T2	62	YCK5
19	ADR0	41	Y5Y3	63	YCK6
20	EST0	42	VSS	64	YCK7
21	EST1	43	YOUT		
22	EST4	44	Y5T4		

Multiple Address Counters

DESIGNATION	PIN	DESCRIPTION	I/O
CS1	0	20	counter 0
	1	21	counter 1
	2	22	counter 2
	3	23	counter 3
	4	24	counter 4
	5	25	counter 5
	6	26	counter 6
AST	0	38	counter 0
	1	39	counter 1
	2	40	counter 2
	3	41	counter 3
	4	42	counter 4
	5	43	counter 5
	6	44	counter 6
	7	45	counter 7
ACK	0	39	counter 0
	1	40	counter 1
	2	41	counter 2
	3	42	counter 3
	4	43	counter 4
	5	44	counter 5
	6	45	counter 6
	7	46	counter 7
ADR	0	19	address(ADRO-ADRC) out enable, active low; high-imp. z
	1	18	counter 0
	2	17	counter 1
	3	16	counter 2
	4	15	counter 3
	5	14	counter 4
	6	13	counter 5
	7	12	counter 6
	8	11	counter 7
	9	10	counter 8
	10	9	counter 9
	11	8	counter 10
	12	7	counter 11
	13	6	counter 12
	14	5	counter 13
	15	4	counter 14
	16	3	counter 15
	17	2	counter 16
	18	1	counter 17
	19	0	counter 18
A	3	MUX, DMUX	
B	7	channel select	
D	4	DMUX inhibit	
INH0	1	DMUX inhibit	
OSCI	34	internal clock	
SC00	35	clock	
CLK	0	37	Generator
	1	52	system clock out 1.0MHz
	2	53	system clock in 1.0MHz
	3	54	nc
	4	55	system clock 100KHz
ARRES	31	reset pulse, active low	
TEST1	48	counter 12/13 bit select	
TEST2	49	IC test	
Vss	10	42	power supply +5V
VDD	26	32	counter gate output low-counter running
CA1	0	31	counter gate output low-counter running
	1	30	counter gate output low-counter running
	2	29	counter gate output low-counter running
	3	28	counter gate output low-counter running
	4	27	counter gate output low-counter running
	5	26	counter gate output low-counter running
	6	25	counter gate output low-counter running
	7	24	counter gate output low-counter running

