

Figure 0-1
ABSTRACT SCHEMATIC

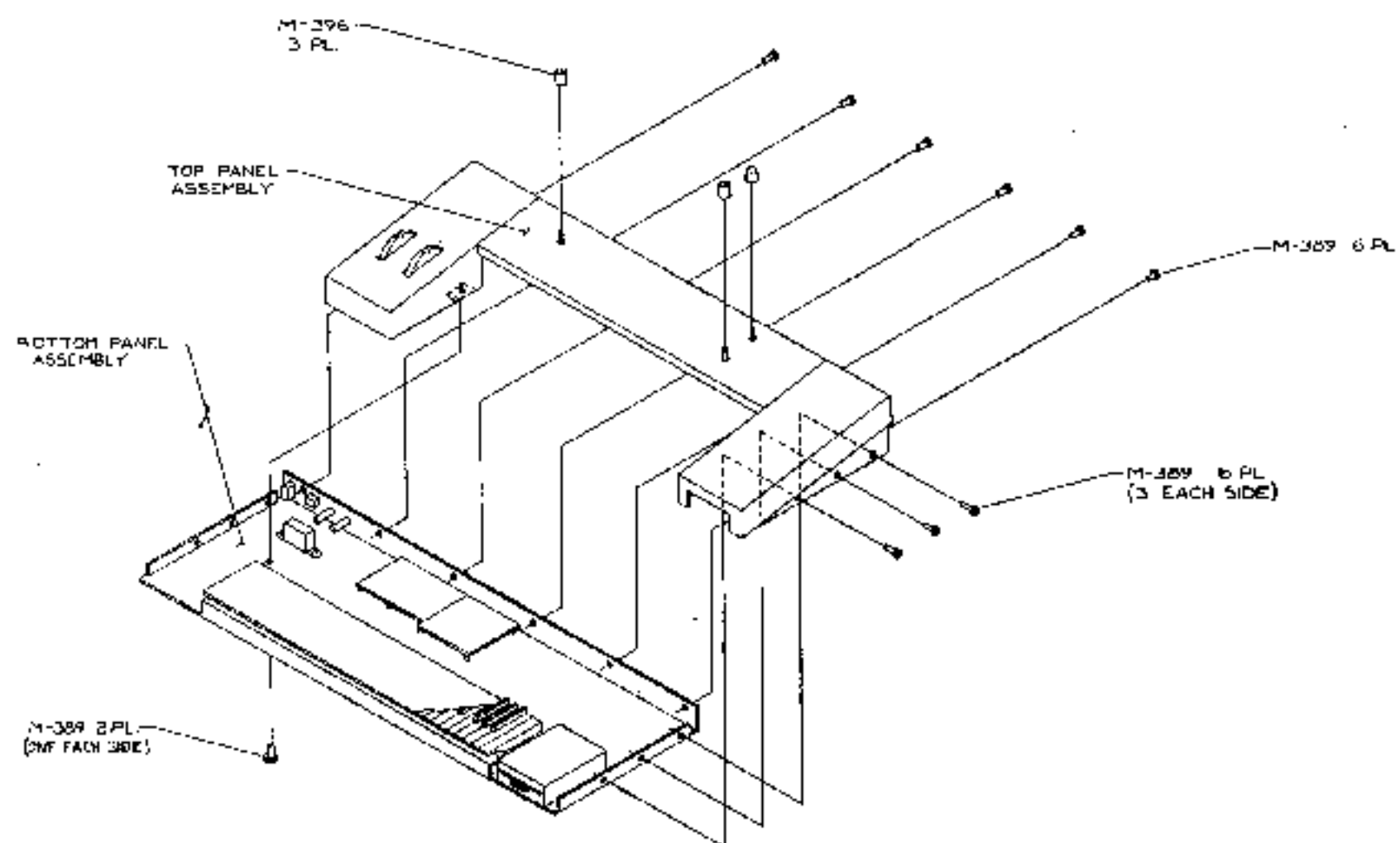


Figure 0.2
POSITION OF BOTTOM PANEL SCREWS

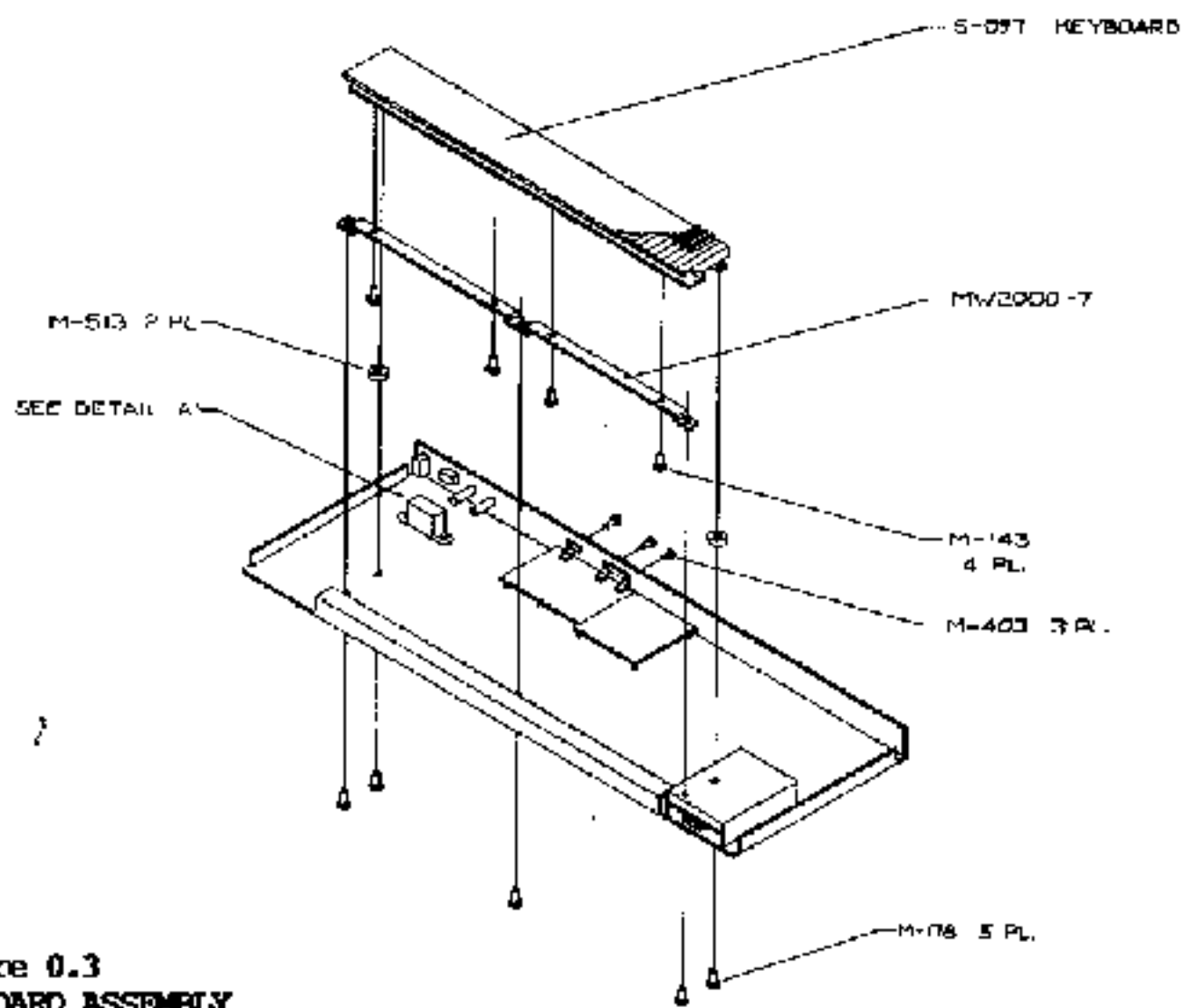


Figure 0.3
KEYBOARD ASSEMBLY

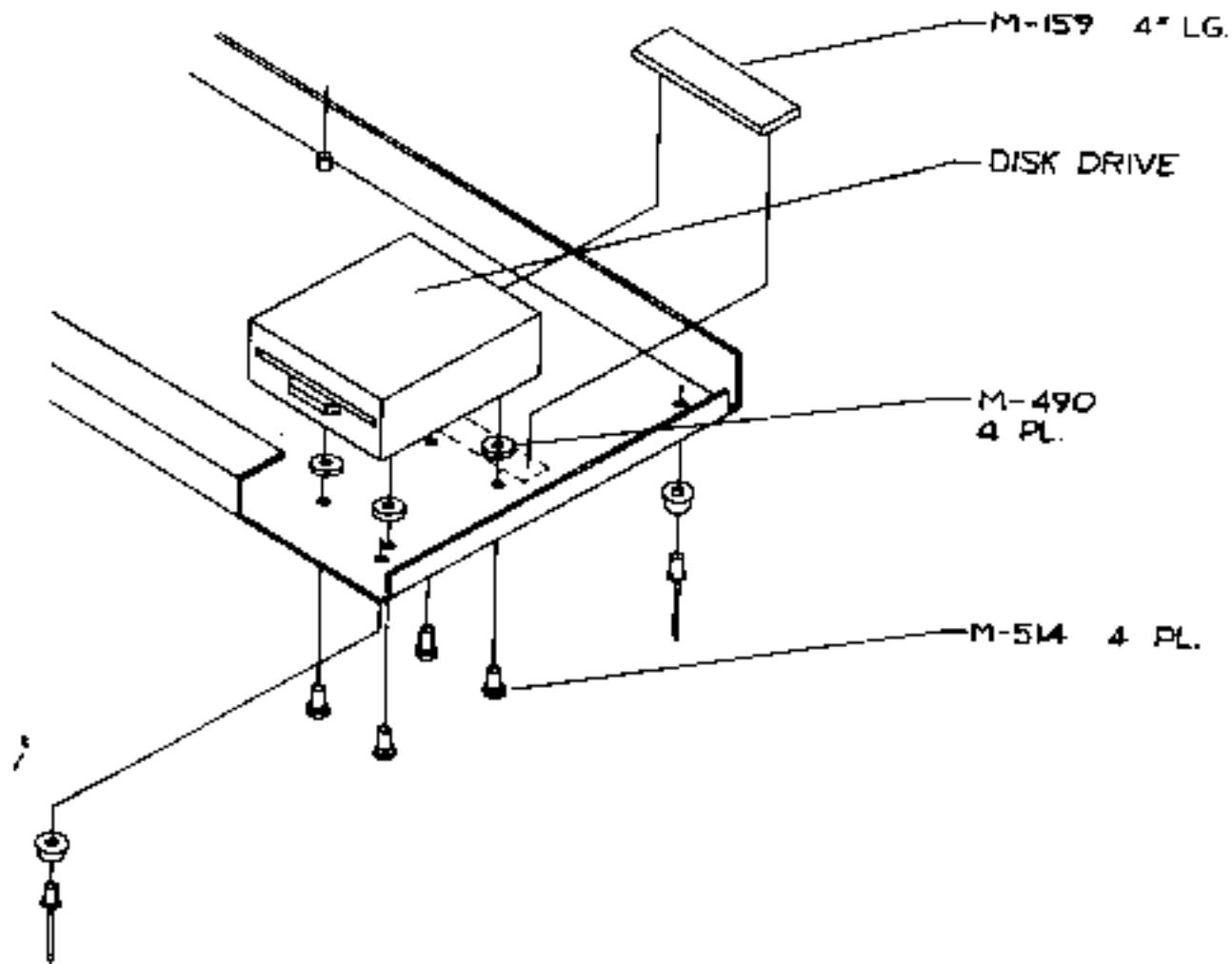
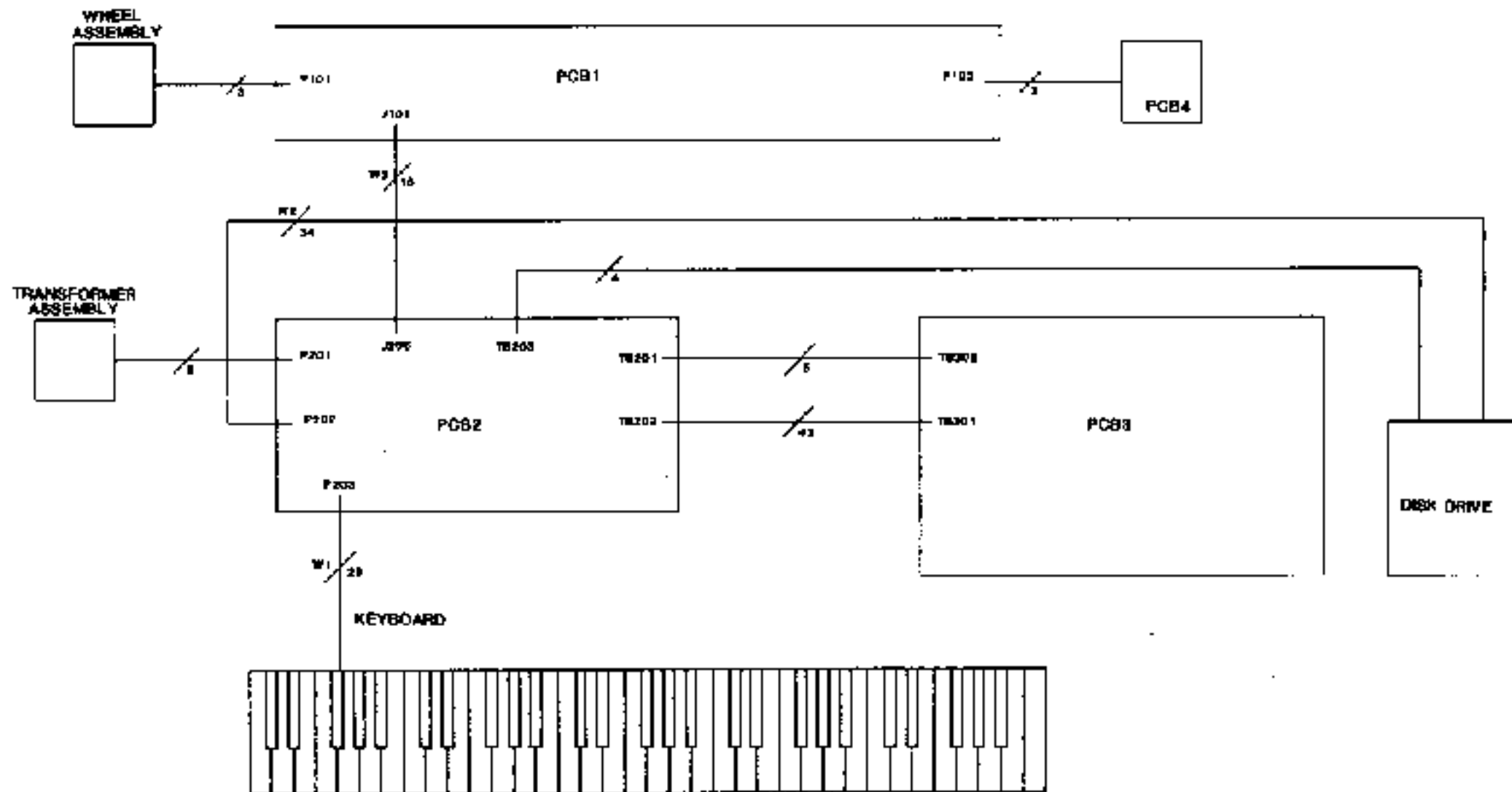


Figure 0.4
POSITION OF DISK DRIVE SCREWS

Figure 0.5
INTERCONNECTION DIAGRAM



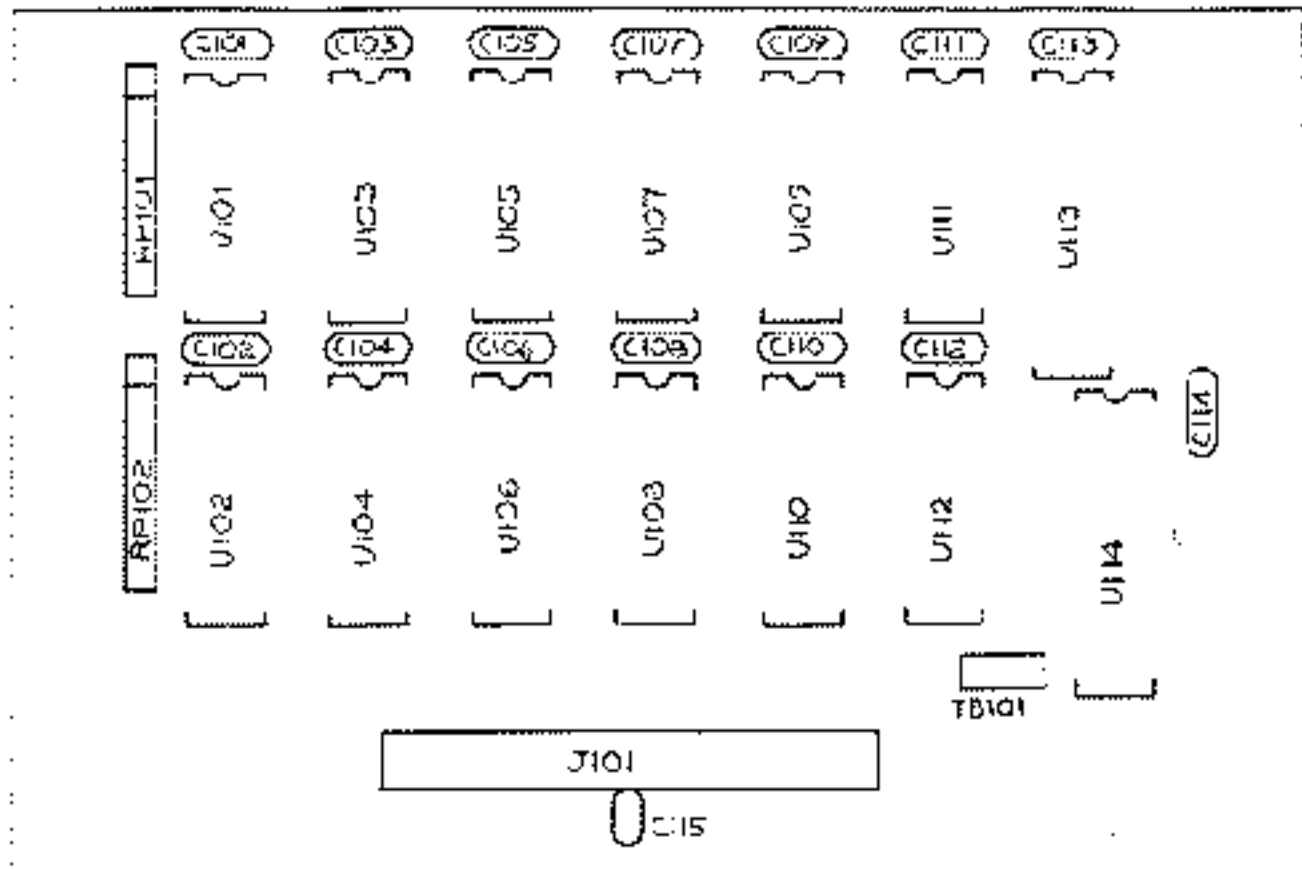
4

3

2

1

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

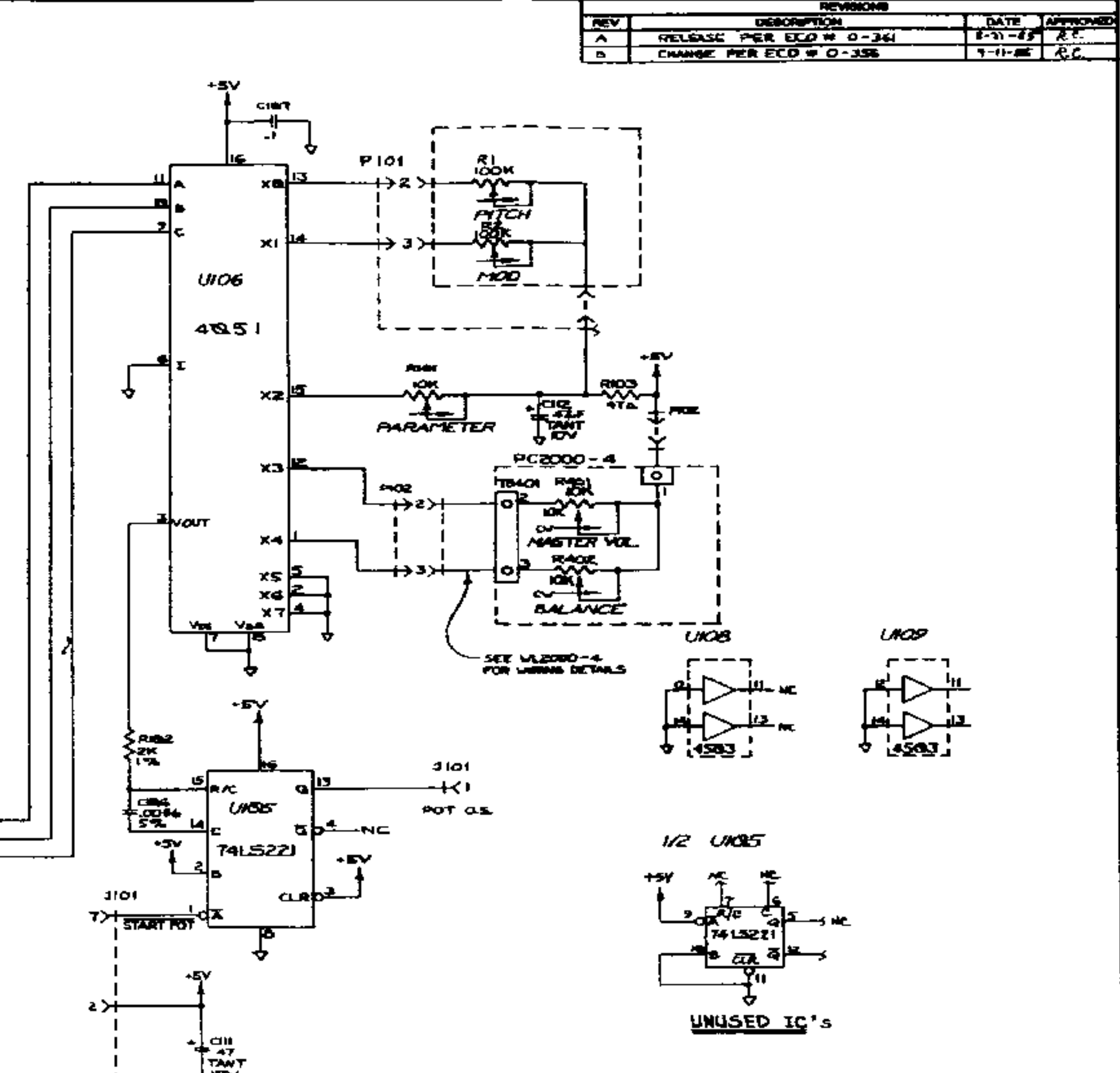
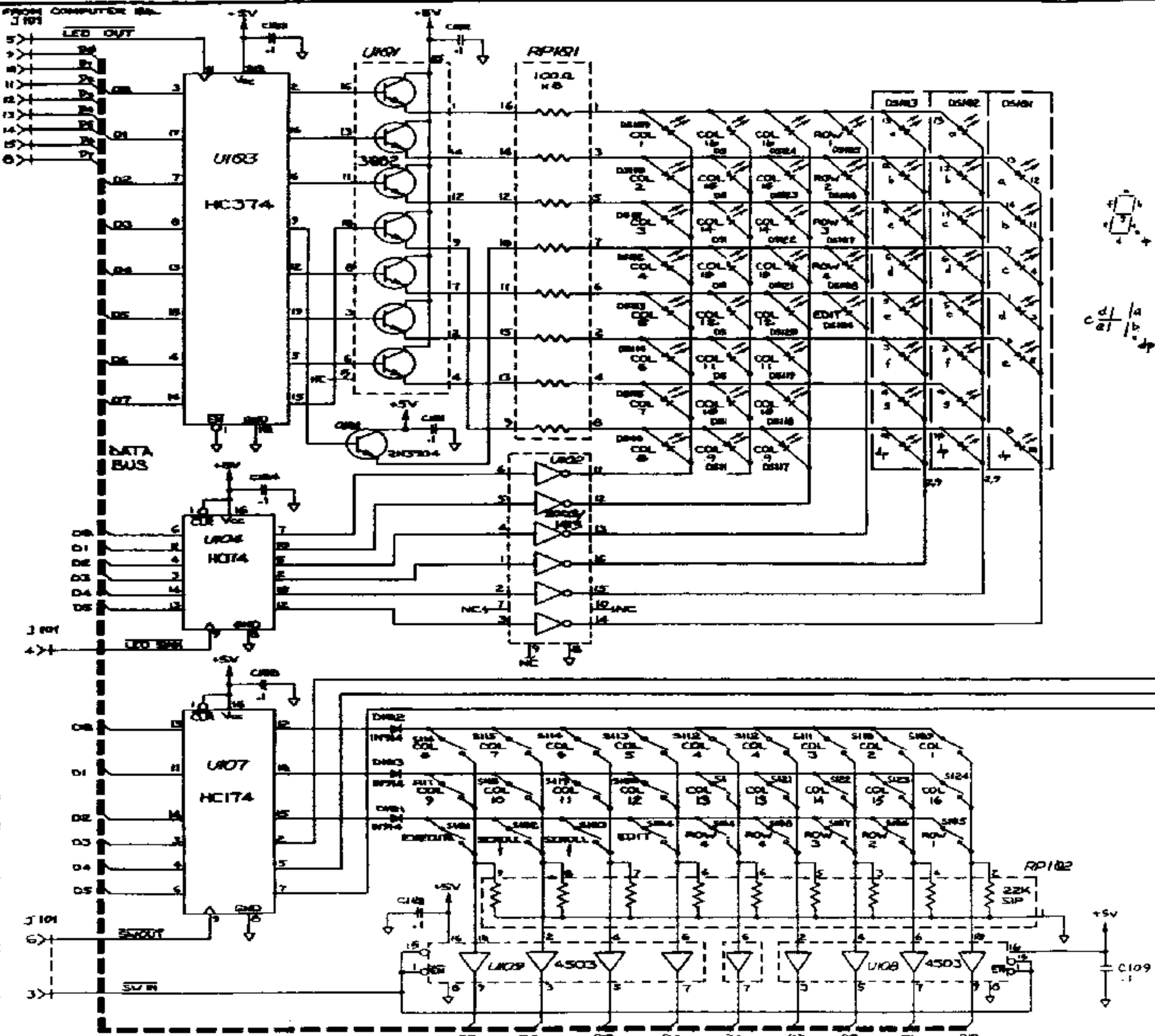


	872
NEXT ABBY	USPO PM
APPLICATION	

DO NOT SCALE DRAWING	
APPROVALS	DATE
DRAWN <i>Ron Chaffin</i>	7-9-88
CHECKED	7-9-88
ELCD, ENGR	
WFO, CHGN	
WFO, ENGR	

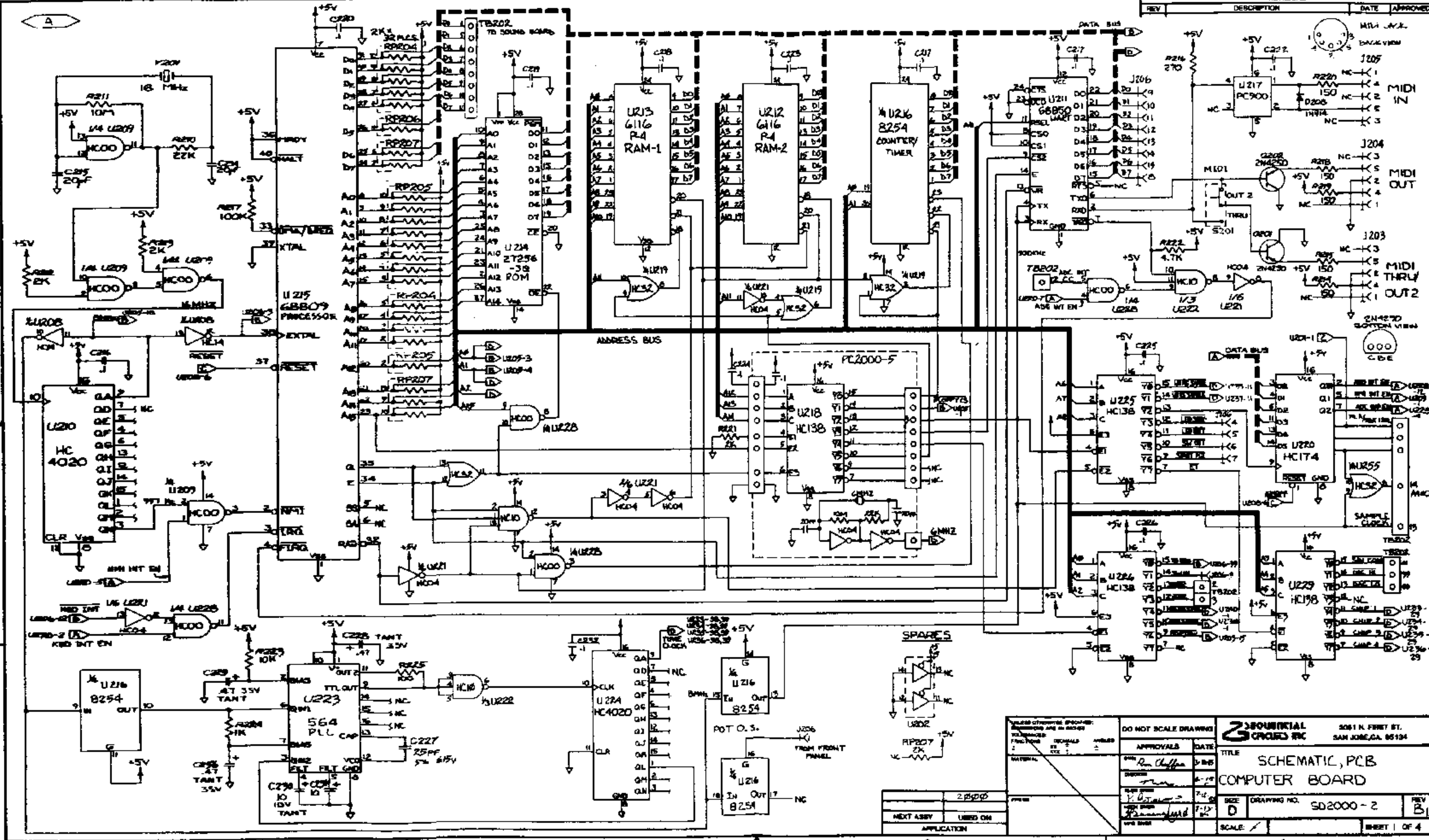
FEDERAL CIRCUITS, INC. 305 F.N. FIRST ST. SAN JOSE, CA 95134	
TITLE DESIGNATOR MAP	
S.C.	DRAWING NO. PP877
REV S1	SCALE: 2/1
SHEET 1 OF 1	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	RELEASE PER ECD # 0-341	8-31-85	R.C.
B	CHANGE PER ECD # 0-356	7-11-86	R.C.



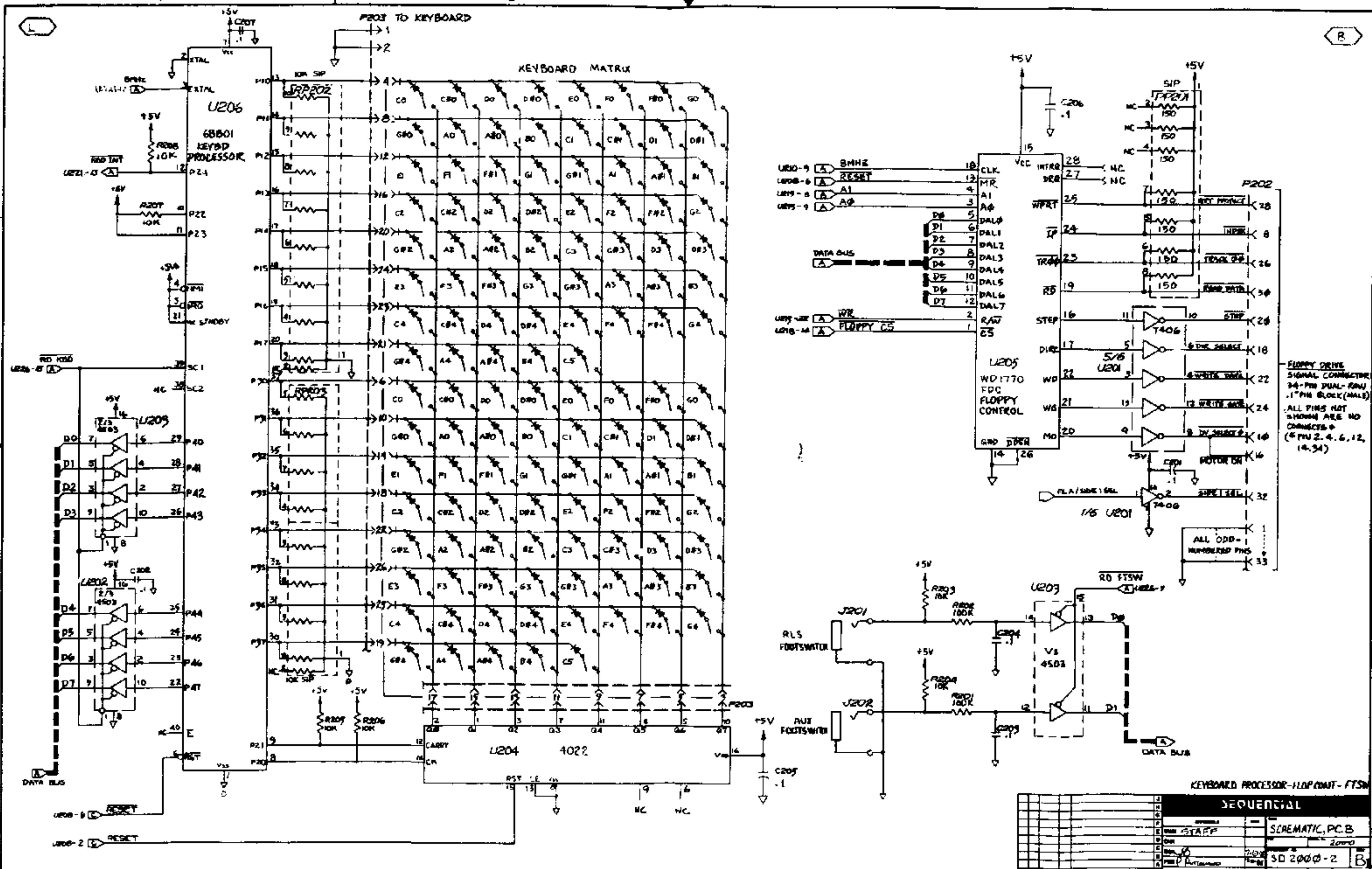
DO NOT SCALE DRAWING		SEQUENTIAL GROUP INC.		3081 N. FIRST ST. SAN JOSE, CA. 95134	
APPROVALS	DATE	TITLE			
BY: <i>Ron Chaffin</i>	8-1-85	FRONT PANEL BD. SCHEMIO			
DESIGNED		SIZE	DRAWING NO.	REV	
		D	SD2000-1	B	
SCALE	N/A	SHEET 1 OF 1			

APPLICATION	
NEXT ASSY	USED ON



REV	DESCRIPTION	DATE	APPROVED
1			

DO NOT SCALE DRAWING		3 SUBSISTENTIAL		5051 N. FIRST ST.	
APPROVALS		DATE		SAN JOSE, CA. 95134	
TITLE		SCHEMATIC, PCB			
DRAWING NO.		SD2000-2		REV B1	
SCALE		1:1		SHEET 1 OF 4	

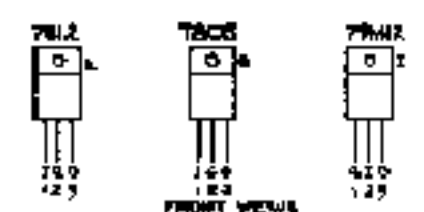
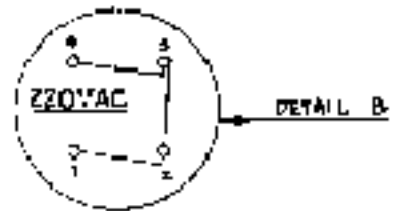
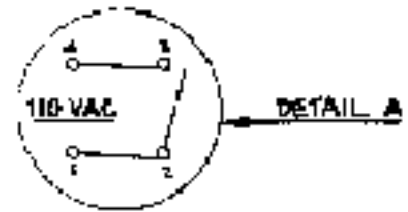
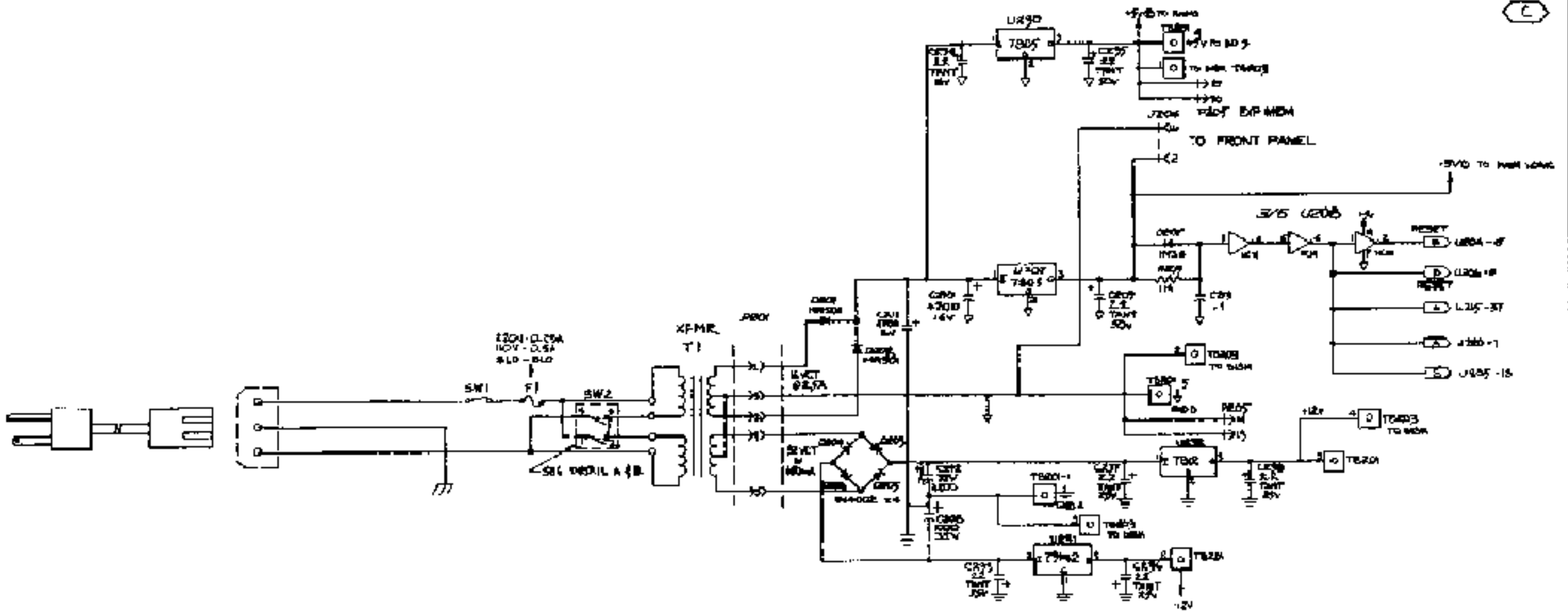


FLOPPY DRIVE SIGNAL CONNECTOR 34-PIN DUAL-ROW .1" PITCH BLOCK (MALE)
 ALL PINS NOT SHOWN ARE NO CONNECTS
 (* PIN 2, 4, 6, 12, 14, 34)

KEYBOARD PROCESSOR-110P CONT-FTSW

SEQUENTIAL	
1	SCHEMATIC, PCB
2	SCHEMATIC, PCB
3	SCHEMATIC, PCB
4	SCHEMATIC, PCB
5	SCHEMATIC, PCB
6	SCHEMATIC, PCB
7	SCHEMATIC, PCB
8	SCHEMATIC, PCB
9	SCHEMATIC, PCB
10	SCHEMATIC, PCB
11	SCHEMATIC, PCB
12	SCHEMATIC, PCB
13	SCHEMATIC, PCB
14	SCHEMATIC, PCB
15	SCHEMATIC, PCB
16	SCHEMATIC, PCB
17	SCHEMATIC, PCB
18	SCHEMATIC, PCB
19	SCHEMATIC, PCB
20	SCHEMATIC, PCB
21	SCHEMATIC, PCB
22	SCHEMATIC, PCB
23	SCHEMATIC, PCB
24	SCHEMATIC, PCB
25	SCHEMATIC, PCB
26	SCHEMATIC, PCB
27	SCHEMATIC, PCB
28	SCHEMATIC, PCB
29	SCHEMATIC, PCB
30	SCHEMATIC, PCB
31	SCHEMATIC, PCB
32	SCHEMATIC, PCB
33	SCHEMATIC, PCB
34	SCHEMATIC, PCB
35	SCHEMATIC, PCB
36	SCHEMATIC, PCB
37	SCHEMATIC, PCB
38	SCHEMATIC, PCB
39	SCHEMATIC, PCB
40	SCHEMATIC, PCB

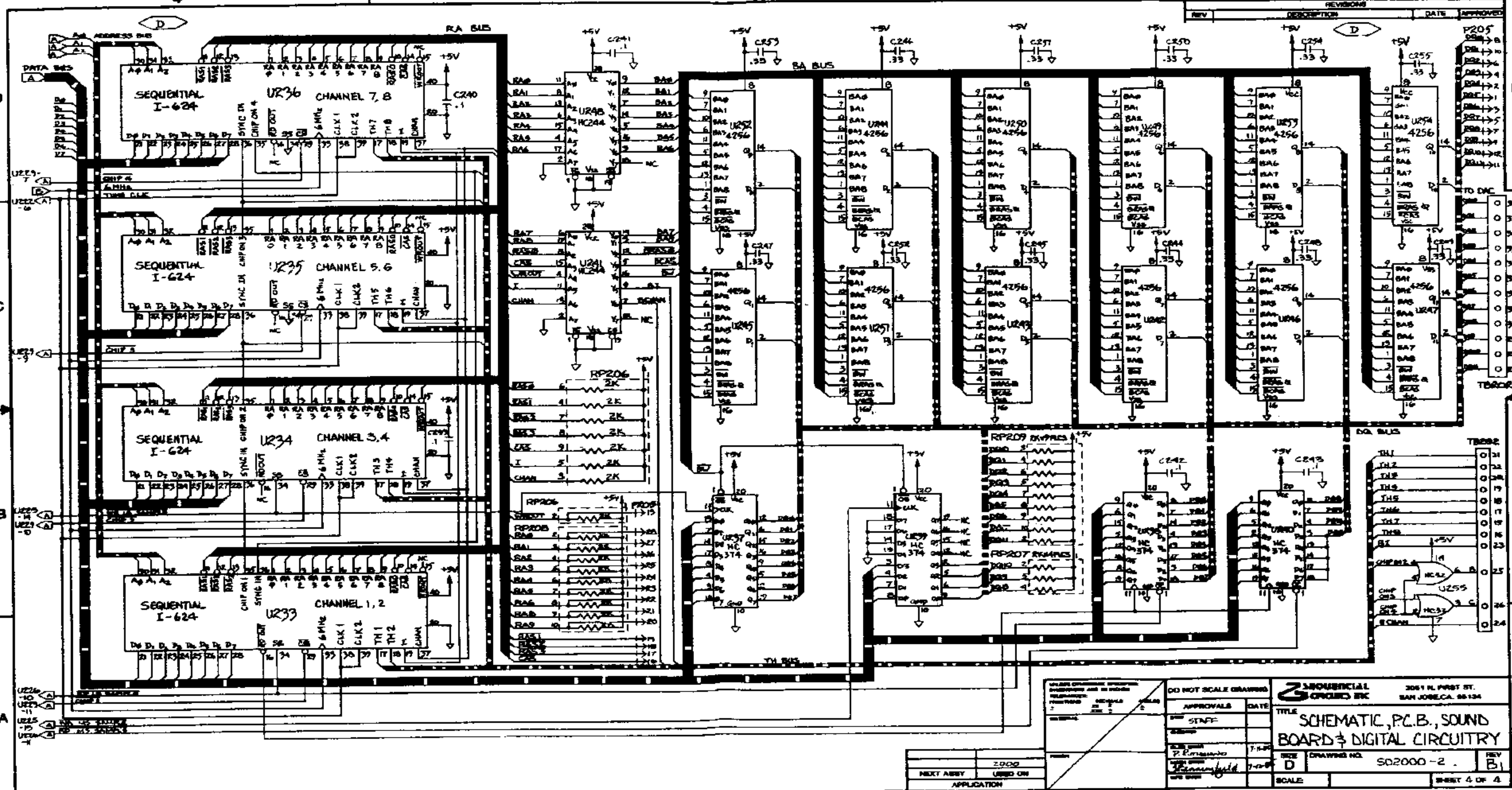
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



↓ DIGITAL GND
 ⊥ ANALOG GND
 ⏏ CHASSIS GND

		3001 N. FIRST ST. SAN JOSE, CA 95134	
TITLE: SCHEMATIC, PC B., POWER SUPPLY			
DES: D DATE:	DRAWING NO: 502000-2	REV: 1	SHEET 3 OF 1

22 Rev 1 7-85



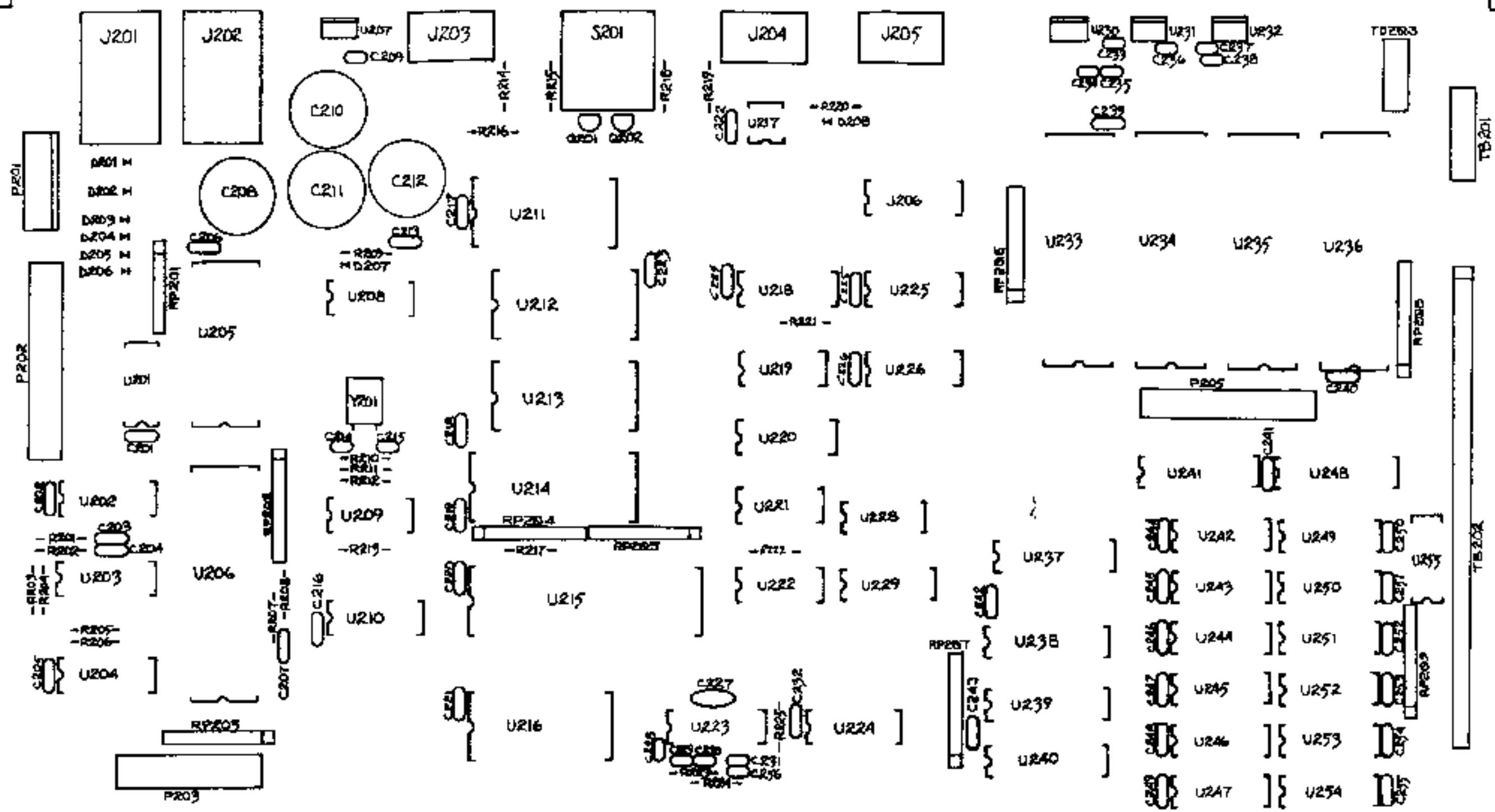
REV	DESCRIPTION	DATE	APPROVED

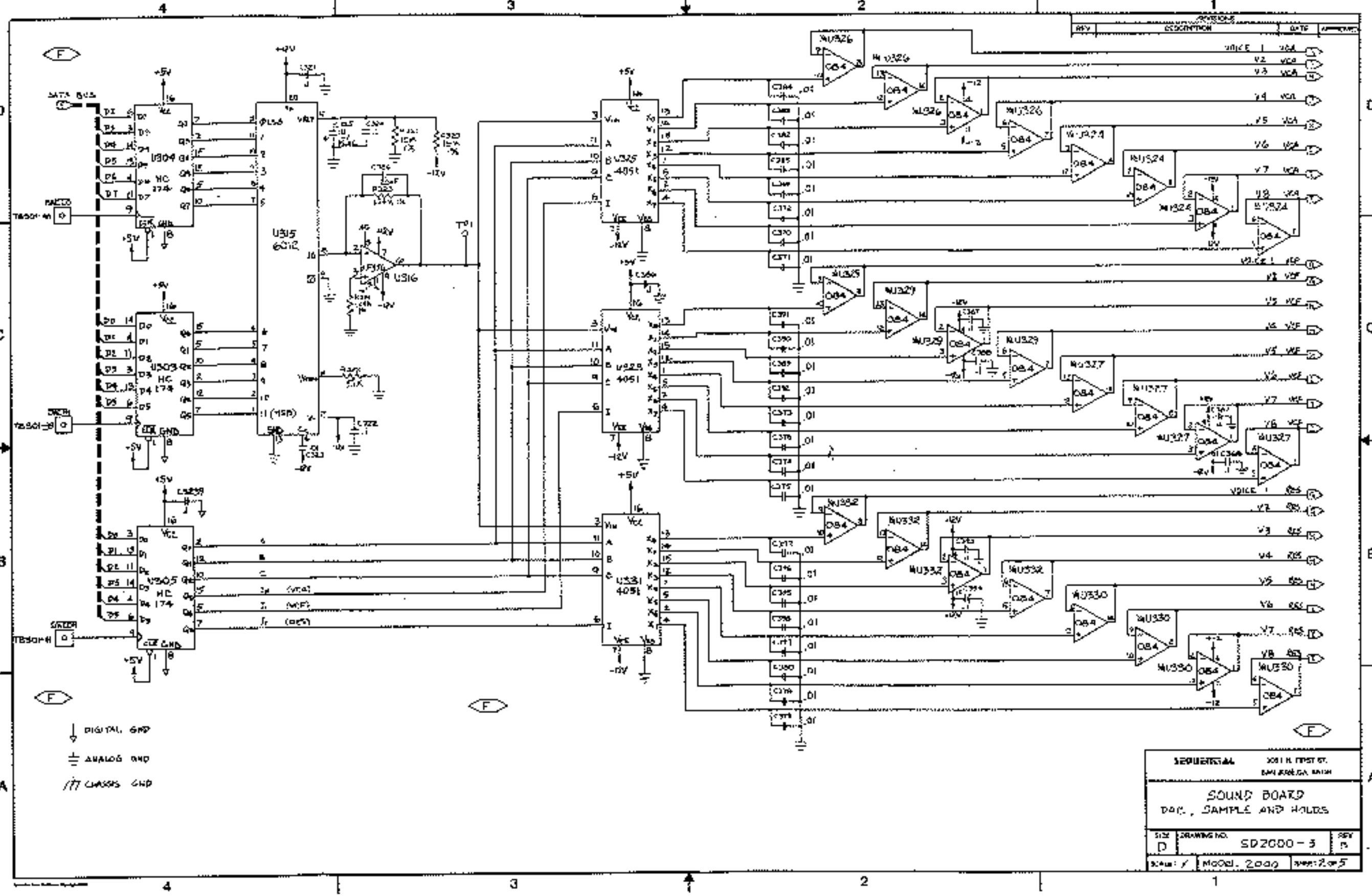
DO NOT SCALE DRAWING
 APPROVALS: _____ DATE: _____
 STAFF: _____
 P. [Signature]
 [Signature]

3 INDUSTRIAL CIRCUITS INC.
 2051 N. FIRST ST.
 SAN JOSE, CA 95134

TITLE: SCHEMATIC, P.C.B., SOUND BOARD & DIGITAL CIRCUITRY
 REV: B1
 DRAWING NO: S02000-2
 SHEET 4 OF 4

	ZDDG
NEXT ASSY	USED ON
APPLICATION	

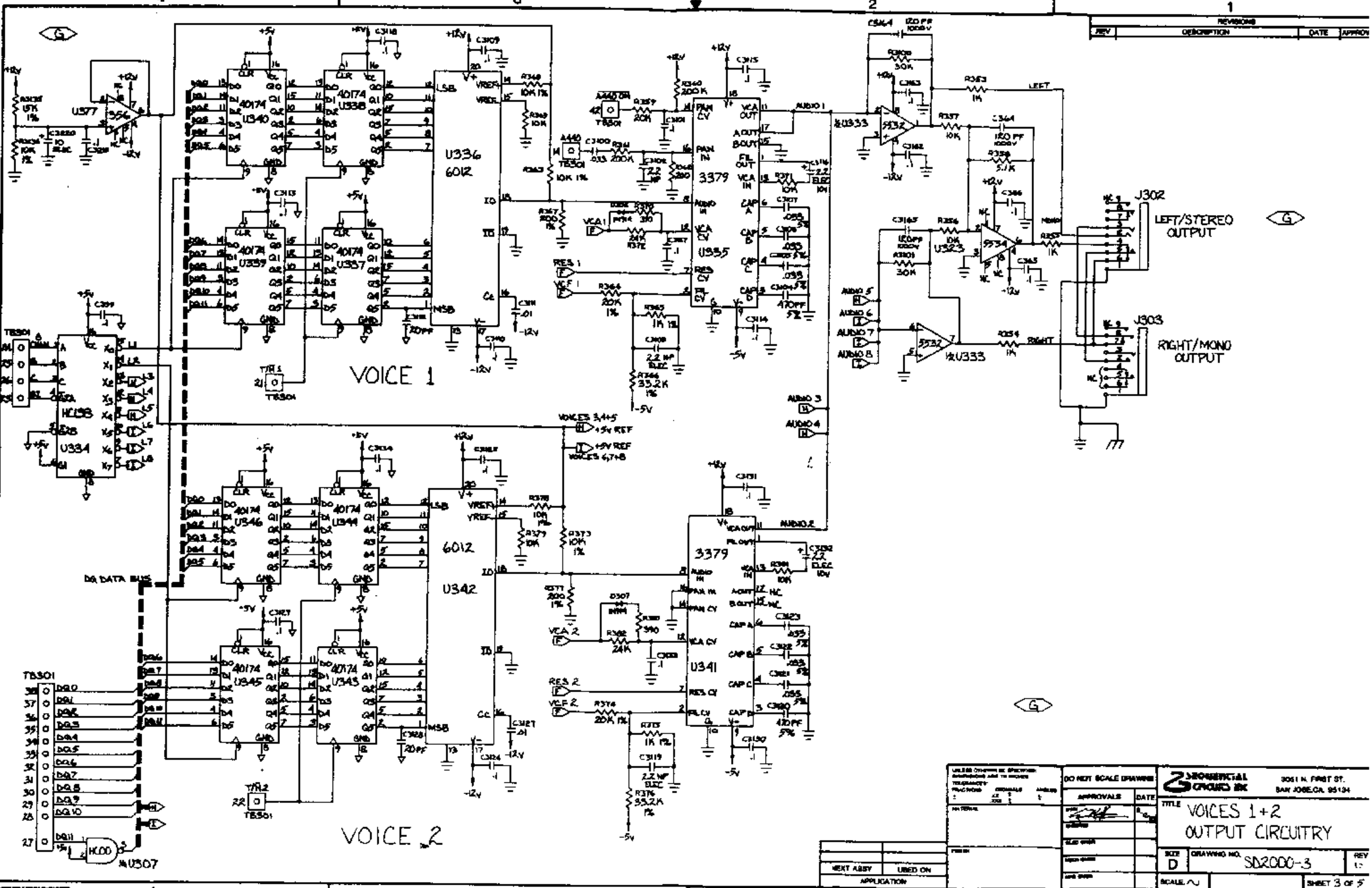




REV	DESCRIPTION	DATE	APPROVED
1	VOICE 1	1/68	
2	VOICE 2	1/68	
3	VOICE 3	1/68	
4	VOICE 4	1/68	
5	VOICE 5	1/68	
6	VOICE 6	1/68	
7	VOICE 7	1/68	
8	VOICE 8	1/68	
9	VOICE 9	1/68	
10	VOICE 10	1/68	
11	VOICE 11	1/68	
12	VOICE 12	1/68	
13	VOICE 13	1/68	
14	VOICE 14	1/68	
15	VOICE 15	1/68	
16	VOICE 16	1/68	
17	VOICE 17	1/68	
18	VOICE 18	1/68	

- ↓ DIGITAL GND
- ⊥ ANALOG GND
- /// CLASS GND

SEQUENTIAL		JOB # 11 FIRST BY	
		EMERSON, BATH	
SOUND BOARD			
DAC, SAMPLE AND HOLDS			
SIZE	DRAWING NO.	REV	
D	SD2000-3	15	
SCALE	MODEL	DATE	
1	2000	2/68	5



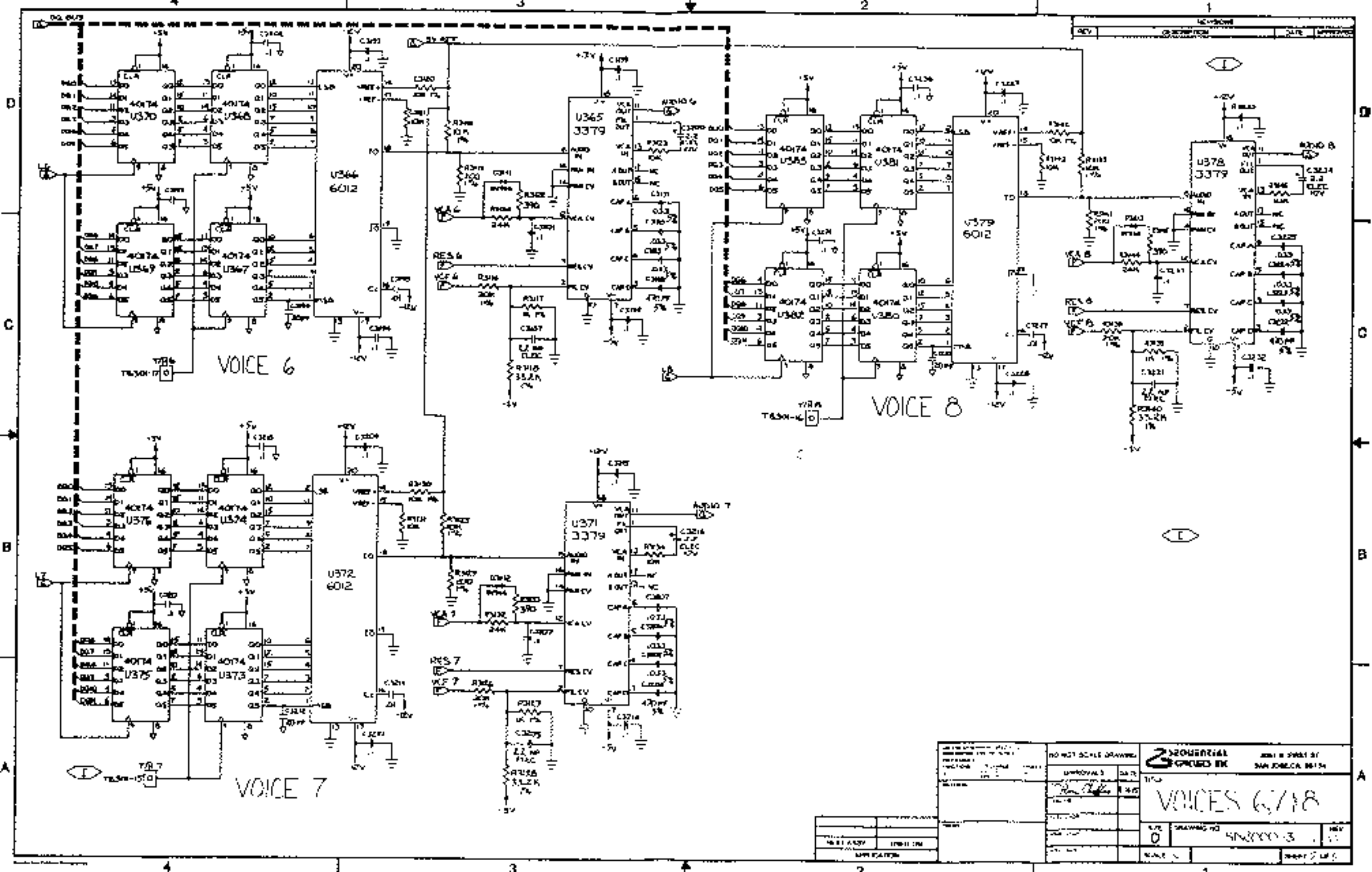
VOICE 1

VOICE 2

LEFT/STEREO OUTPUT

RIGHT/MONO OUTPUT

<small>USE OR CHANGE THE SPECIFICATIONS, DIMENSIONS, AND TO SHOW THE NECESSARY PRECISION.</small> <small>DATE</small>		3 3 COMMERCIAL CIRCUITS INC. 3051 N. FIRST ST. SAN JOSE, CA 95134
DO NOT SCALE DRAWING	APPROVALS DATE	
TITLE VOICES 1+2 OUTPUT CIRCUITRY	SIZE D	DRAWING NO. SD2000-3
NEXT ASSY USED ON APPLICATION	SHEET 3 OF 5	SCALE ~



VOICE 6

VOICE 8

VOICE 7

DO NOT SCALE DRAWING APPROVALS: <i>[Signature]</i> DATE: 8-4-75 TITLE: VOICES 6/7/8		APPROVED BY: <i>[Signature]</i> DATE: 8-4-75 DRAWING NO: 542000-3 REV: 1	
PROJECT: <i>[Blank]</i> SHEET: 1 OF 1		DESIGNED BY: <i>[Blank]</i> CHECKED BY: <i>[Blank]</i> DATE: <i>[Blank]</i>	

PI01

RI01

SI01

DS101
DS102
DS103

C12
R101

SI02
SI03

DS104
SI04

SI05
DS105

SI06
DS106

SI07
DS107

SI08
DS108
DS109
DS110
DS111

SI09

RF101
U101
U102
U103
U104

J101

U105
U106
U107

U108
U109

RP102

DS110
SI10

DS111
SI11

DS112
SI12

DS113
SI13

DS114
SI14

DS115
SI15

DS116
SI16

DS117
SI17

DS118
SI18

DS119
SI19

DS120
SI20

DS121
SI21

DS122
SI22

DS123
SI23

DS124
SI24

TB101
1
2
3