Alarm Sequencer Tells Process Operator Where To Look First

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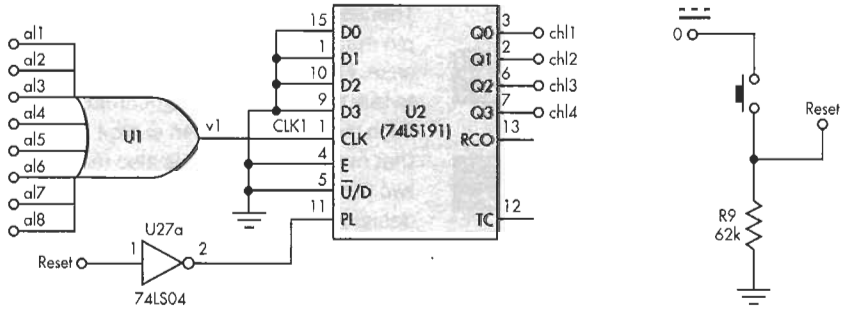


1. The OR gate in the alarm sequencer system determines which alarm signal is active and sends that signal to the clock input of the 4-bit binary counter.

In a typical process plant, a number of plant parameters will be monitored by individual alarms to ensure safety. If any process parameter crosses its upper or lower limit, the control room is alerted. But when a problem occurs, several process parameters typically will cross their limits. To take proper remedial action, the operator must construct a fault tree and identify the root cause of the event.

Using the ISIS Proteus VSM (virtual simulation machine), a circuit design simulation was created for an eight-channel alarm sequencer that identifies the sequence of alarms. This makes it easier for the operator to identify the cause of the process problem. Whenever a process parameter crosses its upper or lower limit, a sensor energizes a relay, which is connected to the sequencer system.

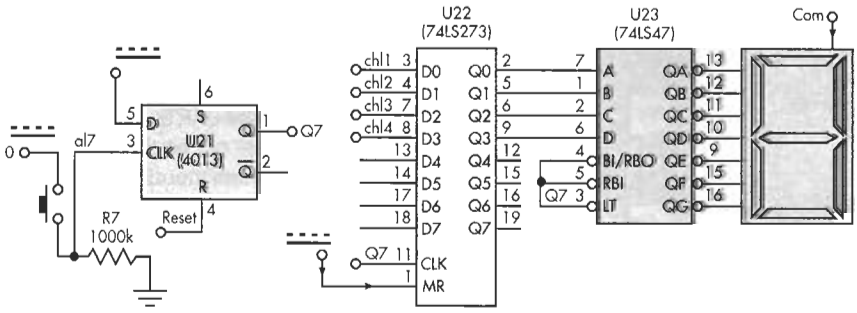
Each of the eight alarm inputs has a seven-segment display. For example, say alarm signals occur sequentially as 7, 6, 3, 8, 2, 5, 4, 1. The display of the seventh input will read as "1," indicating that parameter as the root cause of the event. The display for the sixth input will read as "2," the display for the third input will read as "3," and so on.

The alarm input includes an OR gate, U1, and a 4-bit binary counter, U2 *(Fig. 1)*. Each of the eight display channels includes a 74LS273 8-bit latch, a CD 4013 D flip-flop, a 74LS47 BCD-to-seven-segment decoder, and the seven-segment display *(Fig. 2)*. During power on or manual reset, the displays are blanked to save power. The counter's outputs are connected to the input stages of all the 8-bit latches for the corresponding channel.

In the example scenario, alarm seven (al7) arrives first, becomes the OR gate's output (v1), and generates a clock input (clk1) to the counter. Therefore, the count is incremented to 0001. D flip-flop seven (U21) also is clocked with al7, and U21's output (Q7) enables only the 8-bit latch of the seventh channel (U22). The rest of the channels are disabled. Subsequently, the incremented counter value of 0001 is latched and sent to the decoder (U23), which displays a 1 at the common-anode display of the seventh channel.

Similarly, when al6 arrives second and al7 has gone to low, al6 will become the output of the OR gate and generate the counter's clock input. Therefore, the count will be incremented to 0010. Channel 6's D flip-flop will be clocked with al6 and its output (q6) will enable only the 8-bit latch of the sixth channel, while the rest of the channels are disabled. Then the incremented counter value of 0010 is latched and sent to the channel 6 decoder, which displays a 2 on its display.

The same procedure applies for all of the other channels until the process operator can read the complete alarm sequence. Once all eight alarm inputs are received, the operator can clear the displays with a manual reset. This design simulation can be easily programmed into a VLSI chip for use in an embedded application.



2. In the example scenario, the alarm 7 signal arrives first. The binary counter's 0001 is latched in channel 7's 8-bit latch, and the binary-to-seven-segment decoder lights a 1 on the display.

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