# BUILD A VCT

**So far VCT has been the biggest non-event in component history. Two years of blank looks and still not released. In the meanwhile ETI shows you how to build your very own VCT to worry and amaze your friends!**

THE CIRCUIT SYMBOL of the voltage-current transactor (VCT) is shown in Fig. 1 with both voltage input and current output terminals floating. In the future it is expected that single chip VCTs (Ron Harris, ETI) will challenge the familiar op-amp as the universal linear circuit building block. At present, however, these have yet to emerge. In the meantime considerable familiarity with the VCT concept and with its circuit applications may be achieved by building a PCB version using readily available IC transistor arrays.

A single-ended VCT (C.A. Holt, "Electronic Circuits: Digital and Analog" p.788) is shown in Fig. 2. The floating output version of Fig. 3 corresponds to the circuit discussed before (J. E. Morris, ETI August 1977). In both figures the unfamiliar symbols (boxes) are intended to represent current mirrors. Ideally, the output from the high impedance current source(s) exactly equals the input current into the low impedance terminal (arrow-head). VCT operation is based upon these current mirrors.

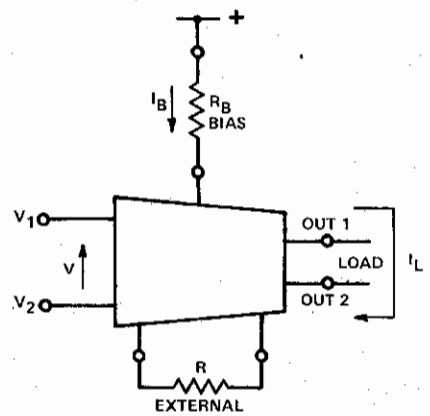



**Fig. 1. VCT symbol and external connections.**

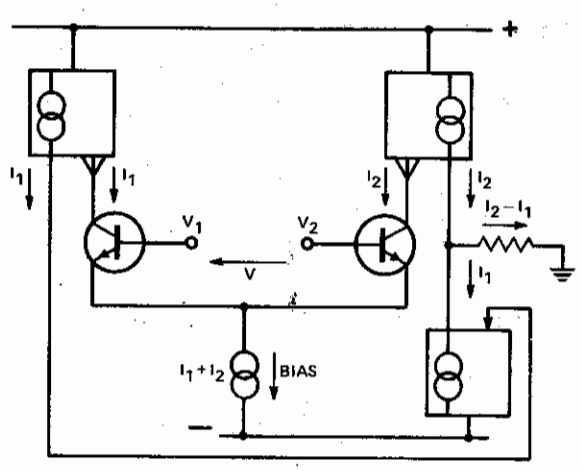



**Fig. 2. Single-ended VCT (e.g. CA3080 operational transconductance amplifier.**

No attempt will be made here to duplicate the earlier explanation of circuit operation which is expected to be reasonably clear from the diagrams (Figs. 2 and 3) anyway). The essential point is that the differential input voltage $V_1 - V_2$ leads to an imbalance in the currents flowing in the two halves of the symmetrical circuit and that this imbalance is translated into a load current I. The load is driven by constant current sources (high impedance) and the input impedance is high to minimise input signal loading. With the system of Fig. 3, load current is given by

$$I_L = \tfrac{2}{3}z(V_1 - V_2)/R_{EXT}$$

up to the point where the bias current is exhausted, i.e. for $I_L < \tfrac{2}{3}I_B$.

## Transistor Arrays

The original intention of the project described here was to build the current mirrors using perfectly matched transistor arrays in miniature flat IC packages. These were to be mounted on an alumina substrate with printed thick film interconnections in the circuit described in the earlier articles. As is often the case with electronics, however, the realities of the situation dictated a very different course.

In the first place both miniature package arrays and arrays of matched transistors were neither readily available nor acceptably priced! After some searching of the data books, we settled for the RCA arrays CA3084 and CA3086 on the basis of price and availability. (The pin diagrams for these are reproduced in Fig. 4). Not all of the components in these packages are used, in particular, the Darlington transistor D in the CA3084 is not employed in the VCT circuit.

The first point to be determined was the effectiveness of these transistor arrays in current mirror circuits. No claim is made for transistor matching in the CA3086 other than the obvious one of thermal matching. In the CA3084, $Q_3$ and $Q_4$ are obviously organized as current mirror outputs and $Q_1$, $Q_2$ are described as a matched

$$I_L = I_1 - I_2$$

$$I_E = 3I_1 - I_B$$

$$I_E = I_B - 3I_2$$

$$I_E = (V_1 - V_2)/R_{EXT}$$

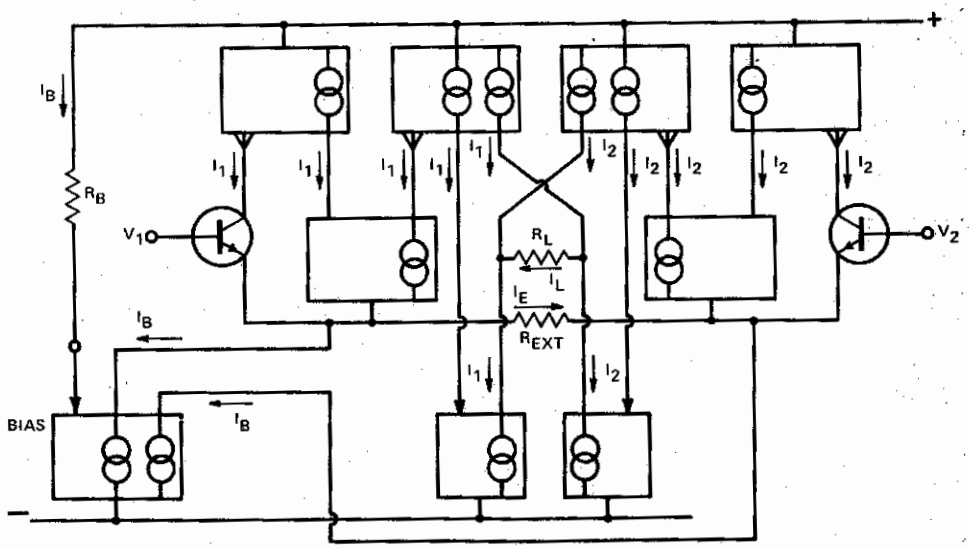



**Fig. 3. VCT with floating input.**

pair. The specifications on $Q_1$, $Q_2$ look impressive and those of $Q_3$, $Q_4$ seem rather inadequate (Fig. 4) but in fact for current mirror applications the reverse is true in both cases. To put these specifications into perspective, consider two similar base-emitter junctions where $I_{E1}$, $I_{S1}$ exp (e $V_{EB1}$/kT) and $I_{E2}$, $I_{S2}$ exp (e $V_{EB2}$/kT). Suppose these two junctions may be regarded as extremely well matched e.g. to ± 1 mV in $V_{BE}$ carrying identical currents $I_E$. Substitution above leads to

$$I_E = I_{S1} \exp(eV_{EB}/kT)$$
$$= I_{S2} \exp(eV_{EB}/kT \exp(e\ 10^{-3}/kT)$$

and if equal $V_{EB's}$ are now specified for the current mirror application

$$I_{E2} = I_{S2} \exp(eV_{EB}/kT)$$
$$= I_{S1} \exp(-e\ 10^{-3}/kT) \exp(eV_{EB}/kT)$$
$$= I_{E1} \exp -(e\ 10^{-3}/kT)$$

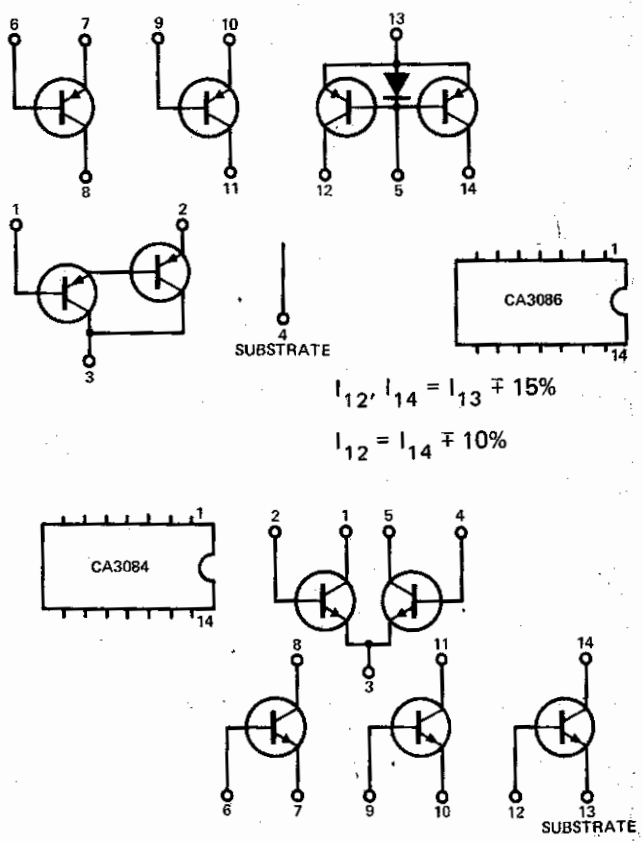
At room temperature, kT 1/40eV and $I_{E2}$ 0.96 $I_{E1}$. So a ± 1 mV matching in $V_{BE}$ leads to a 4-5% error in a current mirror application. In this light, $Q_3$ — $Q_4$ seem to be reasonably matched for the purpose and $Q_1$ — $Q_2$ less so.

Clearly, the point is best resolved by direct measurement of current mirror performance using the arrays themselves.

## Current Mirrors

As a first step, the transistors were checked for matching. For the CA3086, all transistors (except possibly the substrate transistor $Q_5$ whose measurements were later deemed to be suspect) were matched to within a 12 mV spread for a given current up to 500 μA. This figure reduces to a low 1 mV range at 1 mA and increases again with increasing current to about 9 mV at 10 mA. (All measurements at $V_{CE}$ = 3V.) It is only possible to measure terminal characteristics of $Q_1$ and $Q_2$ in the CA3084 and from 10 μA to 10 mA, $V_{BE}$ values were matched to within 1 mV. ▶

**Fig. 4. IC transistor arrays — pin connections and CA3084 specifications. (S — substrate connection to most negative point).**



The performance of the CA3084 current mirror is shown in Fig. 5 and that of a more complex system in Fig. 6. Clearly, the extra components of the more complicated circuit (which are all subject to variations from the nominal device parameters), lead to increased discrepancies in the output current. On the other hand, the simple circuit (as found within the CA3084 chip, for example), provides output matching within specification although the absolute level is lower than expected.

With the CA3086 a slightly different measurement technique was employed (Figs. 7 and 8) where transistor gain was permitted to vary with $V_{CE}$. This accounts for the curvatures of the output characteristics in Fig. 7. In Fig. 8, the performance of the more complex system is seen to be clearly inadequate. (The transistors in these two diagrams with base and collector shorted together function as diodes, as does $Q_4$ in Fig. 6).

The results of this section led immediately to the decision to use only the basic type of current mirror. Both types were examined in the earlier article (ETI August, 1977) and the more complicated form is used in the prototype single chip VCT. The advantage of the complex circuit is that it performs better with low gain transistors but the typical $h_{FE}$ figures of 100 and 40 (for the CA3086 and CA3084 respectively) are expected to be adequate. The problem with the system being developed here is that of poor matching and an elementary worst case analysis demonstrates the superiority of a minimal component count.

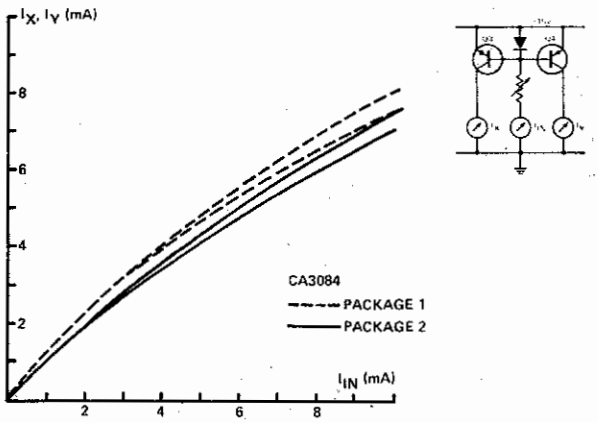



**Fig. 5. Elementary current mirror — output matching test.**

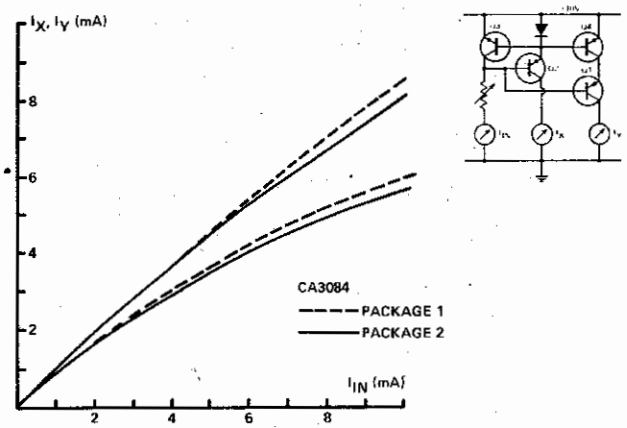



**Fig. 6. Complex current mirror output matching test.**

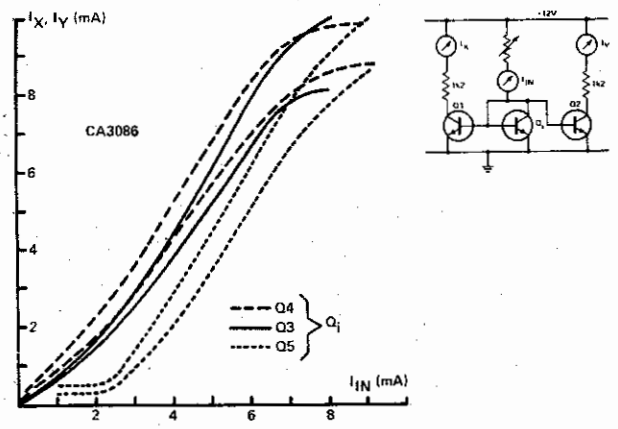



**Fig. 7. Elementary current mirror — transistor matching.**

## Discrete VCT

The actual circuit employed is shown in Fig. 9 and differs markedly from the one discussed in the earlier articles. In the first place, the simple current mirror has been used throughout for reasons given above. Second, there is obviously no opportunity to provide current gain by utilising multiple emitter transistors since these are not provided in the arrays. (This is no disadvantage for the purpose of a familiarisation exercise.) The third discrepancy is apparent by comparison of Fig. 9 with Fig. 3. In recognition of device parameter variations and the asymmetry which these will necessary cause, the bias circuit has been split into two independent sources. In effect, this provides both bias and offset capabilities. Usually one would employ Darlingtons as the input transistors. This step would require an extra CA3086 and has been omitted.

A fifth difference lies with the elimination of any link between the input circuit current mirrors of the two sides. The circuit described in previous articles uses the complex current mirror with diodes shared between the two sides of the VCT. This set-up has been simulated

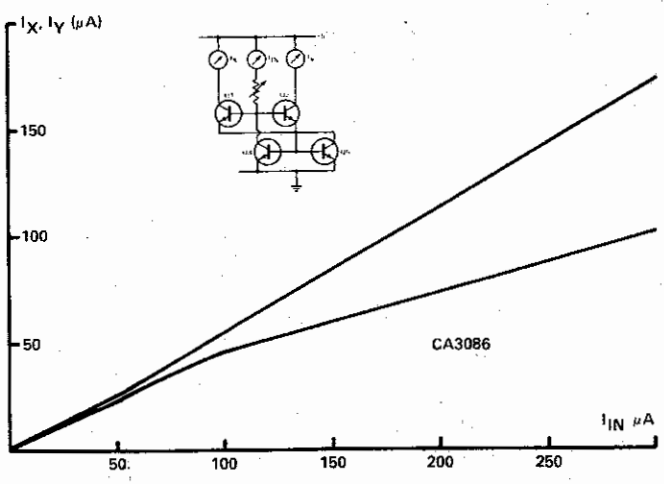



**Fig. 8. Complex current mirror — output matching.**

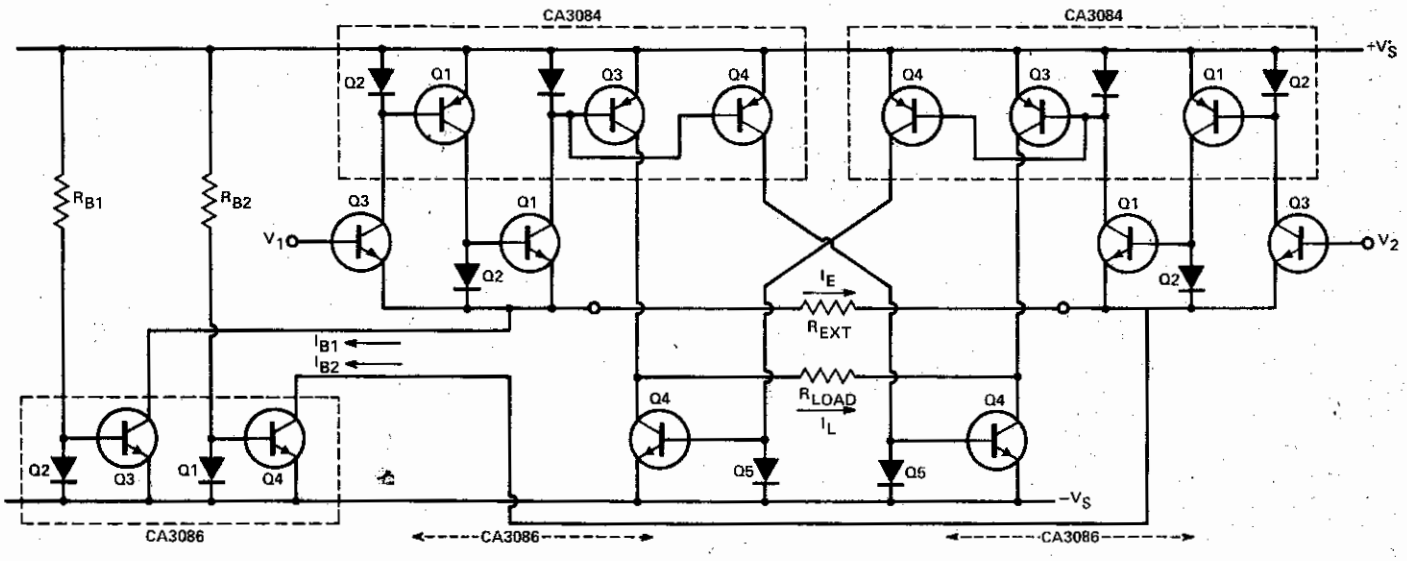



**Fig. 9. Simplified VCT design employing IC transistor arrays.**

(Fig. 10) and found to be ineffective as a means of compensation for bias imbalance between the two sides. If $I_{IN2}$ is increased, for example, the base current of $Q_2$ and hence $I_{O2}$ increase with a compensating decrease in $I_{O1}$. A link of this type is not possible with the simple mirror system adopted here, but would not have been employed with the more complicated circuit anyway.

A printed circuit board layout is shown in Fig. 11. No claim is made with regard to the optimal quality of this layout but it seems satisfactory. ▶

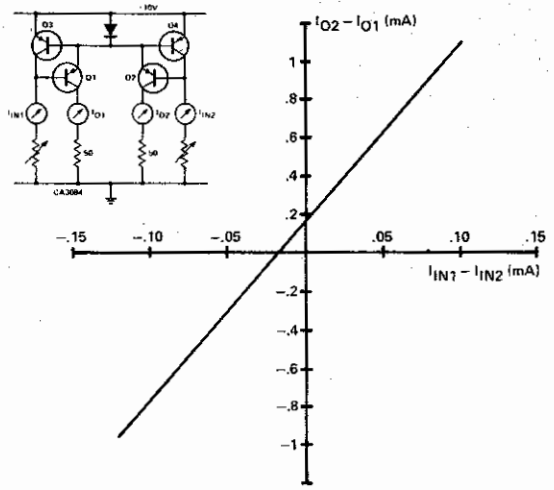
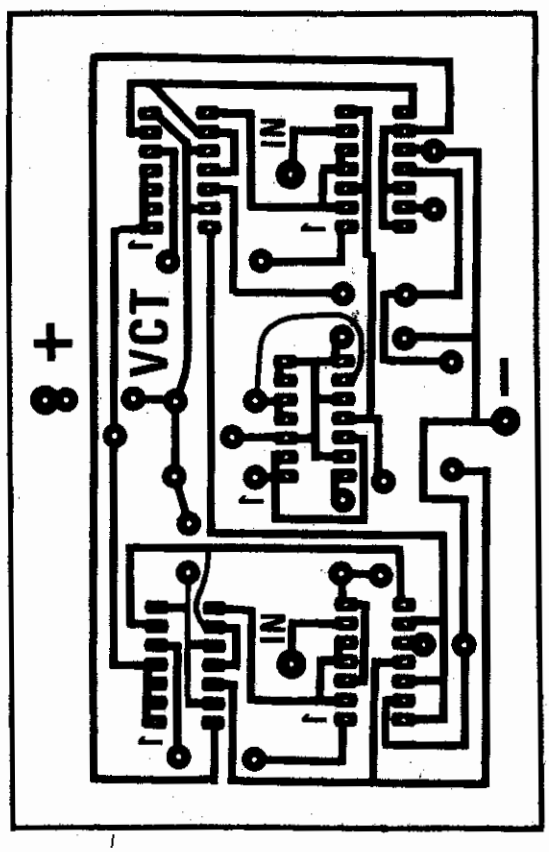



**Fig. 10. Effect of linking current mirrors within the VCT.**



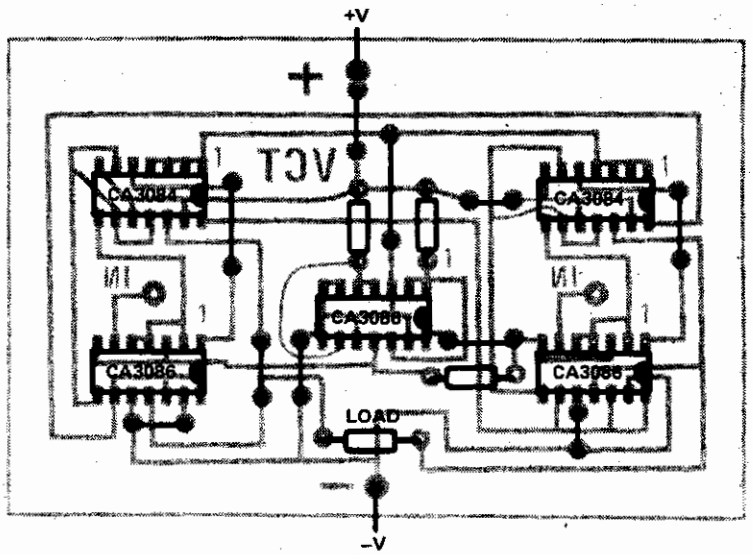




**Fig. 11. PCB layout, showing external components, wire links, etc. — view from component side.**

## VCT Performance

It is not the function of this article to present an exhaustive survey of the circuit's performance in varied applications. Many of these have been proposed elsewhere (ETI, amongst others) and the reader is left to try these individually with his own discrete VCT. There are, however, a few pitfalls which warrant further discussion. Most of these may be classed as limitations of the non-ideal system.

Two VCTs were constructed and these are identified as 'a' and 'b' from here on. In general, they performed similarly, but there were some significant differences. Unless stated otherwise, below, supply voltages of ± 10 volts were employed with $R_{EXT}$ = 1k and only current monitoring as loads. The first test was to establish bias current levels to achieve a null output. $R_{B1}$ was set to 4k with each unit. For VCTa, $R_{B2}$ = 5k212 and for VCTb, $R_{B2}$ = 5k552 established zero output currents for $V_1$ = $V_2$ = 0V. Drifts (of the order of 1 μA for VCTa and 40 μA for VCTb) were noted over the next few minutes and $R_{B2}$ was finally set to 5k2 for VCTa and 5k6 for VCTb. In the test for common mode rejection (Fig. 12) the residual offset and the magnitude of short term drift effects are apparent (output levels must significantly exceed these drifts). As the supply voltages are approached, transistors begin to cut off and this may in turn lead to unpredictable effects depending on the relative parameters of the various devices. The lesson to avoid approaching the supply rails is clear. While the common-mode rejection ratio seems satisfactory for VCTa (Fig. 12), the curve for VCTb clearly indicates an asymmetry in the circuit, i.e. there is at least one transistor mismatched to its counterpart on the other side (this mismatch is most likely in a variation of gain with $V_{CE}$).

Fig. 13 shows the standard transfer characteristics. The slight variations in slope are due to $R_{EXT}$ tolerances

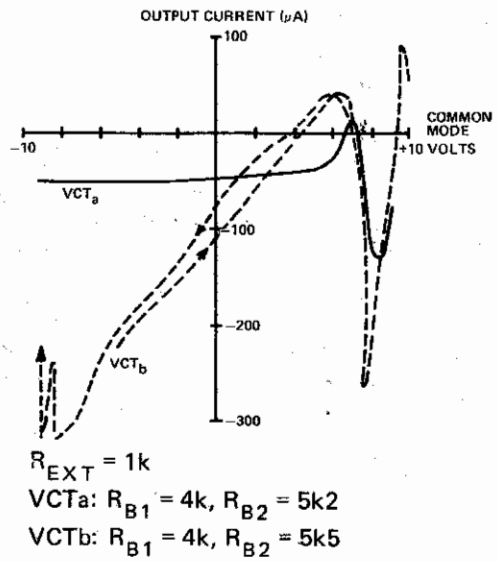



**Fig. 13. Transfer characteristics.**

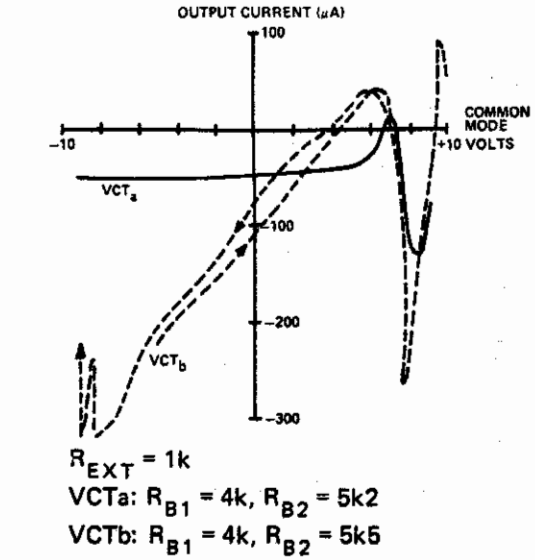



**Fig. 12. Common mode signal transfer (V1 = V2).**

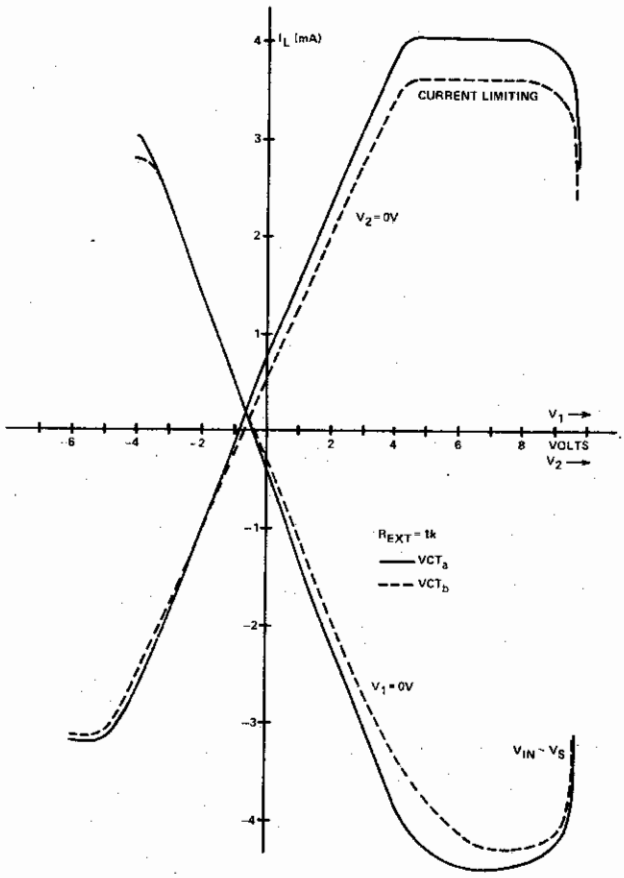



**Fig. 14. Transfer characteristics with one end of the load grounded and with corresponding input grounded.**

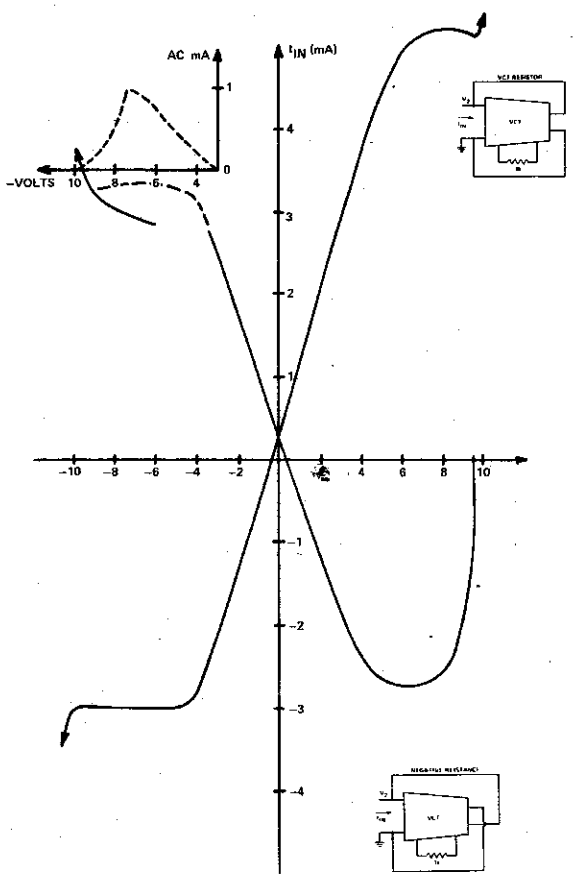



**Fig. 16. VCT 'resistors' — positive and negative.**

and the measured values (VCTa: 1mA/12V and 6mA/7.75V for $R_{EXT}$ ~10k, 1k exceed expectation slightly (c.f. 1mA/15V, 6mA/9V) due to a small current gain cuased by transistor mismatching. This effect also leads to small discrepancies from the expected current limit levels (e.g. ⅔ x 20V/4k and ⅔ x 20V/5k2).

The results described in the preceding paragraph were obtained with one input grounded as a matter of convenience. There is a dramatic shift in the offset current when one end of the load is also grounded (Fig. 14) and when both these fixed points are switched to the other side of the VCT. It would seem that the concept of 'floating' input and output require re-examination.

It must be noted that while one might expect the two ends of the floating load to sit at approximately zero volts, it does not take a great deal of device variation to produce extreme deviations from this. In both the circuits built here, two output transistors ($Q_4$, $Q_5$ of CA3086, see Fig. 9) were saturated at null output. (With different selection of devices, saturation of CA3084 $Q_3$ and $Q_4$ is equally likely). This creates no problems for the floating load unit high frequency or switching applications where performance will be down-graded by transistor saturation. It does, however, mean that the output must be rezeroed if either end of the load is to be tied to a fixed potential as in Fig. 14.

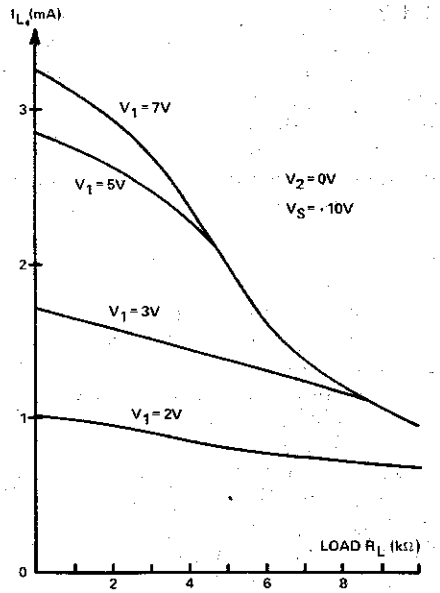



**Fig. 15. Effect of output load resistance.**

The four constant current sources which comprise the output circuitry lead inevitably to saturation as soon as there is an imbalance between them. In many cases zeroing the output current aggrevates the problem. If device selection is contemplated, these are the transistors to consider first.

Variation of load current with load impedance (Fig. 15) suggests that the output impedance is about 40k substiantially below the 60-100 k range expected from the transistor specifications because of saturation. The differential small signal input resistance has been measured at about 35k which is approximately $h_{FE}$ $R_{EXT}$. This figure would be increased by the use of Darlington input transistors.

## Applying Exotics

Up until this stage, none of the more exotic circuit applications has been discussed. A few remarks should be made, however, in closing. Ideally the output is a constant current and can be used to linearly charge a capacitor, e.g. to provide integration. The constant current sourcing is not perfect however and integrating applications will be limited to frequencies greater than $(2\pi\ R_{OUT}C)^{-1}$. A similar limitation will exist for gyrator performance.

A gyrator was built with the two VCTs but oscillated. The oscillation is believed to originate, however, with the use of inadequate power supplies — another point to note in investigating these circuits — rather than with that circuit itself. Gyrators operate on a negative immittance conversion principle so it is instructive to consider the resistance applications of the VCT in Fig. 16 where the terminal resistances are expect to be $\pm\ ^2/_3\ R_{EXT}$. In the negative resistance case an oscillation region was identified (see inset). If the negative resistance circuit is examined, it clearly provides positive feedback if the driving source ($V_2$) impedance is not zero.

In closing I wish to acknowledge the assistance of Jock Howie and others with this project. ETI