# TECHNOLOGICAL RESEARCH AND DEVELOPMENT AUTHORITY (TRDA)

## SUMMARY REPORT:
## NASA COOPERATIVE AGREEMENT NO. NCC10-0008

## "UNIVERSAL SIGNAL CONDITIONING AMPLIFIER"

TECHNOLOGICAL RESEARCH AND DEVELOPMENT AUTHORITY
STATE OF FLORIDA
6750 S. HIGHWAY U. S. 1
TITUSVILLE, FLORIDA 32780

# PERFORMANCE REPORT

**Under**

## NASA COOPERATIVE AGREEMENT NO.: NCC10-0008

**Entitled**

## "Universal Signal Conditioning Amplifier"

**Principal Investigator:** **Frank Kinney**
**Report Period:** **3/15/94 – 12/31/96**

**April 1997**

# TABLE OF CONTENTS

## I. INTRODUCTION

The Technological Research and Development Authority (TRDA) and NASA-KSC entered into a Cooperative Agreement in March of 1994 to achieve the utilization and commercialization of a technology development for benefiting both the Space Program and U. S. industry on a "dual-use basis". The technology involved in this transfer is a new, unique Universal Signal Conditioning Amplifier (USCA) used in connection with various types of transducers. The project was initiated in partnership with I-Net Corporation, Lockheed Martin Telemetry & Instrumentation (formerly Loral Test and Information Systems), and Brevard Community College.

The project consists of designing, miniaturizing, manufacturing, and testing an existing prototype of USCA that was developed for NASA-KSC by the I-Net Corporation. The USCA is a rugged and field-installable self (or remotely) - programmable amplifier that works in combination with a tag random access memory (RAM) attached to various types of transducers.

In September of 1994, the project was modified and extended to also include the development of the Advanced Data Acquisition System (ADAS). The new products developed as part of ADAS includes a USCA Controller/Input card, an ADAS Output card, and the operation software for the ADAS. The ADAS project completes and complements the USCA commercialization project.

Under this co-funded partnership, Loral/Lockheed Martin provided final design assistance to I-Net to assure compatibility with standard manufacturing processes, manufacture both government and non-government (commercial) versions of USCA and ADAS, provide the government version to TRDA for NASA-KSC testing, and place the commercial versions on the open commercial market.

## II. PERFORMANCE

Project performance was tracked by attainment of established Milestones. The Milestones were adjusted several times through agreement of all partners. Changes to the Milestone schedule were necessitated by various design changes incorporated along the way in an effort to enhance the project. The final Milestone Schedules for both the USCA and the ADAS development are included as Attachment "A".

As of October 1996, all USCA and ADAS Milestones have been completed. TRDA had numerous conversations/meetings with Lockheed Martin and I-Net participants to confirm attainment of milestones. TRDA requested a final written project status report from Lockheed Martin, and received this report in March '97. This final report and the other written progress/milestone reports are provided in Attachment "B" of this report.

## III. TRDA PARTNERSHIP TASKS

The tasks performed by TRDA under this partnership arrangement are summarized below:

(1) TRDA provided co-funding of the project in an amount equal to the co-funding provided by NASA-KSC.

(2) TRDA provided the services of staff and professional consultants to provide for the proper implementation and business and technical management of the project Executive Director Frank Kinney and Business Manager Matthew La Vigne provided oversight and direct interface with all project partners. Associated clerical/secretarial support was also provided. Regular contact was maintained with all partners both via telephone and visits/meetings. Additionally, TRDA retained qualified technical support (via contractual relationship with Mr. Tom Davis) to assure the technical components of the project were being sufficiently managed.

(3) In March of 1994, TRDA negotiated and contracted with Brevard Community College (BCC) to provide required assistance. BCC assisted in the administration of subcontracts and in the hiring of qualified college co-op students to support the project. Students from Florida Tech, the University of Central Florida, and Bethune-Cookman College were hired through BCC to assist project engineers in USCA and ADAS development.

(4) TRDA served as the main interface and point of contact for all partners. Periodic site visits to Lockheed Martin's (Loral's) Sarasota facility took place, as well as numerous meetings in the local area. Regular contact is maintained with project engineers, managers, and contract personnel, as well as project management personnel at BCC and lead technical personnel at KSC.

(5) Progress reviews took two forms: formal and informal. Formal reviews were made in conjunction with the submission of established Milestone Reports. On an informal basis, regular contact with project personnel enabled us to keep abreast of the work being performed on a continual basis.

(6) Performance schedules take the form of agreed upon Milestone Schedules. These schedules have been mutually established by all partners. The Milestone Schedules were modified several times to meet expected performance. TRDA oversaw the schedules and confirmed that changes were both reasonable and required.

(7) TRDA acquired reports as per the Milestone Schedules. These amounted to reporting requirements in excess of quarterly reports, however, we felt they were necessary to assure and track performance. These reports, as well as other appropriate documentation, were submitted to NASA in our required Performance and Summary Reports.

(8) TRDA submitted the required cash transaction reports to NASA to provide for their agreed to funding of the project, and have maintained appropriate records/files in connection with this project.

## IV. SUMMARY

Although the USCA/ADAS dual-use project took longer and was more expensive than originally planned, we should all be extremely pleased with the results. Lockheed Martin Telemetry & Instrumentation (LMTI) believed in the potential of the NASA technology from the outset and therefore invested heavily in the project to ensure its success.

Through the partnership, NASA-KSC and LMTI have successfully completed a transfer of NASA technology to a commercial manufacturing environment. Commercial products are now being produced and delivered to NASA by LMTI, and the products have been introduced to the commercial marketplace. While the product launch is still in its infancy, marketplace reaction is very encouraging.

This project was a true example of partnership. The cooperation between all parties was been exceptional. KSC participants have expressed their pleasure with the cooperation they have received from LMTI concerning all elements of the project, from design, to testing, to manufacturing. Likewise, LMTI has stated that they have never participated in a project with the level of cooperation and teamwork that they experienced with the USCA/ADAS project. All partners should be commended for their efforts and participation in this project.

TRDA wishes to express our appreciation to NASA-KSC for their tremendous cooperation and support in this successful dual-use commercialization.

# ATTACHMENT "A"

**USCA MILESTONES**
**ADAS MILESTONES**

# USCA COMMERCIALIZATION PROJECT (TRDA #405)
# MILESTONES FOR PAYMENT

| ACTIVITY COMPLETED/DELIVERABLES | % OF BUDGET TO BE PAID |
|---|---|
| • Deliver to TRDA electrical and mechanical components inputs for final Version 2 design of USCA. Provide this information with component descriptions, part numbers, etc. necessary for NASA to complete Version 2 design package. This information of electrical and mechanical components will be focused on improving the manufacturability of USCA and reduce the product cost. | **25%** |
| • Complete the incorporation of the final Version 2 USCA design package, released by NASA on April 29, into the Loral CAD system. Provide CAD design package to TRDA. | **15%** |
| • Complete manufacturing and deliver to TRDA five copies of design Version 3 USCA's. These Version 3 USCA's will be manufactured according to the final approved Version 3 design contained within the Loral CAD system. | **20%** |
| • Release final Version 3 USCA design package. This version will be released as a Loral Standard Component, and will be available as a catalog item.<br><br>Complete design of Commercial Version 1 of USCA. | **20%** |
| • Complete final design package for Loral Commercial Version of USCA. This Loral Commercial Version of USCA will be a Loral Standard Component and will be available as a procured item. | **20%** |

## ADAS COMMERCIALIZATION PROJECT (TRDA #410)
## MILESTONES FOR PAYMENT

| ACTIVITY COMPLETED/DELIVERABLES | % OF BUDGET TO BE PAID |
|---|---|
| • Complete the ordering of the materials for the Input Card manufacturing and testing. Input design package to Loral. | **25%** |
| • Complete the CAD Schematic Design of the Output Card | **15%** |
| • Complete Output Card PC Board fabrication. | **15%** |
| • Complete the CAD Schematic Design of the Input Card. | **15%** |
| • Complete the Input Card PC Board fabrication. | **10%** |
| • ADAS System test. In conjunction with NASA-KSC, complete final design, testing, and acceptance of the total ADAS. | **20%** |

# ATTACHMENT "B"

## MILESTONE/PROGRESS REPORTS

Fr: Dean R. Becker
Re: USCA milestone 1

LDS has delivered inputs on the electrical, mechanical, and component elements of the NASA USCA design. We have provided information with component descriptions, part numbers, etc. necessary for NASA to complete the version 2 design. We have also assisted with the overall design of the USCA as well as the system with which it operates. See the attachment A. Included is an updated project schedule for the USCA development. See Attachment B.

ATTACHMENT A

Tasks to be accomplished with NASA

- Discuss and identify actual specifications
  - Electrical operational specifications
    - Analog I/O
    - Digital I/O
  - MTBF
  - Construction
  - Power
  - Frequency response
  - Isolation
  - EMI
- Discuss circuit design
  - Block diagram hiarchial level
    - System I/O definition
    - First level internal
    - Details of first level blocks
    - Identify schematic to these details
    - Discuss certain schematic details
  - Detailed parts list (with full part numbers)
    - Identify questionable part descriptions
    - Surface mount versions
- Discuss certain component selection
  - Mechanical relays
  - Potentiometers
  - Monostable multivibrators
  - Temperature sensors
  - Crystal
  - Power supplies
  - Fuses
  - Special hybrid IC
  - PALs?
  - Gaps?
- Discuss firmware program flow
  - Tag RAM format definition
  - Tag RAM programmer definition
  - Micro controller Firmware
  - DSP Firmware
- Discuss setup sequence and defaults
- Discuss mechanical design
  - Boards
    - Number
    - Placement
    - Interconnects
  - Components
    - Ferrite beads

- Connectors
- Shock and vibration damping
- Shielding
- Shape
- Material

**Discuss current and future testing**

- Written test procedures
- EMI/RFI
- Environmental

**Discuss cost and schedule**

- Re-draw schematics
- Enter parts definitions into Cadence
  - Possible new parts libraries
- Worst case simulation?
  - Analog
  - Digital
- Plans and expectations for the prototype under development
  - NASA built
- Plans and expectations for final prototype
  - Loral built
- Final unit cost

**Discuss the rolls of NASA and Loral**

- NASA
  - Electrical design
  - Mechanical design
  - Test definition
  - Fabrication of prototypes
- Loral
  - Transfer of all design information
  - Integration of this information into development system
  - Integration into manufacturing system
  - Last prototype fabrication
  - Production fabrication
  - Definition of commercialized product
  - Design and fabrication of commercialized product

I.version 1

A. generate true set of specs
    1. (3.3.2)MTBF
    2. (3.5.1)Power 100 mA
    3. (3.5.8)Frequency Response 150 Hz
    4. (3.5.15)driving 100000 ohm output
    5. (3.5.16)Isolation 100 Megaohms
    6. (3.5.18)Insulation 100 Megaohms for connectors
    7. (3.5.23)Cable Length
    8. (3.5.24)Common Mode Rejection (still Valid)
    9. (3.6.3)EMI Spec

B. address multichip module
C. walk thru design with I-Net
D. PDR/CDR on version 1 todays version versus specs
E. Testing on todays version
    1. Preliminary Electrical Requirements Testing
    2. Preliminary EMI
    3. Preliminary Vibration analysis
    4. Component Analysis availability- reference Multichip module
    5. Temperature Analysis

II. Identify SAMS info

III. Generate USCA working environment for support
A. compiler
B. DSP stuff
C. Analog Library

IV. Generate buildable set of
A. Schematics
    1. New Bodies

B. Board Layout
C. Block Diagrams
D. Parts list
E. Parts Description
F. released Software
    1. uprocessor
    2. DSP
    3. SAMS
    4. Tag Ram Programmer

V. MTBF analysis

VI. System Level Interface and Documentation

VII.version 2

A. Liason work on USCA
    1. Mechanical Design (includes form factor)
    2. Electrical Designs
    3. Components
B. Version 2 testing
    1. Electrical Testing
    2. Mechanical Testing
    3. EMI Testing
    4. Vibration Testing

VIII. Version 3 ( nasa final version)

A. Liason work on USCA
    1. Mechanical Design
    2. Electrical Designs
    3. Components
    4. Cost
B. Version 3 testing
    1. Electrical Testing
    2. Mechanical Testing
    3. EMI Testing
    4. Vibration Testing

IX. Loral's Commercial Version

A. generate specifications
    1. Form factor
    2. cost
B. Preliminary Design
C. Design Review
D. Prototype Build
E. Prototype test
F. Design Modifications
G. Critical Design Review
H. Final Version Build
I. Final Version Test
J. Release

*USCA PDR TOPICS*

## Specifications

### Electrical specifications

#### Analog I/O

Input signal level

**Voltage: -10V to +10V**
**Current: Max: Typ:**
**Bandwidth: DC to 10kHz**

Output signal level

**Voltage mode: 0 to +5 VDC**
Current: Max: Typ:
Bandwidth:

**Voltage mode: -5 to +5 VDC**
Current: Max: Typ:
Bandwidth:

**Voltage mode: 0 to +10 VDC**
Current: Max: Typ:
Bandwidth:

**Voltage mode: -10 to +10 VDC**
Current: Max: Typ:
Bandwidth:

**Current mode: 4 to 20 mA**
Voltage: Max:
Bandwidth:

Excitation signal level

**Voltage mode:**
Current: Max:

**Current mode:**
Voltage: Max:

#### Digital I/O

Tag RAM Input

**Voltage:**
**Current:**
**Bit rate:**

Tag RAM Output

**Voltage:**
**Current:**
**Bit rate:**

SAMS Input

**Voltage:**
**Current:**
**Bit rate:**

SAMS Output

**Voltage:**
**Current:**
**Bit rate:**

Output signal

**Voltage:**
**Current:**
**Bit rate:**

- Other specifications

Detailed parts list
- Surface mount
  - For temperature sensors
  - For gaps
  - For ferrite beads
- Specific areas of concern
  - Potentiometers: change to EEpots
  - Monostables to be eliminated
  - Mechanical relays: changed to optical
  - Smaller power supplies
- Parts description book
  - Detailed data sheets for each part used

Schematics, latest version

Tag RAM format
- Tag RAM programmer

Hierarchical block diagram for hardware
- System I/O definition
- First level internal
- Details of first level blocks
- Identify schematic to these details
- Discuss certain schematic details

Hierarchical block diagram for software
- Microprocessor flow diagram
  - Top level
  - Detailed level
- Initialization flow and defaults: State diagram

Digital output definition
- Bit rate
- Structure
  - Number of bits per word:
  - Header:
  - Error detection/correction:

Test procedures
- Electrical
- Environmental
- EMI

Discussion
- SAMS
- Identify assembler/compiler for microprocessor
- Identify DSP software package
- Walk through design from block diagram through schematics
- Mechanical considerations
  - PCBs

- Enclosure
  - Mounting
- Diagnostics
  - Power up
  - Continuous
- Integration path into Loral manufacturing
  - Schematics
  - PCB layout
  - Parts placement for auto insertion
  - Mechanical drawings and fabrication

Universal Signal Conditioning Amplifier System

Universal Signal Conditioning Amplifier - USCA
Self Awareness Measurement System - SAMS
Advanced Data Acquisition System - ADAS
Tag RAM Programmer - TRP
Pro 550 interface

PDR Meeting with NASA, I-NET, TRDA - Feb. 15, '94

For this meeting I brought along the following list of things to be covered:
*USCA PDR TOPICS*

Specifications

Electrical specifications - *Specifications are still in work, some details of the digital and analog I/O are available.*

Analog I/O
Digital I/O

Other specifications

Detailed parts list

Surface mount

For temperature sensors - *Temperature sensors are to be eliminated inside the USCA.*
For gaps - *These do not exist but the thought is to have this part of the circuitry on a separate round PCB at the output end of the USCA and to have the other PCBs plug into it.*
For ferrite beads - *These exist and I have given some data sheets to Pedro on this.*

Specific areas of concern

Potentiometers: change to EEpots - *These will be eliminated with the new calibration scheme.*
Monostables to be eliminated - *They will not be used.*
Mechanical relays: changed to optical - *All have been changed or are being changed to optical.*
Smaller power supplies - *Pedro is looking into this to see what the actual circuit power requirements are.*

Parts description book

Detailed data sheets for each part used - *This is in work for the USCA version 2.*

Schematics, latest version - *Pedro has given me the latest schematics.*
Tag RAM format - *This was given to me during the SAMS discussion with Carl.*

Tag RAM programmer - *Still to be defined, this will probably be a good co-op job to do.*

Hierarchical block diagram for hardware - *Pedro has given this to me along with the detailed discussion of the USCA hardware.*

System I/O definition
First level internal
Details of first level blocks
Identify schematic to these details
Discuss certain schematic details

Hierarchical block diagram for software - *James has given this to me along with the detailed discussion of the USCA firmware.*

Microprocessor flow diagram
Top level
Detailed level
Initialization flow and defaults: State diagram

Digital output definition - *Curtis of NASA is assigned to this task, this is still in work.*

Bit rate
Structure
Number of bits per word:
Header:
Error detection/correction:

Test procedures - *Formal procedures are down the road with USCA version 2, however preliminary procedures exist for electrical and for environmental. The procedure for EMI will be done by another group at NASA.*

Electrical
Environmental
EMI

Discussion

SAMS - *Discussed details with Carl, System level concepts to be discussed with Bill Larson.*
Identify assembler/compiler for microprocessor - *Done*
Identify DSP software package - *Done*
Walk through design from block diagram through schematics - *Done*
Mechanical considerations - *I discussed my findings with LDS manufacturing.*

PCBs - *Consider three rectangular boards, surface mount on both sides, plugging into each other, and plugging into a common round mother board at one end with lightning protection at that end. (This is of course for version 2.)*
Enclosure - *Plan for a stainless steel enclosure slightly larger than the example we had at LDS for the temperature bulb.*

Mounting - *Consider a direct connect of the mother board to the MS connector at that end and an internal connector for the MS connector at the other end to avoid internal cables.*

Diagnostics

Power up - *Pedro and I will discuss this.*

Continuous - *This will be accomplished with the continuous calibration technique to be used.*

Integration path into Loral manufacturing

Schematics - *These will have to be re drawn into the LDS system. A discussion with Mike Nastanski confirmed that this is the most efficient way based on his previous experiences. We do not intend to do circuit simulation.*

PCB layout - *PCBs will be laid out by NASA / I-NET for the version 2 USCA. Placement for parts and critical circuits will be entered by hand at LDS and non-critical digital circuits will be auto routed. Net lists will come from the re done schematics.*

Parts placement for auto insertion - *Since we are entering the PCBs into the LDS system this will follow normally.*

Mechanical drawings and fabrication - *NASA will supply LDS with basic mechanical drawings which LDS will have to redraw to LDS standards.*

<u>The following are points which came out of the meeting:</u>

The qualifications of the part time students needs to be defined.

SAMS and the TRP are an integral part of the program and need to be brought in as an addendum to the contract.

The ADAS and APME (APME is part of the ADAS but its funding is separate)

ADAS funding is for FY '94

APME funding is for FY '94 & FY '95

Meetings are needed to discuss the following:

Mux bus extender / 550 interface

USCA digital output format

Discussion of:

<u>System overview concepts</u>

<u>Lightning protection actually needed</u>

<u>Power supply specs - max.</u>

SAMS format description needs to be defined.

Tag RAM Programmer schematics and software need definition.

This needs to be coordinated with the Calibration facility

Need to do cable testing at the pad for long cable runs between USCA and the pad collection point. This is to find out how the present cables which are used to monitor the analog voltages

from sensors will work with the digital output signal the USCA will eventually send.
Software used for USCA

Monarch DSP - 904 371 2567 ($349)
Dallas semiconductor DS5000TK V3.1 evaluation kit
8051 ASM Archimedies V2.02
C51 Compiler V4.23B
Xlink V4.43

Following this meeting I discussed the details of the USCA software design with the NASA designer (who I only know at this point as James).

The following day I went with several of their engineers to Pad A to do testing on one of the long cable runs between USCA and the collection point. We focused on a cable from the liquid oxygen pumps to the pad. Since the cable was originally intended for the transmission of low frequency analog signals its characteristics for carrying the digital USCA output were unknown. Definition of the USCA output depended on the cables characteristics as they are not to be replaced. We found that the frequency response exhibited a standard LC roll off starting around 600 kHz. We also rigged up a TDR to look for impedance anomalies in the overall cable run. This testing took up the entire morning.

Following this I discussed the details of the SAMS design with Carl Hallberg of I-NET.

Next I discussed design details of the USCA hardware with Pedro Medelius. We also discussed a new self calibration approach and USCA diagnostics.

Software documentation for USCA, SAMS, etc. - *Two different students could document the software for the USCA and possibly expand on the software for the SAMS.*

Development of units

SAMS - *Once SAMS is a well defined system a student could help with prototyping and documentation.*

Tag RAM Programmer - *This would be a very good student project for both hardware and software.*

***Basically co-op students will be needed with the following backgrounds:***

*Mechanical design, possibly with Auto CAD*

*Electrical design with microprocessor*

***software***

***hardware***

**The new method of calibrating the USCA automatically using the A / B channel method will be implemented in the version 2 USCA as discussed with Pedro previously.**

**An expanded list of possible SAMS commands for USCA needs to be established. - *James will do this by March 1, '94.***

**An expanded definition for Tag RAM utilization needs to be developed. - *To be done in 2 weeks.***

**Diagnostics internal to the USCA**

Feed output voltage back to input - ***This presents a special problem in the USCA due to the galvanic isolation required between the input and output. The output voltage cannot be monitored by the input of the USCA, however the excitation voltage can be used to test the input. The excitation voltage will be controlled by the DSP in the version 2 USCA and by this creates an easily controlled situation for testing the input. The output voltage of the USCA will need to be checked in the lab but will not be self correcting while in use. This is not a major concern as the digital output will be replacing the analog output in the future.***

Self calibration - ***A dual input path will be used where one path is switched to a standard voltage while the other is in use. The two will flip flop in time thereby maintaining calibration for any gain or offset adjustments.***

Excitation voltage / current to input - ***This will be used as just described.***

SAMS / Tag RAM Interface - ***This will not have a special test. If the SAMS cannot communicate then this interface has a problem indicating that the particular USCA needs to be repaired.***

Multiple frequency sinusoidal waveform for DDF testing - ***This can now be done using the excitation voltage. These frequencies need to be defined.***

Control test - *A power up test can be done to give credibility to the operation of the micro controller.*

Digital output test - *This could be feed back into the DSP using optical isolation and a test pattern. The utility of this is somewhat questionable.*

USCA digital output definition - ***This is being worked on by Pedro and Curtis.***

**The Tag RAM device is a sole source chip made by Dallas semiconductor. The entire system evolving out of the USCA is revolving around the Tag RAM and its unique format and control. I feel that with the dependence on this part being so critical an alternate approach should be explored should Dallas decide by their whim not to make this part in the future. - *Yoseph will look into this.***

**The Tag RAM only uses one fourth of its memory space. The other areas have different access requirements but need to be used as well. The current one forth of the device is already full based on current information definition. - *This will be done.***

**What results have been found from the temperature and EMI tests. - *The results from the temperature tests are good. Due to the results of this other DC to DC converters will need to found. No other problems surfaced. EMI testing has not been done. This is controlled by another NASA lab and must be time phased to meet their needs.***

A project plan needs to be developed for: - ***This is recognized and is TBD.***

SAMS

TRP

ADAS

**Bring the serial interface from the micro controller out of the USCA for diagnostics and setup. - *Pedro and I discussed the possibility of bringing this out on two 'unused' pins on the MS output connector.***

Use of the Dallas 5000 micro controller vs. an 8751

**The 5000 requires software to be loaded into its battery backed up RAM after manufacture.**

**This chip is not available in surface mount and is very tall.**

**The 5000 costs much more than the 8751**

**The 8751 will work in this application with no need to rewrite the basic functional software.**

***Pedro agrees with these points and is looking into using the 8751 or an equivalent.***

What is the status of the Tag RAM board layout and component selection? - ***This is in work as the mechanical relay needs to be replaced with an optical relay.***

Universal Signal Conditioning Amplifier System

Universal Signal Conditioning Amplifier - USCA
Self Awareness Measurement System - SAMS
Advanced Data Acquisition System - ADAS
Tag RAM Programmer - TRP
Pro 550 interface

Meeting with NASA, I-NET, Grumman - Feb. 23, '94

*No major problems were uncovered, however the following points were discussed:*

Considering up to 12 Bit Sync / Decoms in the PRO550 at LCC (Launch Control Center). These would have fiber optic links as inputs.

Fiber optic link bandwidth is 2 MHz now but is apparently only limited by the transmitters / receivers now being used. The fiber optic link output will be coming from the individual ADAS units.

USCA linearization was only up to 5th order at maximum input sample rate. This has been increased to 7th order.

Grumman expressed concern over the possible effects of the DDF FIR filter coefficients windowing. This is a 512 tap filter and the coefficients are being computed by an algorithm such as Parks - McClellan so the window effects are not likely to be a concern. Pedro is going to run an example to show that the effects of this on the data are below the effective quantization level.

A question was raised on the jitter specification for the excitation pulses from the USCA. This needs to be specified but will likely not be a problem as the excitation voltage or current in version 2 of the USCA will be controlled by the DSP chip instead of the micro controller.

Mike Maxwell of Bionetics was also at this meeting to represent the NASA calibration facility. He was asked to give any input with respect to the Tag RAM Programmer interface and existing calibration facility equipment.

Following this meeting I discussed some other concerns with Bill Larson. Pedro was called in for parts of this. For this meeting I brought along the following list of things to be covered:

Capabilities and requirements for the student co - ops

Mechanical - *A student working at NASA could document with drawings the version 2 USCA enclosure.*

What are the specifications for the filters being defined for the DDF? - *Pedro will supply this.*

*The LDS proposal has been received by NASA and is in their accounting department.*
*NASA can have their mechanical drawings done in Auto CAD.*
*We need to see if we can take this directly into our system.*
*We need to supply them with example drawings of our standards.*
*This could be done by a co-op student at NASA.*
*I explained to Bill Larson the operation of the CMUX and how it could be used for the ADAS. He seemed very interested and requested documentation be sent immediately for Curtis to read.*
*I will be gathering together the cost of parts as they can best be defined at this point to come up with an estimate of cost for the USCA.*

*I was given a schedule on the development of the SAMS. The current prototype is being built and considering several facets of the project this is just as well. This will test out the driver circuitry for the follow on which may be a significantly different over all design. The system philosophy needs to be discussed further.*

*LDS needs to get contractually involved with the entire system surrounding the USCA.*
*LDS has approval to use the USCA as a paper for conferences.*

From: Dean Becker
Telecon with Bill Larson on March 10, '94

- Environmental testing is progressing on the version 1 USCA
  - Temperature testing -20 to +50 degrees C.
  - Unity gain and 10X gives accuracy of 15.5 bits
- Tag RAM
  - An alternate chip has been found for this critical purpose
    - Less cost
    - Board layout of equal size
- SAMS PCBs have gone out for fabrication
  - They will be stuffed next Friday
- There will be an in house (@NASA) design review for the SAMS on the 21st of March
- The USCA contract
  - Scheduled for completion on Monday March 14
  - Should be released to TRDA the next day
- There was an internal design review for the TRP (Tag RAM Programmer)
  - It is planned to be a black box with a serial interface
  - Can be used by any computer system
- Tag RAM Partitioning
  - There are 4 sections to be used
    - The first part will contain Calibration lab information such as coefficients and calibration due date
    - The next part will contain information such as desired filter information
    - The rest is still undefined but this leaves plenty of room for expansion.
- The Digital output section definition is still in work
- The Specifications are in work and on schedule

From Dean Becker
March 11, '94
USCA Status

First milestone is April 4,'94

LDS is to provide NASA with component selection advice

NASA has been given some information already

**Alternative for Tag RAM**

System critical single source item

**8751 substitute for DS5000**

Less expensive, surface mount, low profile

**Help with Digital output definition**

Cable testing, technical discussions, component selection

**Help with diagnostic methodology**

**Help to identify and eliminate one shots, pots, mechanical relays, etc.**

A list of surface mount parts and prices is being generated at LDS based on the version 1 USCA to be given to NASA

We have also helped them with suggestions on physical and mechanical mounting and placement.

We understand all details of the USCA schematics and the flow of the internal control firmware. We have also gone through the preliminary specification in detail.

We need to be involved in all of the system aspects that surround the USCA.

USCA

**This is well defined as per the contract and the schedule.**

SAMS

**We will need a SAMS for our customers for the commercialized version. This is for the NASA version 3 type.**
**Probably best to guide this design then use as is.**

ADAS - Some funding in FY '94 then follow on in FY '95

**We have suggested to NASA that this be a CMUX. A new input card would need to be developed. We need to convince NASA that LDS should do this design.**

TRP

**We will need this for any commercialized version.**
**Likely that this will be done with the co-op help**
**Best to use this design as is with our inputs on the way**

550

**We need to work with NASA and provide help on this as required.**

The integration path into LDS manufacture has been identified.

Schematic entry will be redone at LDS

Board layout will copy NASA boards and auto route as possible

We are working up a per unit price for the USCA

The USCA contract should be released to TRDA March 15, '94

From Dean Becker
March 22 and 23 meeting with NASA
USCA Notes:

- We will need to create a test facility for the individual boards of the USCA for the time when we go into production.
- NASA has done environmental testing.
  - Temperature testing: -30 to +50 degrees C.
  - Operational analog output with 1X and 10X gains.
  - An accuracy of 15.5 bits was obtained.
  - EMI testing not done.
    - To be done on the Version 2 USCA.
- There will be no temperature compensation on the USCA.
  - With the dual calibration path it is not needed.
  - Sensors are not corrected for temperature by the USCA.
- The Burr Brown D/A used for the excitation voltage is running too hot. It is being changed out for one that is smaller and costs less.
- Digital output:
  - Curtis has breadboarded the design
  - It will be asynchronous with:
    - 1 start bit
    - 16 data bits
    - 2 parity bits
    - 1.5 stop bits
  - It will be implemented with the Phillips 87CE558 microprocessor or with a PAL by April 10.
  - I received a fax from Curtis regarding the design plan and direction.
- Multi-chip module (MCM).
  - There is currently about a 50% reduction in the size of the circuitry using surface mount technology. Due to this the use of the MCM is questionable. The MCM requires a $10k NRE.
- Test procedures are 15% complete.
  - Environmental
  - Electrical
- The Mechanical drawings are to be done later than indicated on the schedule. The schedule indicated completion at CDR. Releasing them 2 to 3 weeks later will not impact Lorals ability to fabricate version 3.
- The replacement for the DS5000 will be the Phillips 87CE558.
  - Based on the Intel 8751
  - Has 32k of flash EPROM
- The second source for the tag RAM is a chip set.
  - Cost is less than current tag RAM.
    - May use this instead of the current tag RAM.

Available from more than one source.
Microchip technology PIC16C56 8 bit RISC microcontroller.
1K x 12 program EPROM
32 X 8 data RAM
12 I/O lines
Microchip technology 93AA56 (256 X 8) CMOS EEPROM.

SAMS notes:

NASA Discussed block diagrams (2 enclosed) for the SAMS.
3 SAMS PCBs are in at NASA as of March 18.
NASA will build one.
We will receive one.
We will procure the parts.
We will build for our future use.
NASA will test it for us.
It is to be put into an enclosure for marketing demos.
We are to receive the parts list by fax ASAP.

Grumman gave a detailed description of the NASA sensor data acquisition, collection and distribution system.

NASA KSC/PMS diagrams (2 enclosed) are the present system.
Transducer data collection and distribution diagram (1 enclosed) is the future system.

NASA discussed three approaches to the Advanced Data Acquisition System (ADAS).

A NASA developed VME chassis at the pad
A 550 approach at the pad
A CMUX approach at the pad with data to the 550 at LCC

Each approach includes input cards for the USCA digital output signal. These cards would have 40 (TBD) channels of input each.

Considering Loral's recent experience in this area, NASA is inclined to go with a Loral design.
NASA wants a prototype by this October.
We will prepare a proposal within the next two weeks.

David Payne and I will visit NASA on April 6th and 7th

I will be interfacing with NASA for the electrical and mechanical design issues of the USCA.
We will be presenting NASA with a proposal for the ADAS.

From Dean Becker
April 6 - 8 meetings with NASA/I-NET

USCA

Received latest schematics and parts list

Discussed areas which have changed

Input amplifier chain is now broken into 3 cascaded amplifiers instead of one. This allows calibration without the amplifier offsets becoming a significant part of the reading.

Input multiplexer now has the following inputs:

- Input signal (differential)
- Analog output signal (single ended)
- + Excitation (single ended)
- - Excitation (single ended)
- Temperature (single ended)
- 6.8 V Reference (single ended)
- 0.68 V Reference (single ended)
- 0.0 V Reference (single ended)

Microcontroller

- Currently using only EEPROM for program and external storage.
- Suggested using separate EPROM for program memory and EEPROM for external storage.
  - EEPROM could become altered in program space.
    - USCA would not function
    - EEPROM would need to be unsoldered to reprogram.
  - In this case the EEPROM could be a smaller memory size.
  - The EPROM is not an expensive or large item.
  - I-NET has tentatively agreed to this.

Combinational logic circuits could be replaced by PALs.

- Reduced circuit size.
- Flexibility for change and debug.

Mechanical design - Schematics are now organized by potential physical layout.

Four PCBs.

- I/O Protection
- Input Analog
- Output Analog
- Digital / Processor

LDS will look into possible surface mount connectors for interboard connections.

LDS will look into possible 2 bit parity code schemes for the digital output word.

SAMs

NASA has given LDS one set of the latest SAMS PCBs.

We will procure the parts and assemble the boards.
NASA/I-NET will modify to the current configuration and debug the boards.
We will use them for test and demonstration.

We also have 25 Tag RAM boards which may be assembled for test and demonstration.

Advanced Data Acquisition System (ADAS)

Three possible implementations proposed.
NASA preferred having a CMUX at the pad with data to a 550 at the LCC.

NASA requests a prototype by October '94 and production units by January '94.

Data decimation was discussed.
Decimation will be performed at the USCA
Data rate is expected to be 2 Megasamples / Second.

MLP requirements (there are 3 MLPs).
200 sensors.
Complete redundancy to the ADAS box level. (i.e. 1 USCA feeds 2 ADAS input channels.)

Pad requirements (there are 2 pads).
80 sensors.
Complete redundancy to the ADAS box level. (i.e. 1 USCA feeds 2 ADAS input channels.)

This is a total of 10 ADAS units
54 input cards (assuming 32 channels each)
10 bridge / time code cards
10 output cards
10 CPU cards
10 24 bit decoder cards (for the 550)

Design of the input card will be done by NASA engineering.
The design will use the standard CMUX interface for input cards.
VME interface.
PDB interface.
Simulator and associated circuitry.

The rest of the design is to be done by NASA engineering
LDS will assist with design details and documentation for:
Standard CMUX circuitry
Xilinx design advice
Requirements
Block level design

Design can be done on paper by NASA then input into the LDS Cadence system by LDS.
Simulation would require NASA travel, however this can be minimized by simulation definition and preplanning.
PCB layout will be done at LDS.

LDS action items

- Preliminary functional block diagram and description for
  - Overall system
  - ADAS
    - Hardware
    - Data flow
    - Software
- Preliminary schedule and budget

Received USCA video tape.

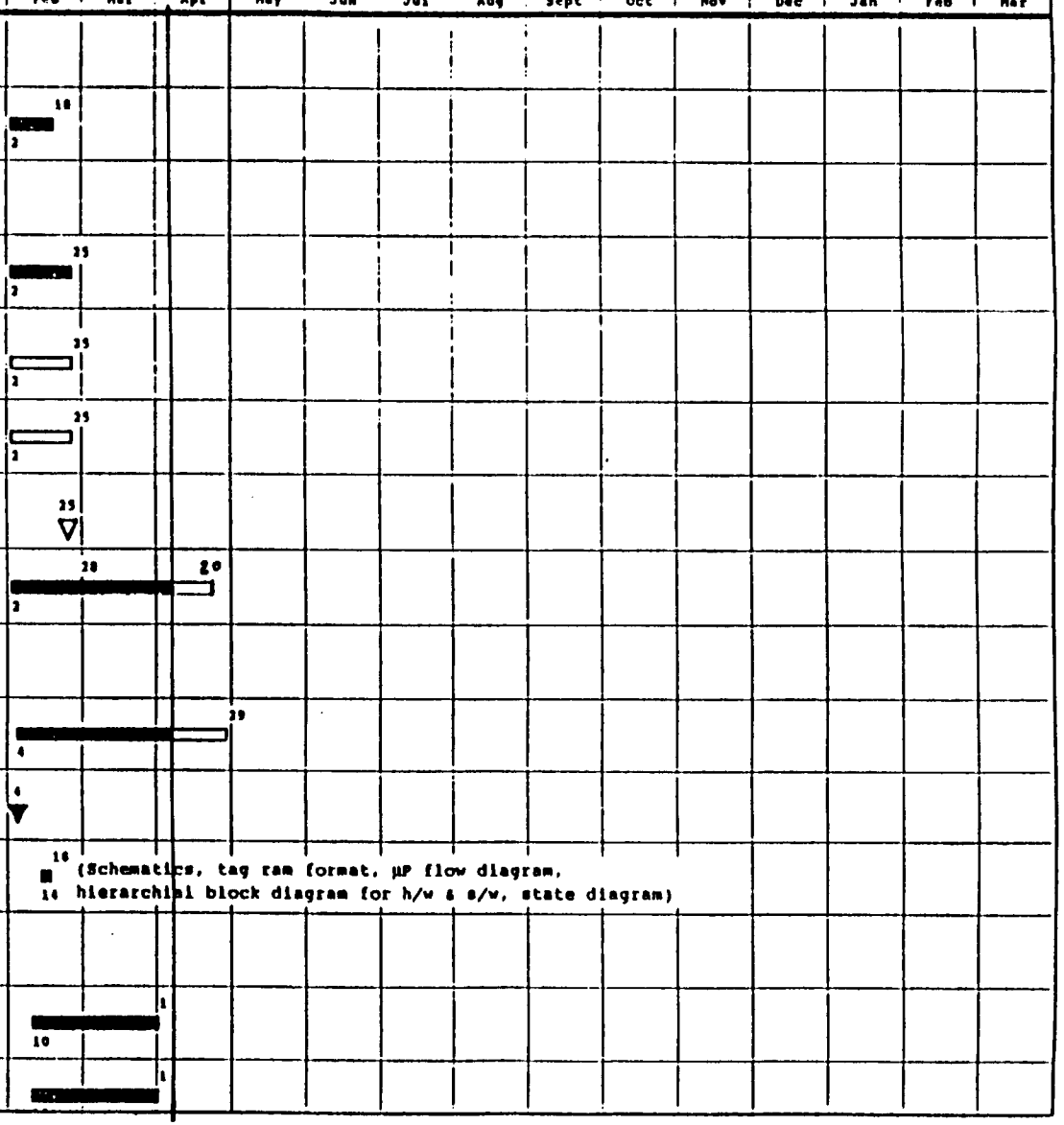
TITLE: MINIATURIZED UNIVERSAL SIGNAL CONDITIONING AMPLIFIER

LAB: DAS

# PROJECT SCHEDULE

ATTACHMENT B 4-13-94

| Item No. | Activities | Status | Proj % Compl |
|---|---|---|---|
| 1.0 | VERSION 1 TEST | | |
| 1.1 | Electrical Test (I-NET) | | |
| 1.2 | Environmental Test | | |
| | Temperature (I-NET) | | |
| | EMI - Radiated (NASA) WILL NOT BE DONE ON VERSION 1 | | |
| | EMI - Susceptability (NASA) WILL NOT BE DONE ON VERSION 1 | | |
| 1.3 | Finish Version 1 Testing | | |
| 1.4 | Digital Output Design | | |
| 2.0 | VERSION 2 DESIGN | | |
| 2.1 | Multi-chip/Hybrid Module Investigation | | |
| 2.2 | 30% Specification - (NASA, I-NET, Loral) | | |
| 2.3 | Preliminary Design Review | | |
| 2.4 | Inputs from Loral | | |
| | Mechanical | | |
| | Electrical | | |



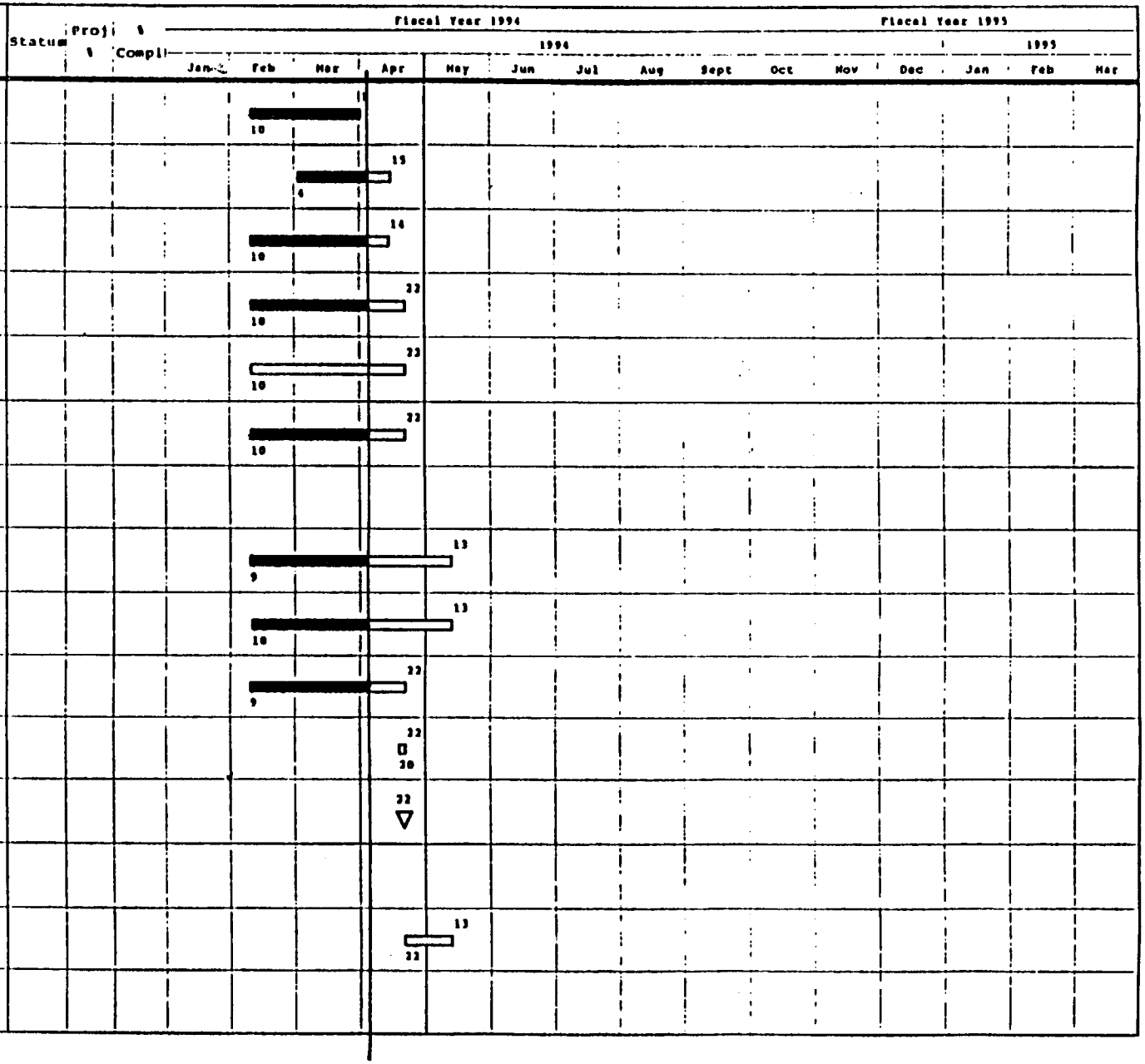

STATUS: 02-10-94

TITLE: MINIATURIZED UNIVERSAL SIGNAL CONDITIONING AMPLIFIER

LAB: DAS

# PROJECT SCHEDULE

| Item No. | Activities | Status | Proj % | % Compl |
|---|---|---|---|---|
| | Components | | | |
| | I-NET Review of Inputs | | | |
| 2.5 | Revise Schematics | | | |
| 2.6 | Revise PCB | | | |
| 2.7 | Create Mechanical Drawing | | | |
| 2.8 | Create S/W Documents | | | |
| 2.9 | Write Test Procedures | | | |
| | Electrical | | | |
| | Environmental | | | |
| 2.10 | 60% Specification | | | |
| 2.11 | Version 2 Critical Design Review | | | |
| 3.0 | RELEASE VERSION 2 DESIGN PACKAGE | | | |
| 4.0 | VERSION 2 DESIGN, BUILD & TEST - I-NET | | | |
| 4.1 | Build 5 Units (I-NET) | | | |
| 4.2 | Test Version 2 | | | |




STATUS: 02-10-94

TITLE: MINIATURIZED UNIVERSAL SIGNAL CONDITIONING AMPLIFIER

LAB: DAS

# PROJECT SCHEDULE

| Item No. | Activities | Status | Proj % | % Compl | Fiscal Year 1994 | | | | | | | | | | | | Fiscal Year 1995 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | 1994 | | | | | | | | | | | | 1995 | | |
| | | | | | Jan | Feb | Mar | Apr | May | Jun | Jul | Aug | Sept | Oct | Nov | Dec | Jan | Feb | Mar |
| 8.1 | Build | | | | | | | | | | | | | 14 30 | 17 31 | | | | |
| 8.2 | Test | | | | | | | | | | | | | | | 16 18 | | | |
| 8.3 | Revise | | | | | | | | | | | | | | | | 30 16 | | |
| 8.4 | Release | | | | | | | | | | | | | | | | | 13 30 | |

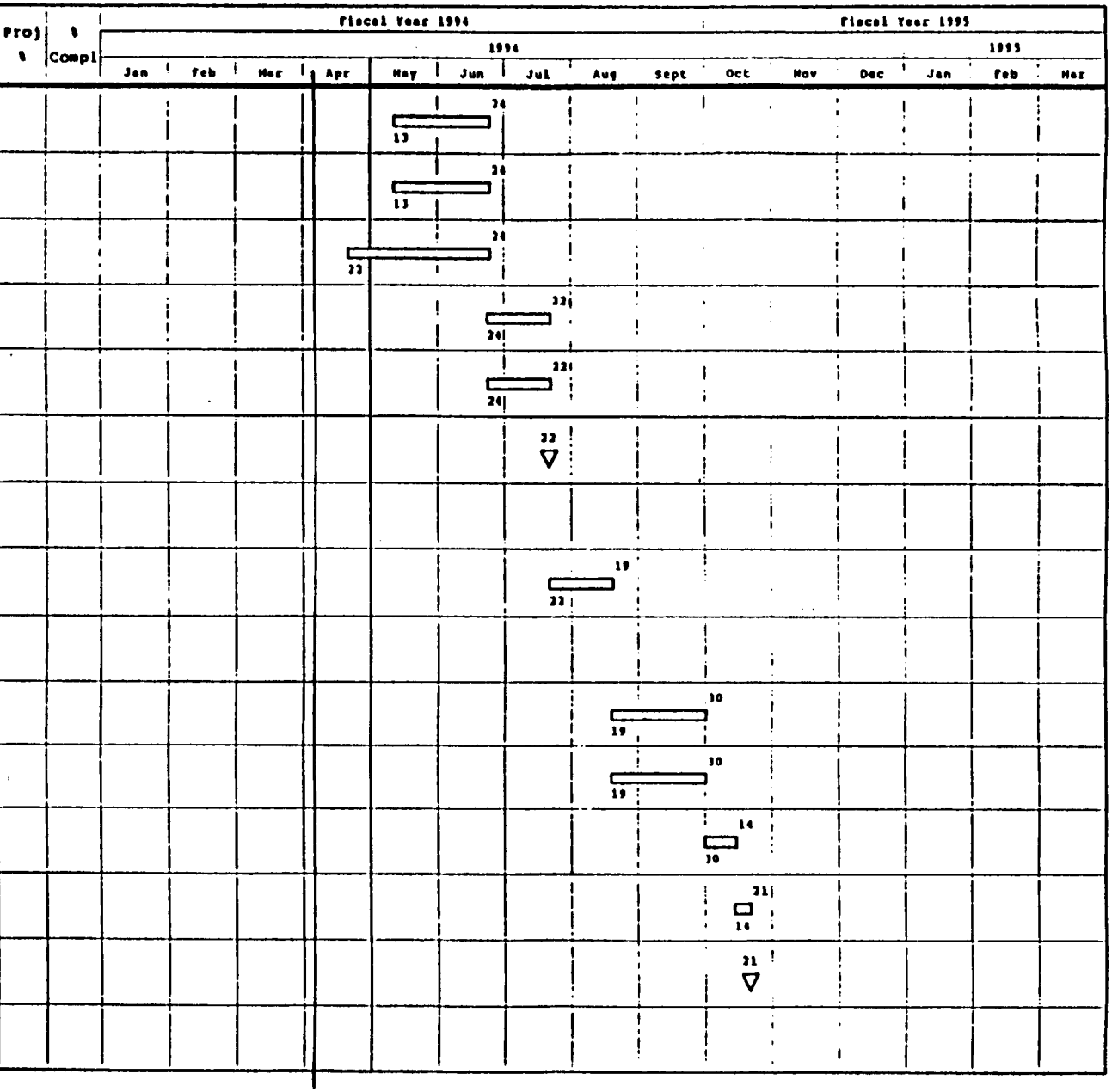
STATUS: 02-10-94

TITLE: MINIATURIZED UNIVERSAL SIGNAL CONDITIONING AMPLIFIER

LAB: DAS

# PROJECT SCHEDULE

| Item No. | Activities | Status | Proj % | % Compl |
|---|---|---|---|---|
| | Electrical (I-NET) | | | |
| | Environmental (EMI,Temp., Vibraton, etc.) NASA | | | |
| 4.3 | Enter Version 2 Design Package (Loral) | | | |
| 4.4 | Revise Version 2 (I-NET, Loral) | | | |
| 4.5 | 90% Specification | | | |
| 5.0 | RELEASE VERSION 3 DESIGN PACKAGE | | | |
| 6.0 | VERSION 3 DESIGN, BUILD & TEST - I-NET AND LORAL | | | |
| 6.1 | Build 5 Units (Loral) | | | |
| 6.2 | Test | | | |
| | Electrical (I-NET) | | | |
| | Environmental (NASA) | | | |
| 6.3 | Revise Loral Package (I-NET, Loral) | | | |
| 6.4 | 100% Specification | | | |
| 7.0 | RELEASE FINAL DESIGN NASA VERSION (LORAL) | | | |
| 8.0 | COMMERCIAL PACKAGE | | | |




STATUS: 02-10-94

Fr: Dean R. Becker
Re: USCA milestone 2

LTIS has input all USCA schematics and parts lists and has delivered the current package with questions to NASA. We have also assisted with the overall design of the USCA as well as the system with which it operates (ADAS). See the attachment A. Included is an updated project schedule for the USCA development. See Attachment B.

From Dean Becker
April 25 - 27 meetings with NASA/I-NET

USCA Design review

Distribution

**USCA specifications**
**Updated schedule**
**Hardware documentation**
**Software documentation**

**Due to recent cost estimates for the USCA, numerous tradeoffs are being considered. This affects the specifications. It also affects the USCA schedule.**

**Possible changes being considered to reduce the price of the USCA.**

**Use components with commercial temperature range (0 to 70 degrees C).**

This needs to be checked with respect to internal heating in the USCA and actual requirements for case temperature range.

**Use single input channel as opposed to the A/B channel calibration scheme.**

This reduces overall gain and offset calibration over temperature. This could be compatible with a system requiring only 10 or 12 bits of accuracy.

**Use DSP chip only and remove the other microprocessor and its support chips.**

This only requires new firmware to be written for the DSP chip. Two EPROMS will need to be added to the DSP circuitry.

**Replace 16 bit A/D with 12 bit A/D.**

The 12 bit A/D is half the price of the 16 bit. Accuracy is compromised.

**Remove the DDF chip.**

Filtering up to 2 kHz can be done in the DSP chip. This compromises use with certain vibration sensors. A 60 Hz analog notch filter will need to be added. Extra code needs to be added to the DSP chip.

**Replace the analog reconstruction filters on the output circuit with less expensive ones.**

Minimal effect.

**Replace PGA (programmable gain amplifier) with less expensive one.**

Tolerable effect on accuracy.

**Due to the redesign effort we are anticipating a one month hold in the schedule to complete version two.**

USCA specification review

**Enclosure must be weatherproof but does not need to be potted.**

A stainless steel enclosure is preferred over aluminum as the aluminum will oxidize in the KSC environment.
The MS connectors on the USCA will not have caps attached.
The ID plate for the USCA may be a stick on or bolt on type rather than etched into the enclosure.
There are some specifications that are changing and evolving due to the above mentioned possible changes that may be applied to the USCA.
NASA will update the specifications to reflect changes identified during the meeting.

## USCA details discussion

There was a discussion on the digital output circuit and format for the USCA.

- Use the UART built into the DSP chip.
  - 8 bit data format, parity, one start bit, one stop bit.
    - Use alternate even/odd parity scheme for high/low byte identification.
  - Limits overall USCA output word rate for 9.6 kHz information output.
    - NASA/Grumman agrees that this is acceptable.
    - This does not change the input sampling, only the Nyquist rate for the output is affected.
    - The original rate supported 10 kHz information.

## ADAS details discussion

Operation using CMUX to a 24 bit decoder in the 550.

- Discussed details of the source, label, packet to tag in the 550.

Discussed schedule for October 1 delivery of first ADAS.

- Input card design
  - NASA design of input circuitry.
  - LTIS aids with integration to existing circuitry.
  - Input is into LTIS schematic, layout, manufacturing system.
- System design aided by LTIS.
- Project management by NASA and LTIS.

Created preliminary schedule and statement of work.

## Continued with further discussions

USCA output definition
ADAS input card definition
USCA cost and tradeoffs
USCA filters, DSP, etc.

## Details on changes for the USCA

### Digital output circuit

**Will use the UART in the DSP chip**

- Eliminates the cost of external circuitry.
- 8 bit data
- One start bit, one stop bit
- One bit that can be parity or user defined

**The 9th bit will be used for parity and for high byte/low byte ID.**

- The high byte will have odd parity
- The low byte will have even parity
- A lookup table will be used in the DSP to do this in real time.
- The parity sequence will define high/low byte of the 16 bit output word.
- The input card in the ADAS can use integration to continue to synchronize high and low bytes with parity errors.

**The serial output will be transferred by current loop**

- This reduces component count in the output circuitry.
- Use optical isolator for galvanic isolation out of the USCA.
- Power for the current loop will come from the ADAS input card.
- Use a 20 mA (TBD) current loop.

**Serial output rate of the USCA**

- The serial output rate of the DSP is limited to 422 kbits/sec.
- The total number of bits as defined above is 22 for each sample to be output.
- This gives a maximum 16 bit word rate of 19.18 kwords/ sec.
- The maximum frequency content of the output data must therefore be less than 9.59 kHz.
  - **NASA and Grumman have agreed that this rate is acceptable.**
- Note: The input sample rate to the USCA remains at 38.4 kHz.

### Preliminary redesign goals for the USCA

**Use components with commercial temperature range (0 to 70 degrees C).**

- This needs to be checked with respect to internal heating in the USCA and actual requirements for case temperature range.

**Continue to use the A/B channel calibration scheme.**

- Grumman has requested that this remain in tact.
- Output calibration circuitry will remain in place as well as input voltage standards and excitation calibration.

**Use DSP chip only and remove the other microprocessor and its support chips.**

- This requires new firmware to be written for the DSP chip.
- Two EPROMS will need to be added to the DSP circuitry.

The 8k x 8 EEPROM will be moved from the 5000 to the DSP.

**The use of the 16 bit A/D is to continue.**

This is under investigation, however preliminary findings are that this will be a requested feature and less bits would take away from the ability to commercialize the USCA.

**Remove the DDF chip.**

Filtering up to 2 kHz can be done in the DSP chip. This compromises use with certain vibration sensors.
A 60 Hz analog notch filter will need to be added.
Extra code needs to be added to the DSP chip.
Decimation can be done in the DSP chip after filtering.

**consider dual filter structure to conserve DSPs resources.**
**IIR then decimate followed by FIR and decimate.**

**Replace the analog reconstruction filters on the output circuit with less expensive ones.**

Minimal effect.

**Replace PGA (programmable gain amplifier) with less expensive one.**

Tolerable effect on accuracy.

**Redesigned digital output circuitry as defined earlier.**

This will reduce component count and therefore cost.

**With the above restrictions we can expect the following conditions:**

12 to 15 bits of digital accuracy
0.2 dB flatness from DC to 8 kHz for gains of .25 to 800
0.2 dB flatness from DC to 1 kHz for gains of 1000 to 2000
Digital filtering will be available from 0 to 2 kHz
The excitation accuracy will be 1 mV
The preliminary components cost for this implementation is $550.00

## Action items

### NASA

**Check out the feasibility of using commercial parts for the USCA.**

Internal heating from power dissipation of components.
Effect of direct sunshine on the USCA case.
Establish a final case temperature range specification based on internal heating effects and the commercial (0 to 70 deg. C.) temperature range.

**Issue a revised specification for the USCA with changes established from the meeting.**

**Issue written test procedures for the USCA when available.**

### Loral

**Check on the cost of PCBs**

Check board specifications that must be held.
Check multiple vendors including the one used by I-NET.

Check feasibility of using 12 bit converter for commercial USCA.
Continue checking on pricing.

Details on the ADAS design

NASA needs a prototype ADAS operating by October 1, '94

An ADAS would include the following:

VME type chassis - will need CMUX backplane
CPU card
Bridge / time code card
Output/recorder interface card
USCA digital input card

The entire system will also need:

A TAXI to fiber optic cable interface at pad for ADAS output.
This will need to be up to 100 meters for the MLP.
Short run in the PTCR.
Interface for the 550 at LCC
A fiber optic to TAXI interface.
A TAXI to byte parallel interface (custom card for the 550).
A 24 bit decoder card for the 550.
Setup and control software for the ADAS
Setup and control software for the 550

SAMS cards will also be resident in the ADAS chassis

The following cards must be designed and built for the complete system:

The USCA digital input card (goes into the ADAS chassis)
The SAMS controller card (goes into the ADAS chassis)
The TAXI to byte parallel interface card (goes into the 550)

Fiber optic interfacing may be handled by a separate unit.

At this time these are the major tasks for the ADAS development.

Design of the USCA digital input card.
This will be a cooperative effort by NASA and Loral.
Overall design of the entire USCA-SAMS-ADAS-550 system.
This will be a cooperative effort by NASA and Loral.
The development of the SAMS controller card may be concurrent but is not subject to the schedule restrictions of the ADAS.
This will be a cooperative effort by NASA and Loral
Development of the setup and control software for the ADAS.
This is to be developed by NASA.
Development of the setup and control software for the 550.
This is to be developed by NASA.

Action items for the ADAS development.

NASA

Check the rate of the fiber optic link.
Can it provide 125 MHz for the TAXI interface?

Loral

**Investigate 24 bit decoder questions further.**

- Can tag be based on label information only?
- Can source be changed without a tag change?
- How is setup programming done?

**Check on TAXI electrical line lengths possible.**

**Verify ADAS output rates and 24 bit decoder input rates.**

**Check on TAXI to 24 bit decoder interface.**

**Write up ADAS:**

- Statement of work
- Operational outline including:
  - **Data flow**
  - **Diagrams**
- Preliminary schedule

From Dean Becker
May 17, '94 Meeting with NASA/I-NET/Grumman

ACTION ITEMS

- Finnish temperature testing - INET/Pedro
- Build and test current loop circuit for USCA output - NASA/Curtis
- Noise testing - NASA/Curtis
- Test SCF analog filter circuit - INET/Pedro
- ADAS proposal write up - Loral/Dean/David
  - Investigation of ADAS output methodology
- USCA specifications - INET/Pedro
  - Input impedance
  - Common mode
  - Output ripple
  - Output load
- USCA input over voltage protection with power off - INET/Pedro
- Issue revised specification for the USCA - NASA/Bill

Temperature testing is in process

- One test run in the lab with 10 Watt load inside large USCA case.
  - External temperature measured 22 degrees C.
  - Case temperature measured 29 degrees C.
  - Inside temperature measured 44 degrees C.
- Testing outside to be done.

USCA output circuit

- The plan is to use a current loop with the current source in the ADAS. Curtis believes that this will cause a problem with frequency response.
- The circuit will be built and tested over a long run.

Noise and error handling

- We do not know what the noise and error results will be at the time of launch.
- Testing will be done with the chosen USCA digital output transmission method using a Bit Error Rate Tester (BERT).
- Test results will show the Error Rate from Noise In the Environment (ERNIE).
  - Test in the lab
  - Test at the pad
  - Test at the pad during launch
- Error handling will be determined by the results of this testing.
- It is anticipated that data with errors will be sent but will be tagged as such.

## Filtering in the USCA

- Filters allowed in the DSP.
  - From 2 to 10 kHz no filtering
  - Below 2 kHz filtering can be done but with less than 511 coefficients.
  - At higher decimation rates more coefficients may be used.
  - May be able to use IIR type filtering
    - Phase irregularities can be removed with post processing if necessary since the characteristics are predictable.
- Anti aliasing analog filter.
  - A Switched Capacitor Filter (SCF) is planned.
    - Low cost - $3 or $4 vs. passive filter aprox. $35.
    - This implementation may create noise problems and so the circuit needs to be tested first.

## Synchronization of sampling in the USCAs.

- Asynchronous sampling
  - Time tagging as will be done in the ADAS is sufficient resolution for NASAs needs.
    - This is within about a 4 microsecond error window.
  - Post processing correlation can be done using ADAS time tags.
    - This would require further processing i.e. interpolation and offset compensation in the correlation.
    - NASA does not have a current requirement for this capability.
  - Maintaining individual ADAS time tags for data samples is not reasonable for storage.
    - If data is regrouped by time then interpolation in the post processing cannot be done.
  - Asynchronous sampling would be sufficient for eyeballing strip charts.
- Synchronous sampling
  - Data would be available for post processing without special processing to fix timing.
  - The process of time tagging in the ADAS would be much easier as would be storage with time information.
  - Impact on the USCA design appears to be minimal (TBD).
  - The ADAS would be the source of this synchronization.
  - The 429s are doing staggered synchronous sampling at this time at the pad.

## ADAS output to the 550

- The 550 bit sync/decoms are limited to 8 or 10 MBit operation.
  - For PCM streams from ADAS this would require 4 lines.
- NASA would like to 'free up' some slots in the 550.

This would require removing the (6) bit sync/decoms and using (possibly) the MNI card.
Use of the MNI would maintain the packetized data concept
New software would not be needed for the MNI card (we think).

We need to write up the ADAS proposal in an open way with respect to the output so that we can start contract work on this.

Tag RAM

Implementation

This function will be done using the Microchip RISC controller chip and a serial EEPROM.

This is less expensive

Not tied to one vendor for parts

Tag RAM programmer

NASA is looking at students as co-ops to do the programmer development.

Transducer health check

The idea was presented

NASA is investigating this type of testing

This is good for a future implementation but not the current design due to time and extra cost.

USCA excitation resolution

The use of 16 bits is somewhat of an emotional issue ( like the input A/D).

The cost of this is minimal

USCA input circuitry

The input attenuator is shunt out when not in use and does not add noise to the amplifier chain.

The input impedance of the USCA is to be found.

The input over voltage protection should work with the power supplies off. This is being checked.

The input multiplexers are good to 35V.

The common mode specifications are being checked.

The gain step size is an implementation choice.

Any gain can be chosen by using the DSP.

USCA analog output

The output ripple specification needs to be looked at.

The high impedance of the sink is desirable.

Check on the output loading specification.

Repeatability specification

Under same conditions
Each test is individually evaluated not averaged.

Accuracy measurements

These are done as a percentage of full scale because this is a common way to do it. It is recognized that percent of reading is better.

Meetings

Bill Larson has indicated that he would like to have a regular (weekly) interchange, in person, to pull together the details of the overall USCA/ADAS/SAMS/550 system and individual details. We need to work out the details that will allow my presents at KSC for several days weekly as required.
Bill Larson will be in San Diego the week of July 24,'94. He has suggested that we use this opportunity to meet with Sarasota and San Diego personnel concerned with the USCA system.

From Dean Becker
May 25 and 26 Meeting with NASA / I-NET / Grumman

Action items

- Order 5 Motorola DSP chips in surface mount. (LTIS/Dean)
  - Get full part number from Pedro.
- Finnish temperature testing (I-NET/Pedro)
- Look into parts for the USCA output circuit. (LTIS/Dean)
  - High speed opto-isolators for current loop.
  - Inexpensive, small DC-DC converter for RS-485 method.
- Finnish USCA output circuit. (NASA/Curtis)
- Noise testing (NASA/Curtis and LTIS/Dean)
  - Develop BER test for use at the pad with new output circuit.
- ADAS proposal write up (LTIS/Dean/David)
  - To be delivered to TRDA in two weeks.
- USCA specifications (NASA/Bill)
  - Complete specifications to date.
- Check data on the MNI card interface. (LTIS/Dean)
  - Speed, drive, number per 550.
- CMUX software (LTIS/Dean)
  - Source code, support tools needed.

USCA items

- The Motorola DSP chip used in the USCA now has a 24 week lead time.
  - NASA has 5 pieces that they will use for the version 2 design.
  - LTIS needs to order 5 pieces for the version 3 design right away.
- USCA temperature testing
  - A version 1 USCA was checked in sunlight with the power off.
    - Outside air temperature was 27 degrees C.
    - The case temperature was measured to be 42 degrees C.
  - This test will need to be performed at a higher ambient temperature with power and load applied.
- USCA output circuit
  - Current loop test circuit
    - Just began testing.
    - Using opto-isolator with built in amplifier for speed.
      - Need to check on high speed opto-isolators with out the amplifier.
      - Considerable roll off in the waveform.
      - Using 60 mA in the loop - too much.
  - Differential transceivers (75ALS176)
    - Need to check on DC to DC converters
      - Price, size, availability
    - This would be a better transmission scheme if the cost works.

Noise testing

LTIS will help with BER testing and setup

**The galvanic isolation is only required at the output of the USCA not at the input to the ADAS.**

### SCF antialiasing filter

**Tested at 10 kHz, switching noise was found to be 1 mV with a 50 nS period.**

This can be reduced with layout and filtering.

**The filter will follow the sample rate change since both are based on the same clock and divider.**

### Overvoltage protection

**This will be tested before version 2.**

### USCA synchronization

**Circuit design is complete.**

**Synchronization clock will be feed to the USCA by the SAMS line.**

This will be the same frequency for all USCAs regardless of the decimation rate of an individual USCA.

The rate will be the maximum A/D sample rate divided by 128 which is 40 kHz/128 = 312 Hz.

This will allow synchronous sampling with decimation rates up to 128 using binary increments.

This clock will be created by the output card in the ADAS and will be available to all other cards via a dedicated line in the PDB that was formerly the Nth sample line.

### Error handling

**When parity errors are detected from USCA to the ADAS input they will set a bit in the output word from the ADAS.**

This could be a bit in the tag or the data field.

### USCA progress

**PCBs will be ready for version 2 USCA by June 17-24.**

## ADAS items

### ADAS output to 550 input

**NASA wants the MNI cards to be used in the 550s**

To free up slots now used for bit sync / decoms.

How many MNI inputs can be used per 550 chassis?

Each ADAS output will be one MNI input

**See system diagram for over all MNI utilization.**

The TAXI output of the MNI format needs to electrically drive from the MLP to the PAD.

It expected that three MNI cards will be needed for each 550.

**PCM output**

NASA does not need this format

**They are willing to include it in the output card design**

It will be a design done by LTIS.

This could be used for initial debug of the ADAS.
LTIS would like to include this format to have a universal output compatible with much existing equipment.

The fiber optic transceivers can operate up to 175 MBit rates.

NASA needs the ability to modify the firmware in the ADAS after delivery.

They will want source code for the card drivers

They will also put into place whatever software tools are needed to support code modification.

What tools are needed?

A specification for the software that will be needed for the 550 system is needed.

Synchronization of USCA sampling.

The output card will be able to be a master or slave to other chassis with the synchronization signal mentioned earlier in this report.

SAMS

The SAMS interface will only be required to communicate with USCAs.

It will not be used to communicate with tag RAMs directly. This will significantly reduce the complexity and cost of the SAMS interface that will reside in the ADAS.

Test

Board testing to be done by LTIS.

Initialization of boards

Initial testing

System testing of the ADAS prototype to be done by NASA.

Documentation

Will follow LTIS CMUX guidelines for board development.

Will follow NASA guidelines at the system level.

Deliverables

See modified preliminary statement of work for LTIS deliverables.

NASA will be responsible for chassis and power supply selection.

Schedule

See attached preliminary schedule.

From Dean Becker
June 13th and 14th meeting with NASA / I-NET

Action Items

Order 5 Motorola DSP chips in surface mount. (LTIS/Dean)

**Part number DSP560001FC27 has been ordered (6 pieces, $32.84 each, and 36 week lead time). The reason for the long lead time is high demand and time phase of the manufacturing cycle. The distributor can help us to deal with this.**

Finnish temperature testing (I-NET/Pedro)

**This will be continuing when the new canister is available and will be done using an internal load.**

Look into parts for the USCA output circuit. (LTIS/Dean)

**An inexpensive, small DC-DC converter for RS-485 method has been found and a sample is to be included in the output circuitry for testing. (NASA/Curtis)**

Finnish USCA output circuit. (NASA/Curtis)

**This is designed using the RS-485 circuitry.**

Noise testing (NASA/Curtis and LTIS/Dean)

**Develop BER test for use at the pad with new output circuit.**

This has been tested in the lab using a 721 BERT.

This is to be tested at the pad.

ADAS proposal write up (LTIS/Dean/David)

**The first cut has been delivered to TRDA.**

USCA specifications (NASA/Bill)

**Specifications are complete to date.**

Check data on the MNI card interface. (LTIS/Dean)

**Speed, drive, number per 550.**

The TAXI interface to the MNI card is at a 125 MHz rate.

This line should drive only a single MNI input.

**If the signal is to go to multiple MNI inputs it should be electrically split using active drive circuitry.**

Any number of MNI cards may be used in the 550 to the limit of its bandwidth.

CMUX software (LTIS/Dean)

**Source code, support tools needed.**

Support tools (PSOS, PROBE) and software required have been identified by LTIS and have been communicated to NASA.

ATP document for the USCA (NASA)

**In work.**

The schematics and parts list for the version 2 USCA are to be complete on June 27.

USCA items

## Tag RAM

**Is being implemented using the 16C54 Microchip controller and a serial EEPROM.**

This gives a cost savings and does not tie the Tag RAM into one manufacturer

**Coding for the 16C54 is being done by Bill, one of the new co-ops.**

**A current loop interface is being implemented that will power the Tag RAM circuitry as well as allow communications with the USCA. This is being worked on by Rich, who is also one of the new co-ops.**

**The Tag RAM programmer will also be done by the co-ops.**

## Output circuit error testing.

**BERT done on RS-485 circuitry using a 2000 foot cable in lab.**

Burst errors were found when the fluorescent lights were turned on.

A 422 kHz square wave signal through a RS-485 driver into the cable with termination at the other end produced a 3 Volt signal on another pair of unterminated lines.

**Wires in the cable are not twisted pairs.**

**Consider filtering on the analog signal from the USCA.**

**Consider turning off the digital output when using the analog output in the system.**

Testing will be done at the pad with the 721 BERT on the 16th.

## USCA to SAMS interface circuit

**The SAMS control circuitry has changed significantly and is now called the ADAS USCA Interface (AUI).**

**This circuit will use RS-485 interface and termination like the output circuit of the USCA but will be half duplex bi-directional.**

**This circuit must provide the following functions:**

Send commands and upload data from the AUI to the USCA.

Send Tag data and status from the USCA to the AUI.

Send the sync signal from the AUI to the USCA.

Send a USCA interrupt from the USCA to the AUI.

**This will be accomplished with the following:**

Transmission on the system will be at 9600 baud, asynchronous.

**This allows communication from a computer terminal for test purposes.**

AUI will always send a word at a 312 Hz rate.

**This provides the sync function.**

USCA will use the start bit from AUI as sync.

**This leaves a gap of slightly more than two words for USCA to send a word back.**

**AUI will hold the line in the mark state for two bits before and two bits after its transmission. From two bits after to two bits before, AUI will tri-state its control of the line.**

During this turn around time USCA will take control of the line with a mark state.

If USCA has something to send to AUI it will do it during this time. If not then USCA will hold the line in the mark state.
This scheme allows for enough inaccuracy in timing between the USCA and the AUI so that the units will not walk on each other. It also forces the line to be driven so that noise will not get into the system.

**The value in the word being sent will determine its function.**
The interrupt from the USCA will have a particular value and will be sent when tag data or status are not expected.
The sync only word from the AUI will be uniquely different from commands.

**The USCA circuitry for this function will be:**
A RS-485 driver receiver pair using the same DC-DC converter as the output RS-485 driver.
A 16C54 microcontroller (like the one in the tag RAM).
**Provides the function of a UART to the DSP and screens the sync words so that the DSP does not need to process them.**
Registers and latches to provide a interface between the DSP and the 16C54.

**The AUI circuitry is still TBD**
Could use off the shelf UARTS
Could use the Xilinx for the UART functions.

**The USCA - AUI protocol has been outlined as of June 16 and is available in a separate document.**

**The schematics and parts list for the version 2 USCA are to be complete on June 27.**

**At this time NASA will begin the fabrication of the version 2 units.**
**At this time LTIS will begin entry into its systems.**

**USCA testing will be as follows:**
**EMI**
**Environmental**
**Functional**
ATP
Go-no go testing

ADAS items

**Xilinx schematic input.**
**If possible should be done with an entry system that can be converted to Concept by Cadence.**

From Dean Becker
June 26th and 27th meetings with NASA/I-NET

Action items

USCA temperature testing to continue with new canister this week. (I-NET/Pedro)
ADAS proposal with budget to TRDA ASAP. (LTIS/David)
USCA software needs (I-NET/James)
- Memory and I/O map
- Task list, complete, to do

ATP document for the USCA (NASA)
ADAS AUI control interface (NASA/Joey)
- Define UART functions, list of tasks, control by sun station.

ADAS input interface (NASA/Curtis)
- Define UART functions, registers, Xilinx functions, priorities.

ADAS VME, PDB, simulator interface and definition. (LTIS/Dean)

USCA items

Noise testing for USCA output circuit
- Implemented at the pad with a loop using the 721 BERT.
- Test is showing no errors.
- This test will be running during the next launch on July 8.

USCA case design
- Consider using end plugs milled out so that the O-ring is captive.
- Looking at thermal considerations of the stainless case.

Schematics and parts list are ready for entry into the LTIS system.
Completed a review of the USCA schematics with only minor changes.
- Also reviewed the schematics for the tag RAM and the tag RAM programmer.

Tag RAM design is complete in hardware and firmware and is being testing.
The USCA software that will reside in the DSP needs
- A memory and I/O map
- A list of the tasks and functions
  - That need to be done.
  - That have been completed.
- A completion date.

Temperature testing using a distributed 10 Watt load will be done using a stainless prototype case in the sun this week.

ADAS items

Focus was on the AUI control interface and the USCA digital output interface.

This will be one card serving 16 USCAs.

Considering UARTS for both circuits

AUI

Discussed sync pulse interface

Use of CTS to sync UARTs

AUI automatic functions

Considering implementation using 8051 like controller with dual port RAM interface to the VME.

Register definition and other documentation.

Diagnostics

Input

Need pull up and down on 485 input for positive detection of absent USCA in analog output mode.

Implementation of multiplex packet control will likely be done in a dedicated Xilinx.

Time stamp packets have priority over data packets inside input card.

Time will be within 3.2 microseconds of data arrival.

Discussed packet protocol.

Register definition and other documentation.

Diagnostics

Data output tagging

Sun station collects ID from USCA via AUI control interface in ADAS.

Using data base Sun station assigns labels for USCA data

This label becomes a tag to the 550

Tag includes PDB type info

The sun station sets up tags in the 550

Next Visit

Discuss CMUX card interfaces for

PDB

VME

Simulator

Discuss overall system aspects

Output card function

550 tag association

Sun station function

From Dean Becker
July 12th through 14th meetings with NASA/I-NET

Action items

Curtis needs a hard copy of Xilinx library for 4000 series. (LTIS/Dean).
Coordinate PDR for ADAS packet - tag protocol. (LTIS/Dean).
Create basic framework schematics from ARINC-429 board for ADAS input card. (LTIS/Dean).
ADAS ATP document for USCA. (NASA/Tony).
Vibration, environmental, EMI, electrical.
ADAS input card needs to begin documentation outline for design. (NASA/Curtis/Joey).

USCA items

Noise testing for USCA output circuit
80 errors were found during the last launch.
Will set up a monitoring function for the August launch to determine the characteristics of the errors.
USCA case design
Will continue now that temperature testing is complete.
Considering internal rail like assembly to thermally conduct heat to the end plates.
Nick is entering the USCA parts list into the LTIS system.
Reviewed specific part choices with Pedro.
Temperature testing using a distributed 10 Watt load has been completed.
With an air temperature of 35 degrees C, in direct sunlight, and in a plastic box to shield the wind:
Circuit board temperatures rose to 80 to 100 degrees C.
Inside air rose to about 70 degrees C.
Case temperature rose to 55 degrees C.
Options available to reduce circuit board temperatures are:
Populate the long edges of the circuit board with copper traces on all layers to conduct heat from the planes to the edges of the board.
Aluminum or copper rails attached to the long edge of the circuit boards to conduct the heat to the end plugs of the USCA.
Consider an aluminum extrusion on the end plates to radiate heat as well as to protect the end connectors.
Mount the USCA with a gasket to a metal structure.
Mount the USCA out of direct sunlight.
This completes temperature testing until the version 2 USCA is available.

A revised schedule for the USCA development has been generated.

ADAS items

The method of interconnection from the input cards to the outside of the ADAS box needs to be determined.

Discussed details of the common CMUX functions for input cards.

VME interface, PDB interface, and the internal simulator circuitry.

Covered details of the schematics of the ARINC-429 card as well as details of the VME Xilinx, and miscellaneous Xilinx.

Discussed details of the packet protocol in the CMUX.

In reference to the USCA input function.

In reference to the 550.

We will have a design review for this at LTIS Sarasota at the end of the week of July 18.

From Dean Becker
September 14th and 15th meetings with NASA/I-NET

Action items

Co-ordinate the mechanical design with Terry Greenfield of NASA and the LTIS shop for aluminum extrusions. (Dean/LTIS)
Co-ordinate the utilization of the use of the NASA Cadance system with Mike Nastanski of LTIS. (Dean/LTIS)
Co-ordinate update of the USCA schedule with Hank Taylor of INET. (Dean/LTIS)

USCA items

USCA case design

Reviewed the new case design with Bud Steinhoff, Bob Wallace, and Mike Moninger. Numerous problem areas were identified, many being cost drivers.
Relayed these items to the mechanical designers at NASA. All items were addressed and the consensus was the same.
We have a go ahead to move toward the use of an aluminum extrusion for the case instead of stainless steel.

This will reduce the cost dramatically by comparison to the previous design.
It will also drastically improve the thermal transfer qualities of the USCA.

The USCA parts list has been entered into the LTIS system.

I have resolved all known problems with the parts list with Pedro.
Nick has the information to correct the list we have.
Nick has one board schematic of the three entered and is working on the second.

Temperature testing will be done on the new case when the prototype is complete.
A revised schedule for the USCA development will be generated.

USCA testing is expected to complete by mid November.

ADAS training as well as other items has affected this.

ADAS items

Curtis is well on his way with the ADAS input design of the Xilinx.
AUI serial I/O circuitry

Consider individual UARTs for each USCA.
Consider design in Xilinx for flexibility.

Training for the 550 hardware and ADAS issues is scheduled to commence October 3rd at KSC.

From Dean Becker
May 9, '94

## USCA COMMERCIALIZATION DISCUSSIONS WITH DICK TALMADGE - CONSULTANT

### Input analog filtering

#### 60 Hz filtering

**The use of a 60 Hz notch filter will also eliminate any desired signals that might exist in its stop band.**

**The use of a switched capacitor filter will create noise and is undesirable for this application.**

**Is 60 Hz the only frequency that might cause this type of interference?**

Does 400 Hz exist?

Are there multi-phase power signals that might cause other frequencies to show up?

**Consider the use of interference tracking and elimination.**

This is done by locking on to the periodic interference with a tracking oscillator and also tracking the RMS amplitude. The created signal is inverted and then added to the input signal to cancel the interference.

This can be implemented in the DSP chip.

This would not eliminate wanted signal information.

This technique has been used before with good results in the bio-medical field.

#### Anti aliasing filter

**What is the expected signal level above Fs/2?**

Based on this, what filter stop band attenuation will be required for a 16 bit A/D?

**Consider 6 pole Butterworth filter**

Phase characteristics are predictable

**Can reconstruct exact signal as required with computer processing in non real time.**

### USCA signal sampling does not support data correlation.

#### Each USCA has its own free running sample clock.

**Samples from one USCA to another are not correlated due to the non synchronous sampling.**

**A random variable of jitter is being introduced.**

**Sample to sample correlation between different USCA data is not possible with the introduction of this random variable.**

Consider the use of a master clock from the ADAS that the USCAs could use to lock up to.

Line length to the USCA would create a delay of the synchronizing clock, but this would be a constant that could be removed in real or non-real time.

The time tagging of the digital sample to the ADAS does not have an effect on the above problem.

The current system of 420s and 429s can do synchronous sampling.

Are they set up this way?

Transducer health check

Consider circuitry to realistically check the transducer.

'Shunt cal' does not check the transducer.

A transformer can be inserted in series with the sensor return.

This would be shorted out during normal operation.

Inject a pulse to get the impulse response of transducer.

This can be processed in the DSP.

It can be used to form the cross correlation of the DFT with that stored in the tag RAM.

The impulse response could be saved in operation using SAMS control.

It could also be reported to the system via the SAMS controller for a health check of the transducer.

Inject a sinusoid of a given frequency to test the response of the transducer.

USCA excitation resolution

What resolution is actually required?

What is the function of the fine resolution of the excitation?

This does not provide added sensor resolution or calibration.

What is the cost of the circuitry required to support 16 bit resolution?

Input circuitry

Input attenuator

Resistor noise effects at high gain settings if attenuator is first.

Is +/- 28 volt maximum input required?

What is the input impedance of the USCA

What is the effect of the input multiplexers on this and the accuracy?

Will the input over voltage protection still function when the USCA power supplies are not operating?

Common mode specifications

At what gain?

At 150 Hz not to 60 Hz?

Gain step size

Consider binary step gain increments

More efficient for processing computations afterward?

Analog output

Output impedance is not matched to the line and sink.

Noise pickup, reflections, etc?

Output ripple specification is too high.

Output loading could be specified by C+R.

Table should not be needed.

Repeatability specification

What are the conditions?

What statistics are to be used?

Accuracy measurements

Allow accuracy measurements to be a percentage of reading instead of a percentage of full scale.

LORAL
Test and Information Systems

| | | | |
|---|---|---|---|
| To: | NASA | From: | Loral Test and Information Systems |
| | KSC, Fl. | | PO Box 3041 |
| | San Diego,Ca | | Sarasota, Fl. 34230 |
| Attn.: | Mr. Bill Larson | | Mr. D. Payne |
| | | | |
| Phone: | 407-867-3185 | Phone: | 813-377-5575 |
| Fax: | 407-867-4079 | Fax: | 813-378-6905 |
| CC: | All Attendees | CC: | Mr. D. Becker ext 5217 |
| | | | Mr. R. Powell ext 4578 |
| | | | Mr. S. Borowski ext 4944 |
| | | | |

10/27/94

| Attendees: | |
|---|---|
| **LTIS** | **NASA/I-Net** |
| Dean Becker | Bill Larson |
| David Payne | Jeff Ake |
| Joel Weber | Hank Taylor |

1. **Unavailability of the DSP chip used in the USCA.** This chip, Motorola 56001, is not available as Motorola is using all of these chips for their celluar phones. NASA and Loral had addressed acquiring the next chip in the family (56002). Loral got a quote from AVNET saying 100's were available next year, with 1000's the year after. We decided to continue with the Motorola family at this time. To test the availability of the chips, Loral will order 25 units.

   **Dean Becker:** Order 25 DSP chips for our USCA builds.

2. **Upgrade of the 4 I-Net systems to the latest release( 6.1).** Current operational status of the 4 units is shown in Figure 1. The basic plan is to upgrade the LCC and DE Units and start the conversion process. The Wave Lab units will be modified after the next launch. In discussions with Doug Gibbs, Doug will provide an estimate of the costs and schedule to install the 6.1 upgrade to the units.

   **Doug Gibbs:** Provide cost estimates and schedule for installation

3. **General training course.** Bill Larson has offered to supply the updated DE unit for the training course. This would provide additional seats for training for operations (Grumman) people. Doug Gibbs will provide a cost for these additional trainees.

   **Doug Gibbs:** Provide a quote to train 2-4 additional people at the Training Course scheduled for Sarasota Nov. 7.

4. **550 development environment at KSC.** The intent is to allow Steve Romine to apply the software training by starting to perform the MNI' module driver modifications.

   **David Payne:** Check with Vince Unger about bringing this to the Software Training course scheduled Nov. 14.

5. **MNI Cable Lengths.** Next, NASA is willing to test whether the MNI will drive the cable lengths (as shown in Figure 2). To support this, Dean Becker and Jeff Kuhn are trying to get two loaner

boards. This would allow this vital link in using the MNI to be tested. I will check to see if the MNI is still part of the ADAS deliverables in the contract.

**David Payne:** Check deliverables on the ADAS schedule
**Dean Becker:** Co-ordinate getting the necessary equipment for NASA to perform these tests.

6. **SCSI VLDS Tape for a 550.** Jeff Kuhn or Rick Powell had mentioned to Bill Larson about a SCSI VLDS tape drive that we could interface into the 550's. This would allow the data to be written to the RAID discs at full rate (i.e. 8-10 MBytes per second) then use SCSI Disc Copy to transfer data to the tape unit at 4 MBytes per second. There may be a possibility that NASA may only need 4 MBytes per second? This tape could then be pulled out and taken to the Wavelab for reduction. Joel Weber talked to Paul Friedman about this. Paul saw no problem to transfer the data from the RAID to the tape at 4 MByte. Bill wants to see this demoed, and volunteered his DE 550, if we can arrange the tape Player from Metrum . There is a question if the Ciprico unit in the 550's has 1 or 2 SCSI ports. Joel is addressing getting a VLDS unit. If this approach works, NASA plans to:

- upgrade his Raids from 8 to 16 GBytes
- Buy two more 32 GByte drives
- purchase 3 VLDS units.

**Paul Friedman:** Does the Ciprico have two ports and do we need a special driver?
If the Ciprico only has one port, can we get another controller to test this.
Would the data be transferred totally on the SCSI bus, or would the VME bus get involved?

**Joel Weber:** Address getting a SCSI VLDS loaner

7. **USCA Schedule.** There are several items that involved the USCA schedule. The final result is NASA will turn over the final USCA design by Dec. 18th. LTIS will have a 3 month process to finish inputting, build and test the rugged version. If minor problems arise in the testing, Changes will be done by NASA and LTIS will incorporate these changes. If there are major problems (i.e. boards bang together, temperature failures, etc. NASA will do another revision level with a corresponding 3 month slip. The determination of Major and Minor, will be done by the USCA design team.

**Mechanical:** The prototype mechanical package was evaluated by LTIS engineers and several suggestions made. The main suggestion was to look at extruded aluminum as a casing. Bill Larson had checked and this should be a suitable casing for the launch environment. The aluminum will need to be anodized, and NASA will have to look at the tie down methods and locations. Dave M. the co-op, is re-addressing this design with light support from Terry Greenfield. NASA will send the newest version drawings to LTIS next week. This is probably "the long pole in the tent."

NASA will run Temperature and Vibration tests on the current rev. of boards and enclosure. The next rev. will include changing from PGA to Flat Pack chips and also look at moving the digital board away from center.

**Pedro Medelius:** Send Mechanical Drawings of the USCA to LTIS. Address sending Autocad files via Internet to David Payne (Payne@world.lds.loral.com)

**Electrical:** Testing of the electrical circuits should be finished by next week. We discussed transfer of the layout information and how to minimize the current risk and future maintainance costs. To minimize risks now, we are planning to copy the current layout, by manual input, as much as possible. We discussed trying to read in the Gerber plots to minimize errors and to reduce development time. We will run a test case with the current board revision levels.

**Pedro Medelius:** Pedro will give Dean the current boards outputs, to test starting work.

**Dean Becker:** Dean will setup the DSP development environment at LTIS, Sarasota. He will also identify who the responsible person on LTIS side will be.

**Programming:** Current DSP programming is 80% done. This should be largely finished by Nov. 20, with refinements to be done until Feb. 2.

**Test Procedures:** Component test procedures will be done by next week. This is a debug level writeup for the components of the USCA. The System Level test will be finished by Nov. 11. This is board level test and debug.

8. **ADAS Schedule.** We addressed the ADAS Schedule, and current plans are to have the ADAS turned over to LTIS by July, 95. We recoginized that the ADAS had to be concurrent with the PMS Replacement project, and a revised schedule, showing the PMS Replacement and ADAS development schedule is being drawn by Hank Taylor. The ADAS specs will be modified and addressed at the next PMS meeting.

**Hank Taylor:** Provide revised ADAS schedule to all members of the team.

**Dean Becker:** Dean Becker will rewrite the ADAS preliminary specifications based on the 550 implementation.

9. **TOA system (Lightning Detection)** LTIS is trying to setup a meeting with the FAA to discuss the use of the NASA developed TOA system. We are trying to co-ordinate this with the Tech 2004 conference. Steve Borowski has been trying to meet with the appropriate Program office. They had cancelled the Thursday meeting, but have rescheduled for Monday. NASA has to know on Monday if this meeting will happen, to get the travel orders done.

10. **Titan/Centaur :** Joel Weber and I borrowed the USCA demo unit and met with Steve Smith of the Titan/Centaur launch people. He is very interested in the USCA/ADAS units. He is building a new payload facility in the next two years and wants to address designing the USCA/ADAS in up front. He is also going to set up a meeting with the other instrumentation people on the Air Force side. This will happen within a month. We are also going to ask him to refer us to the San Diego plant.

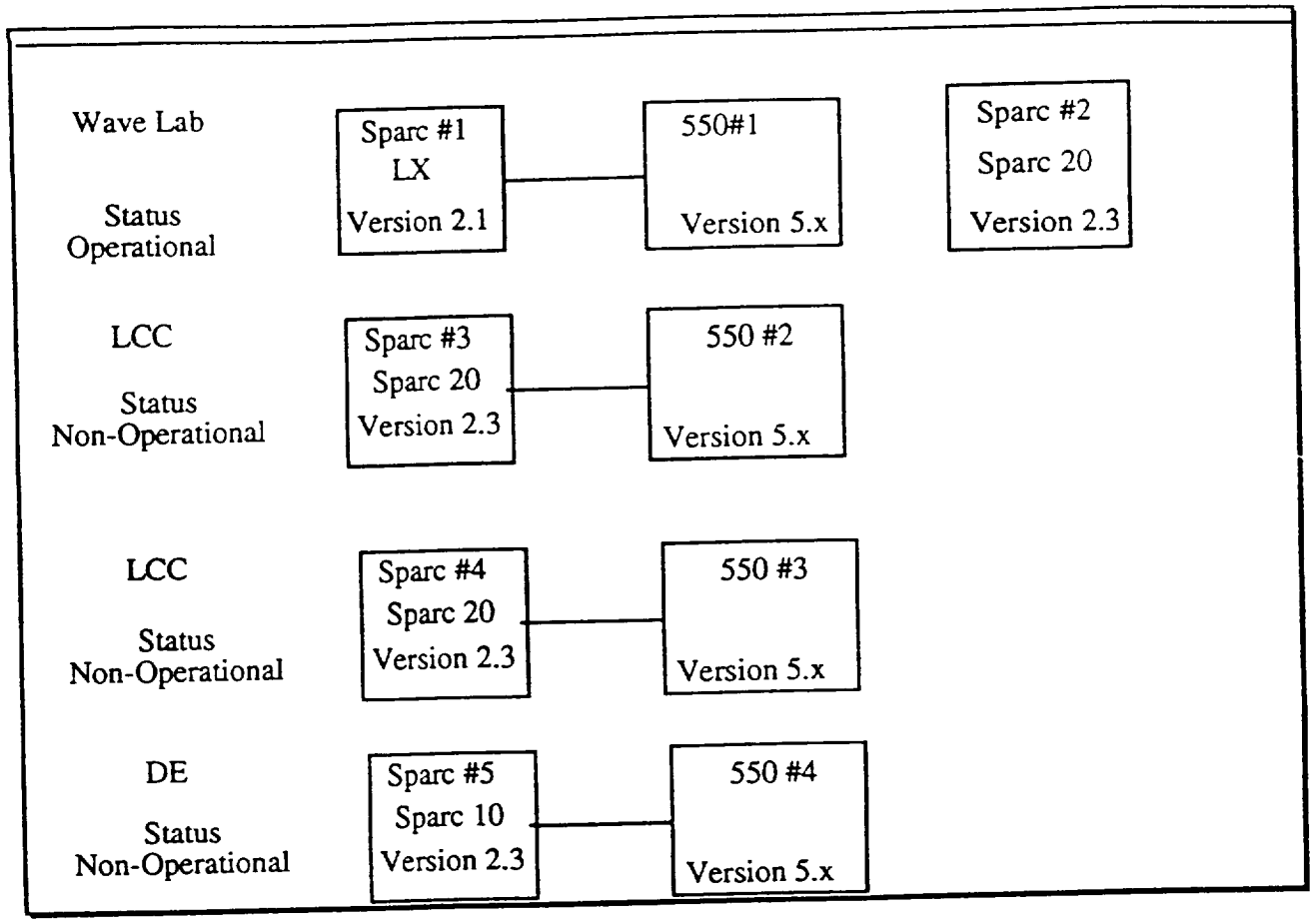



**Figure 1 Current 550 systems**

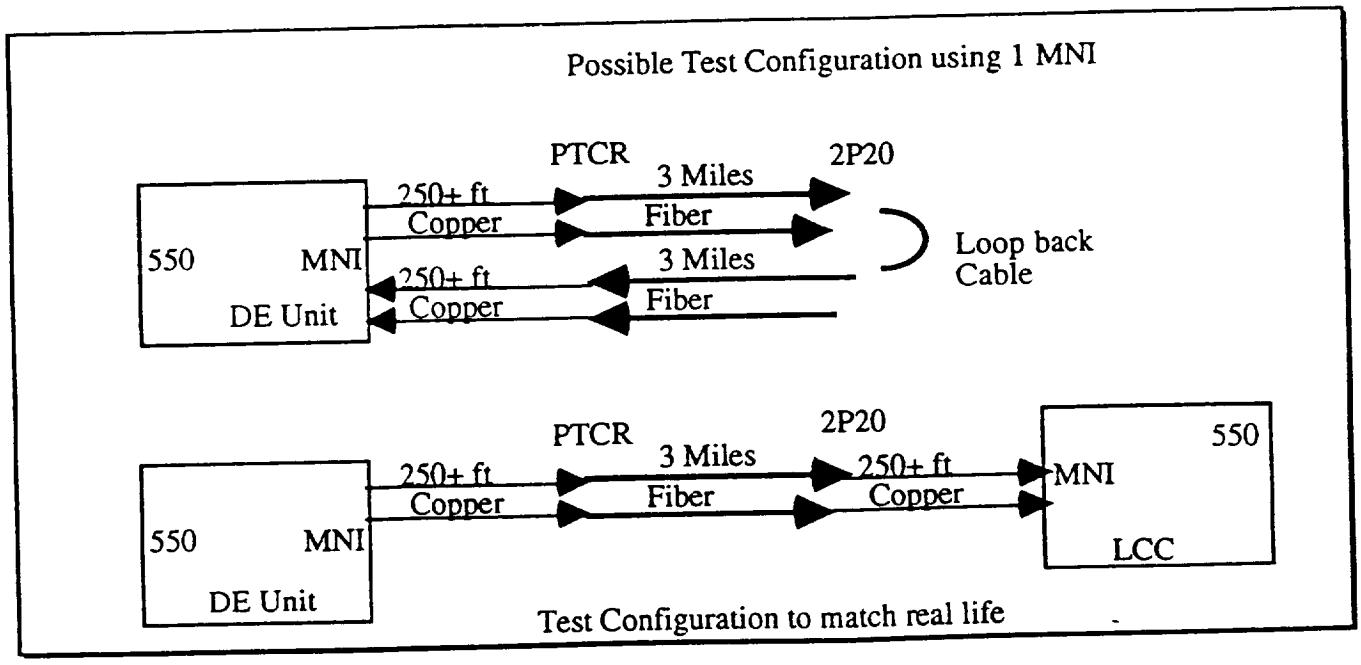



**Figure 2 Test Configuration for MNI Drives**

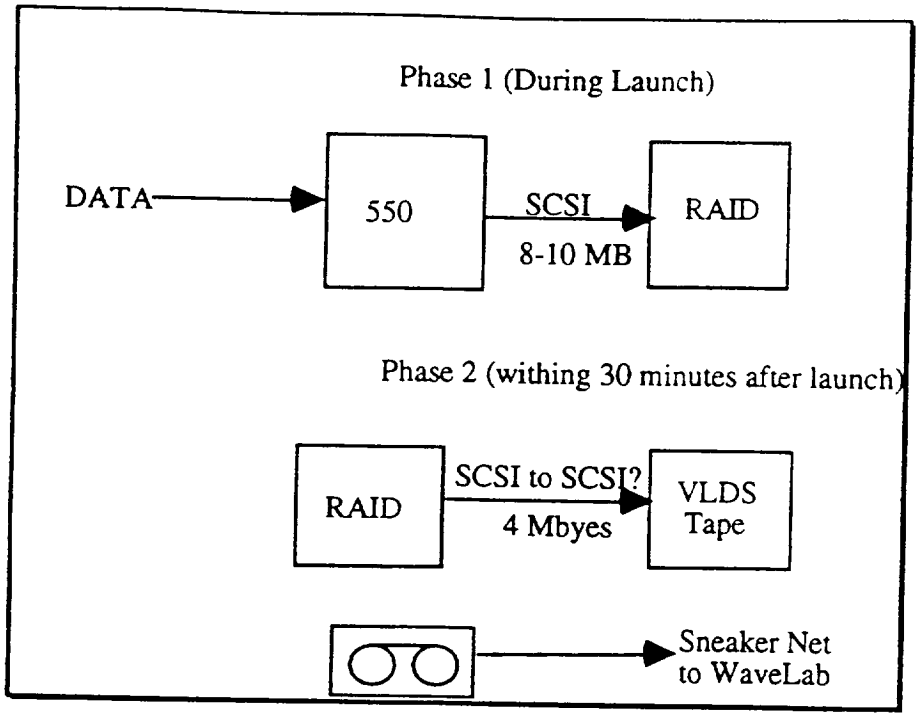



**Figure 3 RAID to VLDS to Wave Lab dataflow**

Best Regards,

Loral Test and Information Systems

David Payne

LORAL
Test & Information Systems

P.O. Box 3041
Sarasota, FL 34230
(941) 371-0811
Fax: (941) 378-1893

July 7, 1995

Brevard Community College
Center of Technology Innovation
250 Grassland Road S.E.
Palm Bay, FL. 32909

Attention: **Mr. Jared Whitcomb**

Subject: **BCC PO #433, TRDA #405; USCA**

Enclosure: **Milestone 3 Invoice**

Reference: **Telcon with J. Whitcomb, BCC & S. Carroll, LTIS of 7/5/95**

Dear Mr. Whitcomb,

Milestone #3 to the subject contract which states: "Complete manufacturing & deliver to TRDA five copies of design Version 3 USCA's. These Version 3 USCA's will be manufactured according to the final approved Version 3 design contained within the Loral CAD System" has been completed. The units were delivered in early June to Mr. Bill Larson at NASA.

Should you have any questions regarding this matter, please do not hesitate to call me at 941/377-5538

Very truly yours,

**LORAL TEST & INFORMATION SYSTEMS**

Stephen G. Carroll
Manager, Contracts Department

SGC/cjm

cc. Matt LaVigne, TRDA

July 12, 1995

TO: Matt
FROM: Tom
SUBJECT: Loral Milestone #3

I have talked to Bill Larson about the LORAL delivery of the five version 3 USCA's. Bill noted that they delivered 12 units, much more than required by contract!!

Bill said the testing is still going on as LORAL had made some mistakes in the delivered units and that had to be corrected first. However, he feels everything is going OK now and testing should be finished soon.

Therefore, I would recommend the Milestone #3 payment be made to LORAL.

Tom Davis

LORAL
Test & Information Systems

P.O. Box 3041
Sarasota, FL 34230
(941) 371-0811
Fax: (941) 378-1893

September 28, 1995

Brevard Community College
Center of Community Innovation
250 Grassland Rd S.E.
Palm Bay, FL 32909

Attention: Mr. Jarad Whitcomb

**Subject: BCC PO #433, TRDA #405; USCA Milestone #4**

Enclosure: (1) Design Package for USCA Version 3

Dear Mr. Whitcomb:

Milestone #4 to the subject contract which states " Release final Version 3 USCA design package. This version will be released as a Loral Standard Component, and will be available as a catalog item" has been completed. NASA testing is complete and the design package is enclosed. Our invoice for this milestone will be submitted under separate cover.

If you have any other questions regarding this matter, please do not hesitate to contact me at 813-377-5538, or by fax at 813-378-6905

Very truly yours,

LORAL TEST & INFORMATION SYSTEMS

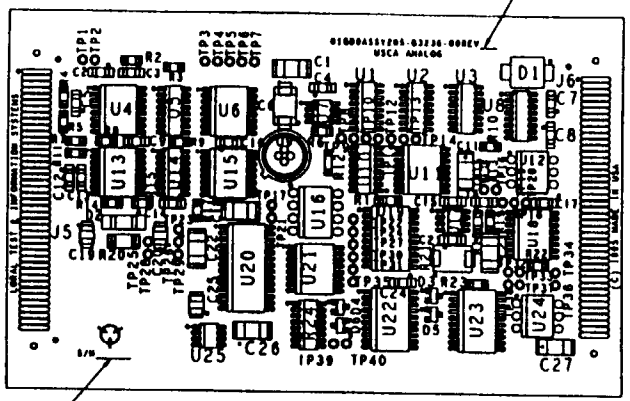
Stephen G. Carroll
Manager, Contracts

cc: Matt LaVigne, TRDA

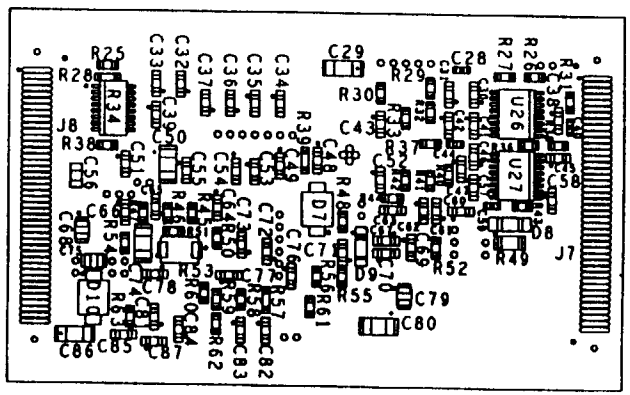
NOTES:
UNLESS OTHERWISE SPECIFIED.

1. MAX. ASSY. HEIGHT: A. TOP SIDE : .530
   B. BOTTOM SIDE: .093
2. DESIGN REF. HEIGHT: N/A
3. ON COMPONENTS OTHER THAN SURFACE MOUNT
   □SQUARE PAD INDICATES PIN 1 (POSITIVE, +) END OF POLARIZED CAPACITORS, PIN 1 (CATHODE) END OF DIODES, AND PIN 1 OF ALL OTHER COMPONENTS WITH MORE THAN 2 LEADS. REFER TO SILKSCREEN IMAGE FOR ANY MECHANICAL ORIENTATION.
4. INFORMATION FOR THIS DRAWING IS CONTAINED IN CADD DATABASE 809-B3236-00.
5. USE CAUTION WHEN HANDLING THIS PWA TO PREVENT DAMAGING BY STATIC ELECTRICITY.
6. APPLY THE CURRENT ASSEMBLY/PARTS LIST REVISION LETTER APPROX. WHERE SHOWN. THE MARKING SHALL BE:
   1.) A FILM LABEL WITH ACRYLIC PRESSURE SENSITIVE ADHESIVE, OR
   2.) INDELIBLE INK PER MIL-I-43553 IN A CONTRASTING COLOR.

   CURRENT ASSY REV LETTER — REV / — CURRENT PL REV LETTER
7. APPLY SERIAL NUMBER (SN XXXXX) APPROX. WHERE SHOWN PER LORAL STD 3.7. THE MARKING SHALL BE:
   1.) A FILM LABEL WITH ACRYLIC PRESSURE SENSITIVE ADHESIVE, OR
   2.) INDELIBLE INK PER MIL-I-43553 IN A CONTRASTING COLOR.




TOP SIDE




BOTTOM SIDE

SEE SEPARATE PARTS LIST

| | | | |
|---|---|---|---|
| 00 | 233-B3282-00 | 4200 | |

L. TOMPKINS
L. TOMPKINS

LORAL Test & Information Systems

PWA
USCA ANALOG

D 01GDO 205-B3236-00

SHEET 1/1

1 205-B3236-00

HOLE CHART

| HOLE | QTY | DESCRIPTION | |
|---|---|---|---|
| ▪ | 552 | Ø .013 +/- .003 | PLATED THRU |
| ● | 40 | Ø .032 +/- .003 | PLATED THRU |
| ▪ | 4 | Ø .035 +/- .003 | PLATED THRU |
| ⊕ | 4 | Ø .100 +/- .003 | NON-PLATED THRU |

REVISIONS

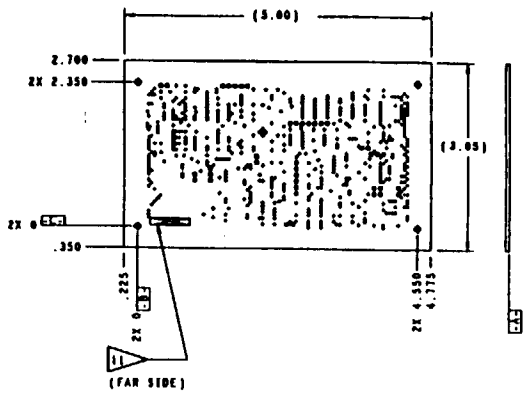
| LTR | DESCRIPTION | EFFECTIVITY | DATE | APPROVED |
|---|---|---|---|---|
| - | - | - | - | - |

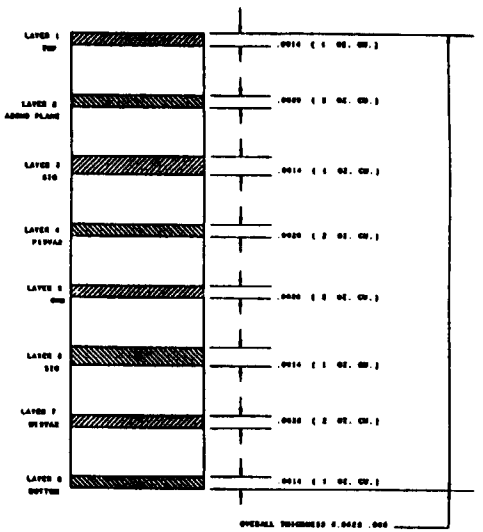
NOTES:
UNLESS OTHERWISE SPECIFIED:

1. THIS PWB SHALL MEET/EXCEED ALL APPLICABLE IPC STANDARDS.
2. ARTWORK 905-83236-02 AT REV -
(CADD DB 800-83236-00) CONSISTS OF:
8 SHEETS CIRCUITRY AT REV -.
ONE SHEET SOLDER MASK (TOP SIDE) AT REV -.
ONE SHEET SOLDER MASK (BOTTOM SIDE) AT REV -.
ONE SHEET SILKSCREEN (TOP SIDE) AT REV -.
ONE SHEET SILKSCREEN (BOTTOM SIDE) AT REV -.
ONE SHEET PASTE MASK (TOP SIDE) AT REV -.
ONE SHEET PASTE MASK (BOTTOM SIDE) AT REV -.
AND ONE DRILL FILE AT REV -.
3. MATERIAL-PLASTIC SHEET — MIL-P-13949/4, TYPE:

| | |
|---|---|
| BASE MATERIAL | GFN |
| BASE THICKNESS | SEE MULTILAYER DETAIL |
| TYPE OF COPPER FOIL | C |
| WEIGHT OF COPPER FOIL | SEE MULTILAYER DETAIL |
| GRADE OF PITS AND DENTS | A |
| CLASS OF THICKNESS TOL | 2 |
| CLASS OF BOW AND TWIST | C (APPLICABLE TO BASE THICKNESS > .020 ONLY). |
| MATERIAL-PREPREG | MIL-P-13949/12, TYPE: |
| PREPREG MATERIAL | PC-GF |
| RESIN MATERIAL | |
| GLASS STYLE | MANUFACTURER'S OPTION |
| NOM RES FLOW | MANUFACTURER'S OPTION |
| NOM GEL TIME | MANUFACTURER'S OPTION |
| NOM RESIN CONTENT | MANUFACTURER'S OPTION |

4. OXIDE TREAT CORE PATTERN
5. THIS PWB REQUIRES ETCHBACK IN ACCORDANCE WITH PARAGRAPH 3.8 5.3 OF MIL-P-55110.
MINIMUM ACCEPTABLE ETCHBACK IS .0001
MAXIMUM ACCEPTABLE ETCHBACK IS .0010
6. VIA HOLES MUST NOT BE PARTIALLY PLATED CLOSED
7. ELECTROPLATE .001 IN. COPPER MINIMUM.
8. APPLY LIQUID PHOTO IMAGEABLE SOLDER MASK WITH GLOSS GREEN FINISH OVER BARE COPPER PER IPC-SM-840 CLASS 3. LEAVE COMPONENT PADS CLEAR OF SOLDER MASK MAINTAINING .005 MAX/.001 MIN CLEARANCE.
9. APPLY TIN/LEAD COATING (63/37) PER MIL-P-55110. COATING MUST BE MELTED ALLOY.
10. LETTER TOP AND BOTTOM SIDES OF PWB USING MASTER PATTERN ARTWORK AND INK PER MIL-I-43553, COLOR YELLOW NO. 13655 PER FED-STD-595.
11. APPLY THE CURRENT PWB DRAWING REVISION LETTER APPROX. WHERE SHOWN. THE MARKING SHALL BE ONE OF THE FOLLOWING:
1.) ETCHED IN ARTWORK
2.) A FILM LABEL WITH ACRYLIC PRESSURE SENSITIVE ADHESIVE
3.) INDELIBLE INK PER MIL-I-43553 IN A CONTRASTING COLOR
206-83236-00REV_ ← CURRENT PWB DRAWING REV LETTER
12. HOLE LOCATIONS AND SIZES ARE PER DRILL FILE. LOCATIONAL DIMENSIONS ARE BASIC AND TOLERANCE IS: ⌖ Ø.020 Ⓜ A B C / Ø.007 Ⓜ A
13. SERIALIZED QUALITY ASSURANCE TEST COUPONS PER MIL-STD-275 SHALL BE SUPPLIED (ONE SET PER PANEL) WITH EACH SET OF PWBS FABRICATED. EXAMPLES OF THE SMALLEST HOLE AND PAD SIZE SHALL BE INCLUDED.




MULTILAYER DETAIL (NOT TO SCALE)

VENDOR ITEM DRAWING

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| -00 | 203-83236-00 | USCA | | | | | | | | | |
| | | | 3 | 4 | 7 | 8 | 9 | 10 | | | |

L. TOMPKINS
L. TOMPKINS

LORAL Data & Information Systems (M)

PWB
USCA ANALOG

| SIZE | CAGE CODE | DRAWING NO. | REV |
|---|---|---|---|
| D | 01GDO | 206-83236-00 | |

SHEET 1/1

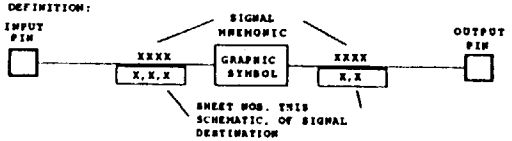
206-83236-001

| COMPONENT CHART | |
|---|---|
| LAST NO USED | UNUSED NUMBER |
| C87 | |
| D10 | |
| J8 | J1 - J4 |
| R42 | |
| TP40 | |
| U27 | |

| REVISIONS | | | | |
|---|---|---|---|---|
| SYM. | DESCRIPTION | EFFECTIVITY | DATE | APPROVED |
| - | - | - | - | - |

5. INFORMATION FOR THIS DRAWING IS CONTAINED IN CADD DATABASE 899-B3236-00.

4. ADDRESS DEFINITION:




3. CIRCUIT RETURN SYMBOLS:


2. FOR TOLERANCES AND RATINGS SEE PARTS LIST.

1. RESISTOR VALUES ARE IN OHMS, CAPACITOR VALUES ARE IN MICROFARADS.

UNLESS OTHERWISE SPECIFIED:
NOTES:

DRAWING
TITLE=905B323601
ABBREV=905B323601
LAST_MODIFIED=Thu Mar 30 07:38:14 1995

| | | | | | |
|---|---|---|---|---|---|
| | -01 | 205-B3236-00 | USCA | DRAWN BY L.TOMPKINS | DATE 3/5/95 |
| | CONFIG. | USED ASSY. NO. | USED ON | DESIGNED B.OSTRYE | 3/06/95 |
| CLASSIFIED TO | APPLICATION | | | CHECKED B.Bouchotte | 3-30-95 |
| | | | | DESIGN ENGINEER - | - |
| | | | | PROJECT ENGINEER D.R.Bouchotte | 3-30-95 |
| | | | | APPROVED - | APPROVED - |
| | | | | APPROVED - | QA (illegible) |



LORAL
VOUGHT & INFORMATION SYSTEMS
P.O. Box 3461
Sarasota, FL 34230

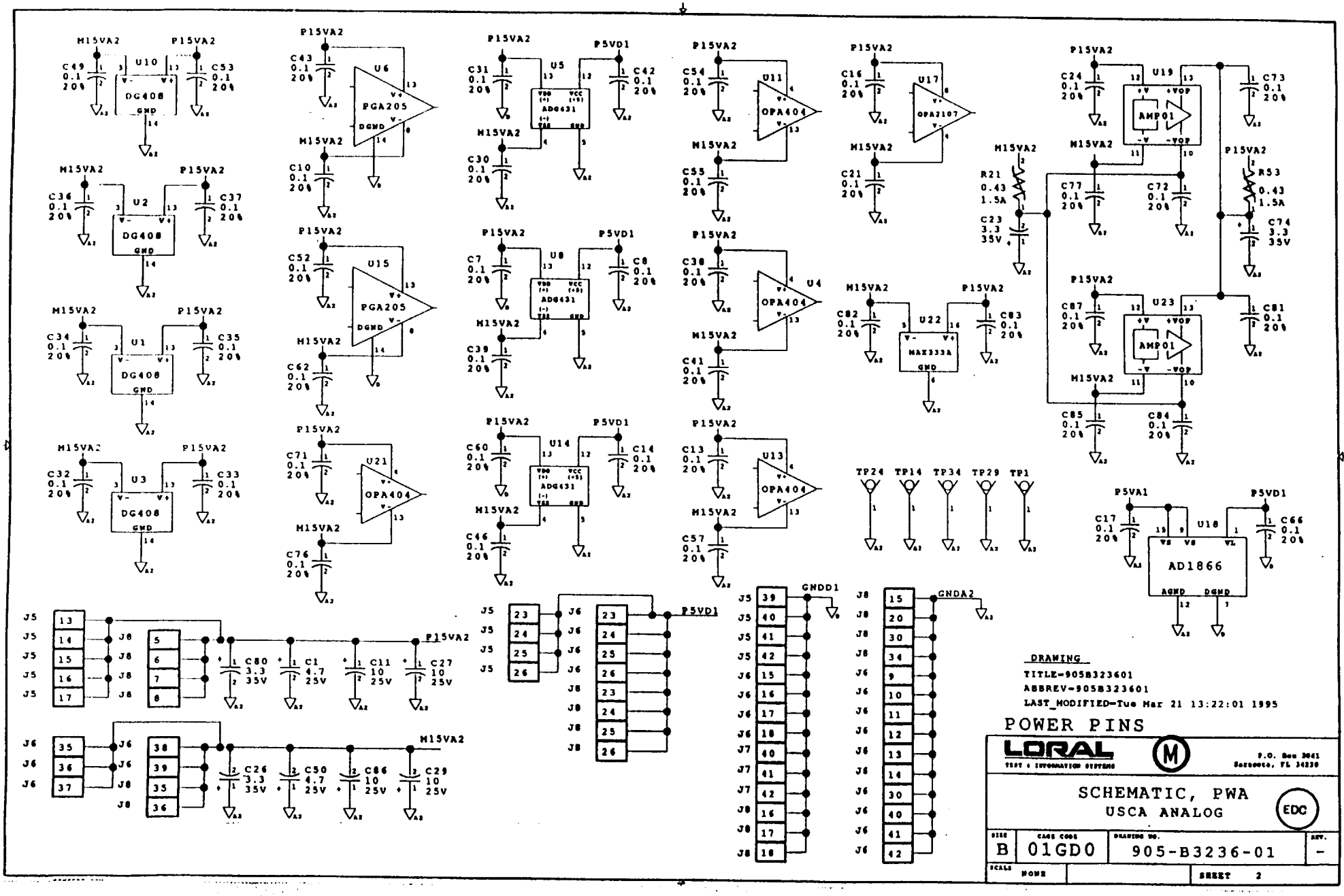
# SCHEMATIC, PWA
## USCA ANALOG

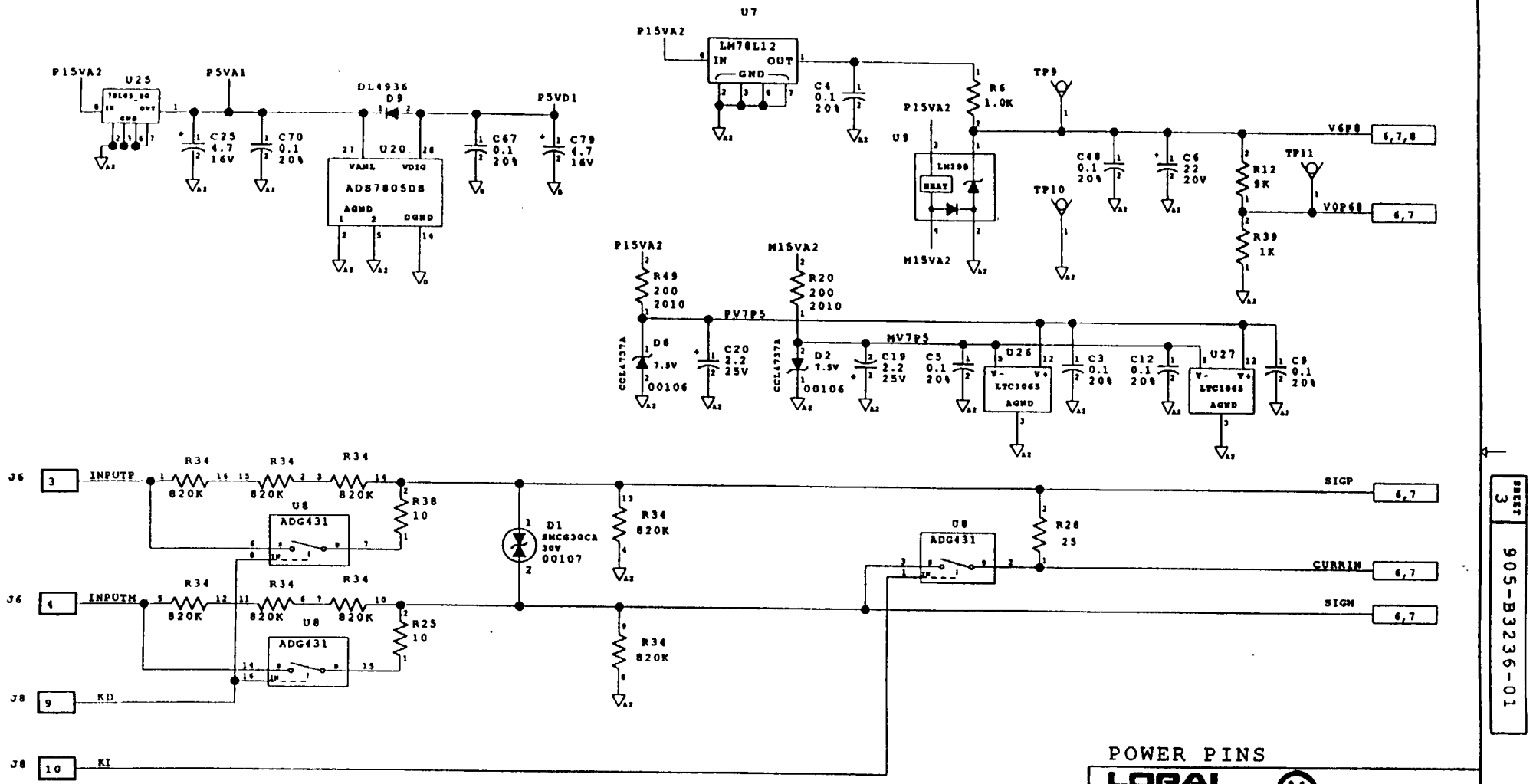
EDC

| SIZE | CAGE CODE | DRAWING NO. | REV. |
|---|---|---|---|
| B | 01GD0 | 905-B3236-01 | - |

SCALE NONE — SHEET 1 OF 8

SHEET 1 — 905-B3236-01


M15VA2
P15VA2
P5VD1
P5VA1
U10
U2
U1
U3
DG408
GND
U6
U15
U21
PGA205
DGND
OPA404
U5
U8
U14
ADG631
U11
U4
U13
OPA2107
U17
U22
MAX333A
U19
U23
AMP01
+VOP
-VOP
R21
0.43
1.5A
R53
C23
3.3
35V
C74
U18
AD1866
AGND
DGND
TP24
TP14
TP34
TP29
TP1
J5
J6
J8
P15VA2
P5VD1
M15VA2
GNDD1
GNDA2
C80
3.3
35V
C1
4.7
25V
C11
10
25V
C27
C26
C50
C86
C29
DRAWING
TITLE=905B323601
ABBREV=905B323601
LAST_MODIFIED=Tue Mar 21 13:22:01 1995
POWER PINS
LORAL
SCHEMATIC, PWA
USCA ANALOG
EDC
SIZE
B
CAGE CODE
01GD0
DRAWING NO.
905-B3236-01
REV.
-
SCALE
NONE
SHEET 2
SHEET
2
905-B3236-01




POWER PINS

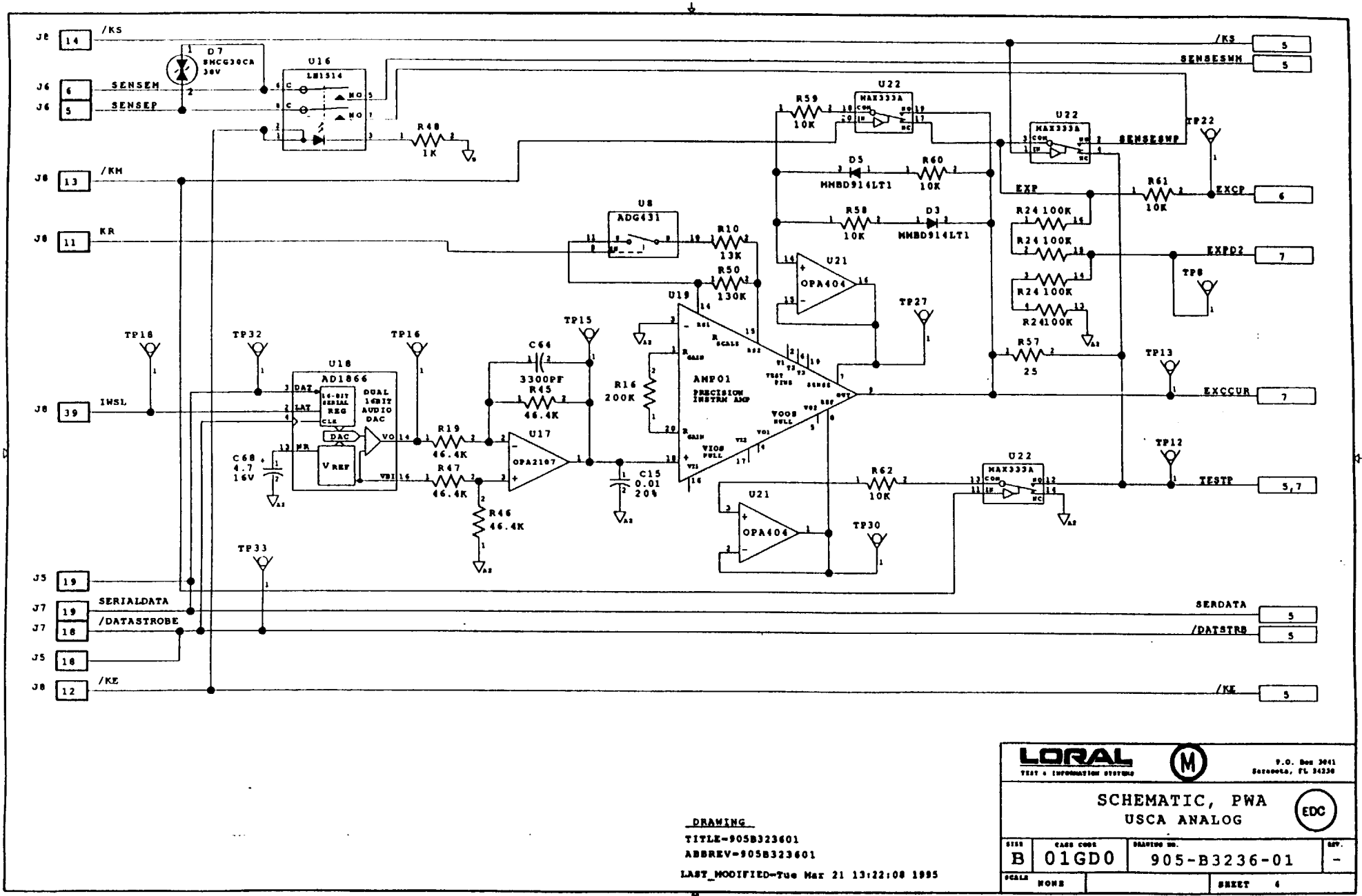
DRAWING
TITLE=905B323601
ABBREV=905B323601
LAST_MODIFIED=Tue Mar 21 13:22:05 1995

LORAL
TEST & INFORMATION SYSTEMS
P.O. Box 3041
Sarasota, FL 34230

SCHEMATIC, PWA
USCA ANALOG
EDC

| SIZE | CAGE CODE | DRAWING NO. | REV. |
|---|---|---|---|
| B | 01GD0 | 905-B3236-01 | - |
| SCALE NONE | | SHEET 3 | |

SHEET 3
905-B3236-01



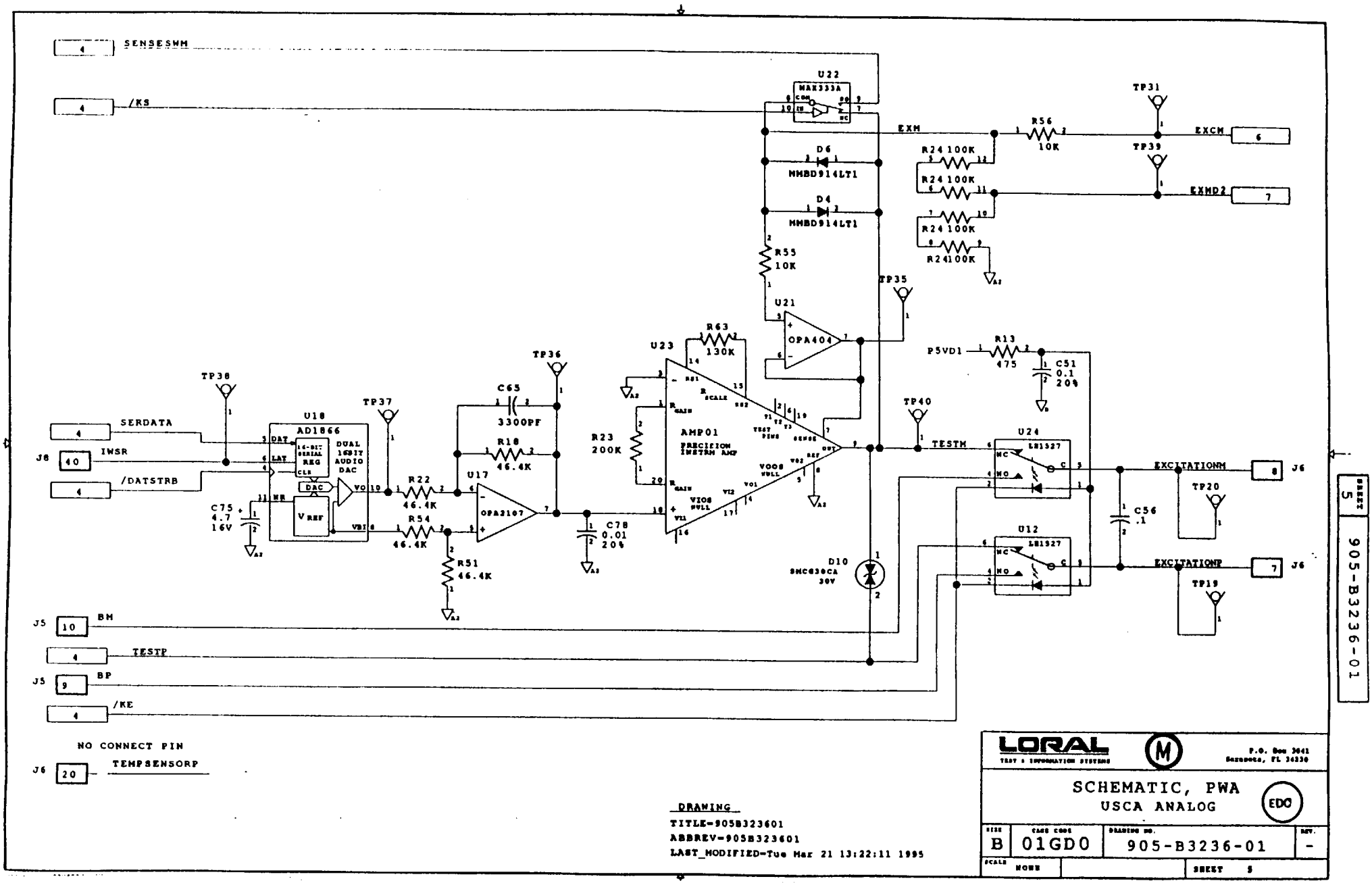

DRAWING
TITLE=905B323601
ABBREV=905B323601
LAST_MODIFIED=Tue Mar 21 13:22:08 1995

LORAL
TEST & INFORMATION SYSTEMS
P.O. Box 3041
Sarasota, FL 34230

SCHEMATIC, PWA
USCA ANALOG
EDC

| SIZE | CAGE CODE | DRAWING NO. | REV. |
|---|---|---|---|
| B | 01GD0 | 905-B3236-01 | - |
| SCALE NONE | | SHEET 4 | |

SHEET 4
905-B3236-01



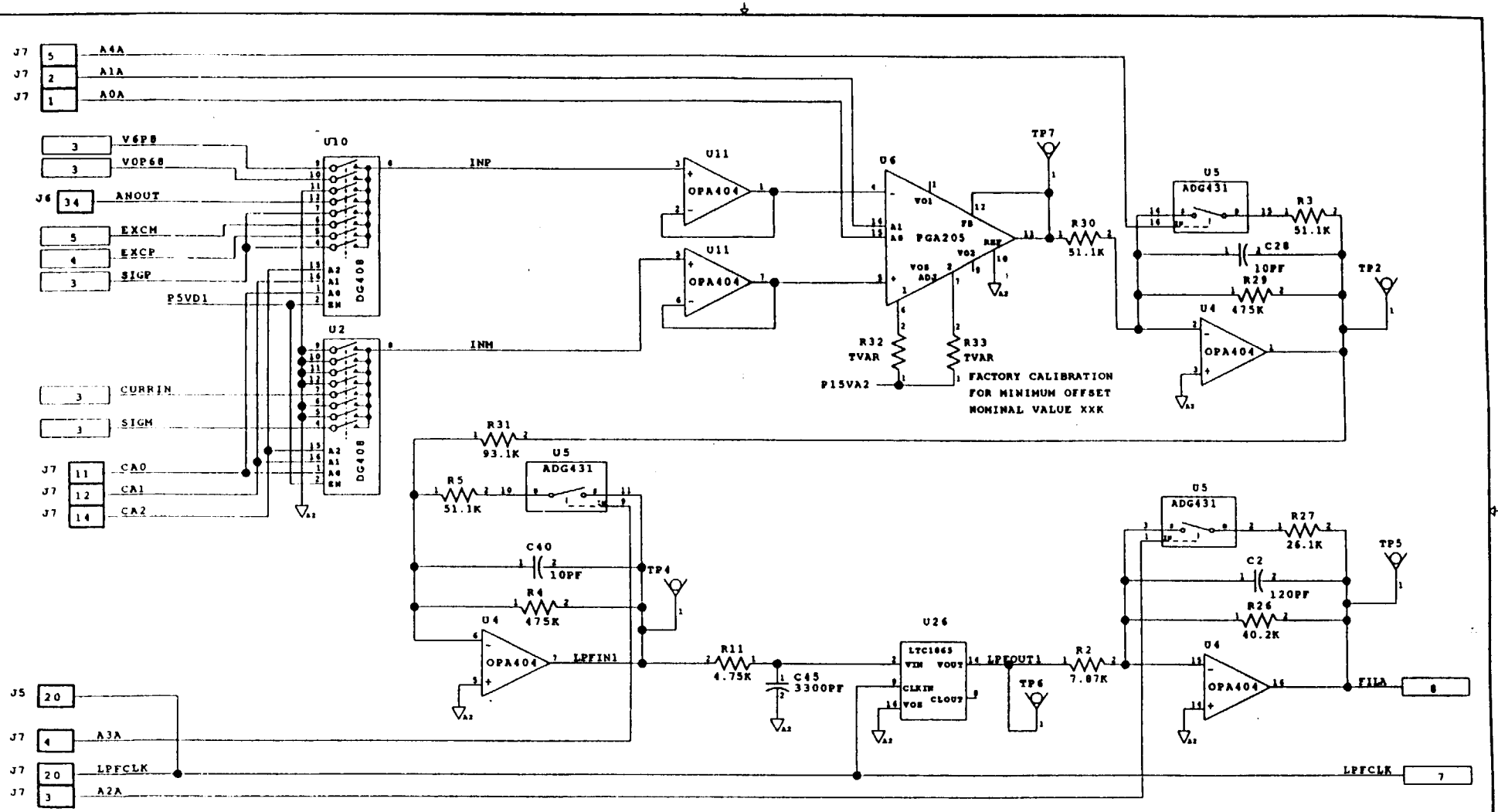

DRAWING
TITLE=905B323601
ABBREV=905B323601
LAST_MODIFIED=Tue Mar 21 13:22:11 1995

LORAL
TEST & INFORMATION SYSTEMS
P.O. Box 3041
Sarasota, FL 34230

SCHEMATIC, PWA
USCA ANALOG
EDO

| SIZE | CAGE CODE | DRAWING NO. | REV. |
|---|---|---|---|
| B | 01GD0 | 905-B3236-01 | - |
| SCALE NONE | | SHEET 5 | |

SHEET 5
905-B3236-01




SHEET 6

905-B3236-01

LORAL
TEST & INFORMATION SYSTEMS

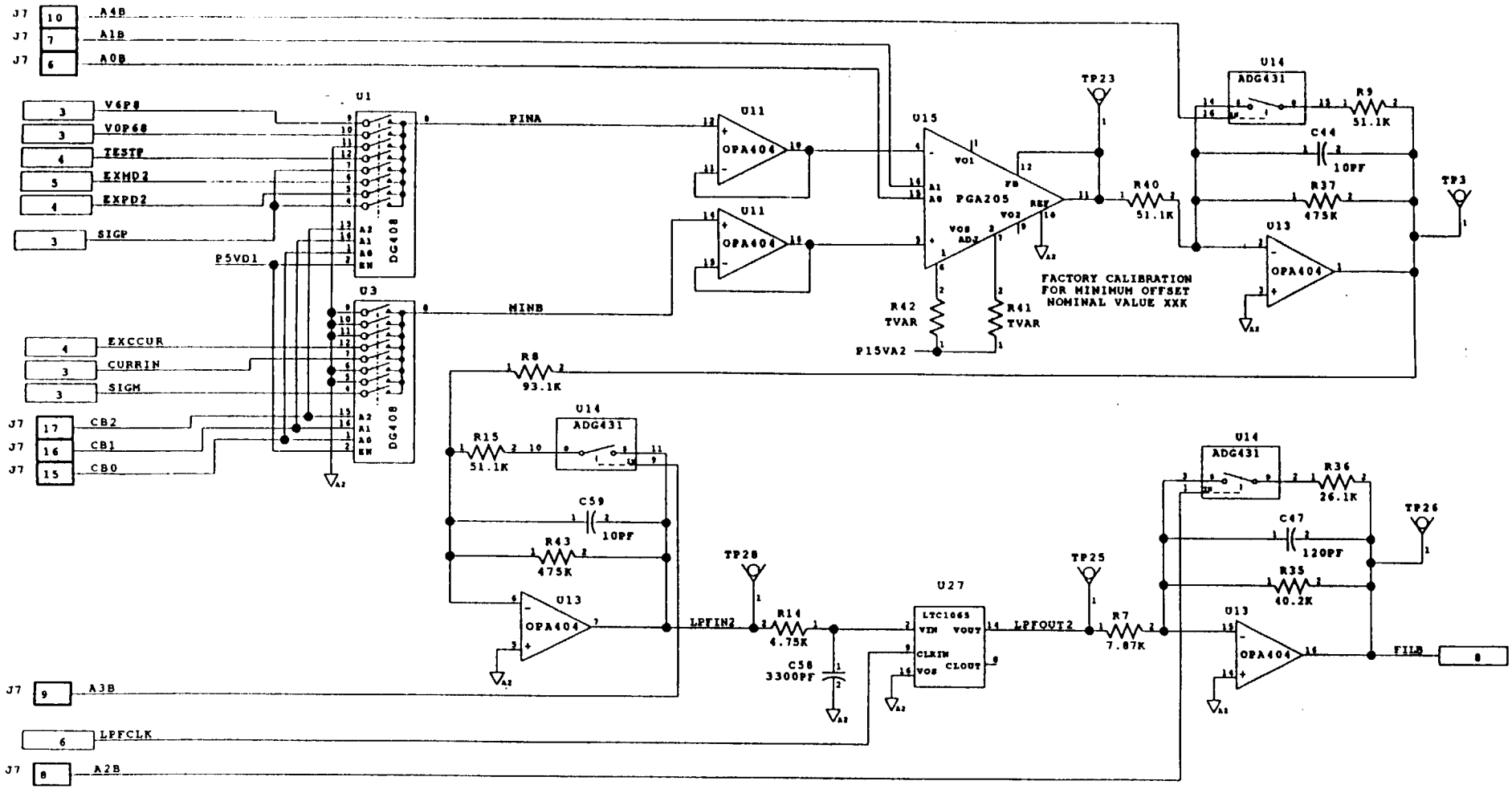
P.O. Box 3041
Sarasota, FL 34230

SCHEMATIC, PWA
USCA ANALOG

EDC

| SIZE | CAGE CODE | DRAWING NO. | REV. |
|---|---|---|---|
| B | 01GD0 | 905-B3236-01 | - |
| SCALE NONE | | SHEET 6 | |

DRAWING
TITLE=905B323601
ABBREV=905B323601
LAST_MODIFIED=Tue Mar 21 13:22:13 1995



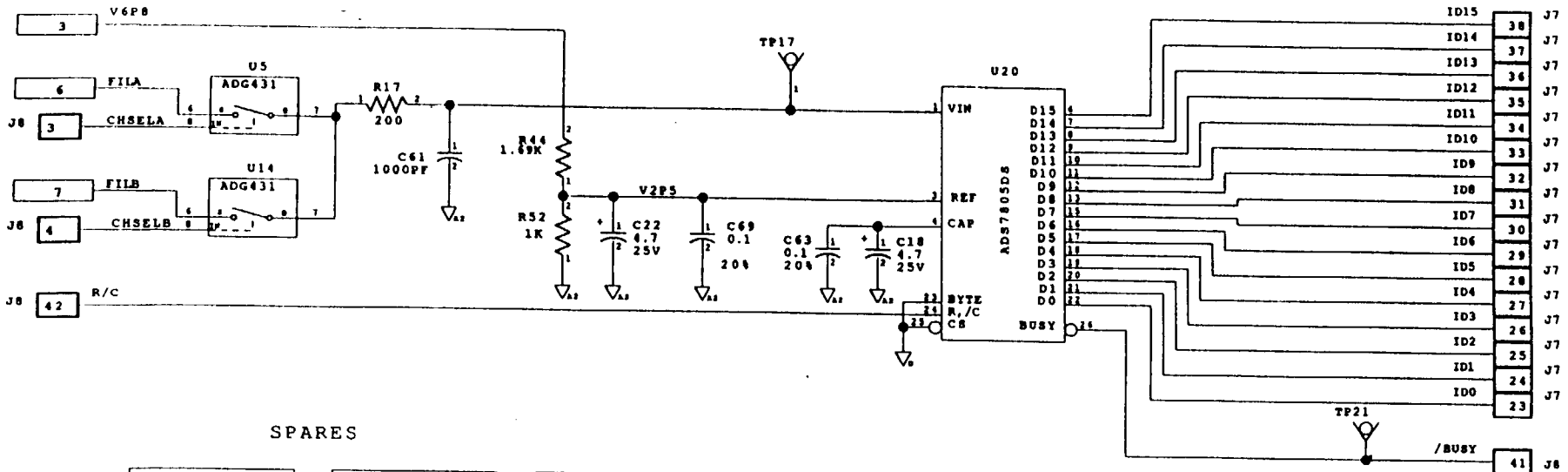

DRAWING
TITLE-905B323601
ABBREV-905B323601
LAST_MODIFIED=Tue Mar 21 13:22:16 1995

LORAL
TEST & INFORMATION SYSTEMS
P.O. Box 3041
Sarasota, FL 34230

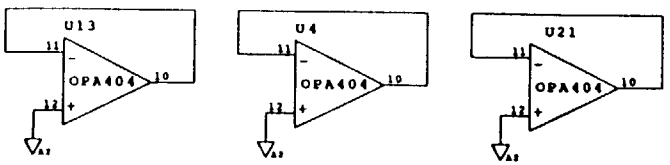
SCHEMATIC, PWA
USCA ANALOG
EDC

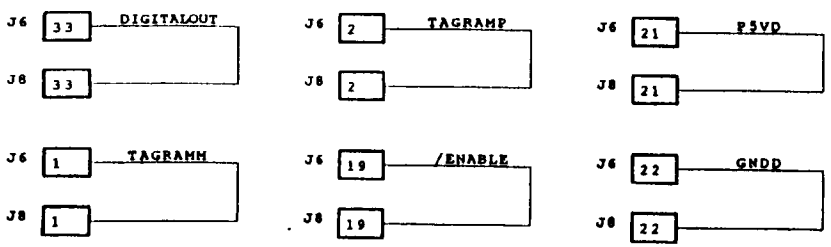
| SIZE | CAGE CODE | DRAWING NO. | REV. |
|---|---|---|---|
| B | 01GD0 | 905-B3236-01 | - |
| SCALE NONE | | SHEET 7 | |

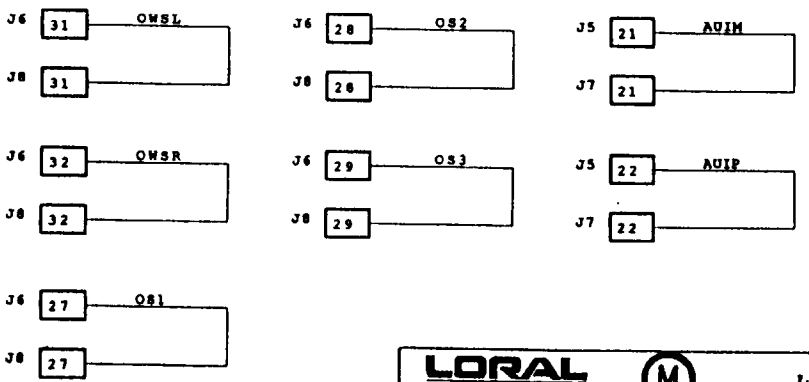
SHEET 7
905-B3236-01




SPARES




DRAWING
TITLE=905B323601
ABBREV=905B323601
LAST_MODIFIED=Tue Mar 21 13:22:20 1995

LORAL
TEST & INFORMATION SYSTEMS
P.O. Box 3041
Sarasota, FL 34230

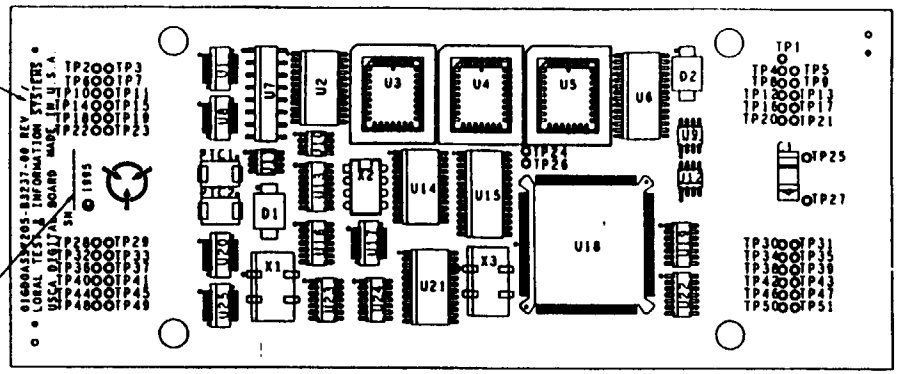
SCHEMATIC, PWA
USCA ANALOG
EDC

| SIZE | CAGE CODE | DRAWING NO. | REV. |
|---|---|---|---|
| B | 01GD0 | 905-B3236-01 | - |

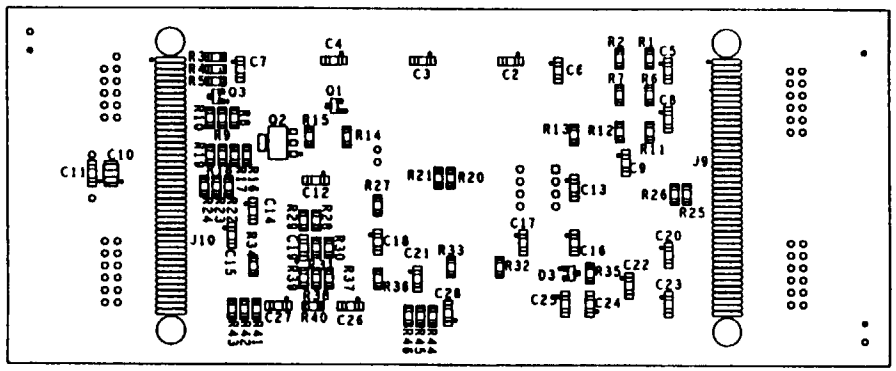
SCALE NONE SHEET 8

SHEET 8
905-B3236-01

| REVISIONS | | | | |
|---|---|---|---|---|
| LTR | DESCRIPTION | APPROVED | DATE | APPROVED |
| . | . | . | . | . |




TOP SIDE




BOTTOM SIDE

NOTES:

UNLESS OTHERWISE SPECIFIED:

1. MAX. ASSY HEIGHT: A TOP SIDE: .200
   B BOTTOM SIDE: .160
2. DESIGN REF. HEIGHT: N/A
3. ON COMPONENTS OTHER THAN SURFACE MOUNT □SQUARE PAD INDICATES PIN 1 (POSITIVE, +) END OF POLARIZED CAPACITORS, PIN 1 (CATHODE) END OF DIODES, AND PIN 1 OF ALL OTHER COMPONENTS WITH MORE THAN 2 LEADS. REFER TO SILKSCREEN IMAGE FOR ANY MECHANICAL ORIENTATION.
4. INFORMATION FOR THIS DRAWING IS CONTAINED IN CADD DATABASE 800-B3190-00.
5. USE CAUTION WHEN HANDLING THIS PWA TO PREVENT DAMAGING BY STATIC ELECTRICITY.
6. APPLY THE CURRENT ASSEMBLY/PARTS LIST REVISION LETTER APPROX. WHERE SHOWN. THE MARKING SHALL BE:
   1.) A FILM LABEL WITH ACRYLIC PRESSURE SENSITIVE ADHESIVE, OR
   2.) INDELIBLE INK PER MIL-I-43553 IN A CONTRASTING COLOR.

   REV
   CURRENT ASSY REV LETTER / CURRENT PL REV LETTER
7. APPLY SERIAL NUMBER (SN XXXXX) APPROX. WHERE SHOWN PER LORAL STD 3.7. THE MARKING SHALL BE:
   1.) A FILM LABEL WITH ACRYLIC PRESSURE SENSITIVE ADHESIVE, OR
   2.) INDELIBLE INK PER MIL-I-43553 IN A CONTRASTING COLOR.

SEE SEPARATE PARTS LIST

| | | |
|---|---|---|
| 00 | 205-B3237-00 | 4Z00 |

N. BUNFORD
N. BUNFORD

LORAL Test & Information Systems

PWA
USCA DIGITAL BOARD

| SIZE | CAGE CODE | DRAWING NO. | REV |
|---|---|---|---|
| D | 01GD0 | 205-B3237-00 | . |

SHEET 1/1

205-B3237-00

| HOLE CHART | | | |
|---|---|---|---|
| HOLE | QTY | DESCRIPTION | |
| ▪ | 734 | Ø .013 +/- .003 | PLATED THRU |
| ▪ | 51 | Ø .032 +/- .003 | PLATED THRU |
| ▪ | 8 | Ø .035 +/- .003 | PLATED THRU |
| ◉ | 2 | Ø .125 +/- .003 | NON-PLATED THRU |
| ◉ | 4 | Ø .188 +/- .003 | NON-PLATED THRU |

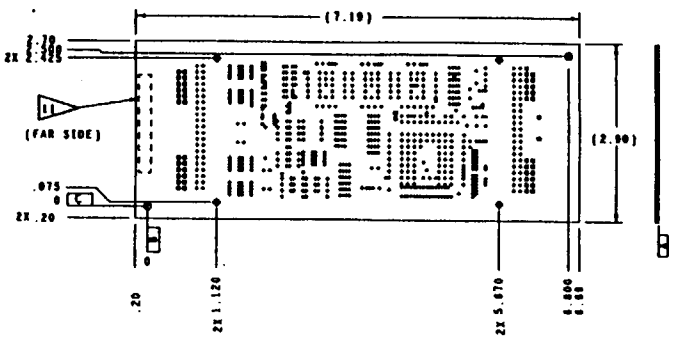
| REVISIONS | | | | |
|---|---|---|---|---|
| ZONE | DESCRIPTION | APPROVED | DATE | APPROVED |
| - | - | - | - | - |

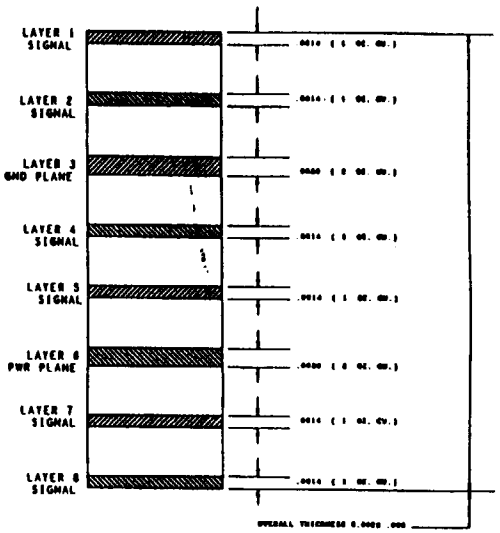
NOTES:
UNLESS OTHERWISE SPECIFIED:

1. THIS PWB SHALL MEET/EXCEED ALL APPLICABLE IPC STANDARDS.
2. ARTWORK 985-B3237-02 AT REV -
(CADD DB 800-B3237-00) CONSISTS OF:
8 SHEETS CIRCUITRY AT REV -,
ONE SHEET SOLDER MASK (TOP SIDE) AT REV -,
ONE SHEET SOLDER MASK (BOTTOM SIDE) AT REV -,
ONE SHEET SILKSCREEN (TOP SIDE) AT REV -,
ONE SHEET SILKSCREEN (BOTTOM SIDE) AT REV -,
ONE SHEET PASTE MASK (TOP SIDE) AT REV -,
ONE SHEET PASTE MASK (BOTTOM SIDE) AT REV -,
AND ONE DRILL FILE AT REV -.
3. MATERIAL-PLASTIC SHEET — MIL-P-13949/4, TYPE:

| | |
|---|---|
| BASE MATERIAL | GFN |
| BASE THICKNESS | SEE MULTILAYER DETAIL |
| TYPE OF COPPER FOIL | C |
| WEIGHT OF COPPER FOIL | SEE MULTILAYER DETAIL |
| GRADE OF PITS AND DENTS | A |
| CLASS OF THICKNESS TOL | 2 |
| CLASS OF BOW AND TWIST | C (APPLICABLE TO BASE THICKNESS > .020 ONLY) |
| MATERIAL-PREPREG | MIL-P-13949/12, TYPE: |
| PREPREG MATERIAL | PC-GF |
| RESIN MATERIAL | |
| GLASS STYLE | MANUFACTURER'S OPTION |
| NOM RES FLOW | MANUFACTURER'S OPTION |
| NOM GEL TIME | MANUFACTURER'S OPTION |
| NOM RESIN CONTENT | MANUFACTURER'S OPTION |

4. OXIDE TREAT CORE PATTERN.
5. THIS PWB REQUIRES ETCHBACK IN ACCORDANCE WITH PARAGRAPH 3.8.5.3 OF MIL-P-55110.
MINIMUM ACCEPTABLE ETCHBACK IS .0001
MAXIMUM ACCEPTABLE ETCHBACK IS .0010
6. VIA HOLES MUST NOT BE PARTIALLY PLATED CLOSED
7. ELECTROPLATE .001 IN. COPPER MINIMUM.
8. APPLY LIQUID PHOTO IMAGEABLE SOLDER MASK WITH GLOSS GREEN FINISH OVER BARE COPPER PER IPC-SM-840 CLASS 3. LEAVE COMPONENT PADS CLEAR OF SOLDER MASK MAINTAINING .005 MAX/.001 MIN CLEARANCE.
9. APPLY TIN/LEAD COATING (63/37) PER MIL-P-55110. COATING MUST BE MELTED ALLOY.
10. LETTER TOP AND BOTTOM SIDES OF PWB USING MASTER PATTERN ARTWORK AND INK PER MIL-I-43553, COLOR YELLOW NO. 13655 PER FED-STD-595.
11. APPLY THE CURRENT PWB DRAWING REVISION LETTER APPROX. WHERE SHOWN. THE MARKING SHALL BE ONE OF THE FOLLOWING:
1.) ETCHED IN ARTWORK
2.) A FILM LABEL WITH ACRYLIC PRESSURE SENSITIVE ADHESIVE
3.) INDELIBLE INK PER MIL-I-43553 IN A CONTRASTING COLOR
206-B3237-00REV
└ CURRENT PWB DRAWING REV LETTER
12. HOLE LOCATIONS AND SIZES ARE PER DRILL FILE. LOCATIONAL DIMENSIONS ARE BASIC AND TOLERANCE IS: ⌖ Ø0.020 Ⓜ A B C / Ø0.007 Ⓜ A
13. SERIALIZED QUALITY ASSURANCE TEST COUPONS PER MIL-STD-275 SHALL BE SUPPLIED (ONE SET PER PANEL) WITH EACH SET OF PWBS FABRICATED. EXAMPLES OF THE SMALLEST HOLE AND PAD SIZE SHALL BE INCLUDED.



MULTILAYER DETAIL (NOT TO SCALE)

VENDOR ITEM DRAWING

| | | | | | |
|---|---|---|---|---|---|
| -00 | 206-B3237-00 | USCA | | | |

| | | | | | | |
|---|---|---|---|---|---|---|
| 4 | 7 | 8 | 9 | 10 | | |

| | | | |
|---|---|---|---|
| DRAWN BY | H. DUNFORD | DATE | APPROVED |
| ENGINEER | H. DUNFORD | | |
| CAD DESIGNER | | | |
| PROJECT ENGINEER | | | |
| MANUFACTURING ENGINEER | | | |

LORAL Test & Information Systems (M) P.O. Box 2000 Binghamton, N.Y. 13902

PWB
USCA DIGITAL

| SIZE | CAGE CODE | DRAWING NO. | REV |
|---|---|---|---|
| D | 01GD0 | 206-B3237-00 | |
| SCALE 1/1 | | SHEET 1 OF 1 | |

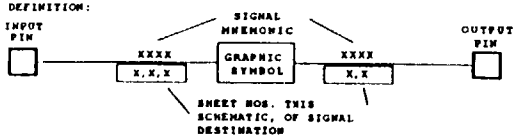
206-B3237-00

| COMPONENT CHART | |
|---|---|
| LAST PC USED | UNUSED NUMBER |
| C | |
| CR | |
| E | |
| J | |
| L | |
| F | |
| Q | |
| R | |
| S | |
| T | |
| TP | |
| U | |

| REVISIONS | | | | |
|---|---|---|---|---|
| SYM. | DESCRIPTION | EFFECTIVITY | DATE | APPROVED |
| - | - | - | - | - |

5. INFORMATION FOR THIS DRAWING IS CONTAINED IN CADD DATABASE 899-XXXXX-00.

4. ADDRESS DEFINITION:




3. CIRCUIT RETURN SYMBOLS:


2. FOR TOLERANCES AND RATINGS SEE PARTS LIST.

1. RESISTOR VALUES ARE IN OHMS, CAPACITOR VALUES ARE IN MICROFARADS.

UNLESS OTHERWISE SPECIFIED:
NOTES:

DRAWING
TITLE=905B323701
ABBREV=905B323701
LAST_MODIFIED=Thu Mar 30 07:40:05 1995

| | | | | | |
|---|---|---|---|---|---|
| | -01 | 205-B3237-00 | USCA | DRAWN BY M.DUNFORD | DATE 3/10/95 |
| | CONFIG. | SHEET ASSY. NO. | USED ON | DESIGNED M.DUNFORD | 3/10/95 |
| SCHEMAS TO | APPLICATION | | | CHECKED B.Burkett | 3-30-95 |
| | | | | DESIGN ENGINEER - | - |
| | | | | PROJECT ENGINEER Dan Bahr | 3-30-95 |
| | | | | APPROVED - | APPROVED - |
| | | | | APPROVED - | APPROVED WA |



LORAL TEST & INFORMATION SYSTEMS
P.O. Box 3041
Sarasota, FL 34230

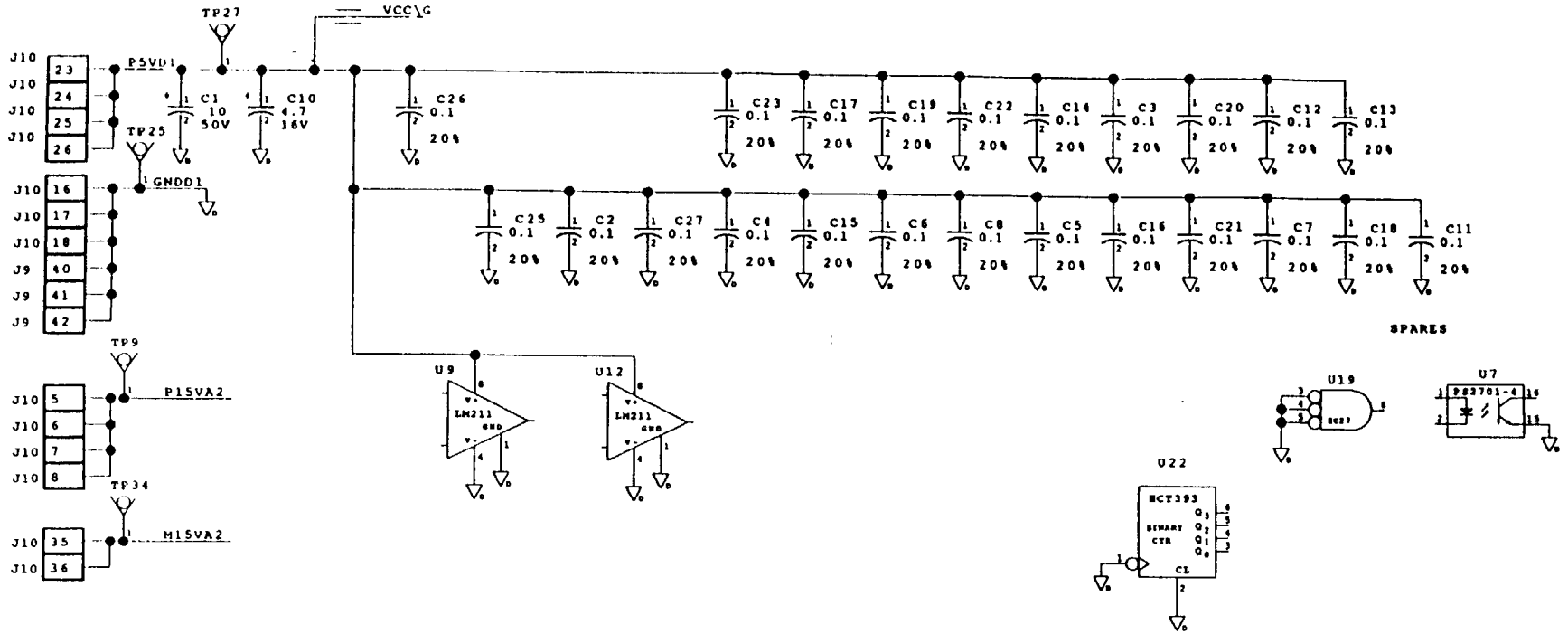
# SCHEMATIC, PWA
## USCA DIGITAL BOARD

EDC

| SIZE | CAGE CODE | DRAWING NO. | REV. |
|---|---|---|---|
| B | 01GD0 | 905-B3237-01 | - |

SCALE NONE | SHEET 1 OF 6

SHEET 1 | 905-B3237-01




NOTE: GND AND PWR PINS NOT SHOWN IN THIS SCHEMATIC:

U01 GND=8, VCC=16
U02 GND=7, VCC=14
U03 GND=7, VCC=14
U04 GND=16, VCC=32
U07 GND=10, VCC=20
U08 GND=7, VCC=14
U09 GND=10, VCC=20
U10 GND=129,122,116,110,105,99,98,92,86,81,75,70,67,62,56,48,36,34,27,22,16,11,5,3
U10 VCC=127,124,113,102,97,89,79,69,66,58,45,37,30,20,9,2
U11 GND=16, VCC=32
U12 GND=7, VCC=14
U13 GND=12, VCC=24
U14 GND=4, VCC=2
U15 GND=12, VCC=24
U16 GND=10, VCC=20
U17 GND=16, VCC=32
U18 GND=10, VCC=20
U19 GND=14, VCC=28
U20 GND=10, VCC=20
U22 GND=7, VCC=14
U24 GND=7, VCC=14
U25 GND=12, VCC=24
X1 GND=2, VCC=4
X2 GND=4, VCC=8

DRAWING
TITLE=905B323701
ABBREV=905B323701
LAST_MODIFIED=Tue Mar 21 13:13:31 1995

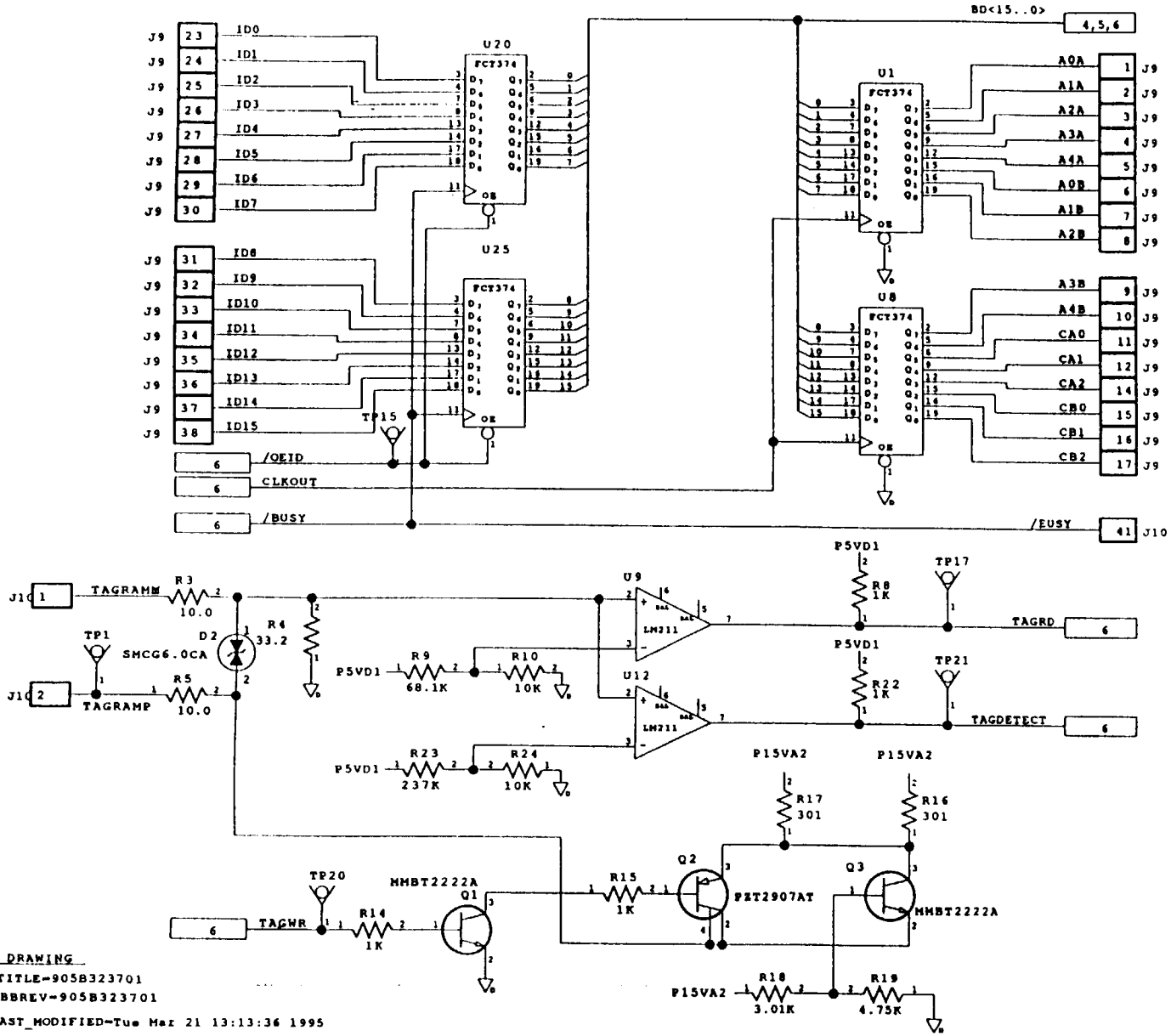
POWER AND CAPS, SPARES

LORAL
TEST & INFORMATION SYSTEMS
P.O. Box 3041
Sarasota, FL 34230

SCHEMATIC, PWA
USCA DIGITAL BOARD
SDC

| SIZE | CAGE CODE | DRAWING NO. | REV. |
|---|---|---|---|
| B | 01GD0 | 905-B3237-01 | - |
| SCALE NONE | | SHEET 2 OF 6 | |

SHEET 2
905-B3237-01



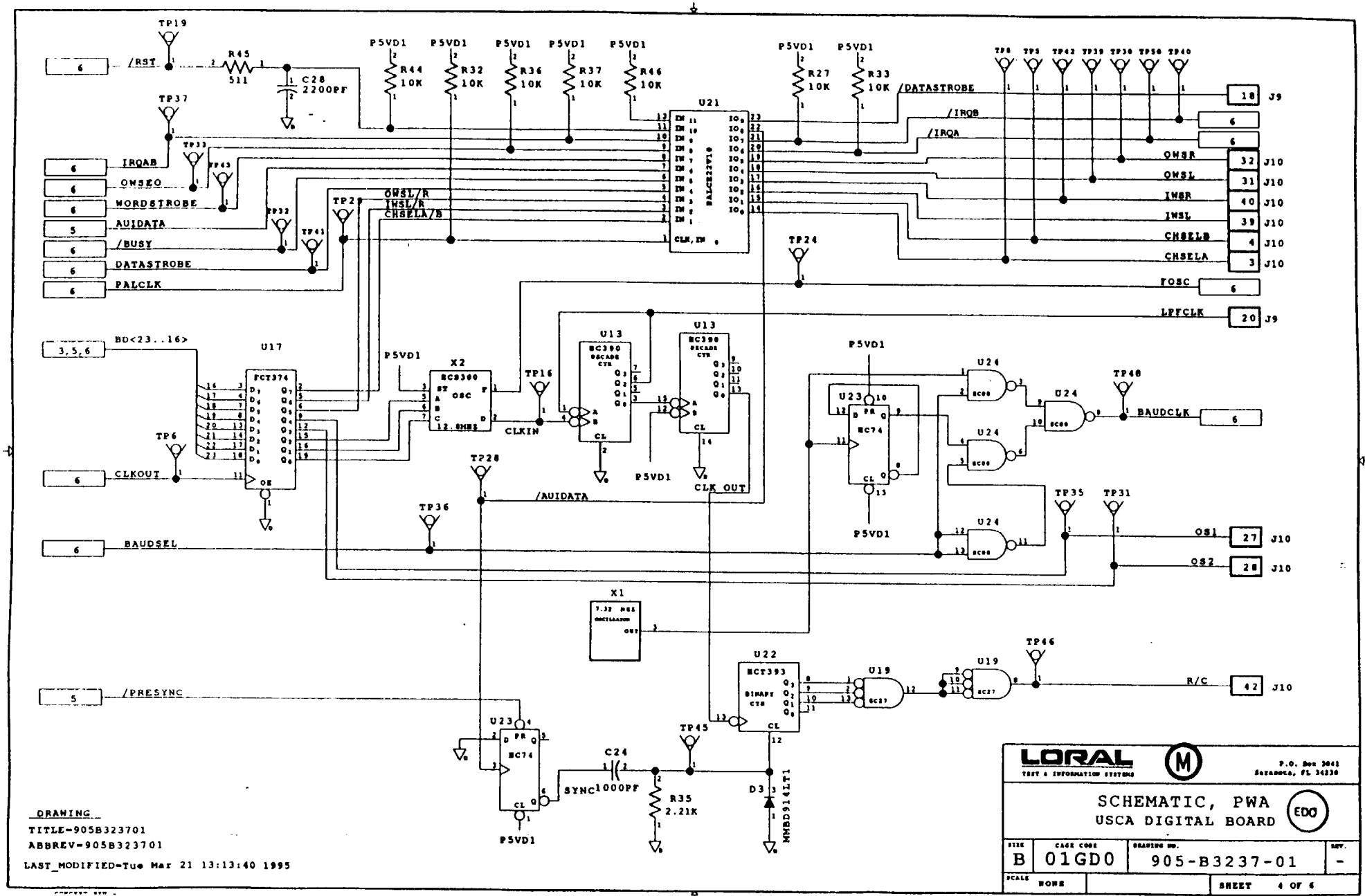

DRAWING
TITLE=905B323701
ABBREV=905B323701
LAST_MODIFIED=Tue Mar 21 13:13:36 1995

LORAL
TEST & INFORMATION SYSTEMS
P.O. Box 3041
Sarasota, FL 34230

SCHEMATIC, PWA
USCA DIGITAL BOARD
EDC

| SIZE | CAGE CODE | DRAWING NO. | REV. |
|---|---|---|---|
| B | 01GD0 | 905-B3237-01 | - |
| SCALE NONE | | SHEET 3 OF 6 | |

SHEET 3
905-B3237-01




DRAWING

TITLE=905B323701

ABBREV=905B323701

LAST_MODIFIED=Tue Mar 21 13:13:40 1995

LORAL TEST & INFORMATION SYSTEMS

P.O. Box 3041 Sarasota, FL 34230

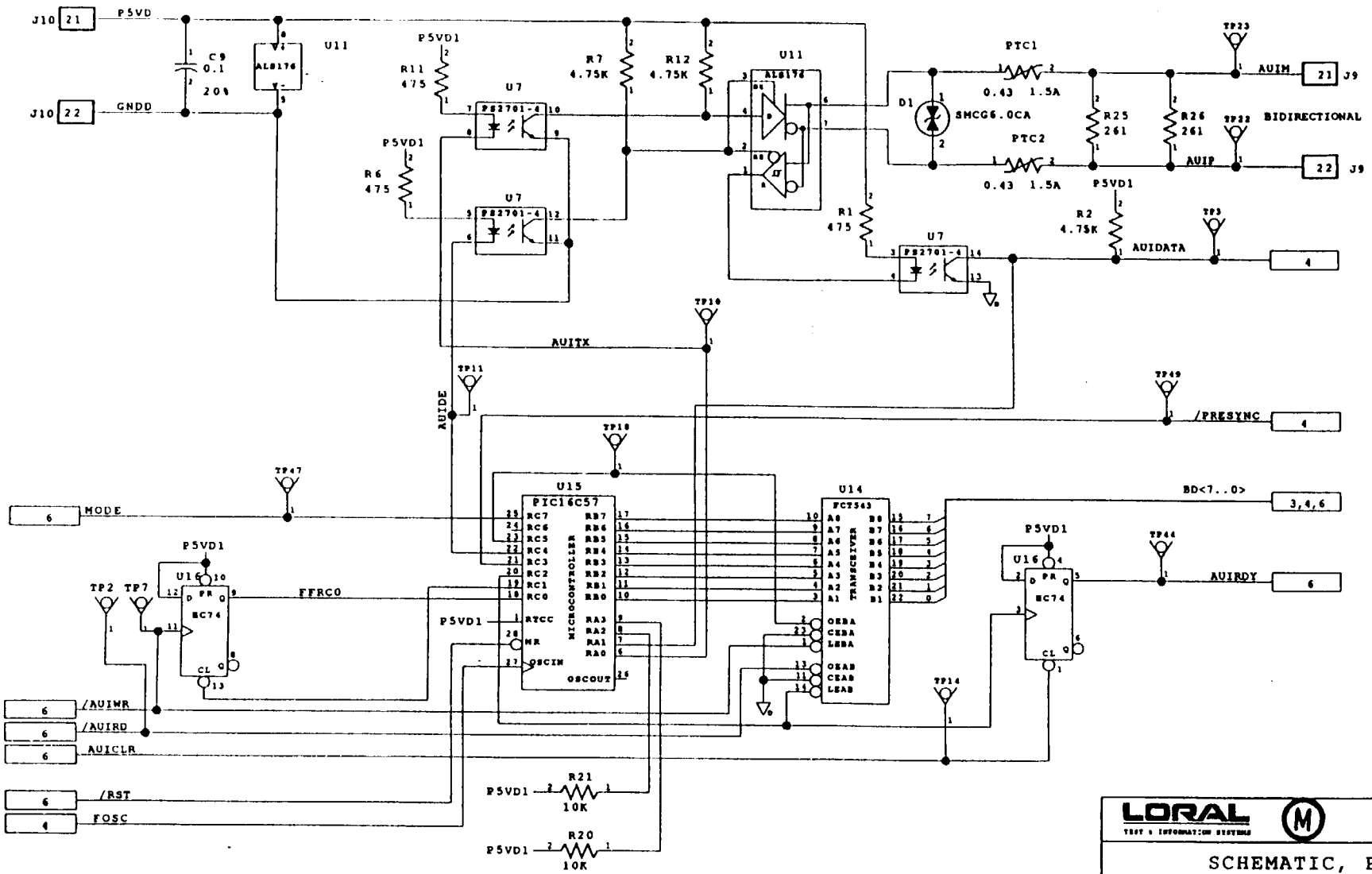
SCHEMATIC, PWA
USCA DIGITAL BOARD

EDO

| SIZE | CAGE CODE | DRAWING NO. | REV. |
|---|---|---|---|
| B | 01GD0 | 905-B3237-01 | - |
| SCALE NONE | | SHEET 4 OF 6 | |

SHEET 4

905-B3237-01



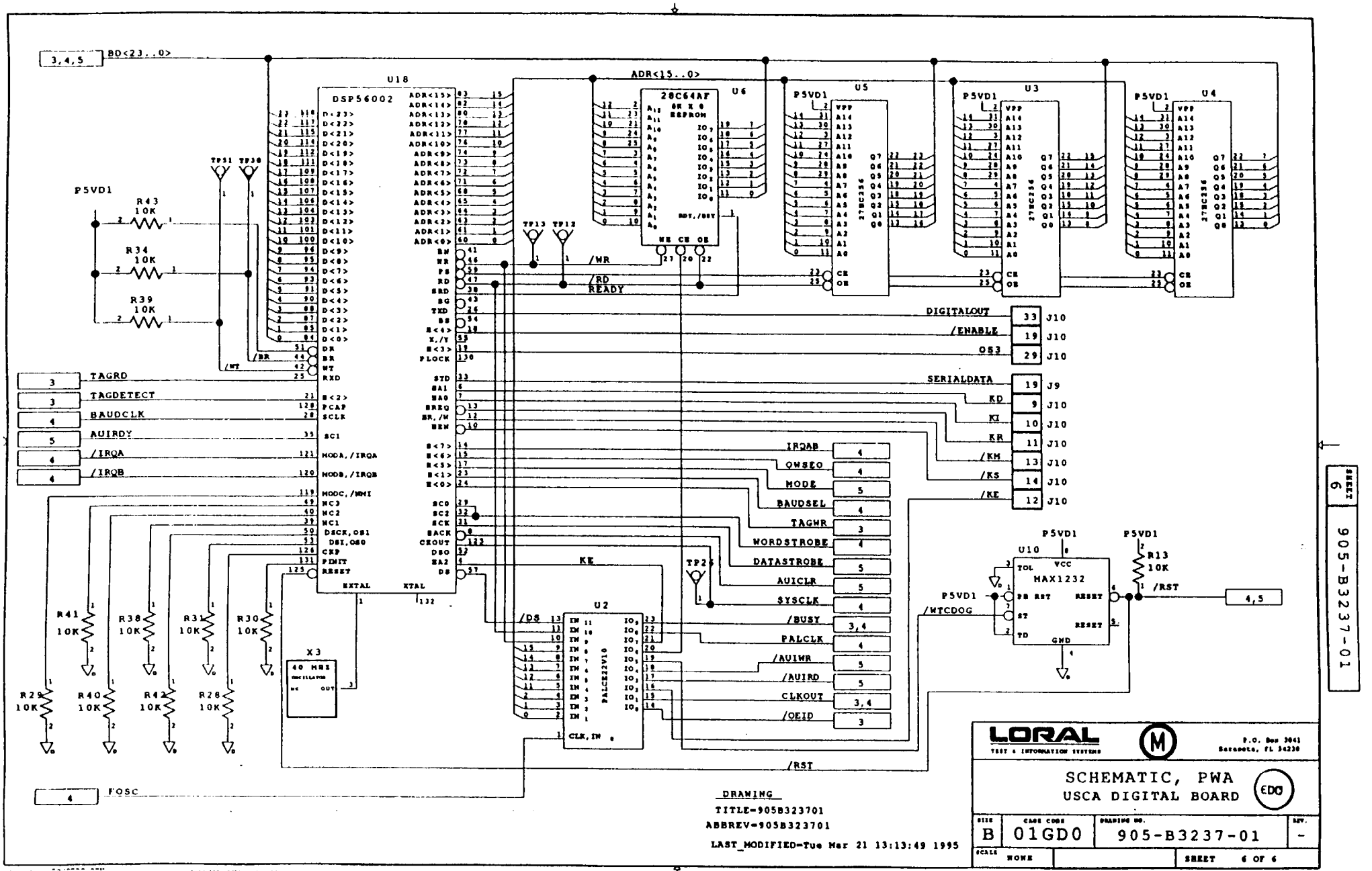

DRAWING
TITLE=905B323701
ABBREV=905B323701
LAST_MODIFIED=Tue Mar 21 13:13:44 1995

LORAL
TEST & INFORMATION SYSTEMS
P.O. Box 3041
Sarasota, FL 34230

SCHEMATIC, PWA
USCA DIGITAL BOARD
EDC

| SIZE | CAGE CODE | DRAWING NO. | REV. |
|---|---|---|---|
| B | 01GD0 | 905-B3237-01 | - |
| SCALE NONE | | SHEET 5 OF 6 | |

SHEET 5
905-B3237-01


3,4,5
BD<23..0>
U18
DSP56002
ADR<15..0>
28C64AF
8K X 8 EEPROM
U6
P5VD1
U5
U3
U4
TP51
TP50
TP13
TP12
/WR
/RD
READY
R43 10K
R34 10K
R39 10K
DIGITALOUT
/ENABLE
OS3
SERIALDATA
KD
KI
KR
/KM
/KS
/KE
J10
J9
TAGRD
TAGDETECT
BAUDCLK
AUIRDY
/IRQA
/IRQB
IRQAB
QWSEQ
MODE
BAUDSEL
TAGWR
WORDSTROBE
DATASTROBE
AUICLR
SYSCLK
/BUSY
PALCLK
/AUIWR
/AUIRD
CLKOUT
/OEID
KE
TP26
U2
PALCE22V10
/DS
U10
MAX1232
/WTCDOG
R13 10K
/RST
4,5
R41 10K
R38 10K
R31 10K
R30 10K
R29 10K
R40 10K
R42 10K
R28 10K
X3
40 MHz
FOSC
DRAWING
TITLE=905B323701
ABBREV=905B323701
LAST_MODIFIED=Tue Mar 21 13:13:49 1995
LORAL
TEST & INFORMATION SYSTEMS
P.O. Box 3041
Sarasota, FL 34230
SCHEMATIC, PWA
USCA DIGITAL BOARD
EDO
SIZE B
CAGE CODE 01GD0
DRAWING NO. 905-B3237-01
REV. -
SCALE NONE
SHEET 6 OF 6
SHEET 6
905-B3237-01

| REVISIONS | | | | |
|---|---|---|---|---|
| LTR | DESCRIPTION | EFFECTIVITY | DATE | APPROVED |
| - | | - | - | |

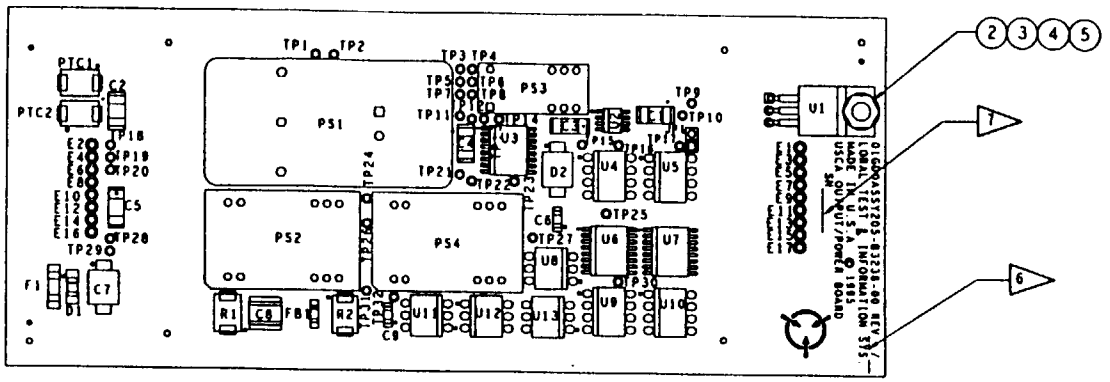
NOTES:
UNLESS OTHERWISE SPECIFIED:

1. MAX. ASSY. HEIGHT: A. TOP SIDE: .500
   B. BOTTOM SIDE: .110
2. DESIGN REF. HEIGHT: N/A
3. ON COMPONENTS OTHER THAN SURFACE MOUNT
   □SQUARE PAD INDICATES PIN 1 (POSITIVE, +) END OF POLARIZED CAPACITORS, PIN 1 (CATHODE) END OF DIODES, AND PIN 1 OF ALL OTHER COMPONENTS WITH MORE THAN 2 LEADS. REFER TO SILKSCREEN IMAGE FOR ANY MECHANICAL ORIENTATION.
4. INFORMATION FOR THIS DRAWING IS CONTAINED IN CADD DATABASE 800-B3180-00.
5. USE CAUTION WHEN HANDLING THIS PWA TO PREVENT DAMAGING BY STATIC ELECTRICITY.

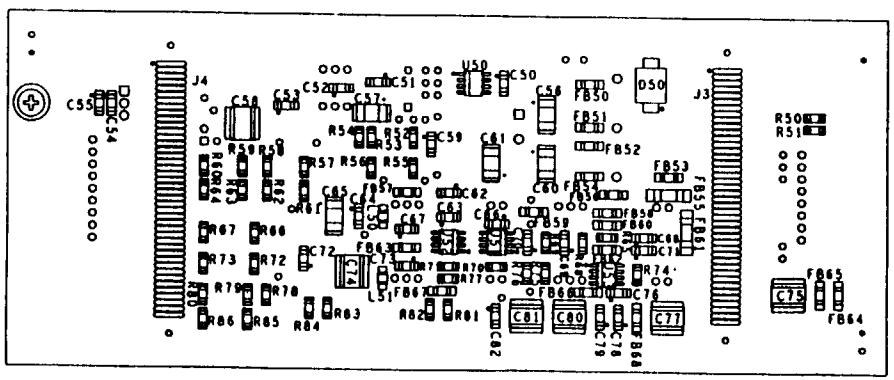
7 APPLY THE CURRENT ASSEMBLY/PARTS LIST REVISION LETTER APPROX. WHERE SHOWN. THE MARKING SHALL BE:
1.) A FILM LABEL WITH ACRYLIC PRESSURE SENSITIVE ADHESIVE, OR
2.) INDELIBLE INK PER MIL-I-43553 IN A CONTRASTING COLOR.

CURRENT ASSY REV LETTER — REV / — CURRENT PL REV LETTER

8 APPLY SERIAL NUMBER (SN XXXXX) APPROX. WHERE SHOWN PER LORAL STD 3.7. THE MARKING SHALL BE:
1.) A FILM LABEL WITH ACRYLIC PRESSURE SENSITIVE ADHESIVE, OR
2.) INDELIBLE INK PER MIL-I-43553 IN A CONTRASTING COLOR.




TOP SIDE




BOTTOM SIDE

SEE SEPARATE PARTS LIST

| | | | |
|---|---|---|---|
| 00 | 253-B3262-00 | 4200 | |

NOTICE TO PERSONS RECEIVING THIS DRAWING: THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO LORAL TEST & INFORMATION SYSTEMS AND MAY NOT BE REPRODUCED OR DISCLOSED WITHOUT PERMISSION FROM LTS. NEITHER THIS DRAWING NOR ANY REPRODUCTION THEREOF MAY BE USED TO MANUFACTURE ANYTHING UNLESS WITHOUT PERMISSION IN WRITING FROM LTS. SPECIFICALLY REFERRING TO THIS DRAWING.

DRAWN BY: L. TOMPKINS
CHECKED BY: L. TOMPKINS

LORAL Test & Information Systems — P.O. Box 2000, Binghamton, N.Y. 13902

PWA
USCA OUTPUT/POWER

| SIZE | CAGE CODE | DRAWING NO. | REV |
|---|---|---|---|
| D | 01GD0 | 205-B3238-00 | |

SCALE: 2/1 — SHEET

205-B3238-00

HOLE CHART

| HOLE | QTY | DESCRIPTION | |
|---|---|---|---|
| • | 313 | Ø .013 +/- .003 | PLATED THRU |
| • | 32 | Ø .032 +/- .003 | PLATED THRU |
| • | 22 | Ø .035 +/- .003 | PLATED THRU |
| • | 25 | Ø .040 +/- .003 | PLATED THRU |
| • | 8 | Ø .055 +/- .003 | PLATED THRU |
| ⊕ | 1 | Ø .140 +/- .005 | PLATED THRU |
| ◉ | 2 | Ø .125 +/- .003 | NON-PLATED THRU |
| ◉ | 4 | Ø .188 +/- .003 | NON-PLATED THRU |

REVISIONS

| ZONE | DESCRIPTION | APPROVED | DATE | APPROVED |
|---|---|---|---|---|
| - | - | - | - | - |

NOTES:
UNLESS OTHERWISE SPECIFIED:

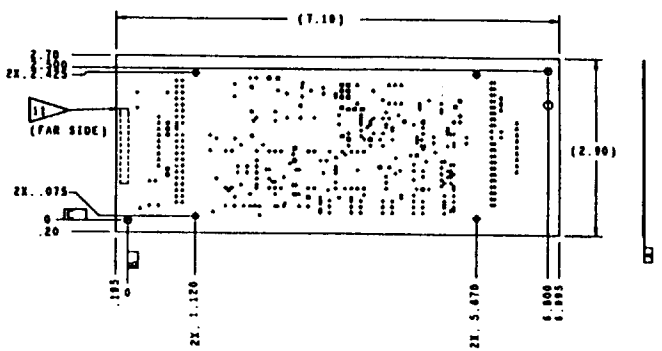
1. THIS PWB SHALL MEET/EXCEED ALL APPLICABLE IPC STANDARDS.
2. ARTWORK 805-B3238-02 AT REV -
(CADD DB 809-B3238-00) CONSISTS OF:
6 SHEETS CIRCUITRY AT REV -,
ONE SHEET SOLDER MASK (TOP SIDE) AT REV -,
ONE SHEET SOLDER MASK (BOTTOM SIDE) AT REV -,
ONE SHEET SILKSCREEN (TOP SIDE) AT REV -,
ONE SHEET SILKSCREEN (BOTTOM SIDE) AT REV -,
ONE SHEET PASTE MASK (TOP SIDE) AT REV -,
ONE SHEET PASTE MASK (BOTTOM SIDE) AT REV -,
AND ONE DRILL FILE AT REV -.
3. MATERIAL-PLASTIC SHEET — MIL-P-13949/4, TYPE:

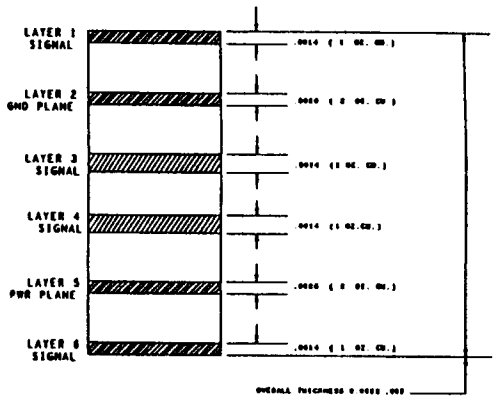
| | |
|---|---|
| BASE MATERIAL | GFN |
| BASE THICKNESS | SEE MULTILAYER DETAIL |
| TYPE OF COPPER FOIL | C |
| WEIGHT OF COPPER FOIL | SEE MULTILAYER DETAIL |
| GRADE OF PITS AND DENTS | A |
| CLASS OF THICKNESS TOL | 2 |
| CLASS OF BOW AND TWIST | C (APPLICABLE TO BASE THICKNESS > .020 ONLY) |

MATERIAL-PREPREG — MIL-P-13949/12, TYPE:

| | |
|---|---|
| PREPREG MATERIAL | PC-GF |
| RESIN MATERIAL | |
| GLASS STYLE | MANUFACTURER'S OPTION |
| NOM RES FLOW | MANUFACTURER'S OPTION |
| NOM GEL TIME | MANUFACTURER'S OPTION |
| NOM RESIN CONTENT | MANUFACTURER'S OPTION |

4. OXIDE TREAT CORE PATTERN.
5. THIS PWB REQUIRES ETCHBACK IN ACCORDANCE WITH PARAGRAPH 3.8.5.3 OF MIL-P-55110.
MINIMUM ACCEPTABLE ETCHBACK IS .0001
MAXIMUM ACCEPTABLE ETCHBACK IS .0010
6. VIA HOLES MUST NOT BE PARTIALLY PLATED CLOSED
7. ELECTROPLATE .001 IN. COPPER MINIMUM.
8. APPLY LIQUID PHOTO IMAGEABLE SOLDER MASK WITH GLOSS GREEN FINISH OVER BARE COPPER PER IPC-SM-840 CLASS 3. LEAVE COMPONENT PADS CLEAR OF SOLDER MASK MAINTAINING .005 MAX/.001 MIN CLEARANCE.
9. APPLY TIN/LEAD COATING (63/37) PER MIL-P-55110. COATING MUST BE MELTED ALLOY.
10. LETTER TOP AND BOTTOM SIDES OF PWB USING MASTER PATTERN ARTWORK AND INK PER MIL-I-43553. COLOR YELLOW NO. 13655 PER FED-STD-595.
11. APPLY THE CURRENT PWB DRAWING REVISION LETTER APPROX. WHERE SHOWN. THE MARKING SHALL BE ONE OF THE FOLLOWING:
1.) ETCHED IN ARTWORK
2.) A FILM LABEL WITH ACRYLIC PRESSURE SENSITIVE ADHESIVE
3.) INDELIBLE INK PER MIL-I-43553 IN A CONTRASTING COLOR
206-B3238-00REV
CURRENT PWB DRAWING REV LETTER




MULTILAYER DETAIL (NOT TO SCALE)

12. HOLE LOCATIONS AND SIZES ARE PER DRILL FILE. LOCATIONAL DIMENSIONS ARE BASIC AND TOLERANCE IS:

| | | | | |
|---|---|---|---|---|
| ⌖ | Ø.026 Ⓜ | A | B | C |
| | Ø.007 Ⓜ | A | | |

13. SERIALIZED QUALITY ASSURANCE TEST COUPONS PER MIL-STD-275 SHALL BE SUPPLIED (ONE SET PER PANEL) WITH EACH SET OF PWBS FABRICATED. EXAMPLES OF THE SMALLEST HOLE AND PAD SIZE SHALL BE INCLUDED.

VENDOR ITEM DRAWING



| | | |
|---|---|---|
| -00 | 205-B3238-00 | USCA |

| | | | | |
|---|---|---|---|---|
| 4 | 7 | 8 | 9 | 10 |

| | | |
|---|---|---|
| DRAWN | M. DUNFORD | |
| CHECKED | M. DUNFORD | |
| ENGINEER | | |
| PROJECT ENGINEER | | |
| APPROVED | | |

LORAL Vought Systems Corporation, P.O. Box 2000, Greenville, TX 75403

PWB
USCA OUTPUT/POWER

| SIZE | CAGE CODE | DRAWING NO. | REV |
|---|---|---|---|
| D | 01GD0 | 206-B3238-00 | |

SCALE 1/1 SHEET 1 OF 1

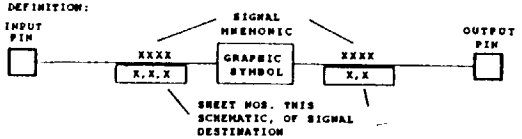
206-B3238-00

| COMPONENT CHART | |
|---|---|
| LAST NO. USED | UNUSED NUMBER |
| C | |
| CR | |
| E | |
| J | |
| L | |
| P | |
| Q | |
| R | |
| S | |
| T | |
| TP | |
| U | |

| REVISIONS | | | | |
|---|---|---|---|---|
| LTR. | DESCRIPTION | EFFECTIVITY | DATE | APPROVED |
| - | - | - | - | - |

5. INFORMATION FOR THIS DRAWING IS CONTAINED IN CADD DATABASE 899-XXXXX-00.

4. ADDRESS DEFINITION:




3. CIRCUIT RETURN SYMBOLS:


2. FOR TOLERANCES AND RATINGS SEE PARTS LIST.

1. RESISTOR VALUES ARE IN OHMS, CAPACITOR VALUES ARE IN MICROFARADS.

UNLESS OTHERWISE SPECIFIED:
NOTES:

DRAWING
TITLE=905B323801
ABBREV=905B323801
LAST_MODIFIED=Thu Mar 30 07:42:51 1995

| | | | |
|---|---|---|---|
| | -01 | 205-B3238-00 | USCA |
| | CONFIG. | NEXT ASSY. NO. | USED ON |
| SIMILAR TO | APPLICATION | | |



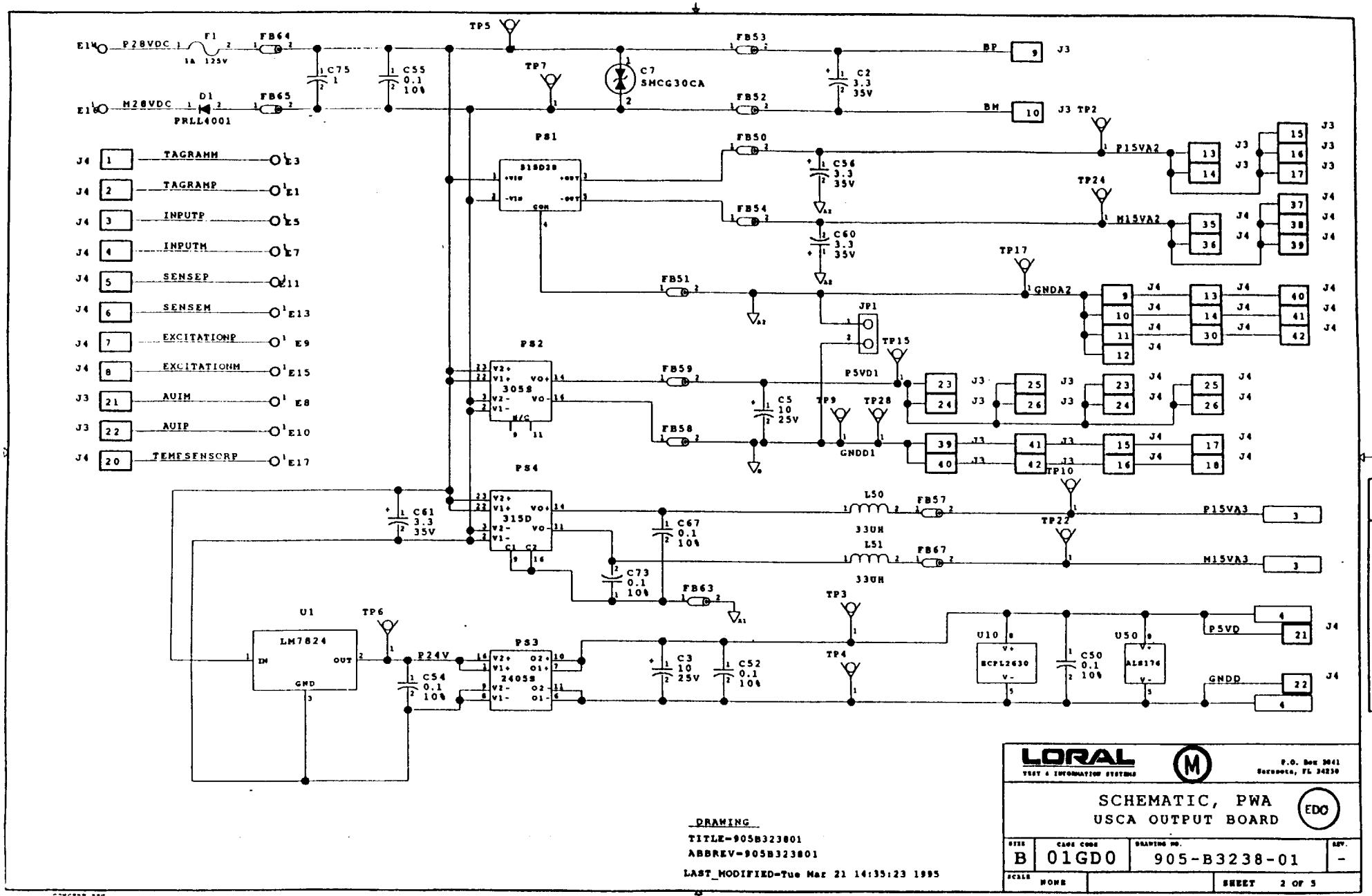
| | | |
|---|---|---|
| DRAWN BY L.TOMPKINS | DATE 3/13/95 | |
| DESIGNER M.OSTRYE | 3/10/95 | |
| CHECKED | 3-30-95 | |
| DESIGN ENGINEER - | - | |
| PROJECT ENGINEER | 3/30/95 | |
| APPROVED - | APPROVED - | |
| APPROVED - | Q.A. | |

LORAL TEST & INFORMATION SYSTEMS
P.O. Box 3041
Sarasota, FL 34230

SCHEMATIC, PWA
USCA OUTPUT BOARD (EDC)

| SIZE | CAGE CODE | DRAWING NO. | REV. |
|---|---|---|---|
| B | 01GD0 | 905-B3238-01 | - |
| SCALE NONE | | SHEET 1 OF 5 | |

SHEET 1
905-B3238-01

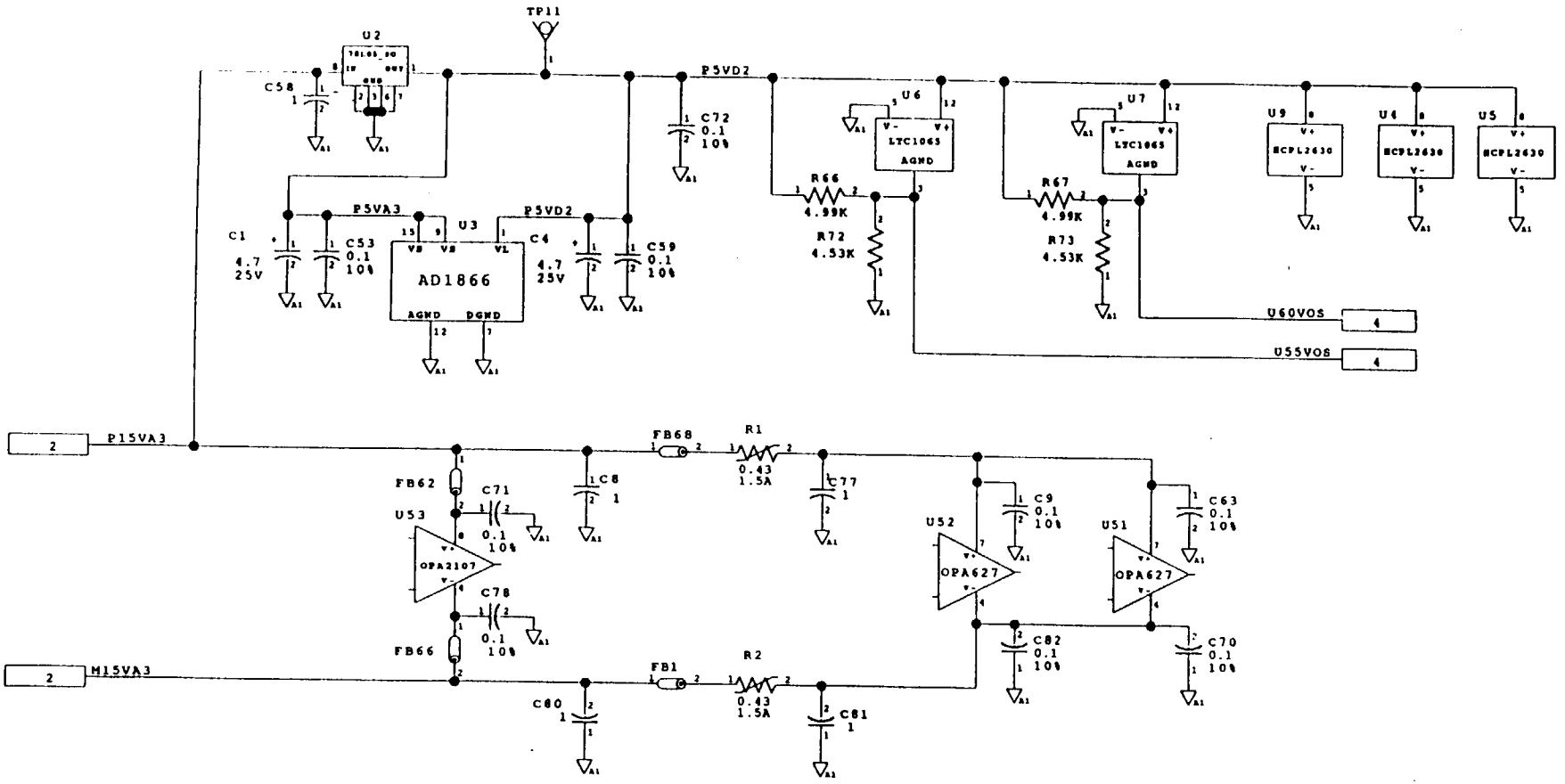



DRAWING
TITLE=905B323801
ABBREV=905B323801
LAST_MODIFIED=Tue Mar 21 14:35:23 1995

LORAL
VISY & INFORMATION SYSTEMS
P.O. Box 3041
Sarasota, FL 34230

SCHEMATIC, PWA
USCA OUTPUT BOARD
EDO

| SIZE | CAGE CODE | DRAWING NO. | REV. |
|---|---|---|---|
| B | 01GD0 | 905-B3238-01 | - |
| SCALE NONE | | SHEET 2 OF 5 | |




DRAWING

TITLE=905B323801

ABBREV=905B323801

LAST_MODIFIED=Tue Mar 21 14:35:27 1995

LORAL
TEST & INFORMATION SYSTEMS

P.O. Box 3041
Sarasota, FL 34230

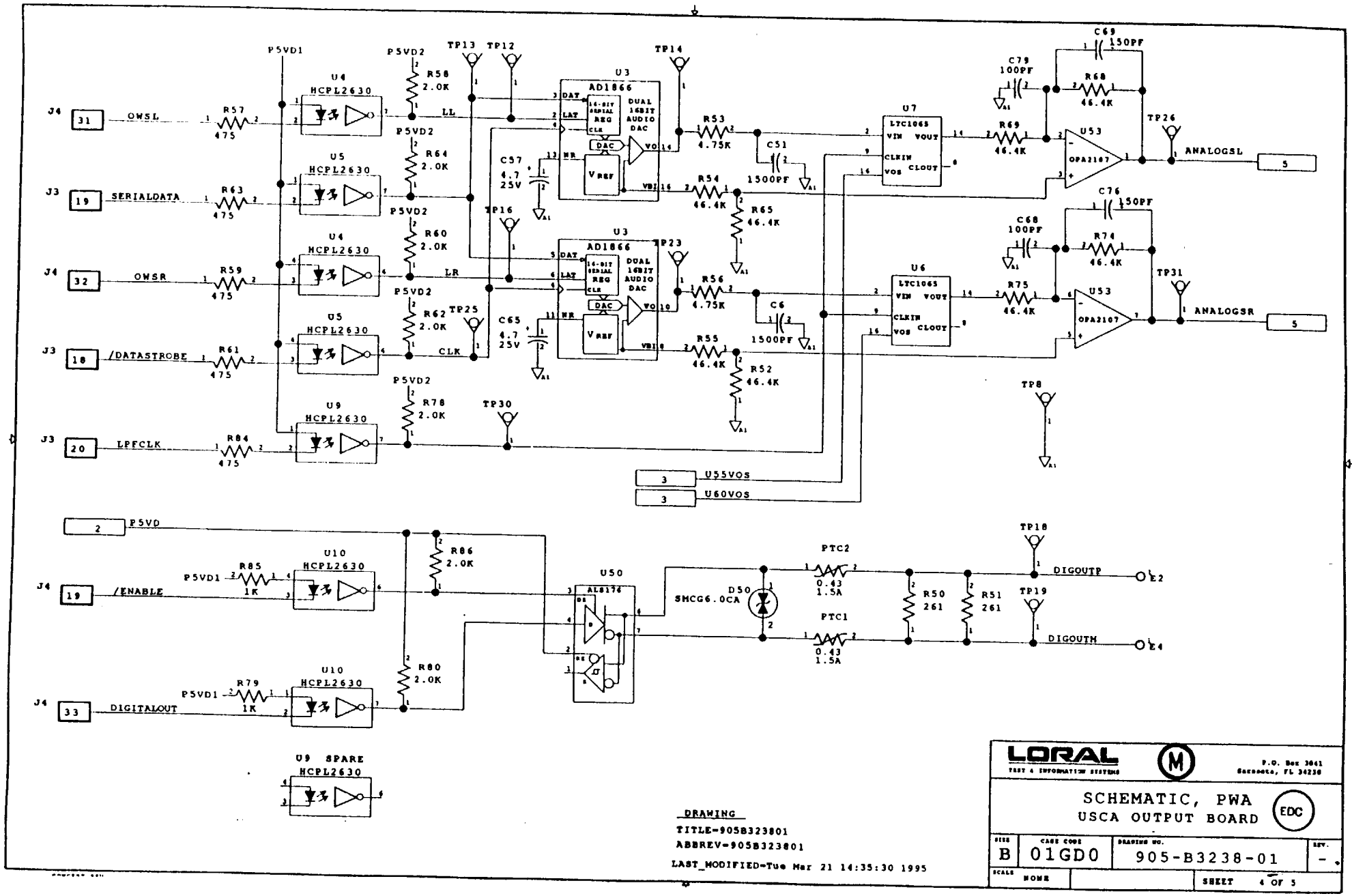
SCHEMATIC, PWA
USCA OUTPUT BOARD

EDC

| SIZE | CAGE CODE | DRAWING NO. | REV. |
|---|---|---|---|
| B | 01GD0 | 905-B3238-01 | - |
| SCALE NONE | | SHEET 3 OF 5 | |

SHEET 3

905-B3238-01



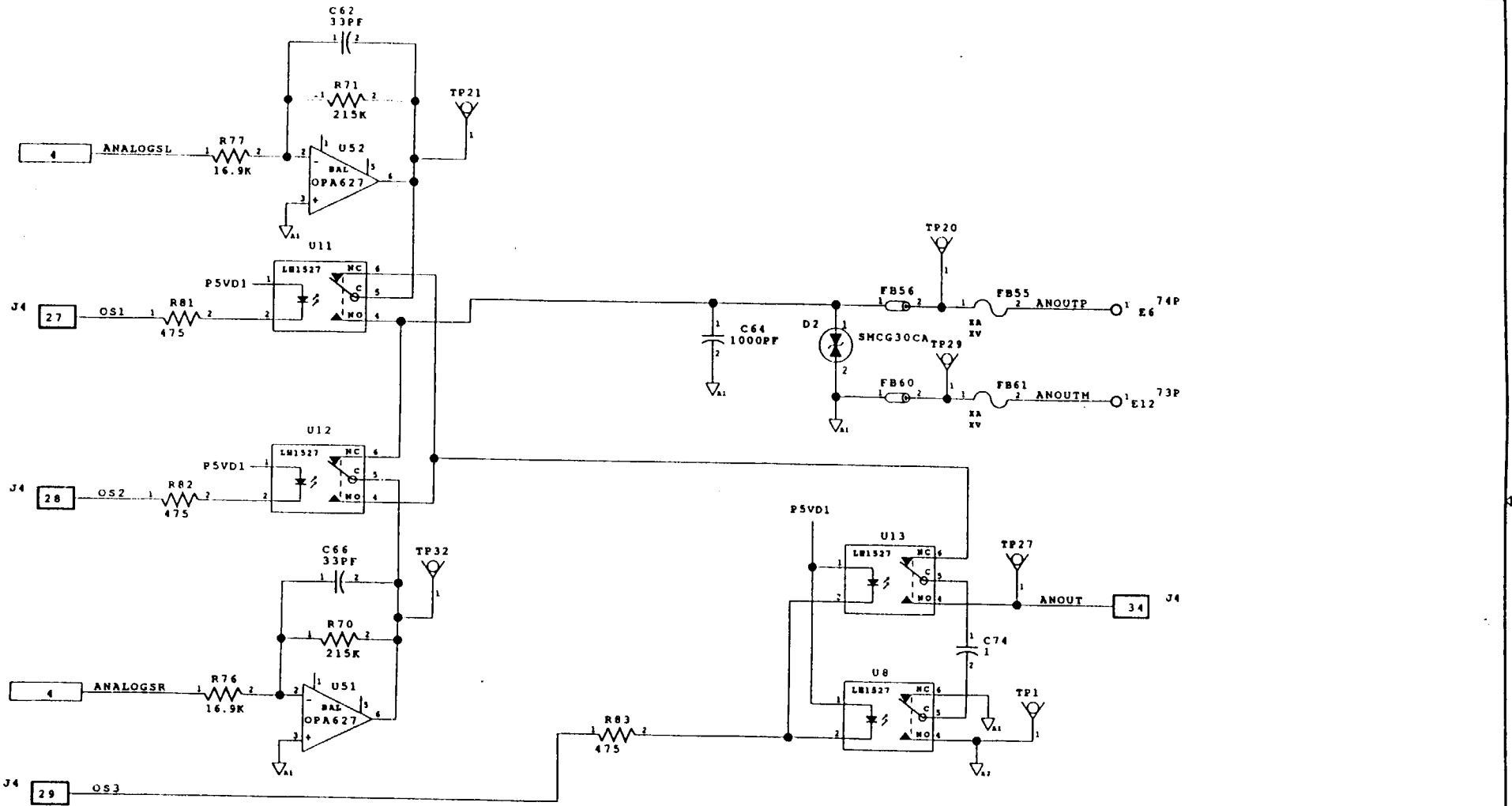

DRAWING
TITLE=905B323801
ABBREV=905B323801
LAST_MODIFIED=Tue Mar 21 14:35:30 1995

LORAL
TEST & INFORMATION SYSTEMS
P.O. Box 3041 Sarasota, FL 34230

SCHEMATIC, PWA
USCA OUTPUT BOARD
EDC

| SIZE | CAGE CODE | DRAWING NO. | REV. |
|---|---|---|---|
| B | 01GD0 | 905-B3238-01 | - |
| SCALE NONE | | SHEET 4 OF 5 | |

SHEET 4
905-B3238-01




DRAWING

TITLE-905B323801

ABBREV-905B323801

LAST_MODIFIED-Tue Mar 21 14:35:32 1995

LORAL

TEST & INFORMATION SYSTEMS

P.O. Box 3041
Sarasota, FL 34230

SCHEMATIC, PWA
USCA OUTPUT BOARD

EDC

| SIZE | CAGE CODE | DRAWING NO. | REV. |
|---|---|---|---|
| B | 01GD0 | 905-B3238-01 | - |

SCALE NONE

SHEET 5 OF 5

SHEET 5

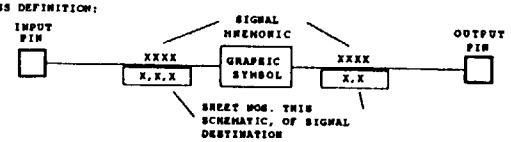
905-B3238-01

| COMPONENT CHART | |
|---|---|
| LAST NO USED | UNUSED NUMBER |
| P2 | |

| REVISIONS | | | | |
|---|---|---|---|---|
| SYM. | DESCRIPTION | EFFECTIVITY | DATE | APPROVED |
| - | - | - | - | - |

5. INFORMATION FOR THIS DRAWING IS CONTAINED IN CADD DATABASE 699-B3254-00.

4. ADDRESS DEFINITION:




3. CIRCUIT RETURN SYMBOLS:


2. FOR TOLERANCES AND RATINGS SEE PARTS LIST.

1. RESISTOR VALUES ARE IN OHMS, CAPACITOR VALUES ARE IN MICROFARADS.

UNLESS OTHERWISE SPECIFIED:
NOTES:

DRAWING
TITLE=905B325401
ABBREV=905B325401
LAST_MODIFIED=Thu Mar 30 07:50:22 1995

| | | | |
|---|---|---|---|
| | -01 | 205-B3254-00 | USCA |
| | CONFIG. | NEXT ASSY. NO. | USED ON |
| SIMILAR TO | APPLICATION | | |

NOTICE TO PERSONS RECEIVING THIS DRAWING: THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO LORAL TEST & INFORMATION SYSTEMS AND MAY NOT BE REPRODUCED WITHOUT WRITTEN PERMISSION FROM LTIS. NEITHER THIS DRAWING NOR ANY REPRODUCTION THEREOF MAY BE USED TO MANUFACTURE ANYTHING SHOWN THEREIN WITHOUT PERMISSION IN WRITING FROM LTIS TO USER SPECIFICALLY REFERRING TO THIS DRAWING.

| | | DATE |
|---|---|---|
| DRAWN BY | L.TOMPKINS | 3/30/95 |
| DESIGNER | M. OSTRYE | 3/30/95 |
| CHECKER | B Bennett | 3-30 |
| DESIGN ENGINEER | - | - |
| PROJECT ENGINEER | David Beck | 3-30-95 |
| APPROVED | - | - |
| APPROVED | - | - |
| APPROVED | - | - |

LORAL TEST & INFORMATION SYSTEMS
P.O. Box 3041
Sarasota, FL 34230

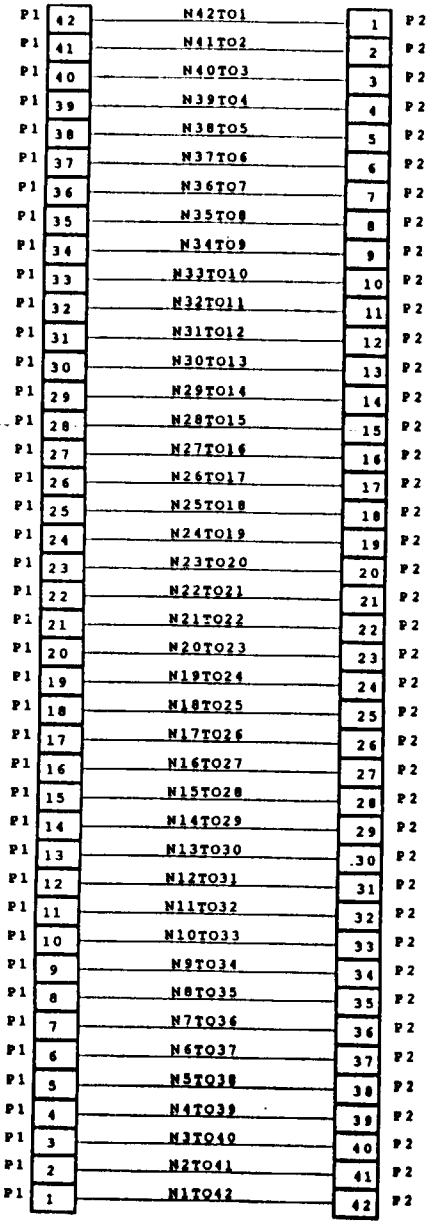
# SCHEMATIC, PWA
## USCA TEST BOARD

EDC

| SIZE | CAGE CODE | DRAWING NO. | REV. |
|---|---|---|---|
| B | 01GD0 | 905-B3254-01 | - |
| SCALE NONE | | SHEET 1 OF 2 | |

CONCEPT REV -

SHEET 1
905-B3254-01




DRAWING
TITLE=905B325401
ABBREV=905B325401
LAST_MODIFIED=Thu Mar 30 07:49:57 1995

LORAL
TEST & INFORMATION SYSTEMS

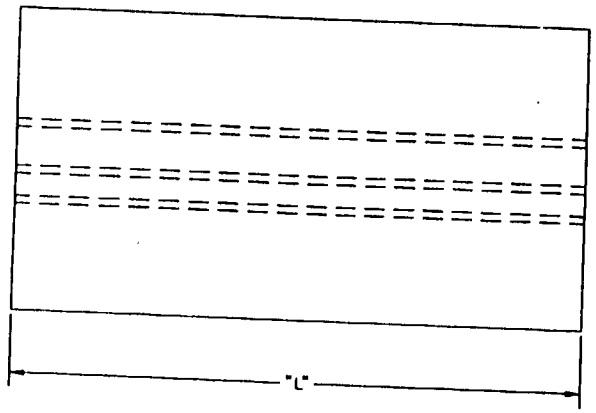
P.O. Box 3041
Sarasota, FL 34230

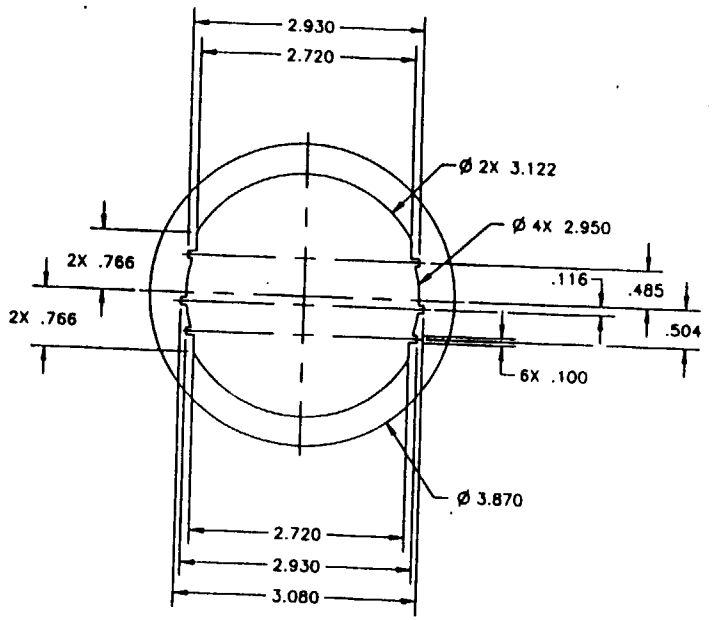
SCHEMATIC, PWA
USCA TEST BOARD

| SIZE | CAGE CODE | DRAWING NO. | REV. |
|---|---|---|---|
| B | 01GD0 | 905-B3254-01 | - |
| SCALE NONE | | SHEET 2 | |

SHEET 2
905-B3254-01

| REVISIONS | | | | |
|---|---|---|---|---|
| SYM. | DESCRIPTION | EFFECTIVITY | DATE | APPROVED |
| 1 | REV. VERTICAL .750 DIM TO .766 | 3/23/95 | 3/23/95 | |
| KA | ECO 11008 UPDATE FOR RELEASE | 5/3/95 | 5/3/95 | |




NOTES:
UNLESS OTHERWISE SPECIFIED

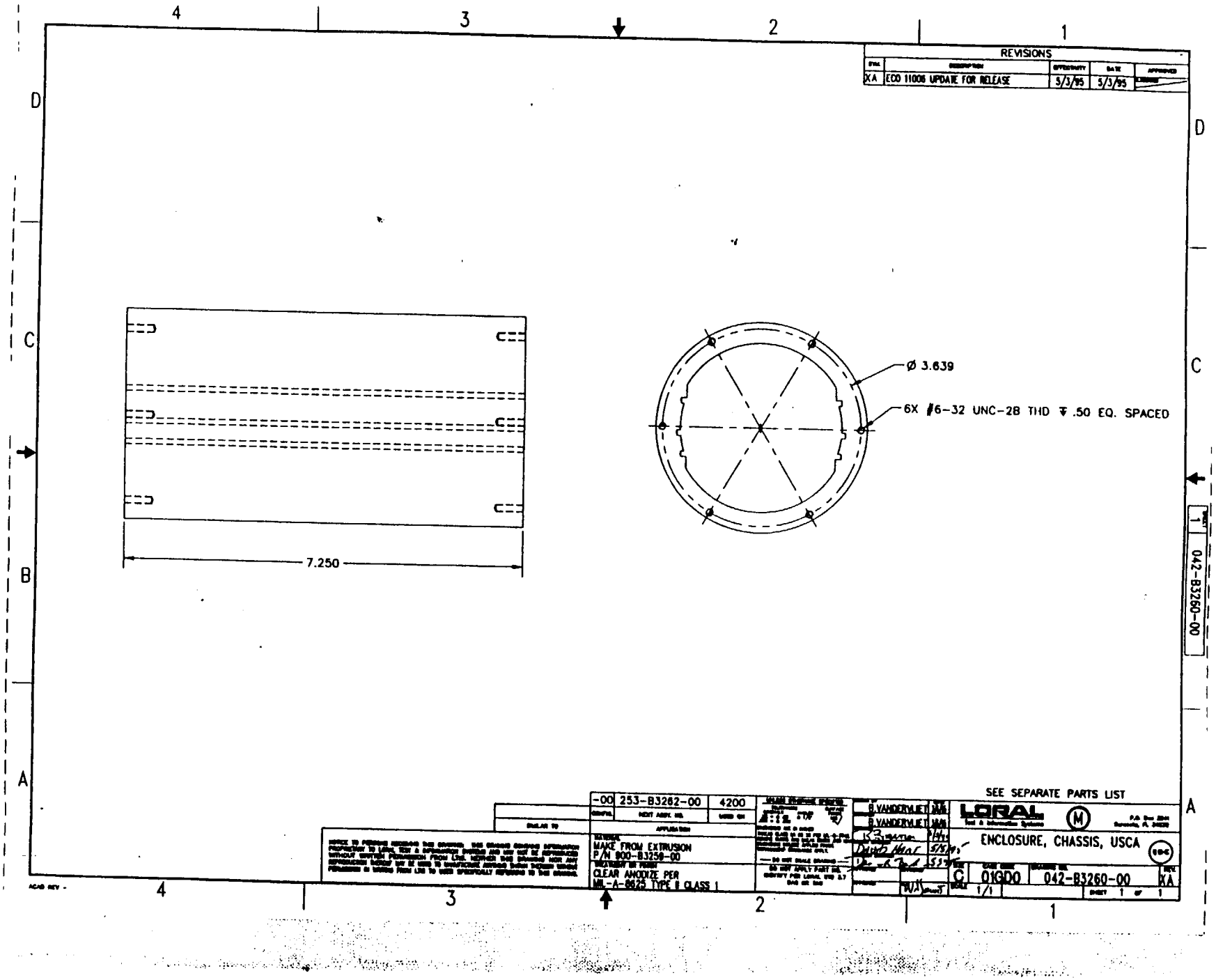
1. TOLERANCE FOR ALL DIMENSIONS IS ±.020.

SPECIFICATION CONTROL DRAWING

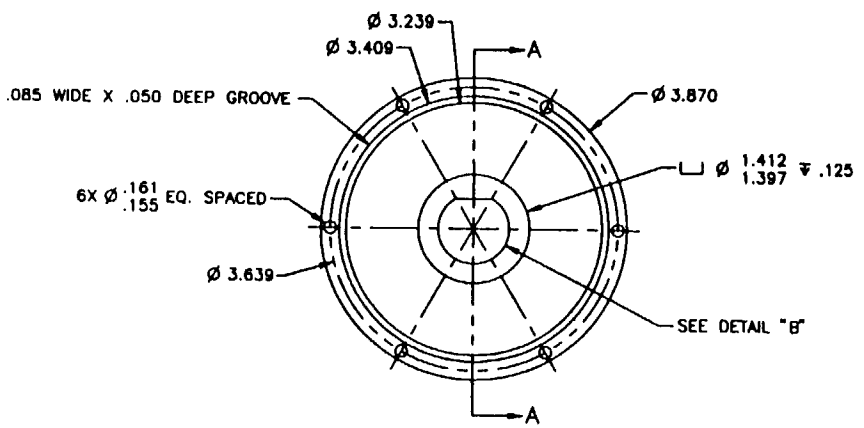
| | | | | | |
|---|---|---|---|---|---|
| -00 | 042-B3260-00 | 4200 | | | |
| | NEXT ASSY. NO. | | | | |
| | APPLICATION | | | | |
| MATERIAL: ALUMINUM ALLOY 6081-T6 | | | | | |

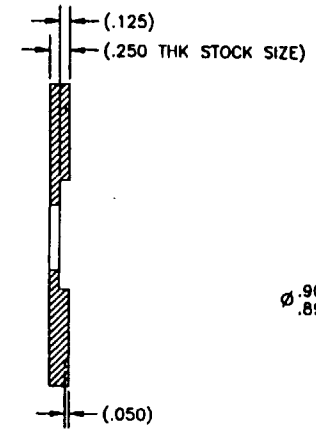
| | | | | | |
|---|---|---|---|---|---|
| | | | G. VANDERVLIET | | LORAL |
| | | | G. VANDERVLIET | | EXTRUSION, ENCLOSURE, USCA |
| SIZE C | CAGE CODE 01GD0 | DRAWING NO. 900-B3259-00 | | | REV KA |
| SCALE 1/1 | | | | SHEET 1 OF 1 | |

900-B3259-00

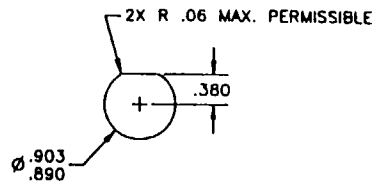

REVISIONS
XA ECO 11006 UPDATE FOR RELEASE 5/3/95 5/3/95
7.250
Ø 3.639
6X #6-32 UNC-2B THD ₸ .50 EQ. SPACED
SEE SEPARATE PARTS LIST
ENCLOSURE, CHASSIS, USCA
042-B3260-00
01GD0
MAKE FROM EXTRUSION P/N 900-B3258-00
CLEAR ANODIZE PER MIL-A-8625 TYPE II CLASS 1

| REVISIONS | | | | |
|---|---|---|---|---|
| SYM | DESCRIPTION | EFFECTIVITY | DATE | APPROVED |
| 1 | ADD 2X R .06 TO DETAIL "B" | 4/4/95 | 4/4/95 | |
| KA | ECO 11006 UPDATE FOR RELEASE | 5/3/95 | 5/3/95 | |




SECTION A-A




DETAIL "B"

SEE SEPARATE PARTS LIST

| | | | |
|---|---|---|---|
| -00 | 253-B3262-00 | 4200 | |
| MATERIAL: ALUMINUM ALLOY 6061-T6 | | | |
| FINISH OR PLATE: CLEAR ANODIZE PER MIL-A-8625 TYPE II CLASS 1 | | | |

| | |
|---|---|
| B.VANDERVLIET | MAR |
| B.VANDERVLIET | MAR |
| R.ZOERNER | MAR |
| DAVID HART | MAR |
| DEAN BECKER | MAR |
| WAYNE SAHM | |

LORAL (M)

PLATE, END CAP, USCA

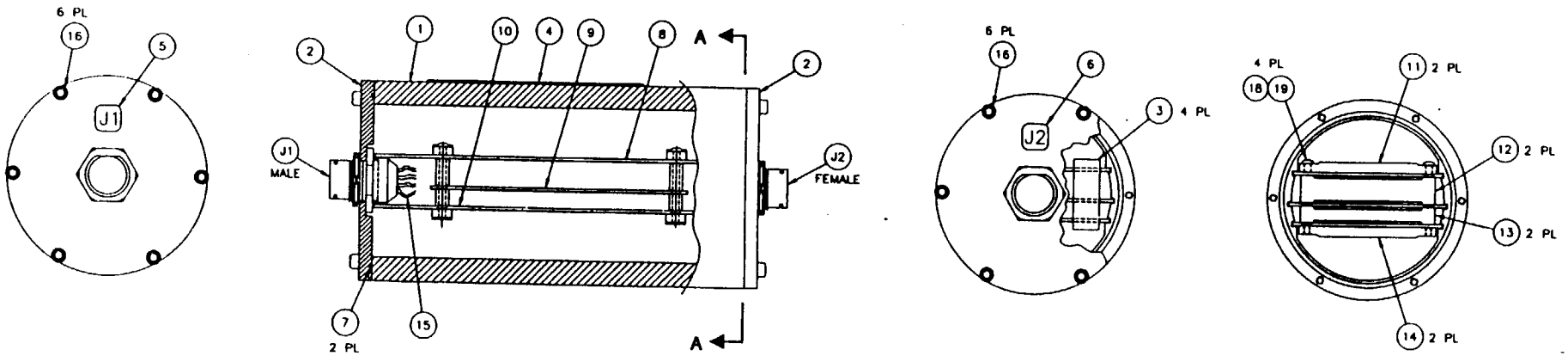
| SIZE | CAGE CODE | DRAWING NO. | REV |
|---|---|---|---|
| C | 01GD0 | 196-B3261-00 | KA |

SCALE 1/1 SHEET 1 OF 1

196-B3261-00

| WIRING DATA | | | |
|---|---|---|---|
| FROM | TO | LENGTH | DESCRIPTION |
| J1-A | E6 | 1.5" | ANOUTP |
| J1-B | E12 | 1.5" | ANOUTM |
| J1-C | E16 | 1.5" | M28VDC |
| J1-D | E14 | 1.5" | P28VDC |
| J1-E | E10 | 1.5" | AUIP |
| J1-F | E8 | 1.5" | AUIM |
| J1-G | E2 | 1.5" | DIGOUTP |
| J1-H | E4 | 1.5" | DIGOUTM |
| J1-J | | | N/C |
| J1-K | | | N/C |
| J2-A | E5 | 1.5" | INPUTP |
| J2-B | E7 | 1.5" | INPUTM |
| J2-C | E15 | 1.5" | EXCITATIONM |
| J2-D | E9 | 1.5" | EXCITATIONP |
| J2-E | E1 | 1.5" | TAGRAMP |
| J2-F | E3 | 1.5" | TAGRAMM |
| J2-G | E11 | 1.5" | SENSEP |
| J2-H | E13 | 1.5" | SENSEM |
| J2-J | | | N/C |
| J2-K | | | N/C |

| REVISIONS | | | | |
|---|---|---|---|---|
| LTR | DESCRIPTION | ORIGINATOR | DATE | APPROVED |
| XA | ECO 11008 UPDATE FOR RELEASE | | 5/3/95 | |
| XB | ECO 11089 UPDATE WIRING INFORMATION | | 6/20/95 | |




SECTION A - A

J2 REMOVED FOR CLARITY

NOTES
UNLESS OTHERWISE SPECIFIED

1. ALL WIRE IS #22 STRD WHT.

SEE SEPARATE PARTS LIST

LORAL

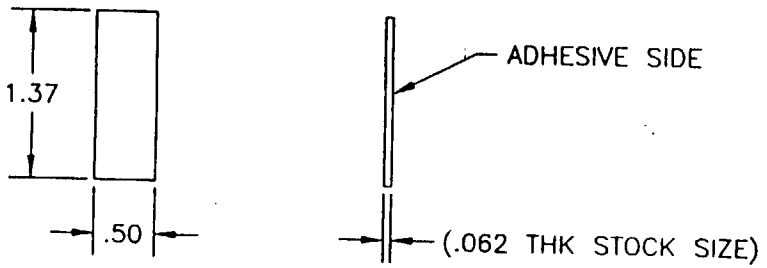
ASSEMBLY, UNIVERSAL SIGNAL CONDITIONING AMPLIFIER

| SIZE | CAGE CODE | DRAWING NO. | REV |
|---|---|---|---|
| D | 01300 | 253-B3262-00 | XB |

SHEET 1/1

253-B3262-00

| REVISIONS | | | | |
|---|---|---|---|---|
| SYM. | DESCRIPTION | EFFECTIVITY | DATE | APPROVED |
| XA | ECO 11006 UPDATE FOR RELEASE | 5/3/95 | 5/3/95 | |




SHEET 1

189-B3263-00

SEE SEPARATE PARTS LIST

| -00 | 253-B3262-00 | 4200 |
|---|---|---|
| CONFIG. | NEXT ASSY. NO. | USED ON |

SIMILAR TO

APPLICATION

MATERIAL
.062 THK HD CEL. URETHANE
ADHESIVE BACKED

TREATMENT OR FINISH

UNLESS OTHERWISE SPECIFIED
TOLERANCES
DECIMALS ANGLES SURFACE FINISH
.XX = ± .03 ± 1/2° 125
.XXX = ± .010
DIMENSIONS ARE IN INCHES
THREAD CLASS 2A OR 2B PER MIL-S-7742.
REMOVE BURRS AND BREAK EDGES .020 MAX.
DIMENSIONS INCLUDE APPLIED FINISH.
WORKMANSHIP STANDARDS APPLY.
— DO NOT SCALE DRAWING —
DO NOT APPLY PART NO. IDENTIFY PER LORAL STD 3.7 BAG OR TAG

| | | | |
|---|---|---|---|
| DRAWN BY | B.VANDERVLIET | JVV | 5/5/95 |
| DESIGNED | B.VANDERVLIET | JVV | 5/5/95 |
| CHECKED | | | 5/5/95 |
| ENGR. APPROVAL | | | 5/5/95 |
| MFG. APPROVAL | | | |
| QUALITY APPROVAL | | | |

LORAL
Test & Information Systems
P.O. Box 3041
Sarasota, FL 34230

PAD, PWA RETAINER, USCA

EDC

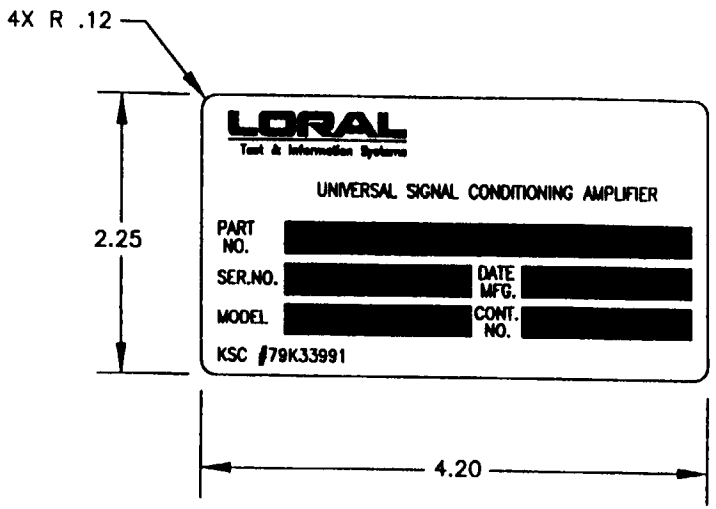
| SIZE | CAGE CODE | DRAWING NO. | REV. |
|---|---|---|---|
| B | 01GD0 | 189-B3263-00 | KA |

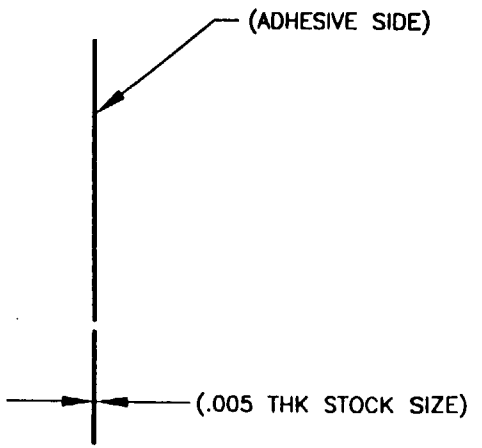
SCALE 1/1 SHEET 1 OF 1



ACAD REV –

| REVISIONS | | | | |
|---|---|---|---|---|
| SYM. | DESCRIPTION | EFFECTIVITY | DATE | APPROVED |
| XA | ECO 11006 UPDATE FOR RELEASE | 5/3/95 | 5/3/95 | |
| XB | ECO 11019 CHANGED MATERIAL THICKNESS | 5/3/95 | 5/3/95 | |




NOTES:
UNLESS OTHERWISE SPECIFIED

1. GRAPHICS ETCHED ON FOTOFOIL PER ARTWORK 905-B3264-10, CHARACTERS AND BLOCKS TO BE SILVER ON MATTE BLACK FIELD (REVERSE OF SHOWN). (CADD DB 898-B3264-00) CONTAINS: ONE SHEET OF LETTERING AT REV A.

2. REAR SURFACE OF LABEL IS TO HAVE PRESSURE SENSITIVE, DRY RELEASE ADHESIVE APPLIED.

SHEET 1 | 166-B3264-00

VENDOR ITEM DRAWING

| -00 | 253-B3262-00 | 4200 |
|---|---|---|
| CONFIG. | NEXT ASSY. NO. | USED ON |

SIMILAR TO

APPLICATION

MATERIAL 1

TREATMENT OR FINISH 2

UNLESS OTHERWISE SPECIFIED
TOLERANCES DECIMALS ANGLES SURFACE FINISH
.XX ± .03 ± 1/2° 125
.XXX ± .010
DIMENSIONS ARE IN INCHES
THREAD CLASS 3A OR 3B PER MIL-S-7742, REMOVE BURRS AND BREAK EDGES .005 MAX. DIMENSIONS INCLUDE APPLIED FINISH.
TOLERANCING STANDARDS APPLY.
DO NOT SCALE DRAWING
DO NOT APPLY PART NO. IDENTIFY PER LORAL STD 3.7 BAG OR TAG

| | | |
|---|---|---|
| DRAWN BY | B.VANDERVLIET | 1/4/95 |
| ENGINEER | B.VANDERVLIET | 1/4/95 |
| CHECKED | R.ZOERNER | 4/28/95 |
| DESIGN MANAGER | D.HART | |
| PROJECT MANAGER | D.BECKER | |
| APPROVED | | |
| APPROVED | Q.A. W.SARNE | |

LORAL Test & Information Systems (M) P.O. Box 3041 Sarasota, FL 34230

LABEL, PRODUCT IDENT, USCA (EDC)

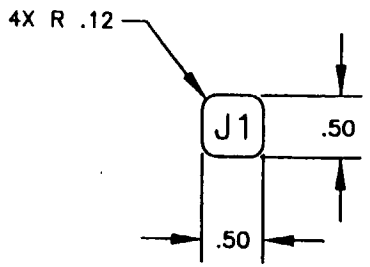
| SIZE | CAGE CODE | DRAWING NO. | REV. |
|---|---|---|---|
| B | 01GD0 | 166-B3264-00 | XB |

SCALE 1/1 SHEET 1 OF 1



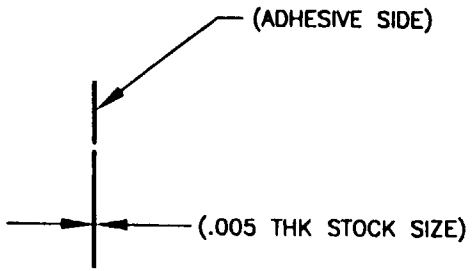
ACAD REV -

| REVISIONS | | | | |
|---|---|---|---|---|
| SYM. | DESCRIPTION | EFFECTIVITY | DATE | APPROVED |
| XA | ECO 11006 UPDATE FOR RELEASE | 5/3/95 | 5/3/95 | |
| XB | ECO 11019 CHANGED MATERIAL THICKNESS | 6/20/95 | 6/20/95 | |




-00 CONFIG.

J2




-01 CONFIG.

NOTES:
UNLESS OTHERWISE SPECIFIED

1. GRAPHICS ETCHED ON FOTOFOIL PER ARTWORK 905-B3265-10, CHARACTERS AND BLOCKS TO BE SILVER ON MATTE BLACK FIELD (REVERSE OF SHOWN). (CADD DB 898-B3265-00) CONTAINS: ONE SHEET OF LETTERING AT REV A.

2. REAR SURFACE OF LABEL IS TO HAVE PRESSURE SENSITIVE, DRY RELEASE ADHESIVE APPLIED.

| CONFIG. | NEXT ASSY. NO. | USED ON |
|---|---|---|
| -01 | 253-B3262-00 | 4200 |
| -00 | 253-B3262-00 | 4200 |

SIMILAR TO

APPLICATION

MATERIAL 1

TREATMENT OR FINISH 2



UNLESS OTHERWISE SPECIFIED
TOLERANCES
DECIMALS ANGLES SURFACE FINISH
.XX = ± .05 ± 1/2° 125
.XXX = ± .010
DIMENSIONS ARE IN INCHES
THREAD CLASS 3A OR 3B PER MIL-S-7742, REGIONS BURRS AND BREAK EDGES .005 MAXIMUM
DIMENSIONS INCLUDE APPLIED FINISH.
WORKMANSHIP STANDARDS APPLY.
DO NOT SCALE DRAWING
DO NOT APPLY PART NO. IDENTIFY PER LORAL STD 3.7 BAG OR TAG

| | | |
|---|---|---|
| DRAWN BY | B.VANDERVLIET | 5/3/95 |
| DESIGNED | B.VANDERVLIET | 5/3/95 |
| CHECKED | R.ZOERNER | 6/20/95 |
| PRODUCT ENGINEER | D.HART | 5/3/95 |
| PROJECT ENGINEER | D.BECKER | 5/3/95 |
| APPROVED | | |
| APPROVED | | |
| APPROVED | W.SARNIE | |

VENDOR ITEM DRAWING

LORAL Test & Information Systems (M) P.O. Box 3041 Sarasota, FL 34230

LABEL, CONN IDENT, USCA (EDD)

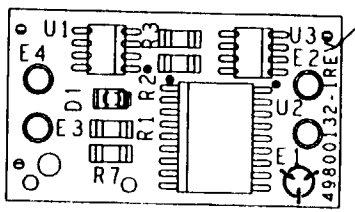
| SIZE | CAGE CODE | DRAWING NO. | REV. |
|---|---|---|---|
| B | 01GD0 | 166-B3265-00 | XB |

SCALE 1/1 SHEET 1 OF 1

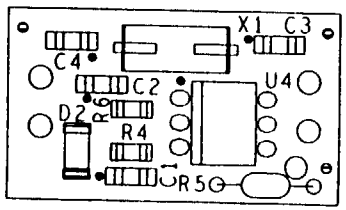
SHEET 1 166-B3265-00

ACAD REV -

| REVISIONS | | | | |
|---|---|---|---|---|
| SYM | DESCRIPTION | APPROVED BY | DATE | APPROVED |
| RA | ECO 11025 RELEASED | | 8-1-05 | 8-1-05 |




TOP SIDE




BOTTOM SIDE

NOTES:

UNLESS OTHERWISE SPECIFIED:

1. MAX ASSY HEIGHT: A TOP SIDE .150
   B BOTTOM SIDE .250
2. DESIGN REF. HEIGHT: N/A
3. ON COMPONENTS OTHER THAN SURFACE MOUNT
   □SQUARE PAD INDICATES PIN 1 (POSITIVE, +) END OF POLARIZED CAPACITORS, PIN 1 (CATHODE) END OF DIODES, AND PIN 1 OF ALL OTHER COMPONENTS WITH MORE THAN 2 LEADS. REFER TO SILKSCREEN IMAGE FOR ANY MECHANICAL ORIENTATION.
4. INFORMATION FOR THIS DRAWING IS CONTAINED IN CADD DATABASE 49800132.
5. USE CAUTION WHEN HANDLING THIS PWA TO PREVENT DAMAGING BY STATIC ELECTRICITY
6. APPLY THE CURRENT ASSEMBLY/PARTS LIST REVISION LETTER APPROX. WHERE SHOWN. THE MARKING SHALL BE:
   1.) A FILM LABEL WITH ACRYLIC PRESSURE SENSITIVE ADHESIVE, OR
   2.) INDELIBLE INK PER MIL-I-43553 IN A CONTRASTING COLOR.

CURRENT ASSY REV LETTER — REV / — CURRENT PL REV LETTER

SEE SEPARATE PARTS LIST

| -1 | FINAL | 4100 |
|---|---|---|



| | |
|---|---|
| DRAWN BY | R. HOANG |
| DESIGNED | R. HOANG |
| ENGINEER | R. TOERNER |
| PROJECT ENGINEER | NICK OSTRYE |
| PROJECT MANAGER | DEAN BECKER |
| QA | W. SARNIE |

LORAL Test & Information Systems
P.O. Box 2004, Sarasota, FL 34230

PWA
4100 TAG RAM

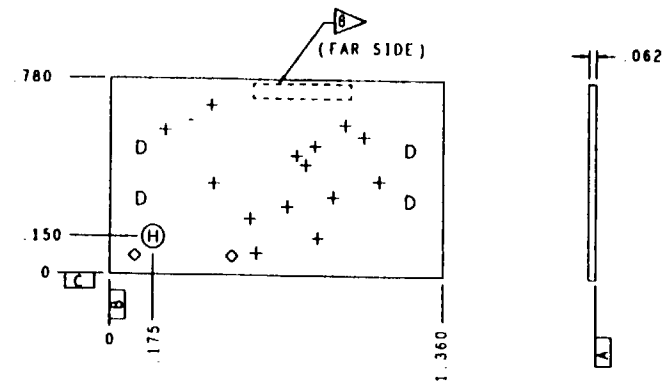
| SIZE | CAGE CODE | DRAWING NO. | REV |
|---|---|---|---|
| D | 01GD0 | 49800132 | XA |
| SCALE | 4/1 | | SHEET 1 OF 1 |

49800132

8 7 6 5 4 3 2 1

| PUNCH | QTY | DESCRIPTION | |
|---|---|---|---|
| ⊥ | 14 | Ø .013 -/- .003 | PLATED THRU |
| ◇ | 7 | Ø .035 -/- .003 | PLATED THRU |
| D | 4 | Ø .063 -/- .003 | PLATED THRU |
| (H) | 1 | Ø .093 -/- .003 | NON PLATED THRU |

| REVISIONS | | | | |
|---|---|---|---|---|
| | DESCRIPTION | PRODUCTION | DATE | APPROVED |
| AA | ECR 11025 RELEASED | 0-1-05 | 0-1-05 | |




NOTES:
UNLESS OTHERWISE SPECIFIED

1. THIS PWB SHALL MEET/EXCEED ALL APPLICABLE IPC STANDARD.
2. ARTWORK 49800133-1 AT REV A
   (CADD DB 49800132) CONSISTS OF:
   2 SHEETS CIRCUITRY AT REV A,
   ONE SHEET SOLDER MASK (TOP SIDE) AT REV A,
   ONE SHEET SOLDER MASK (BOTTOM SIDE) AT REV A,
   ONE SHEET SILKSCREEN (TOP SIDE) AT REV A,
   ONE SHEET SILKSCREEN (BOTTOM SIDE) AT REV A,
   ONE SHEET PASTE MASK (TOP SIDE) AT REV A,
   ONE SHEET PASTE MASK (BOTTOM SIDE) AT REV A,
   AND ONE DRILL FILE AT REV A
3. USE RAW MATERIAL LAMINATE .062, 1/2OZ CU 2 SIDE PER MIL-P-13949 GFN-0620-CH/CH-A2C
4. ELECTROPLATE .001 IN COPPER MINIMUM
5. APPLY DRY FILM OR LIQUID PHOTO IMAGEABLE SOLDER MASK WITH GLOSS GREEN FINISH OVER BARE COPPER PER IPC-SM-840 CLASS 3. LEAVE COMPONENT PADS CLEAR OF SOLDER MASK MAINTAINING .005 MAX / .001 MIN CLEARANCE.
6. APPLY TIN/LEAD COATING (63/37) PER MIL-P-55110. COATING MUST BE MELTED ALLOY.
7. LETTER TOP & BOTTOM SIDES OF PWB USING MASTER PATTERN ARTWORK AND INK PER MIL-I-43553, COLOR YELLOW NO. 13655 PER FED-STD-595
8. APPLY THE CURRENT PWB DRAWING REVISION LETTER APPROX. WHERE SHOWN. THE MARKING SHALL BE ONE OF THE FOLLOWING:
   1.) ETCHED IN ARTWORK
   2.) A FILM LABEL WITH ACRYLIC PRESSURE SENSITIVE ADHESIVE
   3.) INDELIBLE INK PER MIL-I-43553 IN A CONTRASTING COLOR
   49800133-1REV___ — CURRENT PWB DRAWING REV LETTER
9. HOLE LOCATIONS AND SIZES ARE PER DRILL FILE. LOCATIONAL DIMENSIONS ARE BASIC AND TOLERANCE IS:

| | | | | |
|---|---|---|---|---|
| ⌖ | Ø .020 Ⓜ | A | B | C |
| | Ø .007 Ⓜ | A | | |

10. SERIALIZED QUALITY ASSURANCE TEST COUPONS PER MIL-STD-275 SHALL BE SUPPLIED (ONE SET PER PANEL) WITH EACH SET OF PWBS FABRICATED. EXAMPLES OF THE SMALLEST HOLE AND PAD SIZE SHALL BE INCLUDED.

VENDOR ITEM DRAWING

| | | | |
|---|---|---|---|
| -1 | 49800132-1 | 4100 | |

R. HOANG — R. HOANG

LORAL
Test & Information Systems

PWB
4100 TAG RAM

| SIZE | CAGE CODE | DRAWING NO | REV |
|---|---|---|---|
| D | 01GDO | 49800133-1 | XA |

SCALE 4/1 — SHEET 1 OF 1

49800133-1

| COMPONENT CHART | |
|---|---|
| LAST NO. USED | UNUSED NUMBER |
| C4 | |
| C3 | |
| R4 | |
| R7 | |
| C14 | |
| C4 | |
| Y1 | |

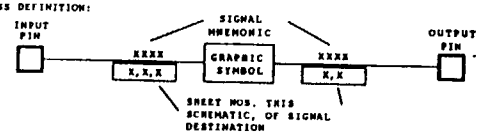
| REVISIONS | | | | |
|---|---|---|---|---|
| SYM. | DESCRIPTION | EFFECTIVITY | DATE | APPROVED |
| XA | ECR 11025 RELEASED | 8/1/95 | 8/1/95 | |

SHEET 1

49800134-1

5. INFORMATION FOR THIS DRAWING IS CONTAINED IN CADD DATABASE 49800132.

4. ADDRESS DEFINITION:




3. CIRCUIT RETURN SYMBOLS:


2. FOR TOLERANCES AND RATINGS SEE PARTS LIST.

1. RESISTOR VALUES ARE IN OHMS, CAPACITOR VALUES ARE IN MICROFARADS.

UNLESS OTHERWISE SPECIFIED:
NOTES:

CONCEPT DEV -

| | | | |
|---|---|---|---|
| | -1 | 49800132-1 | 4100 |
| SIMILAR TO | CONFIG. | NEXT ASSY. NO. | USED ON |
| | APPLICATION | | |



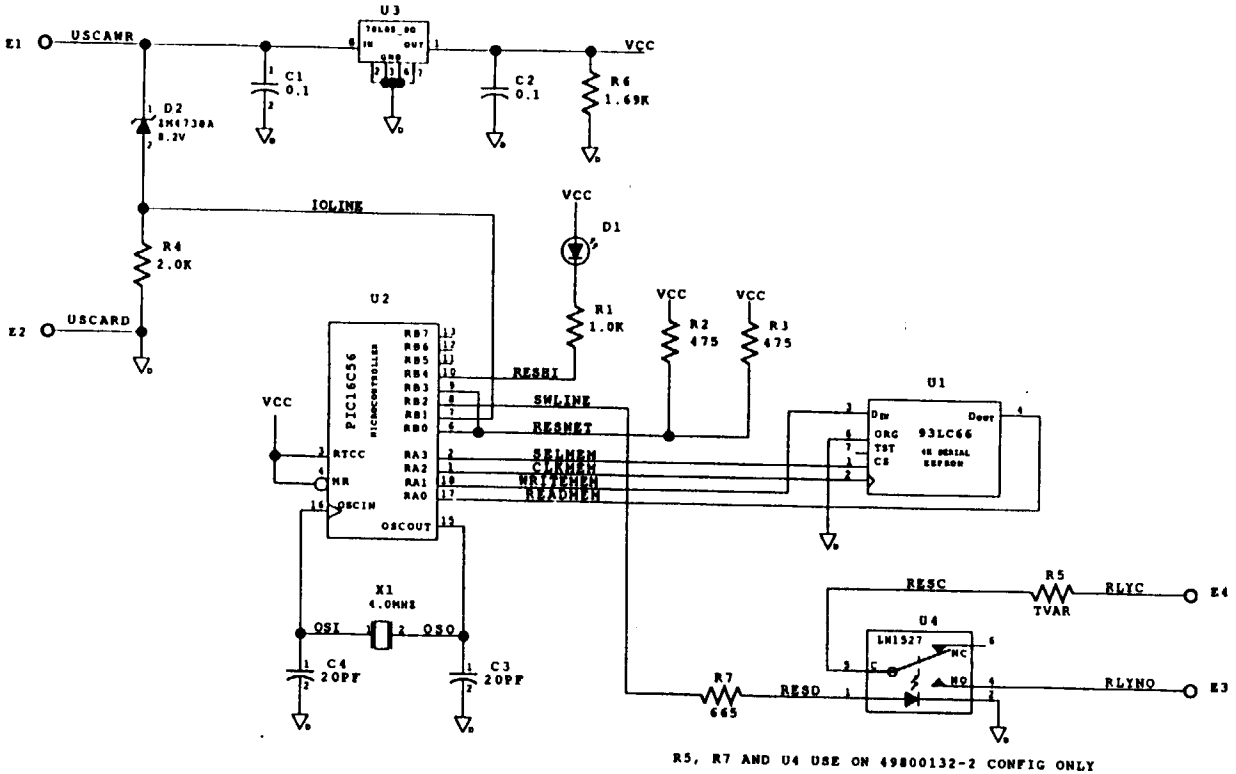
| | | |
|---|---|---|
| DRAWN BY | NICK OSTRYE | 8/1/95 |
| DESIGNED | - | - |
| CHECKED | - K Boerma | 8/1/95 |
| DESIGN ENGINEER | - NCB | |
| PROJECT ENGINEER | DEAN BECKER | 8/95 |
| APPROVED | - | |
| APPROVED | - | |
| APPROVED | - W/O | |

LORAL
TEST & INFORMATION SYSTEMS
P.O. Box 3041
Sarasota, FL 34230

# SCHEMATIC, PWA
# 4100 TAG RAM

| SIZE | CAGE CODE | DRAWING NO. | REV. |
|---|---|---|---|
| B | 01GD0 | 49800134-1 | XA |
| SCALE NONE | | SHEET 1 OF 2 | |

DRAWING 49800134 49800134 LAST_MODIFIED=Tue Aug 1 17:45:48 1995




R5, R7 AND U4 USE ON 49800132-2 CONFIG ONLY

POWER AND GROUND

LORAL
TEST & INFORMATION SYSTEMS
P.O. Box 3041
Sarasota, FL 34230

SCHEMATIC, PWA
4100 TAG RAM

| SIZE | CAGE CODE | DRAWING NO. | REV. |
|---|---|---|---|
| B | 01GD0 | 49800134-1 | XA |
| SCALE NONE | | SHEET 2 | |

SHEET 2

49800134-1

CONCEPT REV -

DRAWING 49800134 49800134 LAST_MODIFIED=Wed Aug 2 08:38:21 1995

LORAL
Test & Information Systems

P.O. Box 3041
Sarasota, FL 34230
(941) 371-0811
Fax: (941) 378-1893

September 28, 1995

Brevard Community College
Center of Community Innovation
250 Grassland Rd S.E.
Palm Bay, FL 32909

Attention: Mr. Jarad Whitcomb

**Subject:** **BCC PO #433, TRDA #405; USCA Milestone #5**

Enclosure:
(1) LTIS Product Sheet
(2) LTIS Customer Newsletter
(3) LTIS Condensed Catalog

Dear Mr. Whitcomb:

Milestone #5 to the subject contract which states "Complete final design package for Loral Commercial Version of USCA. This Loral Commercial Version of USCA will be a Loral Standard Component and will be available as a procured item" has been completed. The following activities have been completed in support of Milestone #5:

- LTIS has prepared and is distributing a USCA product sheet (enclosed) to customers.
- LTIS featured the cooperative development of the USCA with TRDA and NASA in a quarterly newsletter (enclosed) distributed to customers.
- LTIS has added USCA equipment to the Condensed Product Catalog (enclosed).
- LTIS has delivered 1650 Tag Ram assemblies to NASA to be used as part of USCA systems.
- LTIS is proposing the USCA products and enhancements to non-NASA customers in competetive procurements.

Our invoice for this milestone will be submitted under separate cover.

If you have any other questions regarding this matter, please do not hesitate to contact me at 813-377-5538, or by fax at 813-378-6905

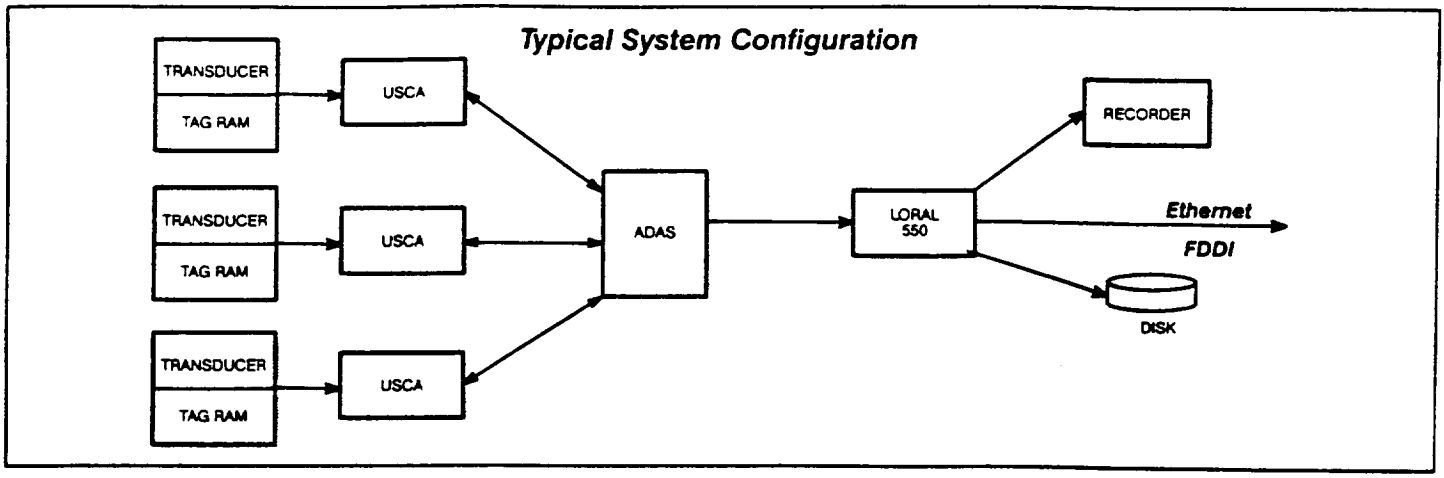
Very truly yours,

**LORAL TEST & INFORMATION SYSTEMS**

Stephen G. Carroll
Manager, Contracts

cc: Matt LaVigne, TRDA

# Universal Signal Conditioning Amplifier *Model 4200*




# *Specifications*

## INPUTS

| | |
|---|---|
| Voltage | −40V to +40V |
| Current | −25mA to +25mA |
| Frequency | 0−10 KHz |

## OUTPUTS

| | |
|---|---|
| Analog Ranges | 0.1% accuracy<br>0 to +5 VDC<br>0 to 10 VDC<br>−5 to 5 VDC<br>−10 to 10 VDC |
| Digital | .02% accuracy |
| Serial Link | 16-bit Words<br>Programmable Output |

## SIGNAL CONDITIONING

| | |
|---|---|
| Accuracy | .02% of full scale (digital output) |
| Gain Range | 0.25 to 2000 |
| Sample Rate | 20 KHz |
| Digital Filter Range | 8 programmable filters (127 tap FIR) |
| Bridge Completion | 1 arm |
| Excitation Voltage | 0 to 27 VDC |
| Excitation Current (internal) | 0 to 30mA |
| Excitation Current (external) | 0 to 250mA |

## PROGRAMMABLE FUNCTIONS

Read Tag ID/Data
Calibration Mode
Change Parameter
- Gain
- Filter
- Excitation Configuration
- Excitation Levels
- Output Range

Read Parameter
Perform Self-Test
Reset
Download Custom Filter Coefficients
Download Linearization Coefficients

## POWER REQUIREMENTS

| | |
|---|---|
| Voltage | 24 to 32 VDC |
| Current | 500mA Max (450 mA typical) |
| Overvoltage | 32 VDC |

## ENVIRONMENTAL CONDITIONS *(Rugged Version)*

| | |
|---|---|
| Temperature | Full accuracy |
| Operating | −25 to 60°C |
| Storage | −40 to 60°C |
| EMI | MIL-STD-561B, Class 1D |
| Vibration | |
| Sine | 10g, 50 to 5000 Hz |
| Random | 20g RMS, 20 to 2000 Hz |
| Shock | MIL-STD-810, Procedure IV |
| Humidity | 1 to 98% non-condensing |
| Resistant to fungus, salt fog, sand, and dust | |

## USCA COMPATIBILITY

*Compatible with many transducers, including:*
Platinum Resistance Temperature
Flow Measurement
Discrete Valve Position Indication
Pressure
Thermocouples with Reference Junction
Low-Level Thermocouples
Discrete Liquid Sensors
Displacement (linear and accelerometer)
Pressure, Current Output
Precision Temperature Bulb
Load Cell
Vapor Detector . . . and many more!


LORAL
Test & Information Systems

15378 Avenue of Science
San Diego, CA 92128-3407
(619) 674-5100 (800) 351-8483
Fax (619) 674-5145

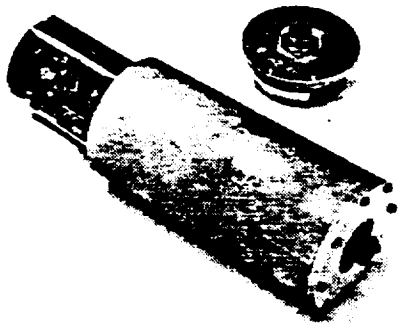
P.O. Box 3041
Sarasota, FL 34230
(813) 371-0811
Fax (813) 378-1893

7 Buckingham Avenue
Slough, Berkshire SL1 4PN, UK
(44) 753-696488
Fax (44) 753-696218

LORAL
Test & Information Systems

## *Series 4000*

# Universal Signal Conditioning Amplifier *Model 4200*

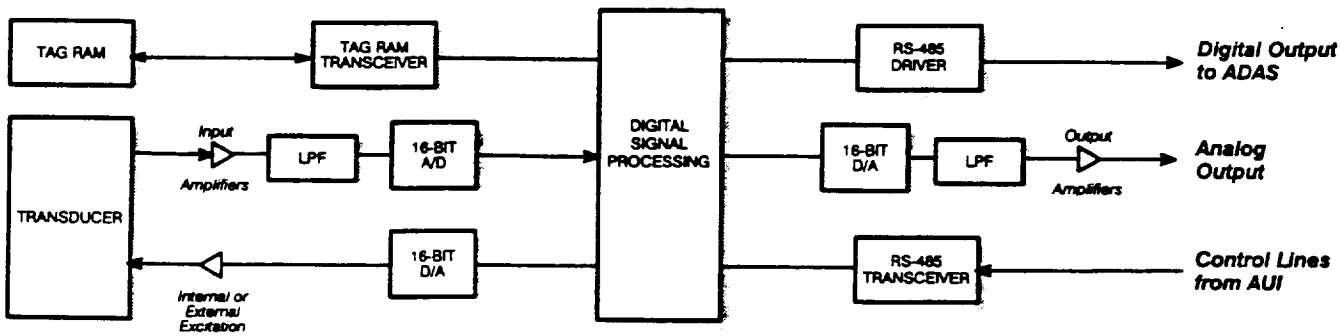


*The Universal Signal Conditioning Amplifier (USCA) functions as a self or remotely programmable Signal Conditioning Amplifier that automatically operates with most types of transducers. The USCA provides transducer excitation, performs filtering using an internal DSP, and provides both analog and digital outputs with better than .024% accuracy. The unit significantly lowers maintenance and operations costs with its Self-Startup, Self-Calibration, and Self-Test capabilities.*

## FEATURES / BENEFITS

- **Self-Configuring**
  - *Provides automatic Offset, Gain, and Excitation values based on transducer information on Tag RAM*
- **Digital Filtering**
  - *Comes with seven standard filters and one custom downloadable filter*
- **Digital Linearization**
  - *Up to 8th order*
- **Analog or Digital Output**
  - *Supports analog or digital multiplexing*
- **Channel to Channel Electrical Isolation**
  - *Galvanically isolates digital and analog outputs from the input circuitry*
- **Remotely Programmable**
  - *Can check and modify configuration, and order self-test*
- **High Resolution and Accuracy**
  - *16-bit A/D with 12-bit or better accuracy*
- **Controlled sampling**
  - *Synchronous or asynchronous sampling*
- **Self-Calibration**
  - *Provides constant gain measurements and correction factors during operation*
- **Automatic Drift Compensation**
  - *Provides Low Drift and High Accuracy operations*
- **Self-Test**
  - *Provides a complete unit test upon command*
- **Reduced Operations and Maintenance**
  - *Minimizes setup and test times with Self-Configuration, Self-Test, and Digital Control capabilities*

***USCA Block Diagram***



LORAL
Test & Information Systems

PO Box 3041
Sarasota, FL 34230
(941) 371-0811
Fax: (941) 378-1893

September 28, 1995

Brevard Community College
Center of Community Innovation
250 Grassland Rd S.E.
Palm Bay, FL 32909

Attention: Mr. Jarad Whitcomb

**Subject: BCC PO #610, TRDA #410; ADAS Milestone #2**

Enclosure: (1) Schematic of Input Card Design
(2) Parts List

Dear Mr. Whitcomb:

Milestone #2 to the subject contract which states "Complete the CAD Schematic Design of the Input Card" has been completed. The Input Card Design Schematics and Parts List are enclosed. Our invoice for this milestone will be submitted under separate cover.

If you have any other questions regarding this matter, please do not hesitate to contact me at 813-377-5538, or by fax at 813-378-6905

Very truly yours,

LORAL TEST & INFORMATION SYSTEMS

Stephen G. Carroll
Manager, Contracts

cc: Matt LaVigne, TRDA

| COMPONENT CHART | |
|---|---|
| LAST NO. USED | UNUSED NUMBER |
| C136 | |
| D84 | |
| E | |
| J4 | |
| L | |
| P3 | |
| Q | |
| R74 | |
| S2 | |
| T | |
| TP86 | |
| U84 | |

| UNUSED CIRCUITS | | |
|---|---|---|
| REF DES | TYPE | CIRCUITS |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |

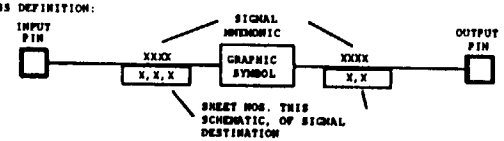
| REVISIONS | | | | |
|---|---|---|---|---|
| SYM. | DESCRIPTION | EFFECTIVITY | DATE | APPROVED |
| - | - | - | - | - |

SHEET 1

49800128-1

5. INFORMATION FOR THIS DRAWING IS CONTAINED IN CADD DATABASE 899-49800117.

4. ADDRESS DEFINITION:




3. CIRCUIT RETURN SYMBOLS:


2. FOR TOLERANCES AND RATINGS SEE PARTS LIST.

1. RESISTOR VALUES ARE IN OHMS, CAPACITOR VALUES ARE IN MICROFARADS.

UNLESS OTHERWISE SPECIFIED:
NOTES:

DRAWING

TITLE=49800128

ABBREV=49800128

LAST_MODIFIED=Wed Sep 27 18:41:53 1995

| | | | | |
|---|---|---|---|---|
| | -1 | 49800126-1 | 550 | |
| | CONFIG. | NEXT ASSY. ID. | USED ON | |
| SIMILAR TO | APPLICATION | | | |



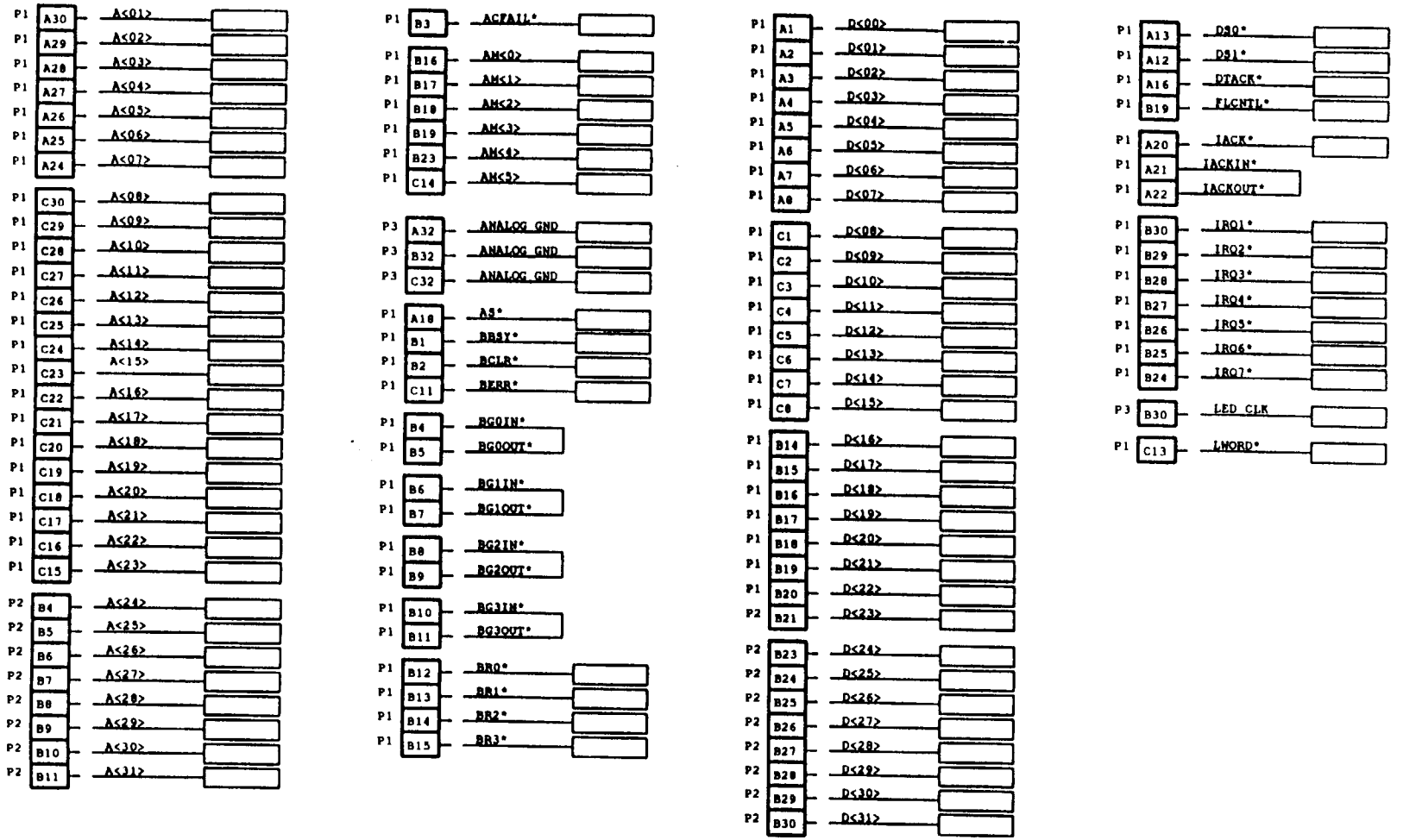
| | | |
|---|---|---|
| DRAWN BY | N. OSTRYE | DATE 8/95 |
| DESIGNER | - | 8/95 |
| CHECKED | R.ZOERNER | 8/29/95 |
| DESIGN ENGINEER | C. INLEFELD | |
| PROJECT ENGINEER | D. BECKER | 8/29/95 |
| APPROVED | - | APPROVED - |
| APPROVED | - | Q.A. W.SARNIE |

LORAL
TEST & INFORMATION SYSTEMS
P.O. Box 3041
Sarasota, FL 34230

# SCHEMATIC, PWA
## AUI

| SIZE | CAGE CODE | DRAWING NO. | REV |
|---|---|---|---|
| B | 01GD0 | 49800128-1 | XA |
| SCALE NONE | | SHEET 1 OF 30 | |

CONCEPT REV -




VME PIN SIGNAL NAMES FROM A TO L

SHEET 2

49800128-1

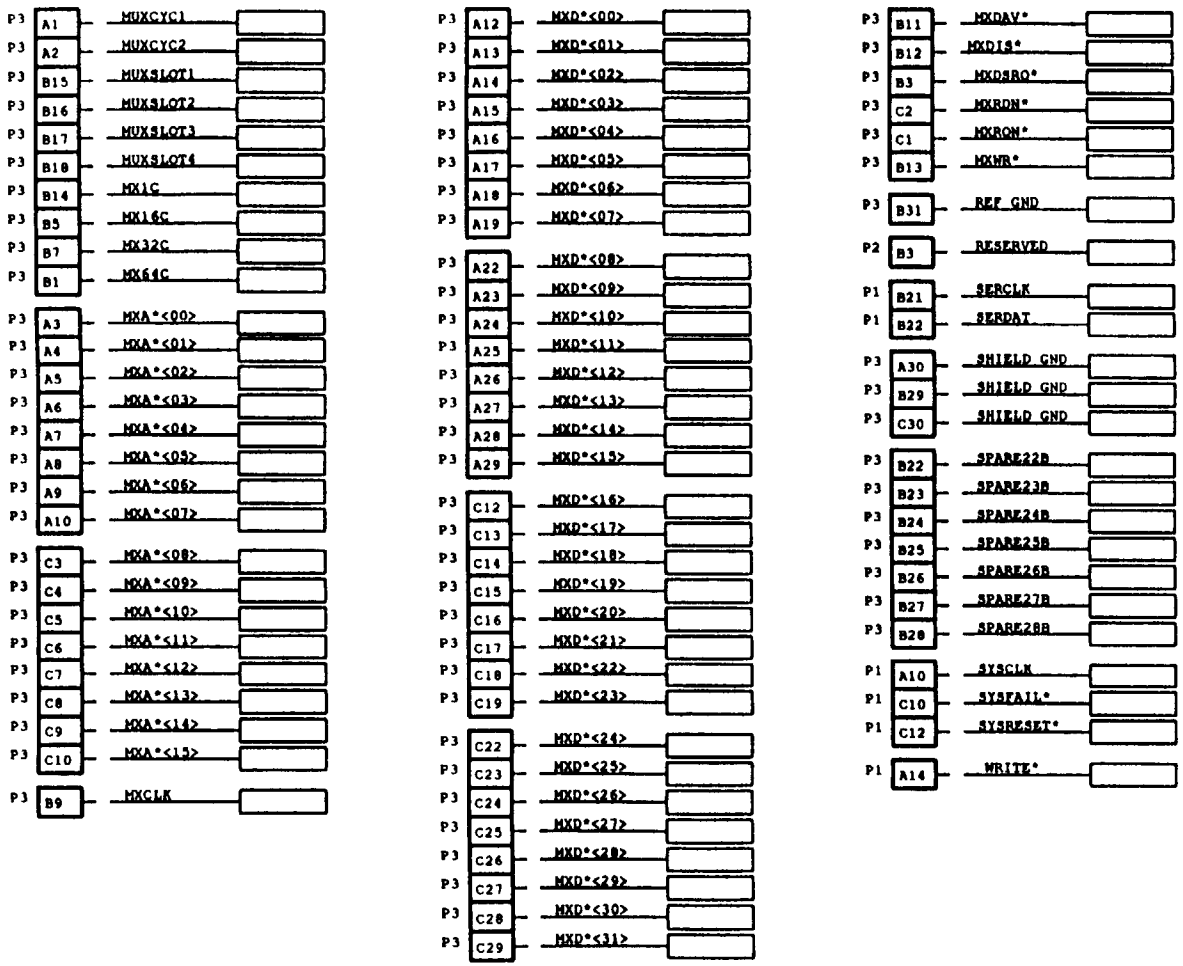
LORAL TEST & INFORMATION SYSTEMS
P.O. Box 3041 Sarasota, FL 34230

SCHEMATIC, PWA
AUI

| SIZE | CAGE CODE | DRAWING NO. | REV. |
|---|---|---|---|
| B | 01GD0 | 49800128-1 | XA |
| SCALE NONE | | SHEET 2 | |

CONCEPT REV -

DRAWING TITLE=49800128 ABBREV=49800128 LAST_MODIFIED=Thu Sep 21 15:34:18 1995




SHEET 3

49800128-1

VME PIN SIGNAL NAMES FROM M TO Z

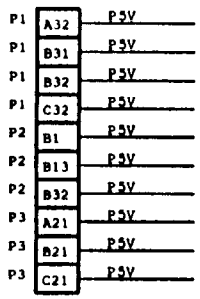
LORAL
TEST & INFORMATION SYSTEMS
P.O. Box 1041
Sarasota, FL 34230

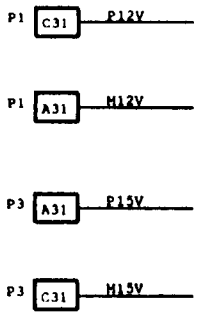
SCHEMATIC, PWA
AUI

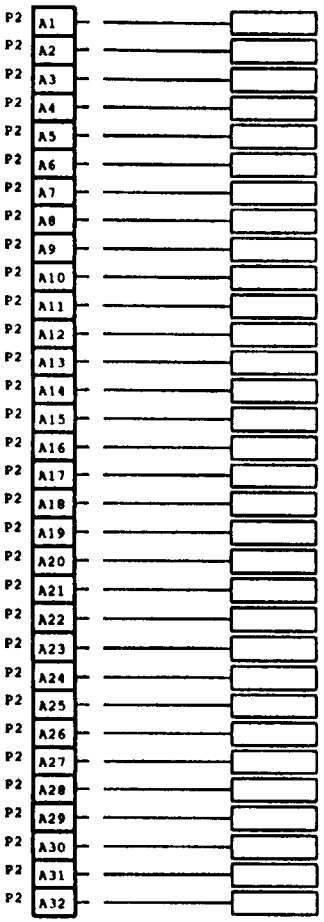
| SIZE | CAGE CODE | DRAWING NO. | REV |
|---|---|---|---|
| B | 01GD0 | 49800128-1 | XA |
| SCALE NONE | | SHEET 3 | |

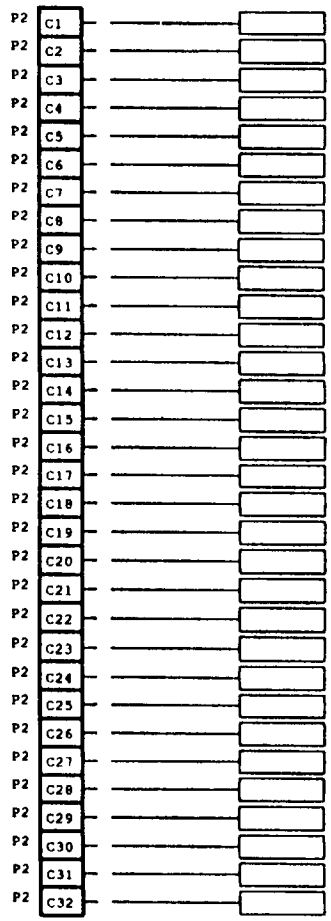
CONCEPT REV -

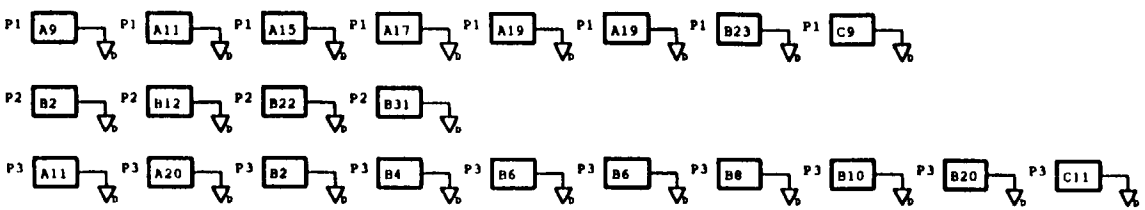
DRAWING TITLE=49800128 ABBREV=49800128 LAST_MODIFIED=Thu Sep 21 12:41:50 1995




VME PINS POWER AND GND
VME USER DEFINED PINS

LORAL
TEST & INFORMATION SYSTEMS
P.O. Box 3041
Sarasota, FL 34230

SCHEMATIC, PWA
AUI

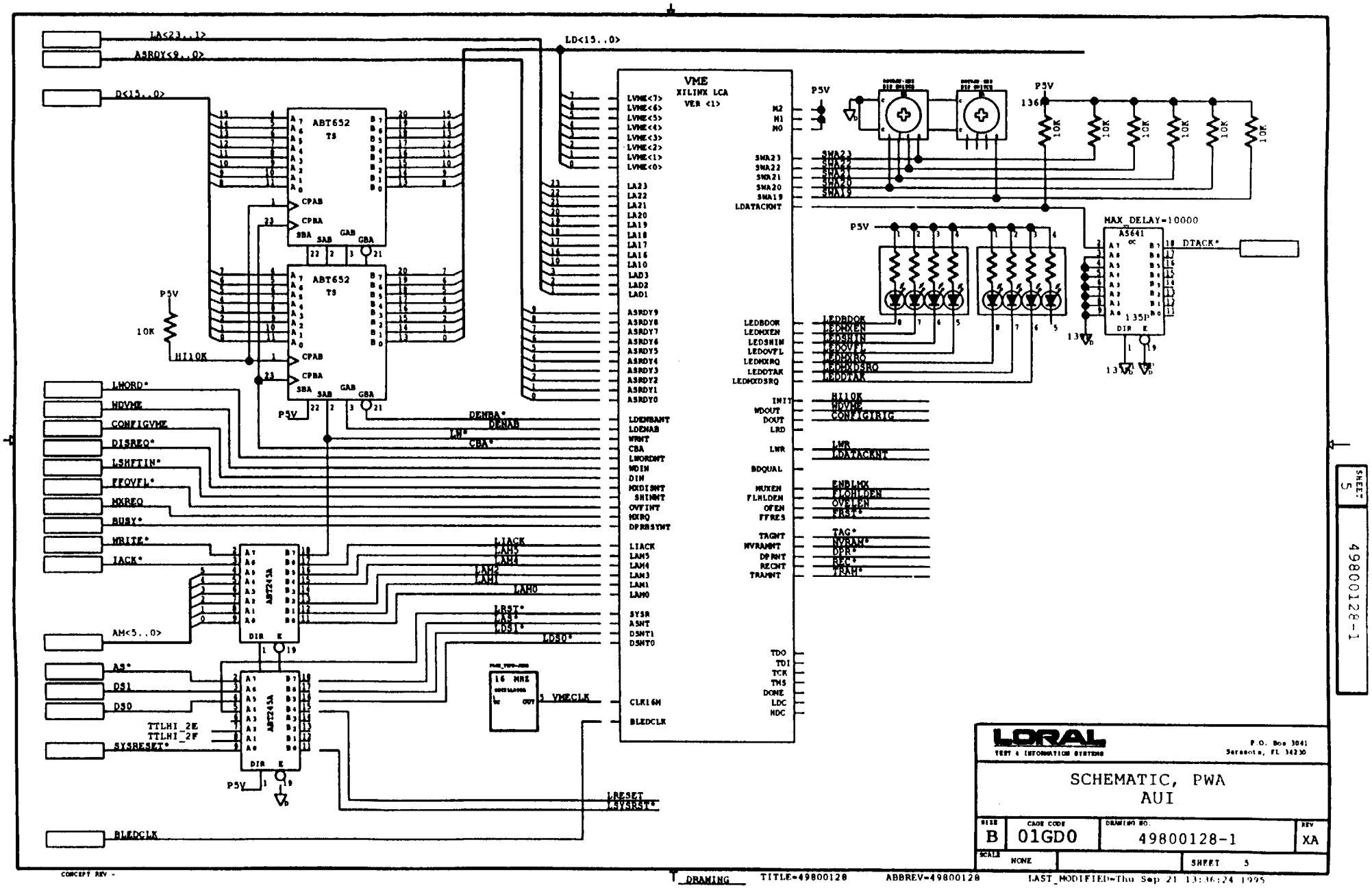
| SIZE | CAGE CODE | DRAWING NO. | REV. |
|---|---|---|---|
| B | 01GD0 | 49800128-1 | XA |
| SCALE NONE | | SHEET 4 | |

SHEET 4

49800128-1

CONCEPT REV -

DRAWING TITLE=49800128 ABBREV=49800128 LAST_MODIFIED=Thu Sep 21 12:38:35 1995




LORAL
TEST & INFORMATION SYSTEMS
P.O. Box 3041
Sarasota, FL 34230

SCHEMATIC, PWA
AUI

| SIZE | CAGE CODE | DRAWING NO. | REV |
|---|---|---|---|
| B | 01GD0 | 49800128-1 | XA |

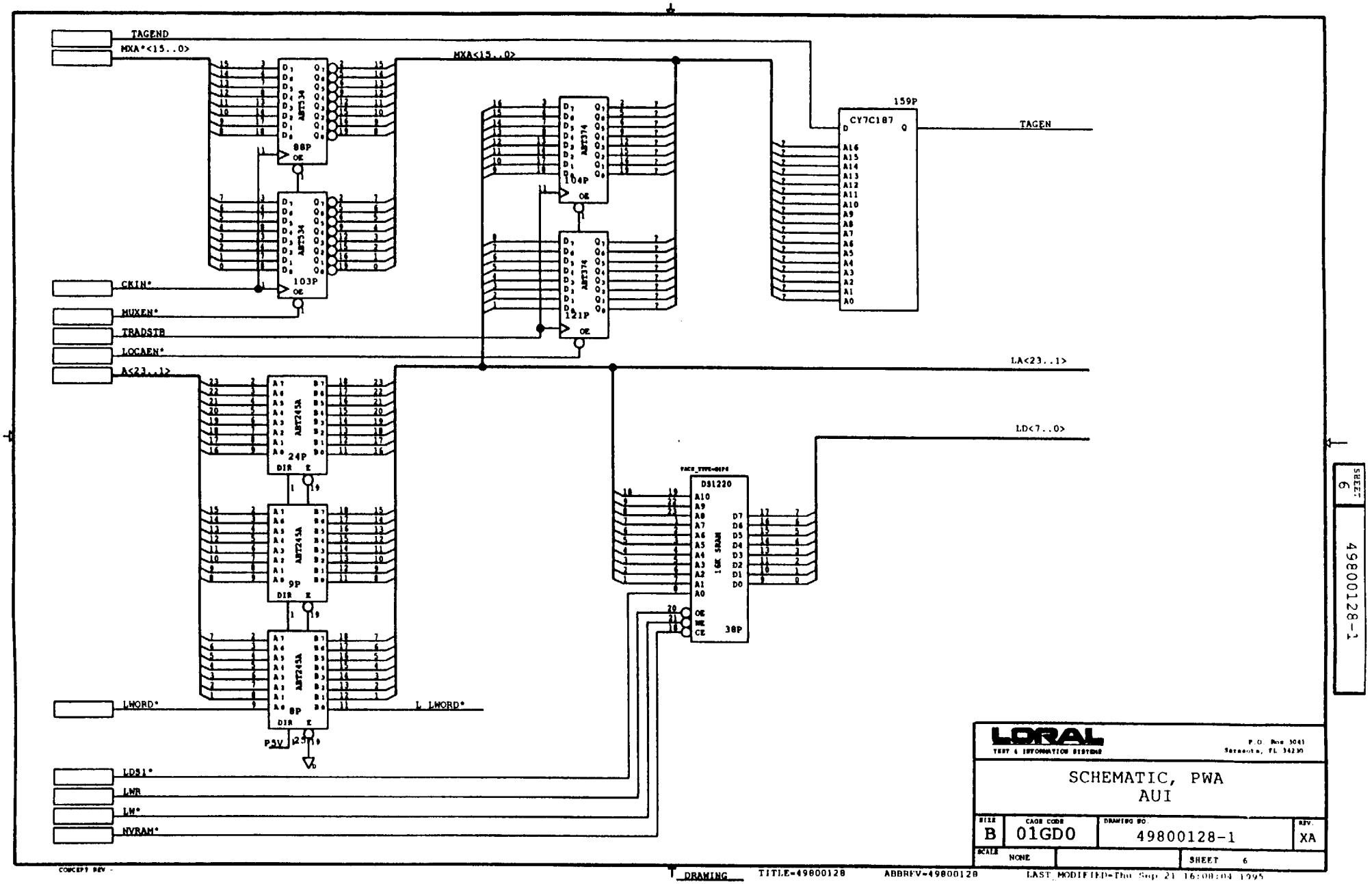
SCALE NONE | SHEET 5

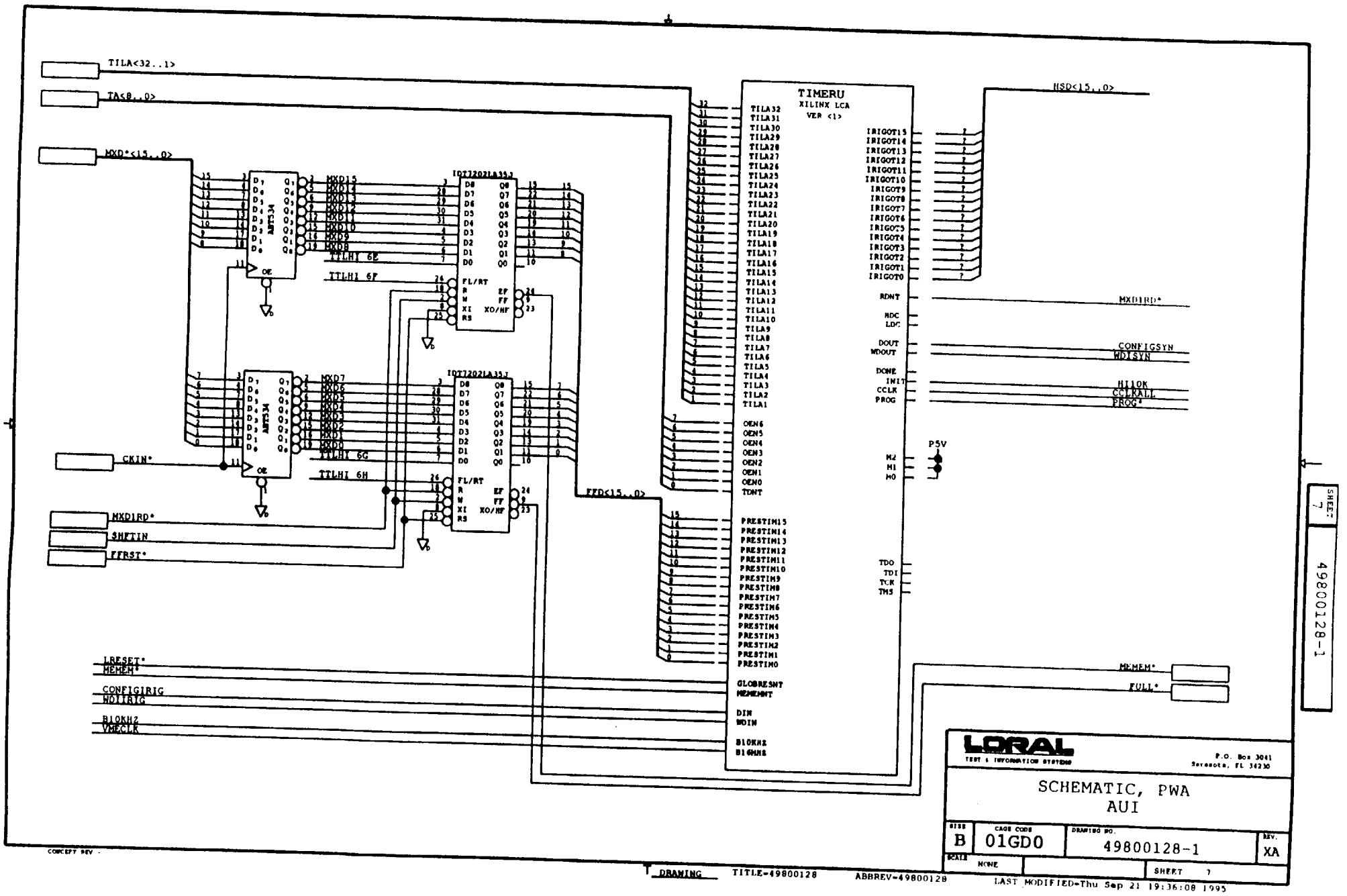
SHEET 5

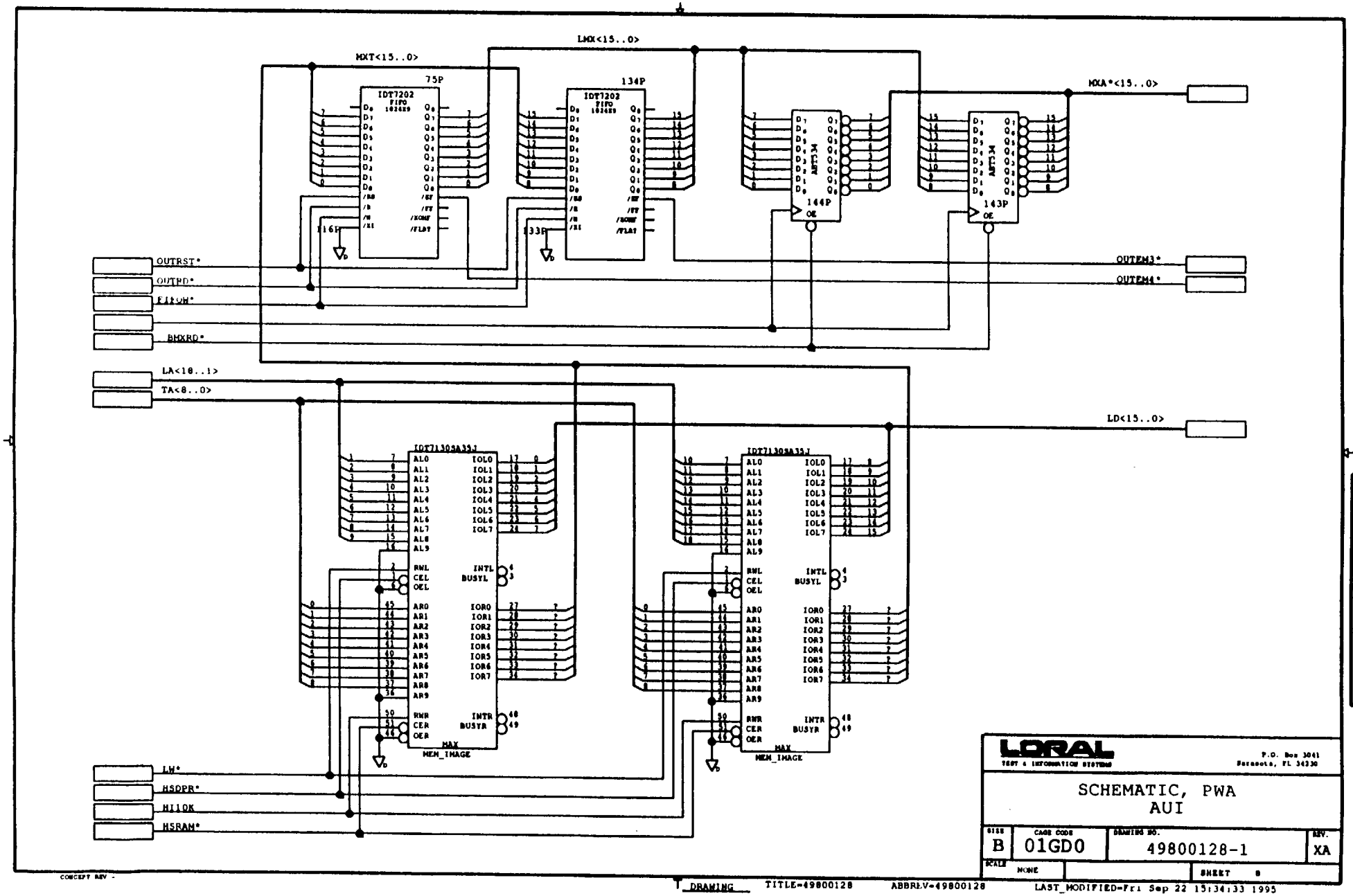
49800128-1

CONCEPT REV -

DRAWING TITLE=49800128 ABBREV=49800128 LAST_MODIFIED=Thu Sep 21 13:36:24 1995


TAGEND
MXA*<15..0>
MXA<15..0>
88P
104P
103P
121P
159P
CY7C187
TAGEN
CKIN*
MUXEN*
TRADSTB
LOCAEN*
AS<23..1>
LA<23..1>
LD<7..0>
24P
9P
8P
DIR
DS1220
16K SRAM
30P
LWORD*
L_LWORD*
PSV
LDS1*
LWR
LW*
NVRAM*
LORAL
TEST & INFORMATION SYSTEMS
SCHEMATIC, PWA
AUI
SIZE
B
CAGE CODE
01GD0
DRAWING NO.
49800128-1
REV.
XA
SCALE
NONE
SHEET 6
SHEET 6
49800128-1
DRAWING TITLE=49800128 ABBREV=49800128


TILA<32..1>
TA<8..0>
MXD*<15..0>
CKIN*
MXD1RD*
SHFTIN
FFRST*
TTLHI 6E
TTLHI 6F
TTLHI 6G
TTLHI 6H
IDT7202LA35J
AM534
TIMERU
XILINX LCA
VER <1>
FFD<15..0>
HSD<15..0>
P5V
LRESET*
MEMEM*
CONFIGIRIG
WDIIRIG
BLOKH2
VMECLK
MEMEM*
FULL*
CONFIGSYN
WDISYN
HI10K
CCLKALL
PROG*
LORAL
TEST & INFORMATION SYSTEMS
P.O. Box 3041
Sarasota, FL 34230
SCHEMATIC, PWA
AUI
SIZE
B
CAGE CODE
01GD0
DRAWING NO.
49800128-1
REV.
XA
SCALE
NONE
SHEET 7
SHEET 7
49800128-1
CONCEPT REV -
DRAWING TITLE=49800128 ABBREV=49800128
LAST MODIFIED=Thu Sep 21 19:36:08 1995




LORAL
TEST & INFORMATION SYSTEMS
P.O. Box 3041
Sarasota, FL 34230

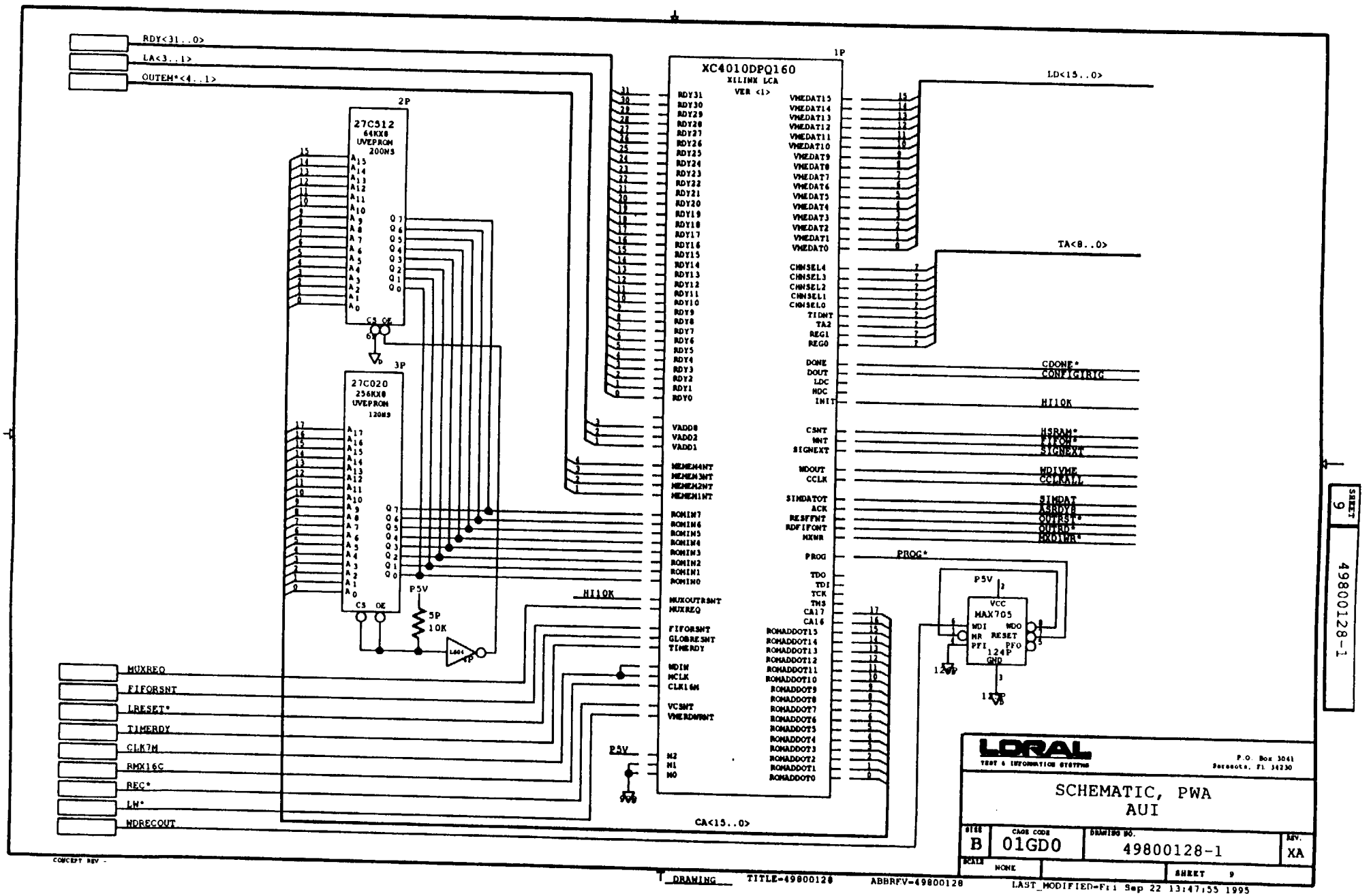
SCHEMATIC, PWA
AUI

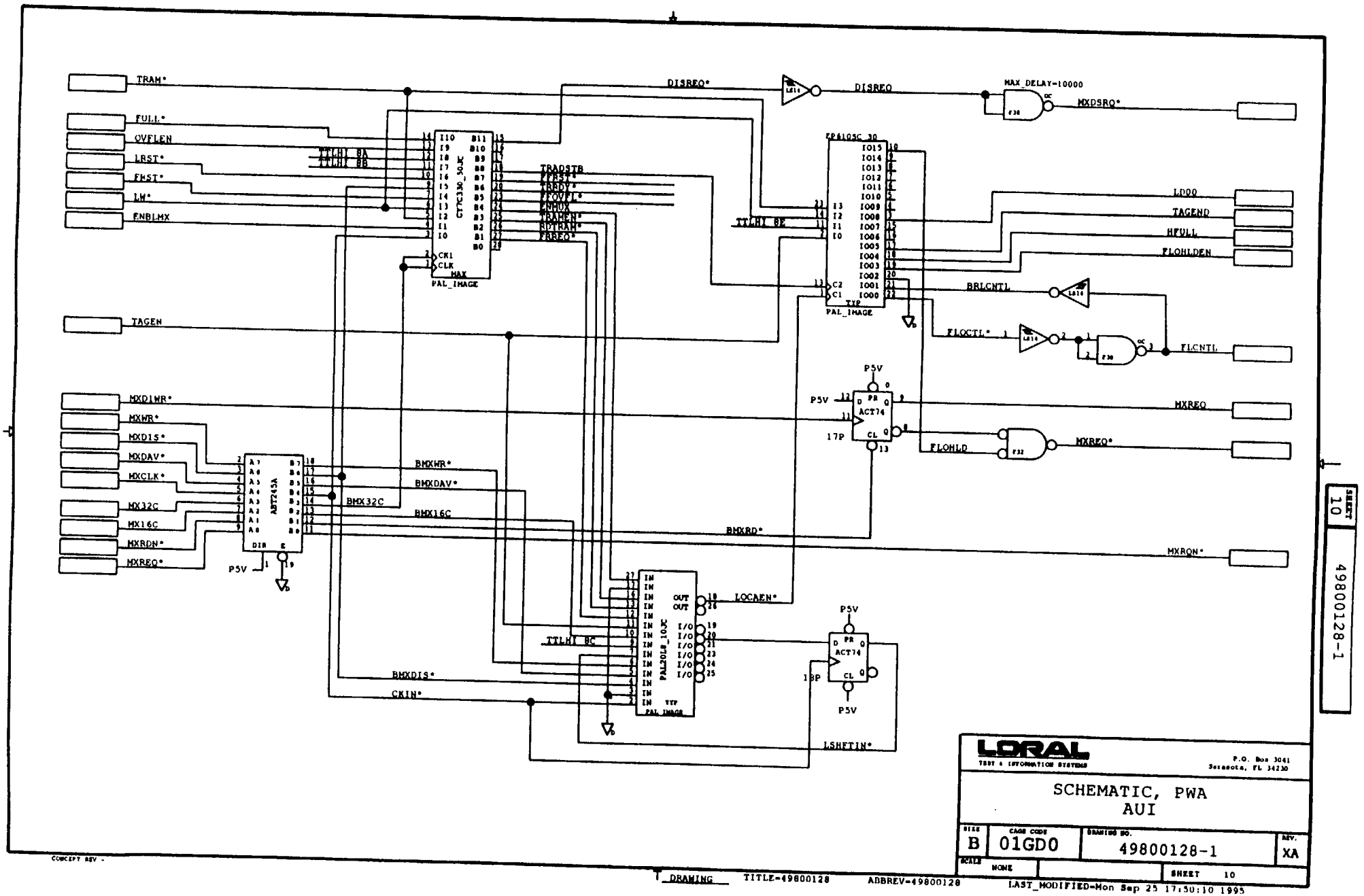
| SIZE | CAGE CODE | DRAWING NO. | REV. |
|---|---|---|---|
| B | 01GD0 | 49800128-1 | XA |
| SCALE NONE | | SHEET 8 | |

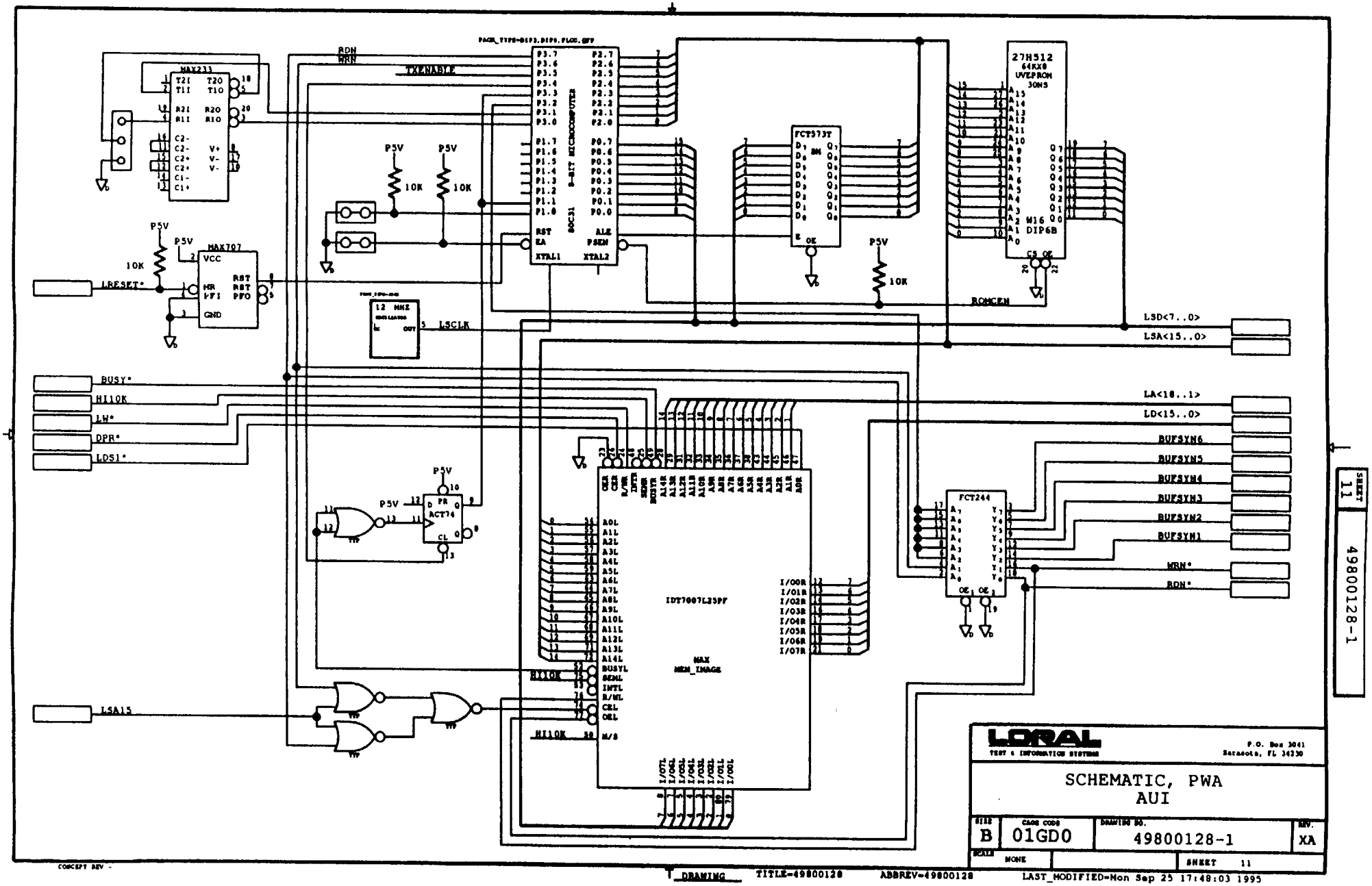
SHEET 8
49800128-1

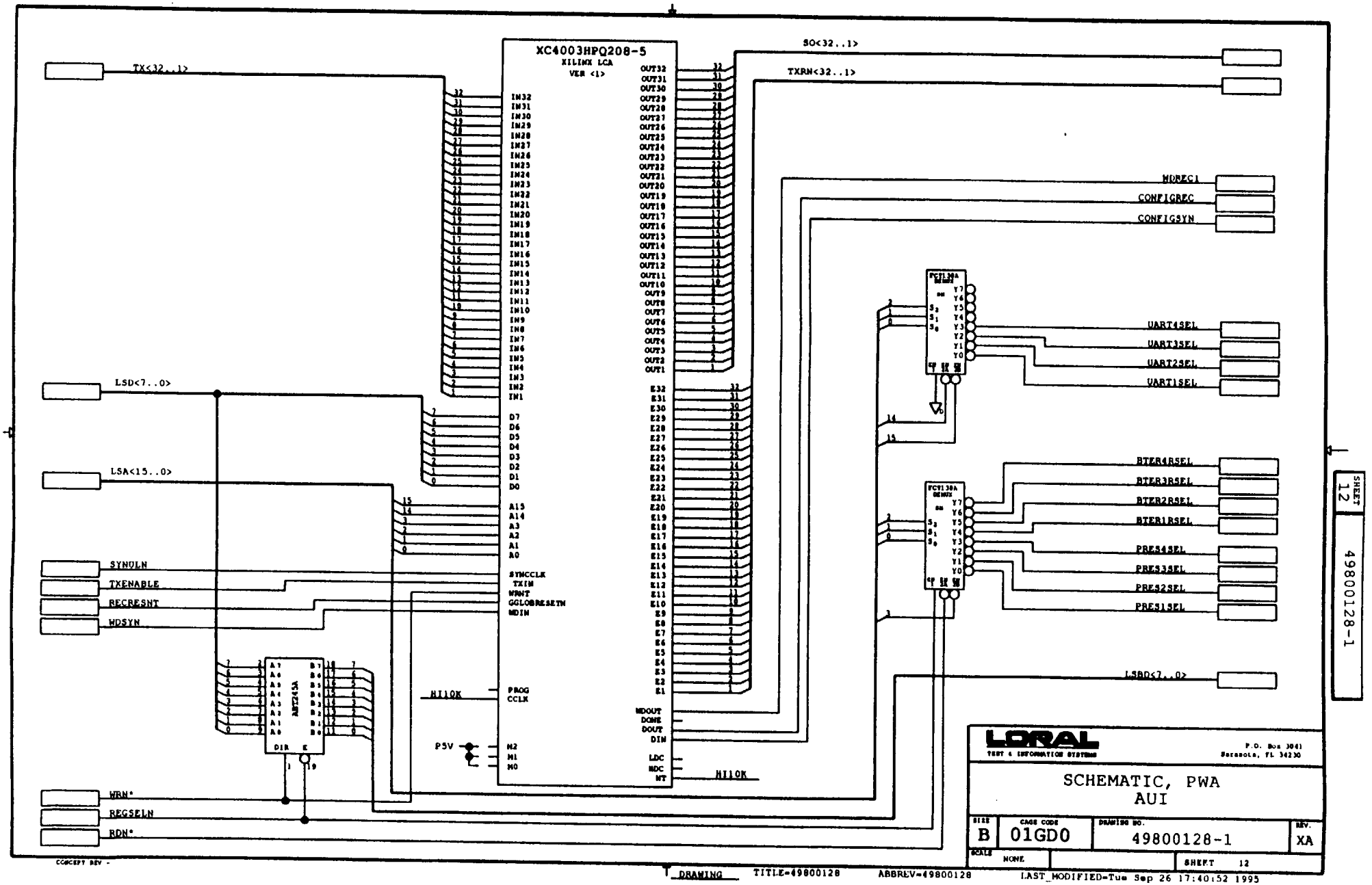
CONCEPT REV -

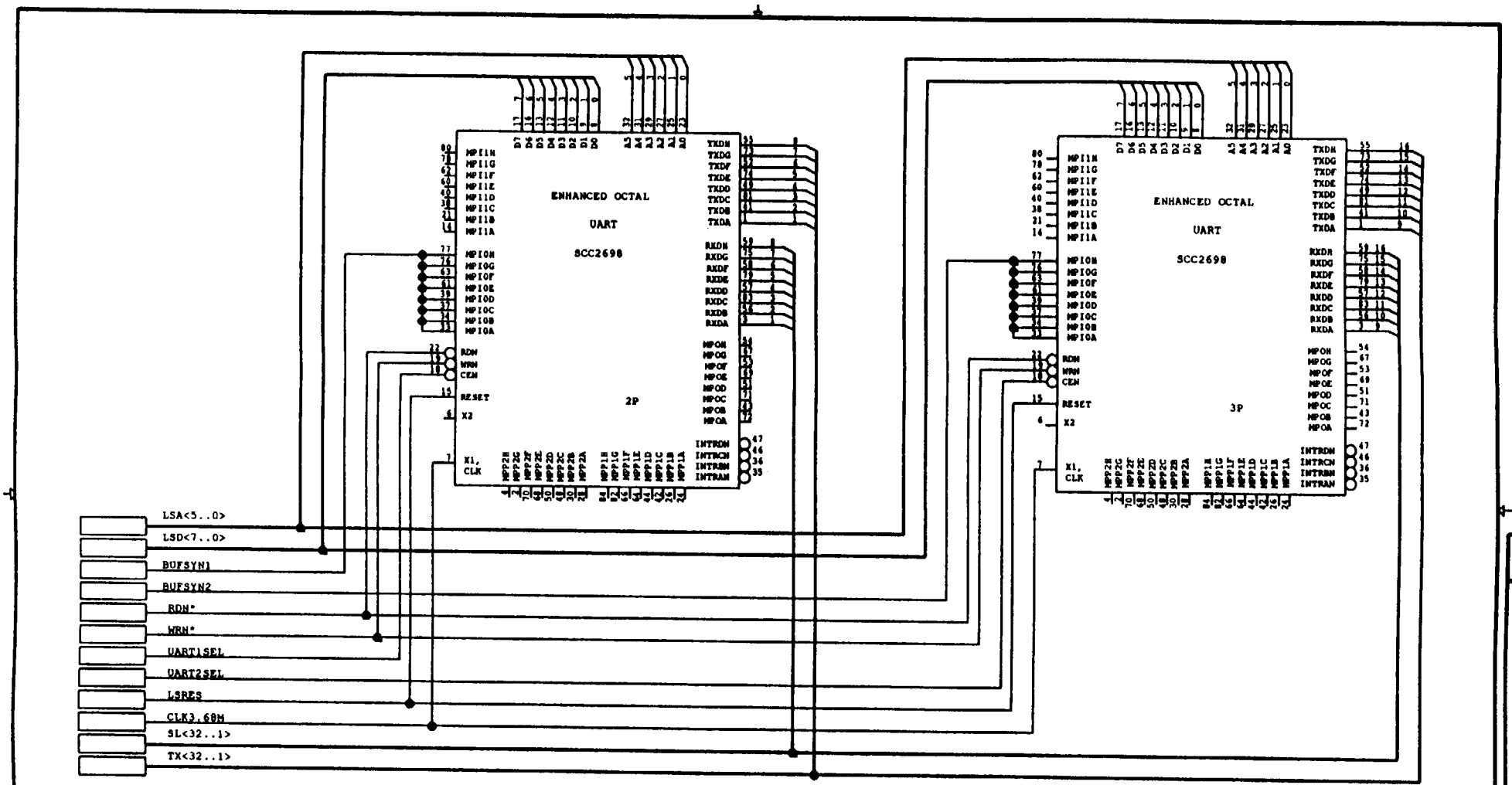
DRAWING TITLE=49800128 ABBREV=49800128 LAST_MODIFIED=Fri Sep 22 15:34:33 1995


RDY<31..0>
LA<3..1>
OUTEM*<4..1>
XC4010DPQ160
XILINX LCA
VER <1>
1P
2P
27C512
64KX8
UVEPROM
200NS
3P
27C020
256KX8
UVEPROM
120NS
LD<15..0>
TA<8..0>
CDONE*
CONFIGTRIG
HI10K
HSRAM*
FIFOR*
SIGNEXT
WDIVME
CCLKALL
SIMDAT
ASRDYB
OUTRST*
OUTEN*
WRDIVR*
PROG*
P5V
5P
10K
MAX705
VCC
MDI
WDO
MR
RESET
PFI
PFO
GND
MUXREQ
FIFORSNT
LRESET*
TIMERDY
CLK7M
RMX16C
REC*
LW*
WDRECOUT
CA<15..0>
M2
M1
M0
DRAWING
TITLE=49800128
ABBRFV=49800128
LAST_MODIFIED=Fri Sep 22 13:47:55 1995
LORAL
TEST & INFORMATION SYSTEMS
P.O. Box 3041
Sarasota, FL 34230
SCHEMATIC, PWA
AUI
SIZE
B
CAGE CODE
01GD0
DRAWING NO.
49800128-1
REV.
XA
SCALE
NONE
SHEET 9
SHEET
9
49800128-1


TRAM*
FULL*
OVFLEN
LRST*
FMST*
LM*
ENBLMX
TAGEN
MXD1WR*
MXWR*
MXD15*
MXDAV*
MXCLK*
MX32C
MX16C
MXRDN*
MXREQ*
DISREQ*
DISREQ
MAX_DELAY=10000
MXDSRQ*
TTLHI 8A
TTLHI 8B
TRADSTB
FREQ*
RDTRAN*
TTLHI 8E
LD00
TAGEND
HFULL
FLOHLDEN
BRLCNTL
FLOCTL*
FLCNTL
MXREQ
MXREQ*
FLOHLD
BMXWR*
BMXDAV*
BMX32C
BMX16C
BMXRD*
MXRQN*
LOCAEN*
TTLHI 8C
BMXDIS*
CKIN*
LSHFTIN*
P5V
PAL_IMAGE
ACT74
ABT245A
PAL20L8_10JC
CY7C330_30JC
CP4105C_30
LORAL
TEST & INFORMATION SYSTEMS
P.O. Box 3041
Sarasota, FL 34230
SCHEMATIC, PWA
AUI
SIZE B
CAGE CODE 01GD0
DRAWING NO. 49800128-1
REV. XA
SCALE NONE
SHEET 10
SHEET 10
49800128-1
CONCEPT REV -
DRAWING TITLE=49800128 ABBREV=49800128
LAST_MODIFIED=Mon Sep 25 17:50:10 1995


MAX233
MAX707
27H512
64KX8
UVEPROM
30NS
FCT573T
FCT244
ACT74
12 MHZ
IDT7007L25PF
MAX
MEM_IMAGE
P5V
10K
RDN
WRN
TXENABLE
LRESET*
LSCLK
ROMCEN
LSD<7..0>
LSA<15..0>
LA<18..1>
LD<15..0>
BUFSYN6
BUFSYN5
BUFSYN4
BUFSYN3
BUFSYN2
BUFSYN1
BUSY*
HI10K
LW*
DPR*
LDS1*
LSA15
SCHEMATIC, PWA
AUI
01GD0
49800128-1
XA
SHEET 11
49800128-1
DRAWING TITLE=49800128 ABBREV=49800128 LAST_MODIFIED=Mon Sep 25 17:48:03 1995


XC4003HPQ208-5
XILINX LCA
VER <1>
TX<32..1>
SO<32..1>
TXRN<32..1>
MDREG1
CONFIGREC
CONFIG3YN
LSD<7..0>
LSA<15..0>
SYNOLN
TXENABLE
RECRESNT
WDSYN
WRN*
REGSELN
RDN*
HI10K
P5V
UART4SEL
UART3SEL
UART2SEL
UART1SEL
BTER4RSEL
BTER3RSEL
BTER2RSEL
BTER1RSEL
PRE4SEL
PRE3SEL
PRE2SEL
PRE1SEL
LSBD<7..0>
LORAL
TEST & INFORMATION SYSTEMS
P.O. Box 3041
Sarasota, FL 34230
SCHEMATIC, PWA
AUI
SIZE B
CAGE CODE 01GD0
DRAWING NO. 49800128-1
REV. XA
SCALE NONE
SHEET 12
SHEET 12
49800128-1
DRAWING TITLE=49800128 ABBREV=49800128 LAST_MODIFIED=Tue Sep 26 17:40:52 1995




LORAL
TEST & INFORMATION SYSTEMS
P.O. Box 3041
Sarasota, FL 34230

SCHEMATIC, PWA
AUI

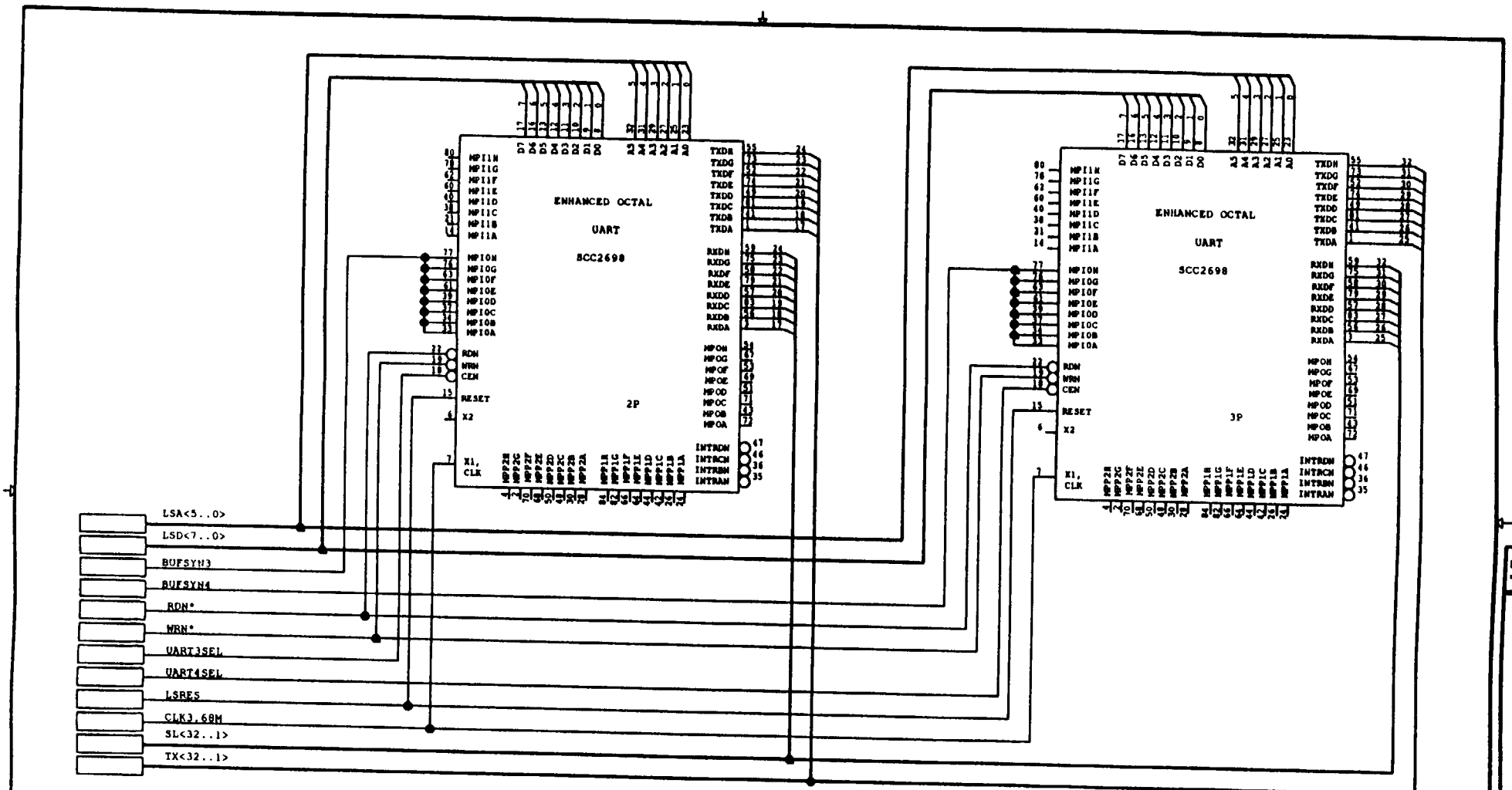
| SIZE | CAGE CODE | DRAWING NO. | REV. |
|---|---|---|---|
| B | 01GD0 | 49800128-1 | XA |

SCALE NONE SHEET 13

SHEET 13 | 49800128-1

CONCEPT REV -

DRAWING TITLE=49800128 ABBREV=49800128 LAST_MODIFIED=Tue Sep 26 14:18:58 1995




LORAL
TEST & INFORMATION SYSTEMS
P.O. Box 3041
Sarasota, FL 34230

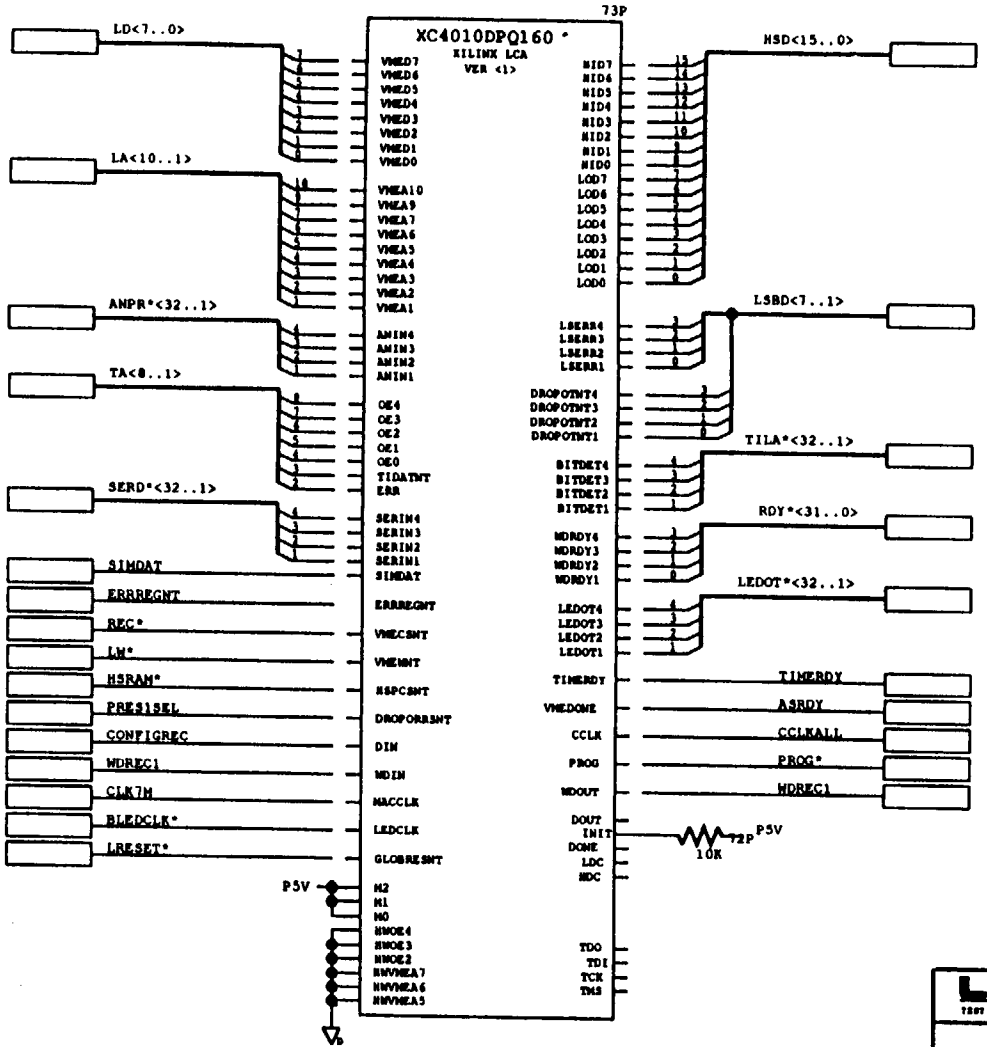
SCHEMATIC, PWA
AUI

| SIZE | CAGE CODE | DRAWING NO. | REV. |
|---|---|---|---|
| B | 01GD0 | 49800128-1 | XA |
| SCALE NONE | | SHEET 14 | |

SHEET 14
49800128-1

CONCEPT REV -

DRAWING TITLE=49800128 ABBREV=49800128 LAST_MODIFIED=Tue Sep 26 14:28:17 1995




SHEET 15

49800128-1

LORAL
TEST & INFORMATION SYSTEMS
P.O. Box 3041
Sarasota, FL 34230

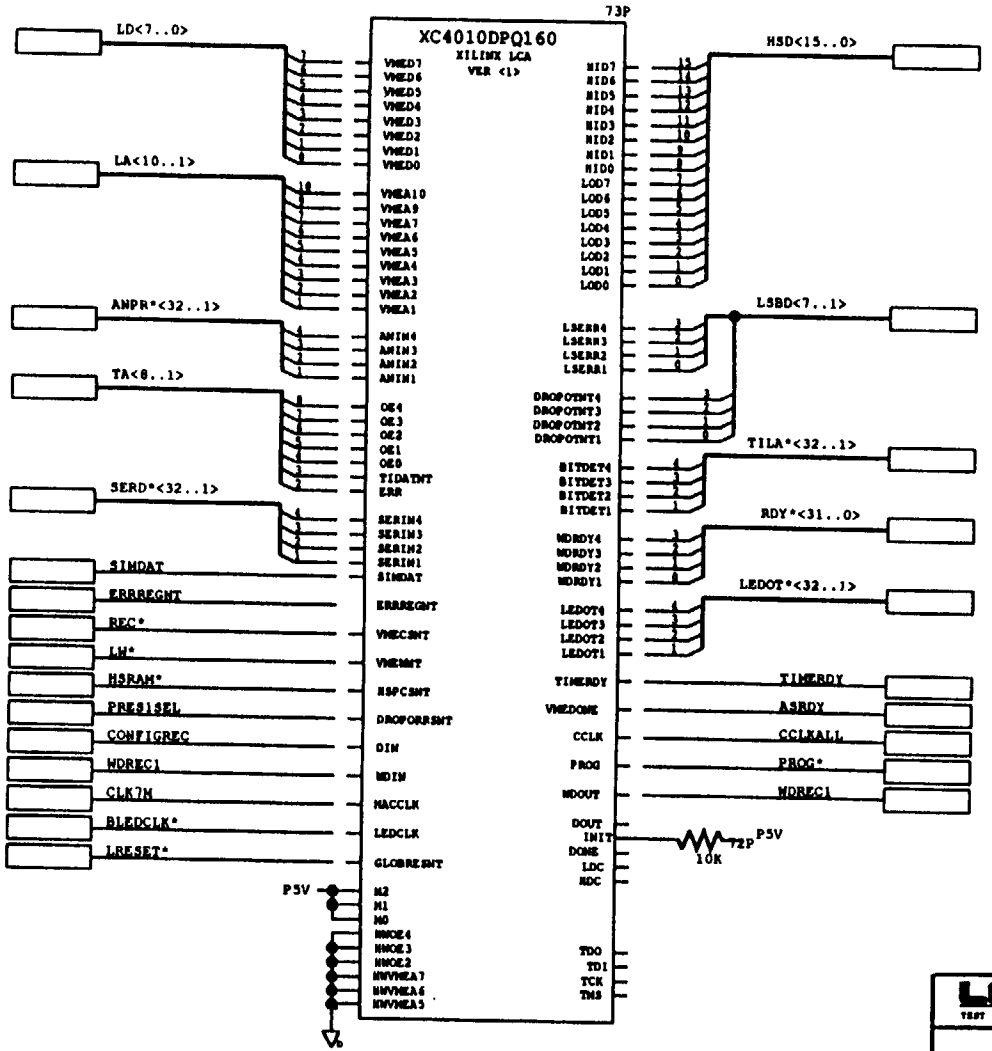
SCHEMATIC, PWA
AUI

| SIZE | CAGE CODE | DRAWING NO. | REV. |
|---|---|---|---|
| B | 01GD0 | 49800128-1 | XA |

SCALE NONE SHEET 15

CONCEPT REV -

DRAWING TITLE=49800128 ABBREV=49800128 LAST_MODIFIED=Wed Sep 27 17:06:15 1995




SHEET 16

49800128-1

LORAL
TEST & INFORMATION SYSTEMS
P.O. Box 3041
Sarasota, FL 34230

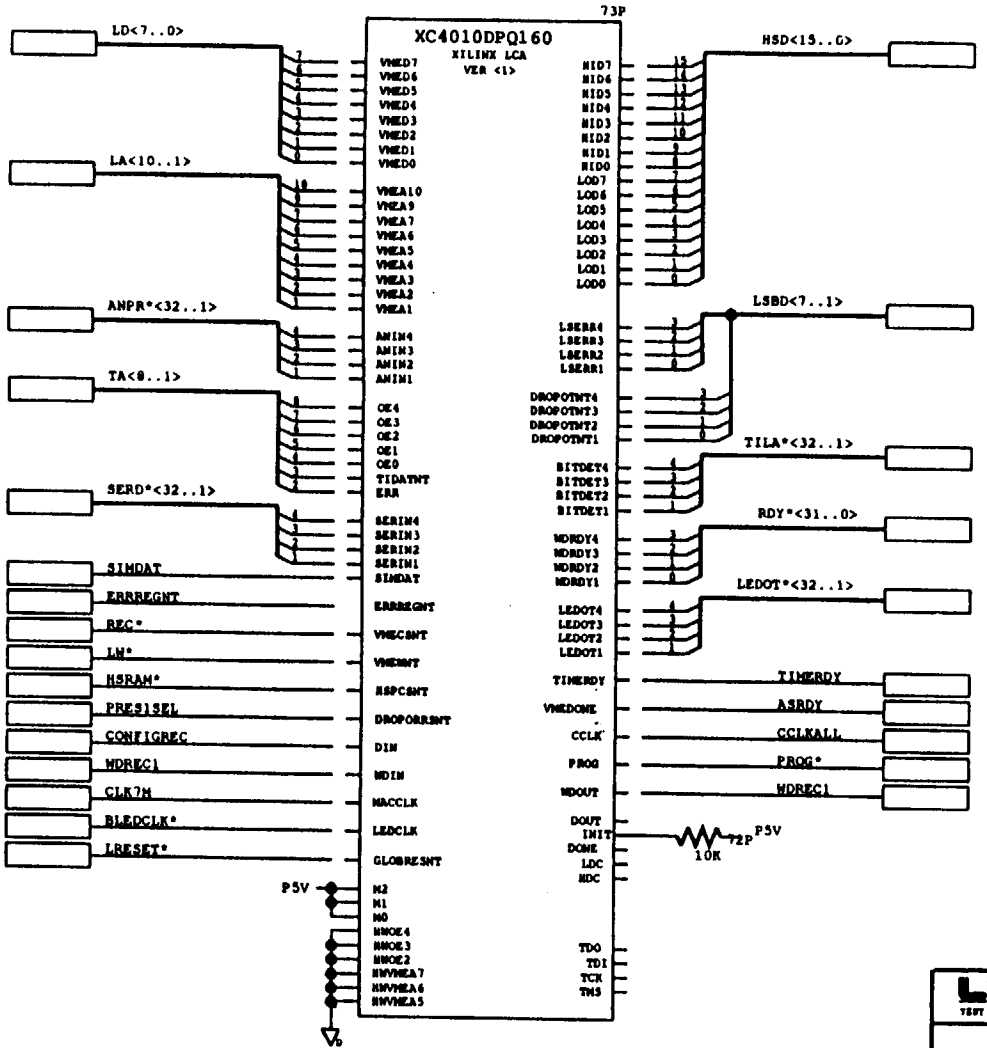
SCHEMATIC, PWA
AUI

| SIZE | CAGE CODE | DRAWING NO. | REV. |
|---|---|---|---|
| B | 01GD0 | 49800128-1 | XA |

SCALE NONE SHEET 16

CONCEPT REV -

DRAWING TITLE=49800128 ABBREV=49800128 LAST_MODIFIED=Wed Sep 27 17:07:35 1995





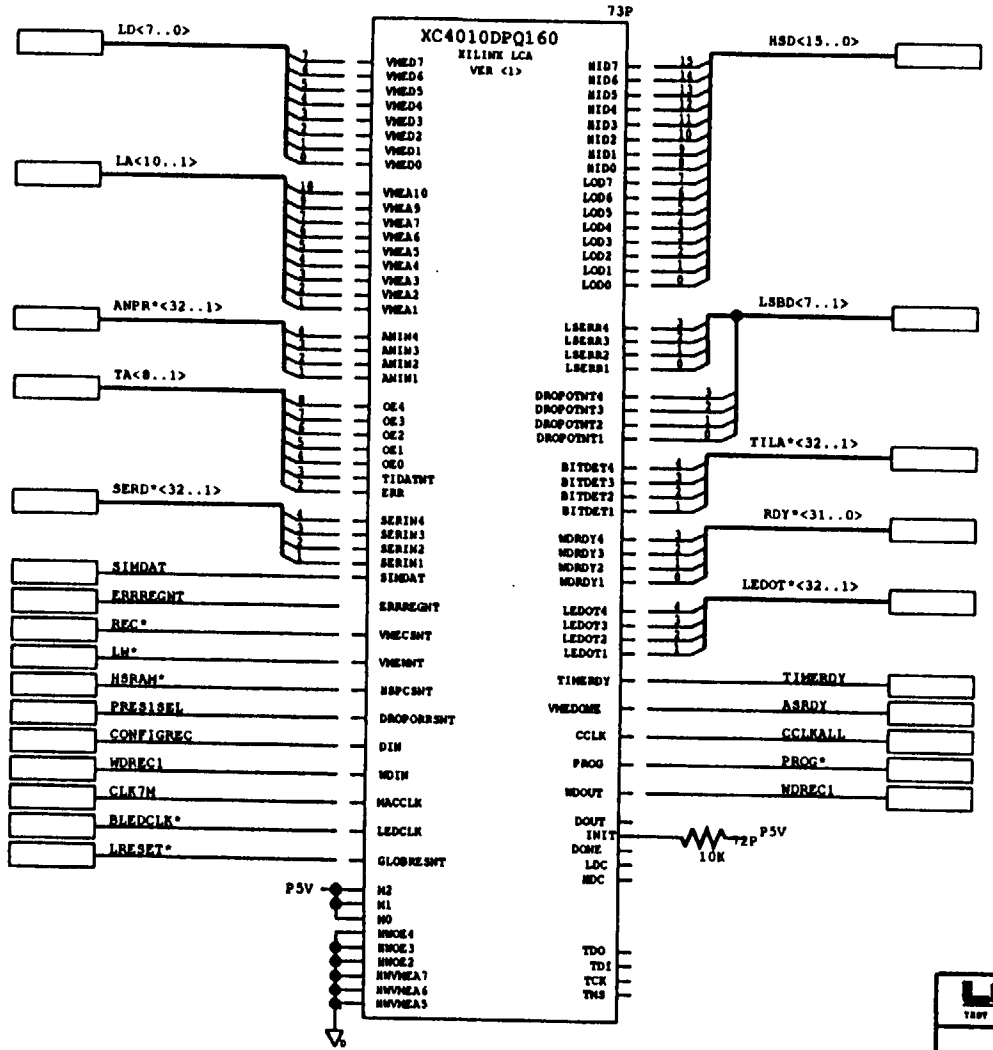

LORAL
TEST & INFORMATION SYSTEMS
P.O. Box 3041
Sarasota, FL 34230

SCHEMATIC, PWA
AUI

| SIZE | CAGE CODE | DRAWING NO. | REV. |
|---|---|---|---|
| B | 01GD0 | 49800128-1 | XA |
| SCALE NONE | | SHEET 17 | |

CONCEPT REV -

DRAWING TITLE=49800128 ABBREV=49800128 LAST_MODIFIED=Wed Sep 27 17:07:59 1995

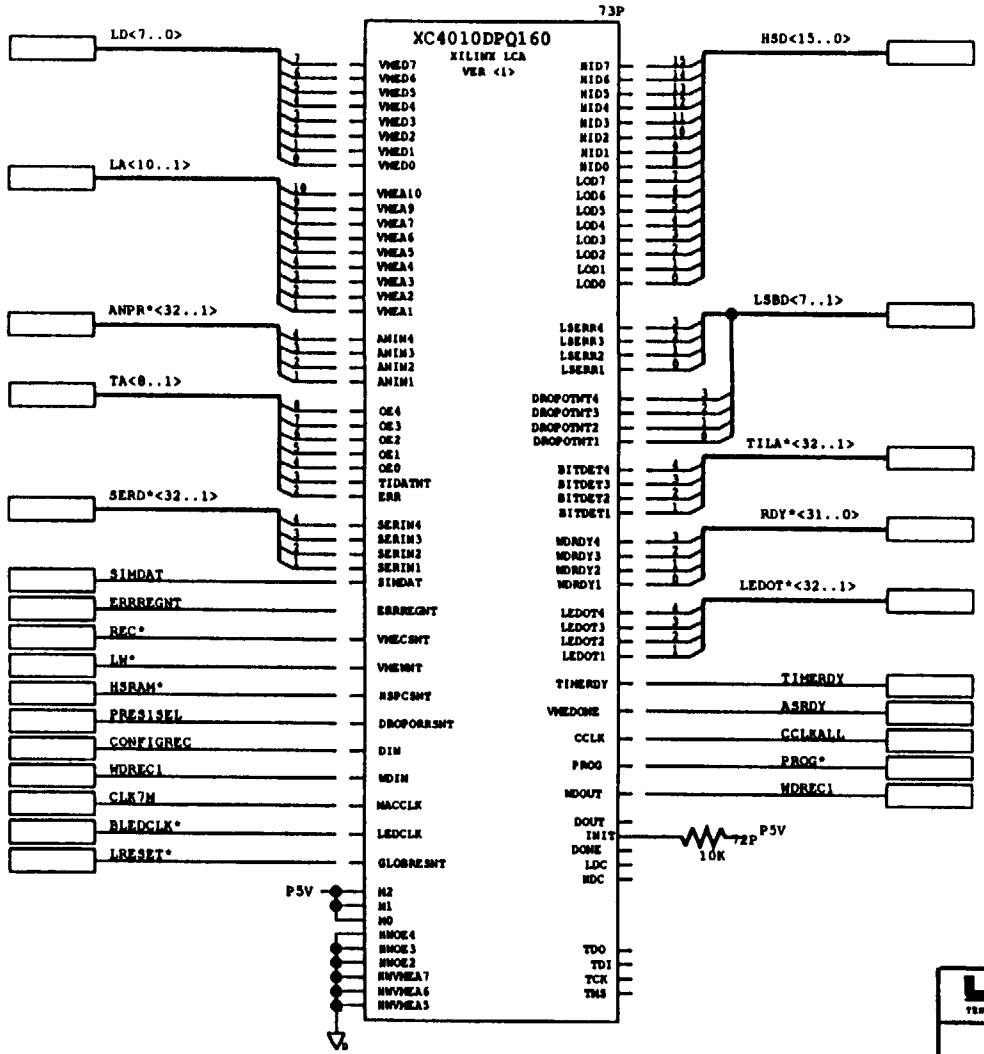



| | | | |
|---|---|---|---|
| LORAL | | | P.O. Box 3041 Sarasota, FL 34230 |
| SCHEMATIC, PWA AUI | | | |
| SIZE B | CAGE CODE 01GD0 | DRAWING NO. 49800128-1 | REV. XA |
| SCALE NONE | | | SHEET 18 |

SHEET 18

49800128-1

DRAWING TITLE=49800128 ABBREV=49800128 LAST_MODIFIED=Wed Sep 27 17:08:30 1995



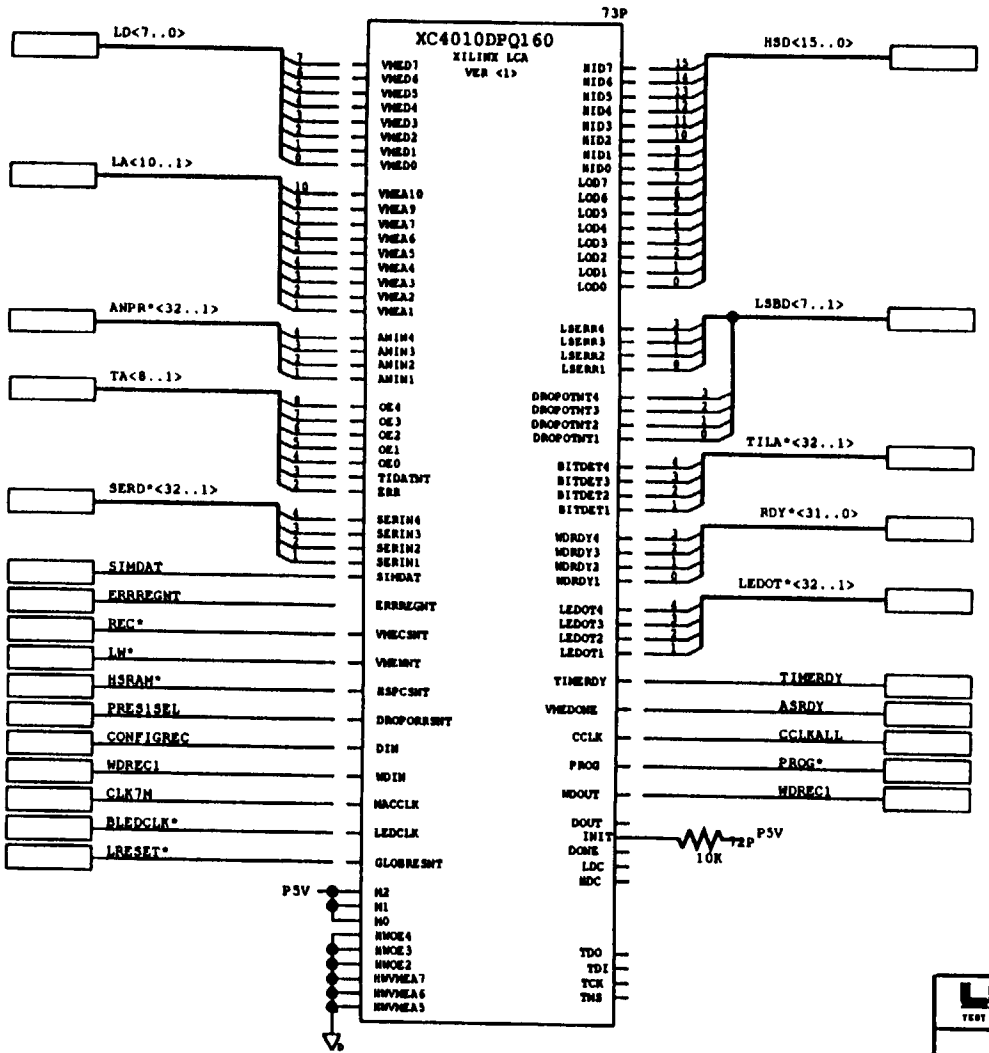

| | | | |
|---|---|---|---|
| LORAL — TEST & INFORMATION SYSTEMS | | P.O. Box 3041 Sarasota, FL 34230 | |
| SCHEMATIC, PWA AUI | | | |
| SIZE B | CAGE CODE 01GD0 | DRAWING NO. 49800128-1 | REV. XA |
| SCALE NONE | | SHEET 19 | |

SHEET 19

49800128-1

CONCEPT REV -

DRAWING TITLE=49800128 ABBREV=49800128 LAST_MODIFIED=Wed Sep 27 17:08:58 1995




| | | | |
|---|---|---|---|
| SIZE B | CAGE CODE 01GD0 | DRAWING NO. 49800128-1 | REV. XA |
| SCALE NONE | | SHEET 20 | |

LORAL — TEST & INFORMATION SYSTEMS — P.O. Box 3041 Sarasota, FL 34230

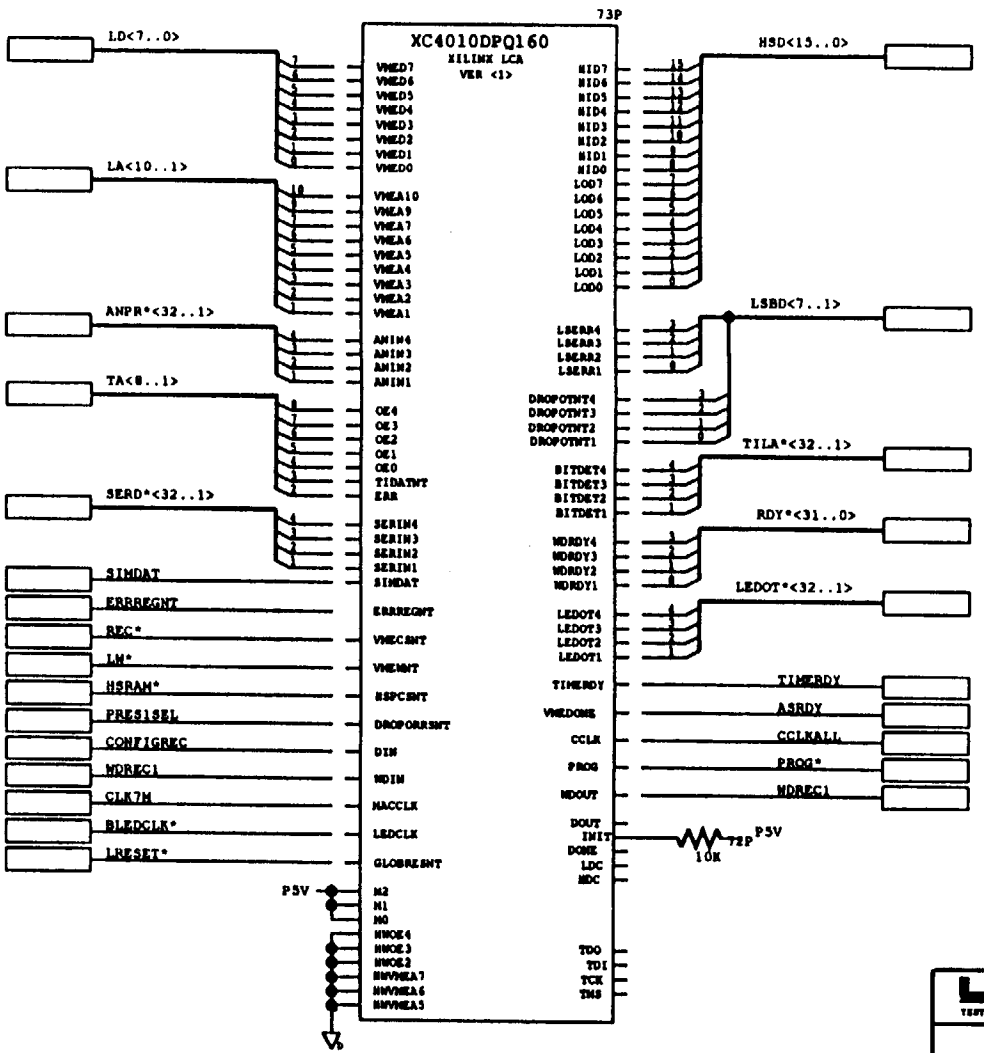
SCHEMATIC, PWA
AUI

SHEET 20

49800128-1

CONCEPT REV -

DRAWING TITLE=49800128 ABBREV=49800128 LAST_MODIFIED=Wed Sep 27 17:09:23 1995




SHEET 21

49800128-1

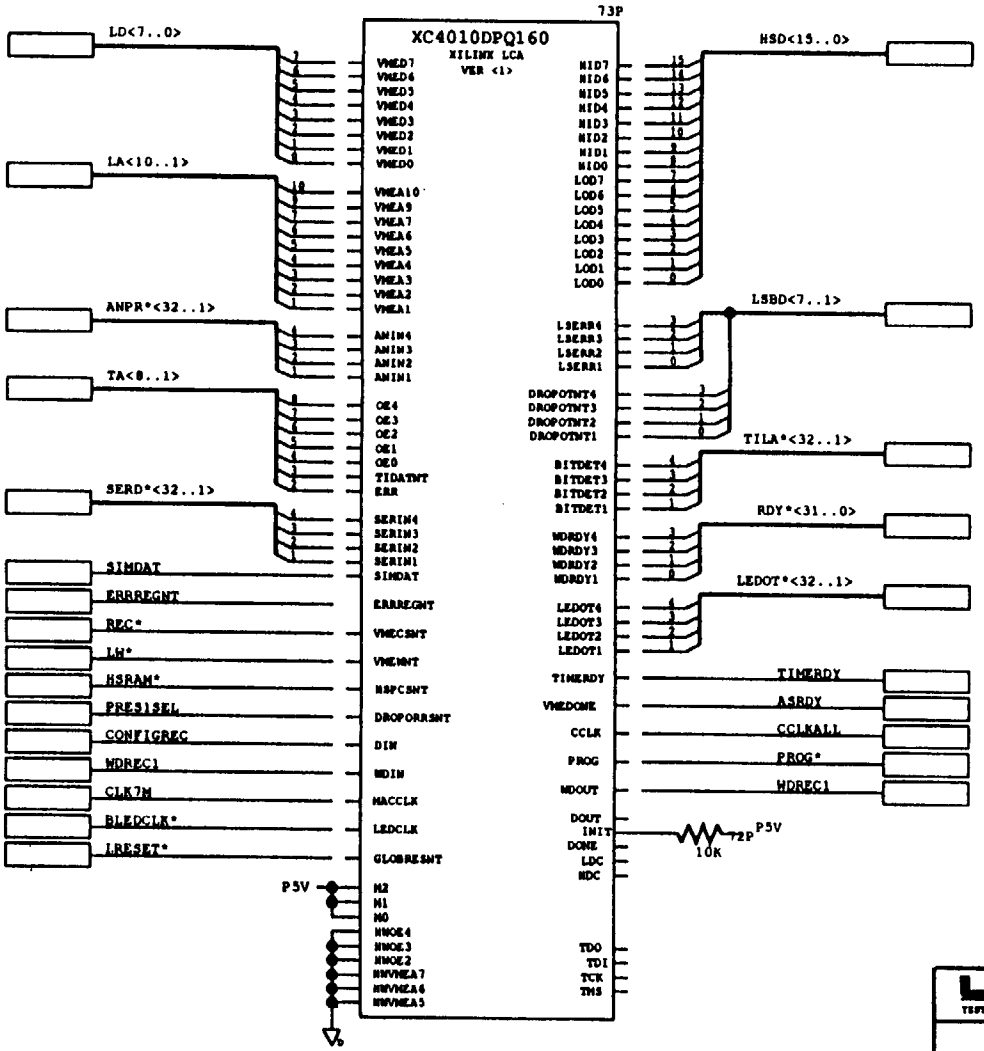
LORAL
TEST & INFORMATION SYSTEMS
P.O. Box 3041
Sarasota, FL 34230

SCHEMATIC, PWA
AUI

| SIZE | CAGE CODE | DRAWING NO. | REV. |
|---|---|---|---|
| B | 01GD0 | 49800128-1 | XA |
| SCALE NONE | | SHEET 21 | |

CONCEPT REV -

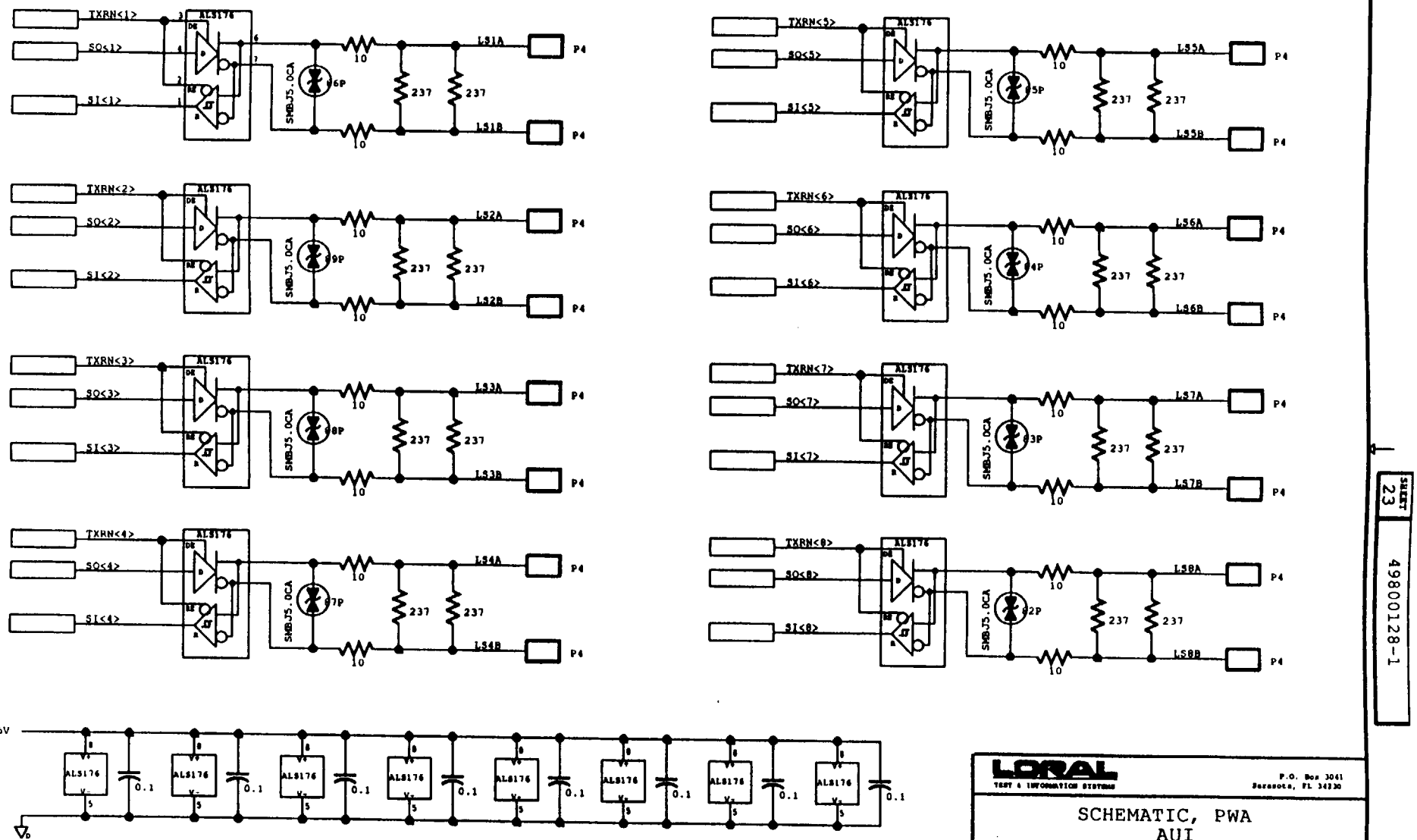
DRAWING TITLE=49800128 ABBREV=49800128 LAST_MODIFIED=Wed Sep 27 17:09:54 1995




| | | | |
|---|---|---|---|
| LORAL TEST & INFORMATION SYSTEMS | | | P.O. Box 3041 Sarasota, FL 34230 |
| SCHEMATIC, PWA AUI | | | |
| SIZE B | CAGE CODE 01GD0 | DRAWING NO. 49800128-1 | REV. XA |
| SCALE NONE | | | SHEET 22 |

SHEET 22 | 49800128-1

DRAWING TITLE=49800128 ABBREV=49800128 LAST_MODIFIED=Wed Sep 27 17:10:26 1995



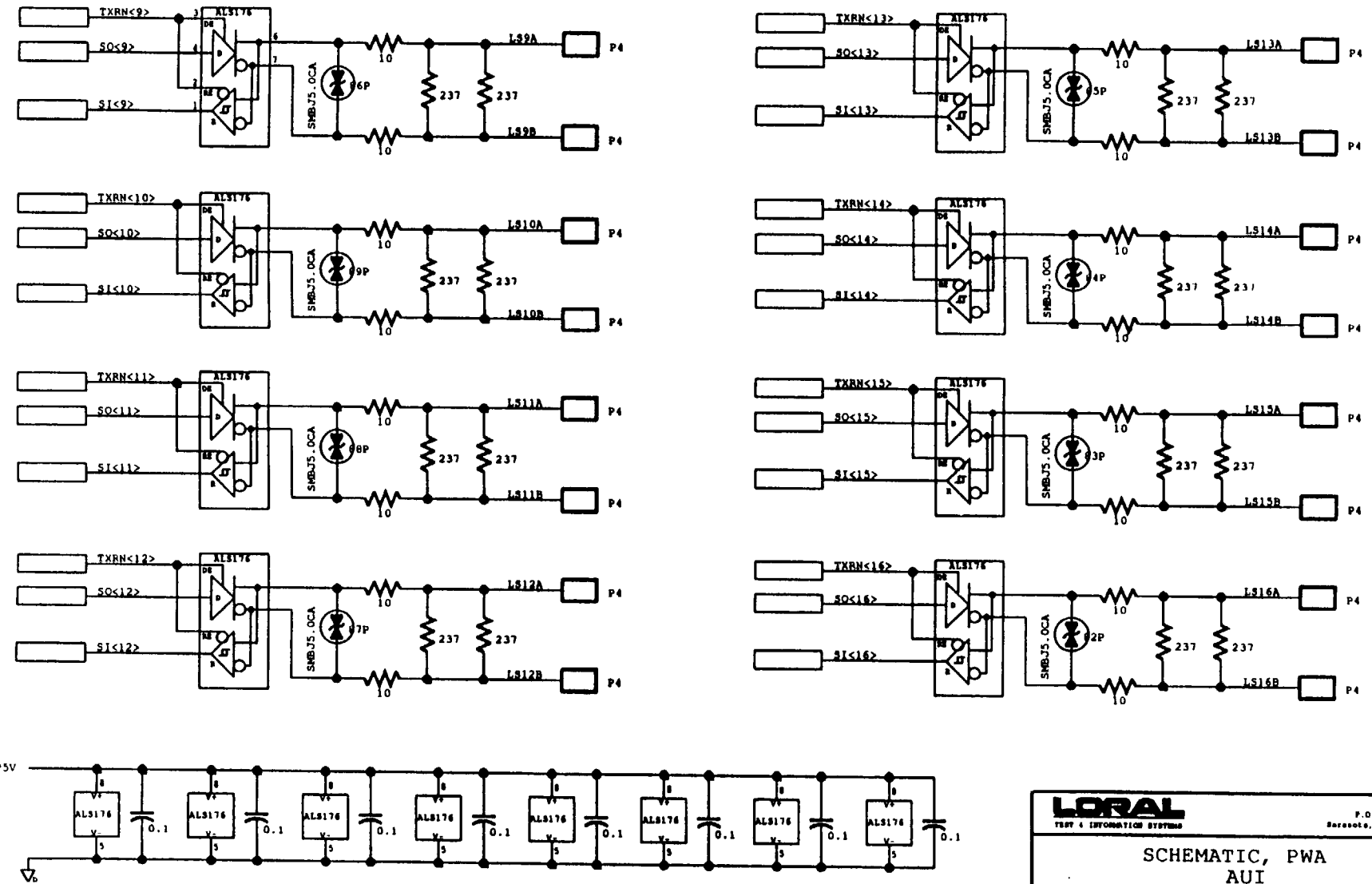

| | | | |
|---|---|---|---|
| LORAL TEST & INFORMATION SYSTEMS | P.O. Box 3041 Sarasota, FL 34230 | | |
| SCHEMATIC, PWA AUI | | | |
| SIZE B | CAGE CODE 01GD0 | DRAWING NO. 49800128-1 | REV. XA |
| SCALE NONE | | SHEET 23 | |

SHEET 23

49800128-1

CONCEPT REV -

DRAWING TITLE=49800128 ABBREV=49800128 LAST_MODIFIED=Wed Sep 27 16:18:14 1995




LORAL
TSAY & INFORMATION SYSTEMS
P.O. Box 3041
Sarasota, FL 34230

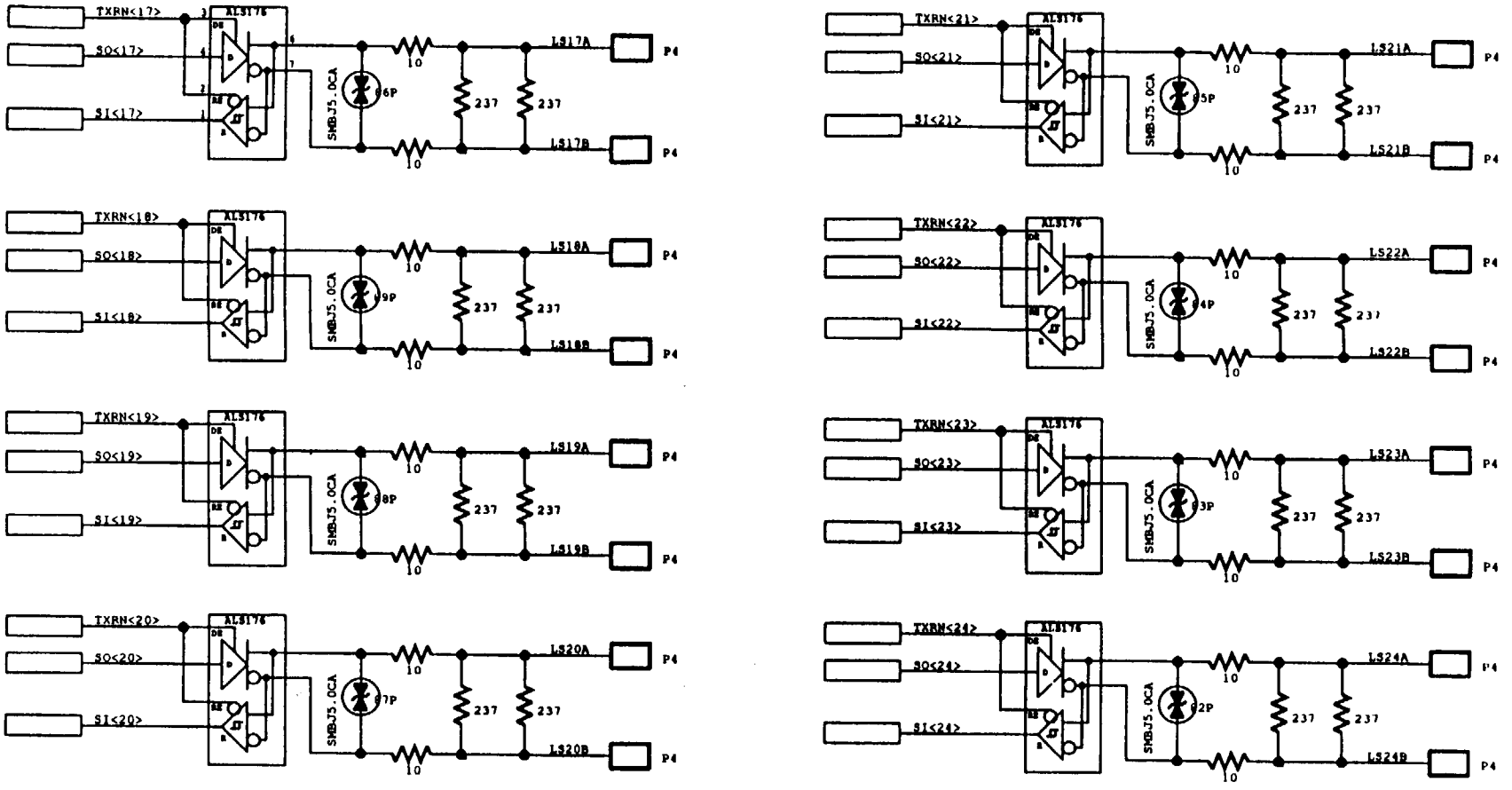
SCHEMATIC, PWA
AUI

| SIZE | CAGE CODE | DRAWING NO. | REV. |
|---|---|---|---|
| B | 01GD0 | 49800128-1 | XA |
| SCALE NONE | | SHEET 24 | |

SHEET 24

49800128-1

DRAWING TITLE=49800128 ABBREV=49800128 LAST_MODIFIED=Wed Sep 27 16:18:48 1995




SHEET 25

49800128-1

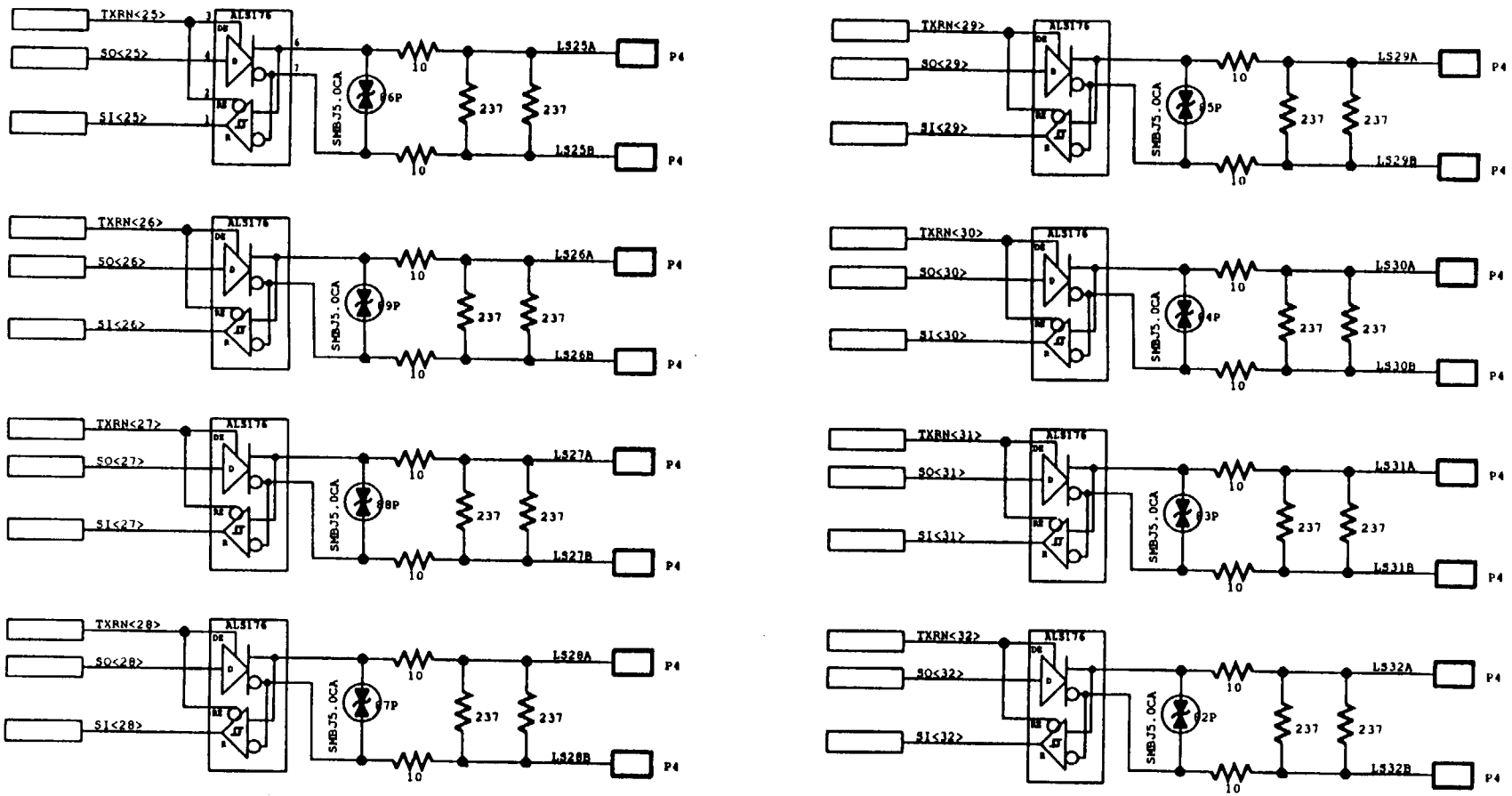
LORAL
TEST & INFORMATION SYSTEMS
P.O. Box 3041
Sarasota, FL 34230

SCHEMATIC, PWA
AUI

| SIZE | CAGE CODE | DRAWING NO. | REV. |
|---|---|---|---|
| B | 01GD0 | 49800128-1 | XA |
| SCALE NONE | | SHEET 25 | |

CONCEPT REV -

DRAWING TITLE-49800128 ABBREV-49800128 LAST_MODIFIED-Wed Sep 27 16:23:31 1995



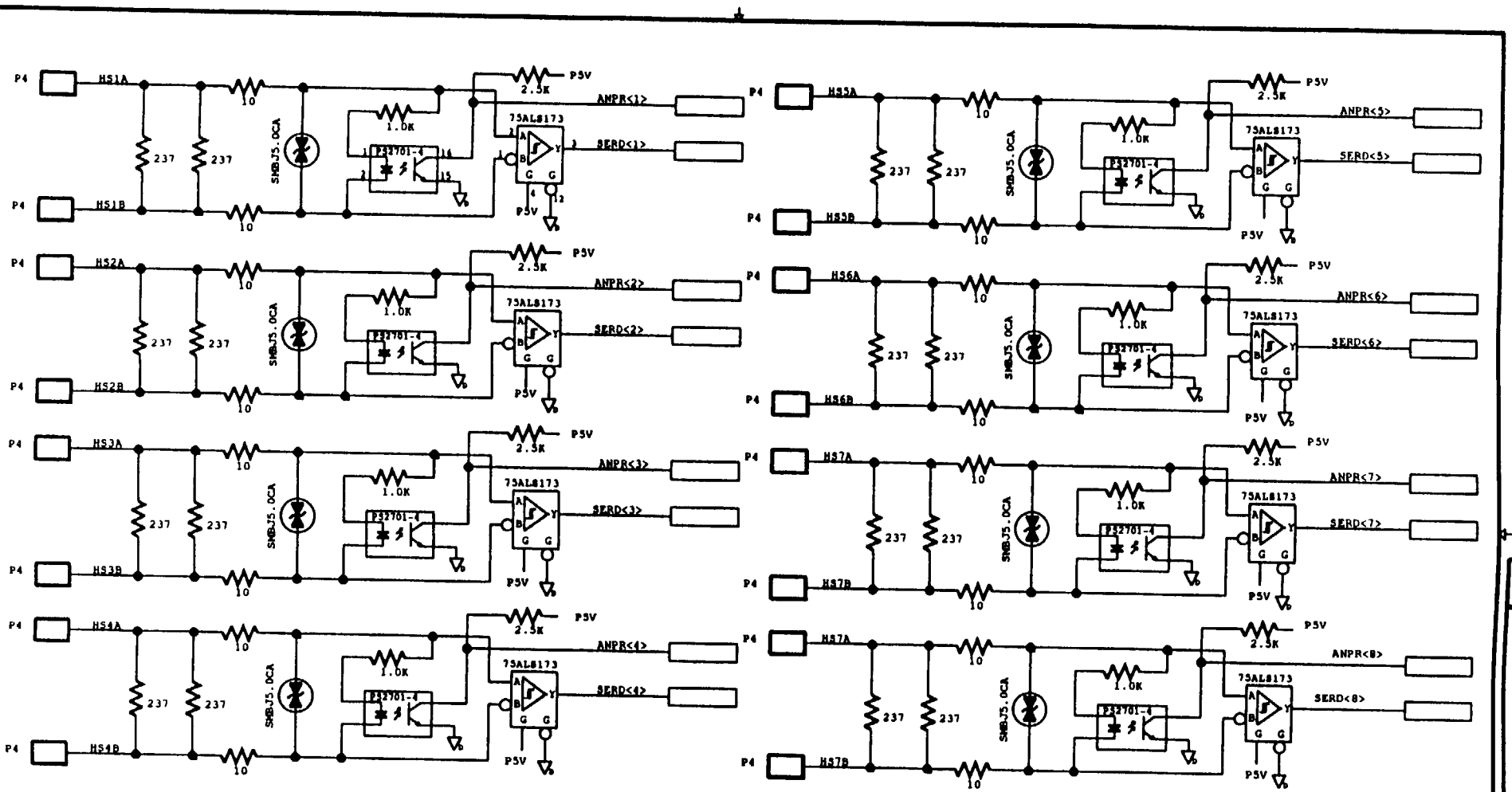

| | | | |
|---|---|---|---|
| LORAL TEST & INFORMATION SYSTEMS | | P.O. Box 3041 Sarasota, FL 34230 | |
| SCHEMATIC, PWA AUI | | | |
| SIZE B | CAGE CODE 01GD0 | DRAWING NO. 49800128-1 | REV. XA |
| SCALE NONE | | SHEET 26 | |

SHEET 26

49800128-1

CONCEPT REV

DRAWING TITLE=49800128 ABBREV=49800128 LAST_MODIFIED=Wed Sep 27 16:30:03 1995




SHEET 27

49800128-1

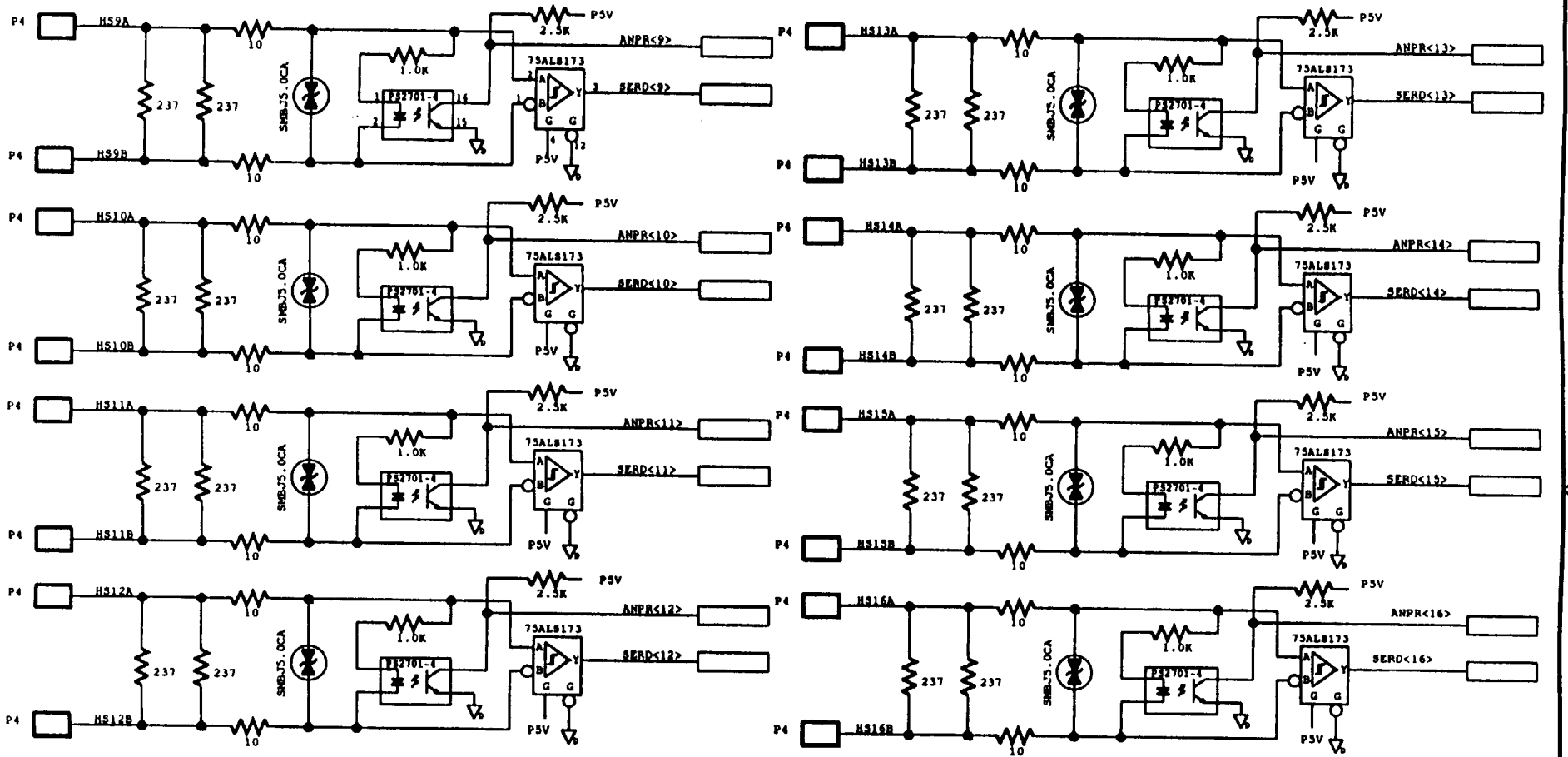
LORAL
TEST & INFORMATION SYSTEMS
P.O. Box 3041
Sarasota, FL 34230

SCHEMATIC, PWA
AUI

| SIZE | CAGE CODE | DRAWING NO. | REV. |
|---|---|---|---|
| B | 01GD0 | 49800128-1 | XA |
| SCALE NONE | | SHEET 27 | |

CONCEPT REV -

DRAWING TITLE=49800128 ABBREV=49800128 LAST_MODIFIED=Wed Sep 27 15:39:34 1995




SHEET 28

49800128-1

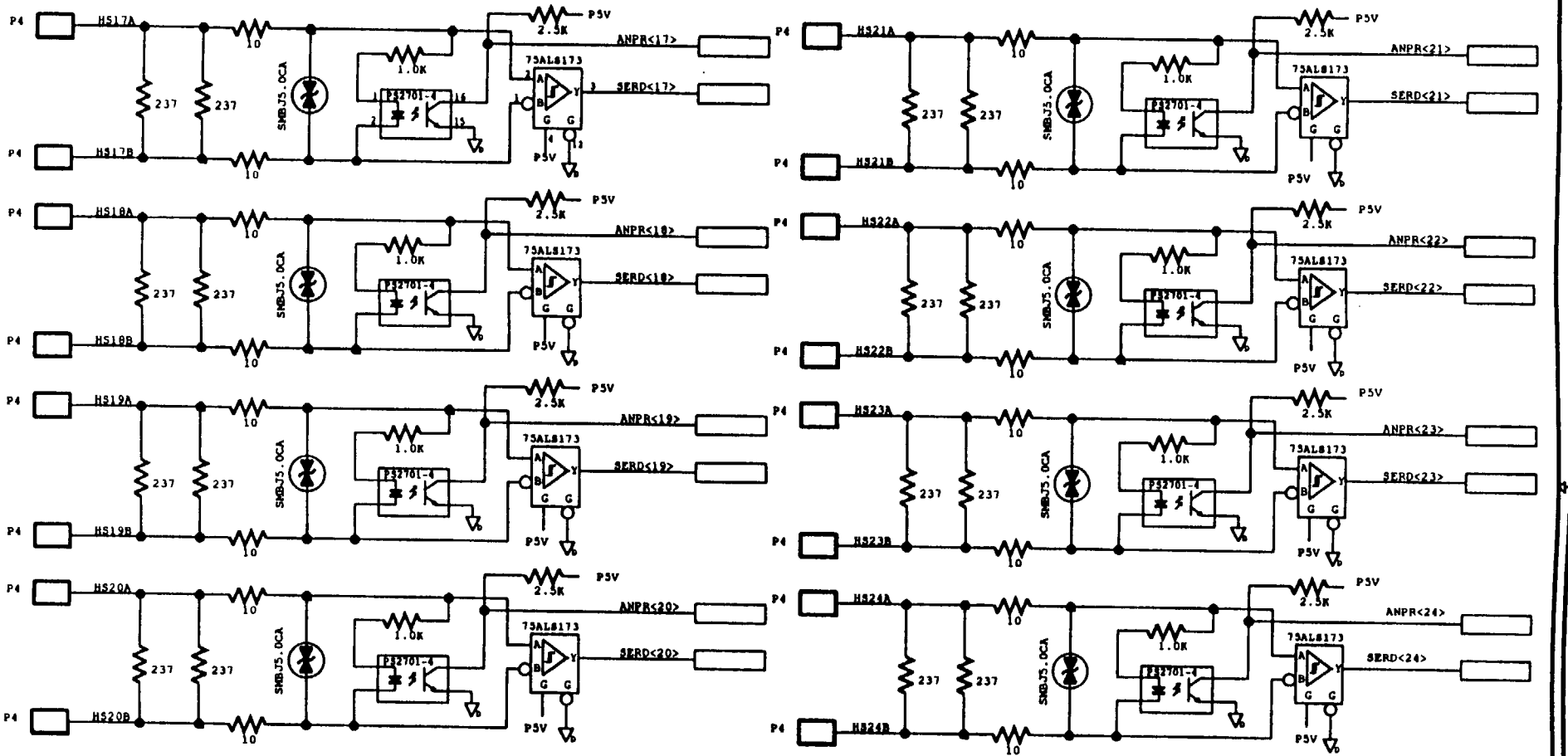
LORAL
TEST & INFORMATION SYSTEMS
P.O. Box 3041
Sarasota, FL 34230

SCHEMATIC, PWA
AUI

| SIZE | CAGE CODE | DRAWING NO. | REV. |
|---|---|---|---|
| B | 01GD0 | 49800128-1 | XA |
| SCALE NONE | | SHEET 28 | |

CONCEPT REV -

DRAWING TITLE=49800128 ABBREV=49800128 LAST_MODIFIED=Wed Sep 27 15:46:16 1995




SHEET 29

49800128-1

LORAL
TEST & INFORMATION SYSTEMS
P.O. Box 3041
Sarasota, FL 34230

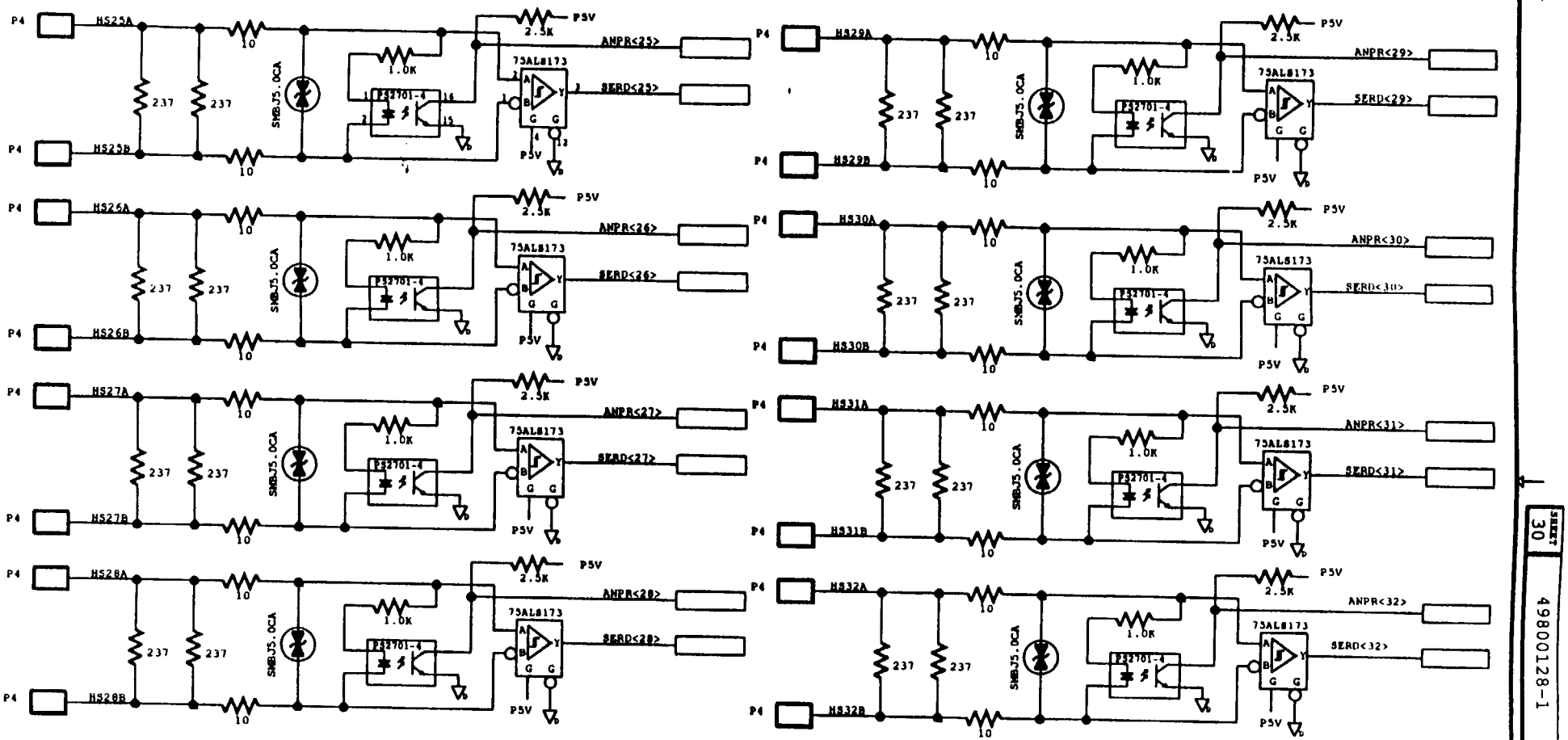
SCHEMATIC, PWA
AUI

| SIZE | CAGE CODE | DRAWING NO. | REV. |
|---|---|---|---|
| B | 01GD0 | 49800128-1 | XA |

SCALE NONE SHEET 29

CONCEPT REV -

DRAWING TITLE=49800128 ABBREV=49800128 LAST_MODIFIED=Wed Sep 27 15:50:37 1995




SHEET 30

49800128-1

CONCEPT REV -

LORAL
TEST & INFORMATION SYSTEMS
P.O. Box 3041
Sarasota, FL 34230

SCHEMATIC, PWA
AUI

| SIZE | CAGE CODE | DRAWING NO. | REV. |
|---|---|---|---|
| B | 01GD0 | 49800128-1 | XA |
| SCALE NONE | | SHEET 30 | |

DRAWING TITLE=49800128 ABBREV=49800128 LAST_MODIFIED=Wed Sep 27 16:00:57 1995

BMFLID FILE - LABOR IN UNITS PER HOUR
ASSEMBLY 49800126-1 PCAX ASSY,AUI B/M REVISION DATE - 26SEP95 U/M - EA

CURRENT REVISION: 1
NO PENDING ENGINEERING CHANGES

| ITEM | PART NUMBER | DESCRIPTION | U/M | REV | QUANTITY REQUIRED | BURD STD COST | BURD EXT COST | OPT # |
|---|---|---|---|---|---|---|---|---|
| 1 | 49800126 | REF DRAWING,AUI | EA | | 0.000000 | 0.0000 | 0.0000 | 1 |
| 2 | 49800127-1 | PCBX PWB,AUI | EA | | 1.000000 | 0.0000 | 0.0000 | 1 |
| 3 | 49800128-1 | REF SCHEMATIC,AUI | EA | | 0.000000 | 0.0000 | 0.0000 | 1 |
| 4 | 58527020-12 | ICXT IC,27C020,UVEPROM,CMOS,256KX8,120NS,DIP632 | EA | | 1.000000 | 4.8620 | 4.8620 | 1 |
| 5 | 58527512-20 | ICXT IC,27C512,UVEPROM,CMOS,64KX8,200NS,TS,DIP628 | EA | | 1.000000 | 2.4420 | 2.4420 | 1 |
| 6 | 58220-32 | ICXT IC,74AS32,OR-GATE,TWO-INPUT,QUAD,SO14 | EA | | 1.000000 | 0.5800 | 0.5800 | 1 |
| 7 | 0469702617 | ICXS IC,DIG,ASTTL,FF,SMT, 14SOIC,NH,DUAL,PRE&CLEAR | EA | | 1.000000 | 0.5227 | 0.5227 | 1 |
| 8 | 58010-38 | ICXS IC,74F38,BUFF,NAND,2-INPUT,OC,QUAD,SO14 | EA | | 1.000000 | 0.2508 | 0.2508 | 1 |
| 9 | 58450-138 | ICXS IC,74FCT138AT,DEC/DEMUX,1-OF-8,W/ENABLE,SO16 | EA | | 2.000000 | 2.0680 | 4.1360 | 1 |
| 10 | 58451-541 | ICXS IC,74FCT541T,BUFF/DRVR,OCTAL,TS,SO20 | EA | | 2.000000 | 1.2100 | 2.4200 | 1 |
| 11 | 58451-573 | ICXS IC,74FCT573T,LATCH,TRNSPRNT,OCTAL,TS,SO20 | EA | | 9.000000 | 1.5400 | 13.8600 | 1 |
| 12 | 57320-14 | ICXS IC,74LS14,INV,SCHMITT-TRIGGER,HEX,SO14 | EA | | 1.000000 | 0.2164 | 0.2164 | 1 |
| 13 | 571253-1 | ICXS IC,75ALS173,RCVR,LN,RS-422A/RS-485,QUAD,DIP16 | EA | | 8.000000 | 1.9580 | 15.6640 | 1 |
| 14 | 0469702522 | ICXS IC,DIG,ALSTTL,XCVR,SMT, 8SOIC,NH,DIFF BUS | EA | | 32.000000 | 1.5840 | 50.6880 | 1 |
| 15 | 571255-1 | ICXS IC,80C31,CMOS,M-CNTLLR,8-BIT,24MHZ,OTP,PLCC44 | EA | | 1.000000 | 3.2340 | 3.2340 | 1 |
| 16 | 0469702613 | ICXS IC,DIG,BICMOS,XCVR,SMT, 20WSO,NH,OCTAL,BUS,3- | EA | | 6.000000 | 1.9602 | 11.7612 | 1 |
| 17 | 58408-374 | ICXS IC,74ABT374,F/F,D-TYPE,OCTAL,TS,SO20 | EA | | 2.000000 | 0.9669 | 1.9338 | 1 |
| 18 | 58408-534 | ICXS IC,74ABT534,F/F,D-TYPE,OCTAL,TS,INV,SO20 | EA | | 10.000000 | 1.2010 | 12.0100 | 1 |
| 19 | 0469702611 | ICXS IC,DIG,BICMOS,XCVR,SMT, 24WSO,NH,REG,3-STATE | EA | | 2.000000 | 2.9076 | 5.8152 | 1 |
| 20 | 58220-641 | ICXS IC,74AS641,XCVR,BUS,OCTAL,OC,SO20 | EA | | 1.000000 | 2.4024 | 2.4024 | 1 |
| 21 | 250115-1 | CONT CONN,PIN,DIN 41612,C,RTANG,96P | EA | | 3.000000 | 2.0720 | 6.2160 | 1 |
| 22 | 5856287-25 | ICXT IC,7C187,SRAM,CMOS,64KX1,25NS | EA | | 1.000000 | 3.2076 | 3.2076 | 1 |
| 23 | 0469702621 | ICXS IC,DIG,CMOS,EPLD,SMT, 28PLCC,NH | EA | | 1.000000 | 10.3070 | 10.3070 | 1 |
| 24 | 5851220-20 | ICXT IC,1220,SRAM,16K,NONVOLATILE,200NS | EA | | 1.000000 | 5.6760 | 5.6760 | 1 |
| 25 | 0469702623 | ICXT IC,DIG,CMOS,EPLD,SMT, 24WSO,NH,16 MACRO CELLS | EA | | 1.000000 | 0.0000 | 0.0000 | 1 |
| 26 | 240060-5 | SWTX SWITCH,RTRY,HEX,R/A,COMPLIMENT | EA | | 2.000000 | 3.7950 | 7.5900 | 1 |
| 27 | 5857007-25 | ICXS IC,IDT7007,DPSRAM,CMOS,32KX8,25NS,TS,TQFP80 | EA | | 1.000000 | 90.9440 | 90.9440 | 1 |
| 28 | 5857130-45J | ICXS IC,7130SA,DUAL-PORT SRAM,CMOS,1KX8,52PLCC | EA | | 2.000000 | 7.5900 | 15.1800 | 1 |
| 29 | 5857202-35 | ICXS IC,7202,FIFO,CMOS,ASYNCH,1KX9,TS,35NS,PLCC32 | EA | | 6.000000 | 6.7200 | 40.3200 | 1 |
| 30 | 1849700131 | CRYT OSC,XTAL,HCMOS,3.6864MHZ, .01%,100PPM,SMT | EA | | 1.000000 | 27.9950 | 27.9950 | 1 |
| 31 | 560101-2 | DIOT DIODE,LED-QUAD,RED,PCB MNT,3MA,@5VDC | EA | | 10.000000 | 1.8200 | 18.2000 | 1 |
| 32 | 5762019-10 | ICXS IC,PAL20L8,40X64&AR,20IN/8OUT,10NS,PLCC28 | EA | | 1.000000 | 2.3856 | 2.3856 | 1 |
| 33 | 1010100027 | LDS DVC,OPTCPLR,QUAD,IF=50MA, BV=2.5KV,SMT,16SOIC | EA | | 8.000000 | 1.1000 | 8.8000 | 1 |
| 34 | 810101-100 | FLOS RES,CHIP,THCK-FLM,10 OHMS,1/8W,5%,SMD1206 | EA | | 128.000000 | 0.0088 | 1.1264 | 1 |
| 35 | 6922110000 | FLOS RES,FIX,TF,1KOHM,1%,.125W ,100PPM,SMT,CHIP,NM | EA | | 32.000000 | 0.0127 | 0.4064 | 1 |
| 36 | 571249-1 | ICXS IC,SCC2698B,UART,CMOS,OCTAL,PLCC84 | EA | | 4.000000 | 24.2267 | 96.9068 | 1 |
| 37 | 310102-6 | CRYS XTAL OSC,HCMOS/TTL,16MHZ,0.01%STB,SMT | EA | | 1.000000 | 4.4800 | 4.4800 | 1 |
| 38 | 540100-1 | DIOS TVS,BIDIRECTIONAL,5VDC(VR),600W(PW),DO-214AA | EA | | 64.000000 | 0.9901 | 63.3664 | 1 |

MATERIAL COST - 481.8645
MATERIAL BURDEN COST - 48.1865

ASSEMBLY NO. 49800126-1
DESC..... PCAX ASSY,AUI

| PART NUMBER.... | ITEM NO. | PN DESC..... | QTY..... | VENDOR PART..... | VENDOR/MFG..... |
|---|---|---|---|---|---|
| 0469702522 | 14 | ICXS IC,DIG,ALSTTL,XCVR,SMT, 8SOIC, NH,DIFF BUS | 32 | SN75ALS176D | TEXAS INSTRUMENTS |
| 0469702611 | 19 | ICXS IC,DIG,BICMOS,XCVR,SMT, 24WSO, NH,REG,3-STATE | 2 | SN74ABT652DW | TEXAS INSTRUMENTS |
| 0469702613 | 16 | ICXS IC,DIG,BICMOS,XCVR,SMT, 20WSO, NH,OCTAL,BUS,3- | 6 | SN74ABT245ADW | TEXAS INSTRUMENTS |
| 0469702617 | 7 | ICXS IC,DIG,ASTTL,FF,SMT, 14SOIC,NH ,DUAL,PRE&CLEAR | 1 | SN74AS74D | TEXAS INSTRUMENTS |
| 0469702621 | 23 | ICXS IC,DIG,CMOS,EPLD,SMT, 28PLCC,N H | 1 | CY7C330-50JC | CYPR |
| 0469702623 | 25 | ICXT IC,DIG,CMOS,EPLD,SMT, 24WSO,NH ,16 MACRO CELLS | 1 | EP610SC-30 | ALTA |
| 1010100027 | 33 | LDS DVC,OPTCPLR,QUAD,IF=50MA, BV=2 .5KV,SMT,16SOIC | 8 | PS2701-4 | NEC |
| 1849700131 | 30 | CRYT OSC,XTAL,HCMOS,3.6864MHZ, .01% ,100PPM,SMT | 1 | JS53@3.6864MHZ | CONW |
| 240060-5 | 26 | SWTX SWITCH,RTRY,HEX,R/A,COMPLIMENT | 2 | DRD16CRA | AUGAT ALCO SWITCH |
| 250115-1 | 21 | CONT CONN,PIN,DIN 41612,C,RTANG,96P | 3 | PC96-03302-100 | METHODE ELECTRONICS |
| | | | | C-96M-C1A-2SN | AEG-INTERMAS |
| | | | | 533 402 | ERNI |
| | | | | 860939671137650 | SOURIAU |
| | | | | 7296-50C2TH | 3M |
| | | | | 161-99630-3008 | THOMAS&BETTS |
| 310102-6 | 37 | CRYS XTAL OSC,HCMOS/TTL,16MHZ,0.01% STB,SMT | 1 | NTH06HC-16.000MHZ | SARONIX |
| | | | | SG-615-16.000MHZ | EPSON AMERICA INC |
| | | | | VF315-16.000MHZ | VALPEY-FISHER |
| | | | | FSO-16.000MHZ | FOX ELECTRONICS |
| | | | | SG-615P-16.000MHZ | EPSON AMERICA INC (ALTERN ATE) |
| | | | | FSO-2-16.000MHZ | FOX ELECTRONICS (ALTERNAT E) |
| 49800126 | 1 | REF DRAWING,AUI | 0 | | |
| 49800127-1 | 2 | PCBX PWB,AUI | 1 | | |
| 49800128-1 | 3 | REF SCHEMATIC,AUI | 0 | | |
| 540100-1 | 38 | DIOS TVS,BIDIRECTIONAL,5VDC(VR),600 W(PW),DO-214AA | 64 | SMBJ5.0CA | GENERAL SEMICONDUCTOR IND |
| | | | | SMBJ5.0CA | MICROSEMI CORP |
| 560101-2 | 31 | DIOT DIODE,LED-QUAD,RED,PCB MNT,3MA ,@5VDC | 10 | 555-4007 | DIALIGHT |
| 571249-1 | 36 | ICXS IC,SCC2698B,UART,CMOS,OCTAL,PL CC84 | 4 | SCC2698BC1A84 | PHILIPS SEMICONDUCTOR |
| 571253-1 | 13 | ICXS IC,75ALS173,RCVR,LN,RS-422A/RS -485,QUAD,DIP16 | 8 | SN75ALS173N | TEXAS INSTRUMENTS |
| 571255-1 | 15 | ICXS IC,80C31,CMOS,M-CNTLLR,8-BIT,2 4MHZ,OTP,PLCC44 | 1 | SC80C31BCPA44 | PHILIPS SEMICONDUCTOR [1] |
| | | | | PCB80C31BH4-24WP | PHILIPS SEMICONDUCTOR [2] |
| 57320-14 | 12 | ICXS IC,74LS14,INV,SCHMITT-TRIGGER, HEX,SO14 | 1 | SN74LS14D | TEXAS INSTRUMENTS |
| | | | | SN74LS14D | MOTOROLA |

| | | | | |
|---|---|---|---|---|
| | | | DM74LS14M | NSC |
| 5762019-10 | 32 | ICXS IC,PAL20L8,40X64&AR,20IN/8OUT, 10NS,PLCC28 | 1 PAL20L8-10JC | AMD |
| | | | TIBPAL20L8-10CFN | TEXAS INSTRUMENTS |
| 58010-38 | 8 | ICXS IC,74F38,BUFF,NAND,2-INPUT,OC, QUAD,SO14 | 1 N74F38D | PHILIPS/SIGNETICS |
| | | | 74F38SC | NSC |
| | | | SN74F38D | TEXAS INSTRUMENTS |
| 58220-32 | 6 | ICXT IC,74AS32,OR-GATE,TWO-INPUT,QU AD,SO14 | 1 SN74AS32D | TEXAS INSTRUMENTS |
| | | | DM74AS32M | NSC |
| 58220-641 | 20 | ICXS IC,74AS641,XCVR,BUS,OCTAL,OC,S O20 | 1 SN74AS641DW | TEXAS INSTRUMENTS |
| 58408-374 | 17 | ICXS IC,74ABT374,F/F,D-TYPE,OCTAL,T S,SO20 | 2 74ABT374D | PHILIPS/SIGNETICS |
| | | | SN74ABT374DW | TEXAS INSTRUMENTS |
| 58408-534 | 18 | ICXS IC,74ABT534,F/F,D-TYPE,OCTAL,T S,INV,SO20 | 10 74ABT534D | PHILIPS/SIGNETICS |
| | | | SN74ABT534DW | TEXAS INSTRUMENTS |
| 58450-138 | 9 | ICXS IC,74FCT138AT,DEC/DEMUX,1-OF-8 ,W/ENABLE,SO16 | 2 IDT74FCT138ATSO | IDT |
| | | | CY74FCT138ATSOC | CYPRESS |
| 58451-541 | 10 | ICXS IC,74FCT541T,BUFF/DRVR,OCTAL,T S,SO20 | 2 IDT74FCT541TSO | IDT |
| | | | PI74FCT541TS | PERICOM SEMICONDUCTOR |
| | | | QS74FCT541TSO | QUALITY SEMICONDUCTOR |
| | | | CY74FCT541TSOC | CYPRESS |
| 58451-573 | 11 | ICXS IC,74FCT573T,LATCH,TRNSPRNT,OC TAL,TS,SO20 | 9 IDT74FCT573TSO | IDT |
| | | | PI74FCT573TS | PERICOM SEMICONDUCTOR |
| | | | QS74FCT573TSO | QUALITY SEMICONDUCTOR |
| | | | CY74FCT573TSOC | CYPRESS |
| 5851220-20 | 24 | ICXT IC,1220,SRAM,16K,NONVOLATILE,2 00NS | 1 DS1220Y-200 | DALLAS SEMICONDUCTOR |
| 58527020-12 | 4 | ICXT IC,27C020,UVEPROM,CMOS,256KX8, 120NS,DIP632 | 1 AM27C020-120DC | AMD |
| | | | TMS27C020-12JL | TEXAS INSTRUMENTS |
| | | | M27C2001-12F1 | SGS-THOMSON |
| 58527512-20 | 5 | ICXT IC,27C512,UVEPROM,CMOS,64KX8,2 00NS,TS,DIP628 | 1 AM27C512-200DC | AMD |
| | | | M27C512-20F1 | SGS-THOMSON |
| | | | TC57512AD-20 | TOSHIBA |
| | | | TMS27C512-20J | TEXAS INSTRUMENTS |
| 5856287-25 | 22 | ICXT IC,7C187,SRAM,CMOS,64KX1,25NS | 1 CY7C187-25PC | CYPRESS |
| | | | IDT7187S25P | IDT [OBSOLETE] |
| | | | M5M5187AP-25 | MITSUBISHI |
| | | | LH5261-25 | SHARP |
| | | | HM3-65787H-5 | HARRIS |
| | | | KM6165P-25 | SAMSUNG |
| | | | CY7C187-15PC | CYPRESS [ALTERNATE] |
| 5857007-25 | 27 | ICXS IC,IDT7007,DPSRAM,CMOS,32KX8,2 5NS,TS,TQFP80 | 1 IDT7007L25PF | IDT |
| | | | IDT7007S25PF | IDT (ALTERNATE) |
| 5857130-45J | 28 | ICXS IC,7130SA,DUAL-PORT SRAM,CMOS, 1KX8,52PLCC | 2 IDT7130SA-35J | IDT |
| 5857202-35 | 29 | ICXS IC,7202,FIFO,CMOS,ASYNCH,1KX9, TS,35NS,PLCC32 | 6 IDT7202LA35J | IDT |
| | | | KM75C02AJ-35 | SAMSUNG |
| | | | AM7202-35JC | AMD/MMI |
| | | | LH5497U-35 | SHARP |
| 6922110000 | 35 | FLOS RES,FIX,TF,1KOHM,1%,.125W ,100 PPM,SMT,CHIP,NM | 32 CR32-1001-F-T | AVX CORPORATION |
| 810101-100 | 34 | FLOS RES,CHIP,THCK-FLM,10 OHMS,1/8W | 128 CRCW1206100JRT2 | DALE ELECTRONICS |

| | | |
|---|---|---|
| ,5%,SMD1206 | RM73B2BTE100J | KOA SPEER |
| | 9C12063A10R0JL | PHILIPS COMPONENTS |

1 records listed.

LORAL
Test & Information Systems

P.O. Box 3041
Sarasota, FL 34230
(941) 371-0811
Fax: (941) 378-1893

September 28, 1995

Brevard Community College
Center of Community Innovation
250 Grassland Rd S.E.
Palm Bay, FL 32909

Attention: Mr. Jarad Whitcomb

**Subject: BCC PO #610, TRDA #410; ADAS Milestone #4**

Enclosure: (1) Schematics of Output Card Design

Dear Mr. Whitcomb:

Milestone #4 to the subject contract which states "Complete the CAD Schematic Design of the Output Card" has been completed. The Output Card Schematics (Receive and Transmit) are enclosed. Our invoice for this milestone will be submitted under separate cover.

If you have any other questions regarding this matter, please do not hesitate to contact me at 813-377-5538, or by fax at 813-378-6905

Very truly yours,

LORAL TEST & INFORMATION SYSTEMS

Stephen G. Carroll
Manager, Contracts

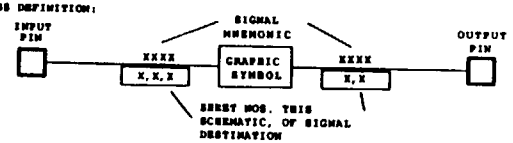
cc: Matt LaVigne, TRDA

| COMPONENT CHART | |
|---|---|
| LAST DES USED | UNUSED NUMBER |
| | |
| | |
| | |
| | |
| | |
| | |
| | |
| | |
| | |
| | |

| REVISIONS | | | | |
|---|---|---|---|---|
| SYM. | DESCRIPTION | APPROVAL | DATE | APPROVED |
| - | - | - | - | |

5. INFORMATION FOR THIS DRAWING IS CONTAINED IN CADD DATABASE 899-XXXXX-00.

4. ADDRESS DEFINITION:




3. CIRCUIT RETURN SYMBOLS:


2. FOR TOLERANCES AND RATINGS SEE PARTS LIST.

1. RESISTOR VALUES ARE IN OHMS, CAPACITOR VALUES ARE IN MICROFARADS.

UNLESS OTHERWISE SPECIFIED:
NOTES:

CONCEPT REV -

DRAWING

TITLE=PIORCVR
ABBREV=PIORCVR

LAST_MODIFIED=Tue Sep 26 11:37:08 1995

| | | | | | |
|---|---|---|---|---|---|
| | -1 | - | 550 | DRAWN BY - | DATE |
| | CONFIG. | NEXT ASSY. NO. | USED ON | DESIGNER - | |
| SIMILAR TO | APPLICATION | | | CHECKER - | |
| | | | | DESIGN ENGINEER - | |
| | | | | PROJECT ENGINEER - | |
| | | | | APPROVED - | APPROVED - |
| | | | | APPROVED - | Q.A. - |



LORAL
TEST & INFORMATION SYSTEMS
P.O. Box 3041
Sarasota, FL 34230

# SCHEMATIC, PWA
## PIO RECEIVER

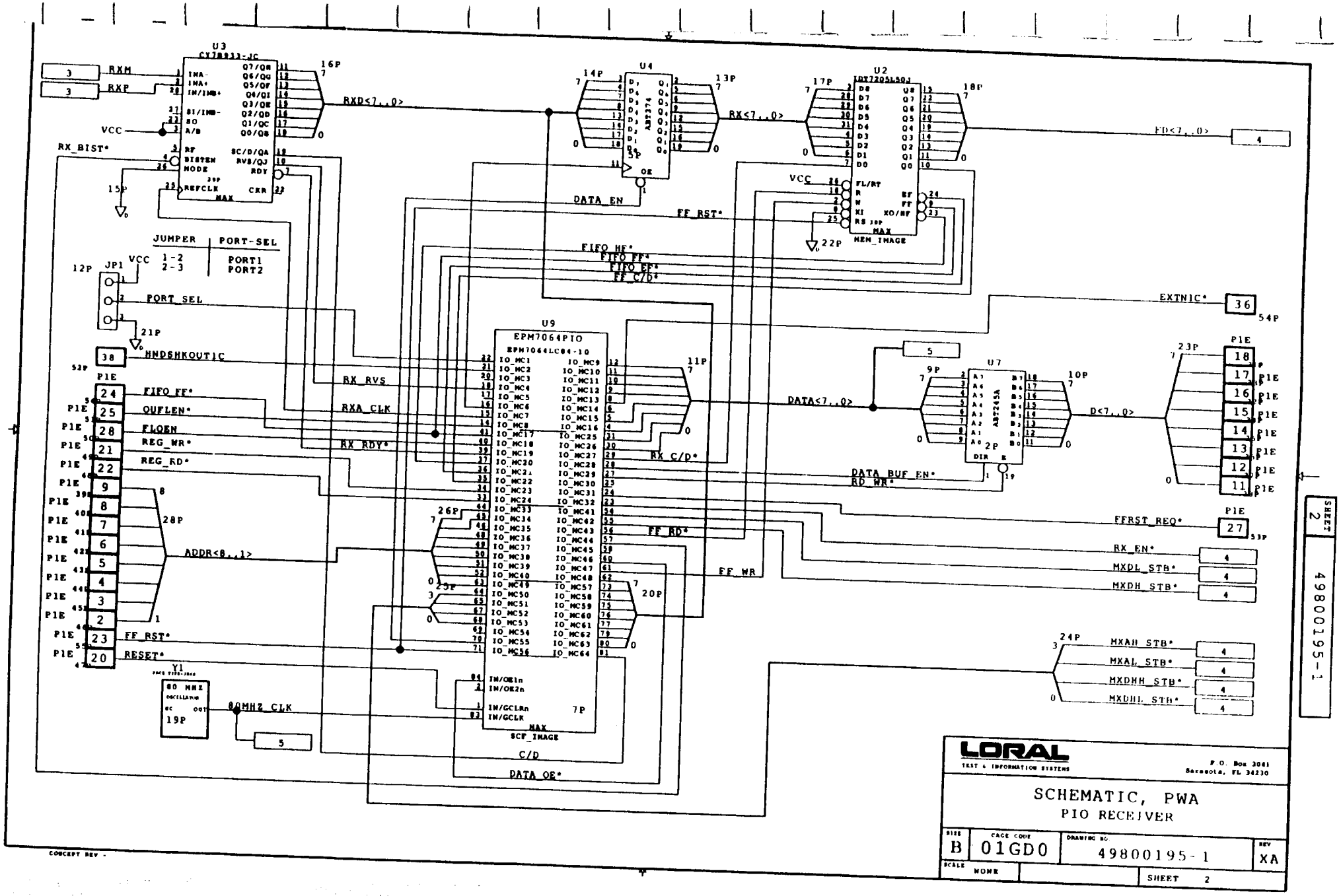
| SIZE | CAGE CODE | DRAWING NO. | REV |
|---|---|---|---|
| B | 01GD0 | 49800195-1 | XA |

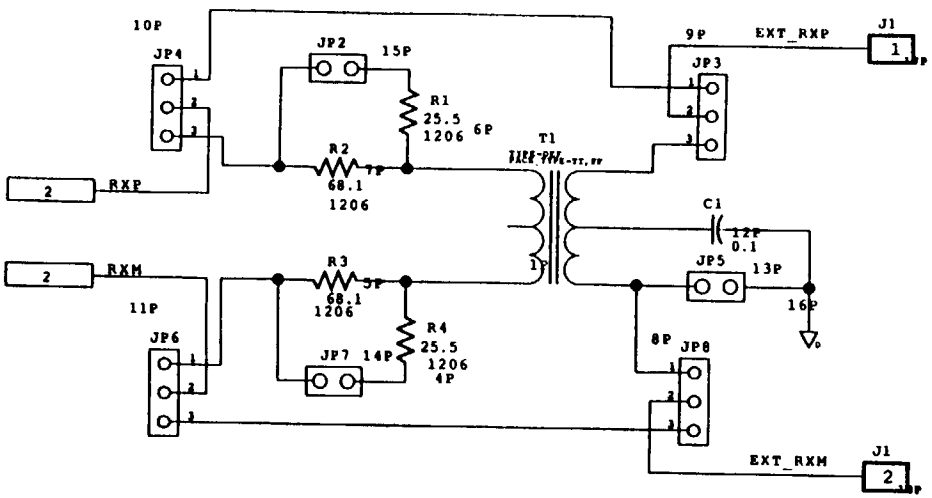
SCALE NONE

SHEET 1 OF 5

SHEET 1

49800195-1


U3
CY7B933-JC
RXM
RXP
VCC
RX_BIST*
RXD<7..0>
16P
U4
14P
13P
RX<7..0>
U2
17P
18P
FD<7..0>
4
DATA_EN
FF_RST*
FIFO_HF*
FIFO_FF*
FIFO_EF*
FF_C/D*
22P
MEM_IMAGE
JUMPER
PORT-SEL
1-2
2-3
PORT1
PORT2
JP1
12P
PORT_SEL
21P
HNDSHKOUT1C
38
52P
P1E
EXTNIC*
36
54P
U9
EPM7064PIO
EPM7064LC84-10
RX_RVS
RXA_CLK
RX_RDY*
11P
RX_C/D*
U7
9P
10P
DATA<7..0>
D<7..0>
23P
DATA_BUF_EN*
RD_WR*
2P
FIFO_FF*
OUFLEN*
FLOEN
REG_WR*
REG_RD*
28P
ADDR<8..1>
FF_RD*
FF_WR
FFRST_REQ*
27
53P
RX_EN*
MXDL_STB*
MXDH_STB*
24P
MXAH_STB*
MXAL_STB*
MXDHH_STB*
MXDHL_STB*
FF_RST*
RESET*
Y1
80 MHZ
19P
80MHZ_CLK
5
26P
25P
20P
7P
MAX
SCF_IMAGE
C/D
DATA_OE*
LORAL
TEST & INFORMATION SYSTEMS
P.O. Box 3041
Sarasota, FL 34230
SCHEMATIC, PWA
PIO RECEIVER
SIZE
B
CAGE CODE
01GD0
DRAWING NO
49800195-1
REV
XA
SCALE
NONE
SHEET 2
SHEET 2
49800195-1




LORAL
TEST & INFORMATION SYSTEMS

P.O. Box 3041
Sarasota, FL 34230

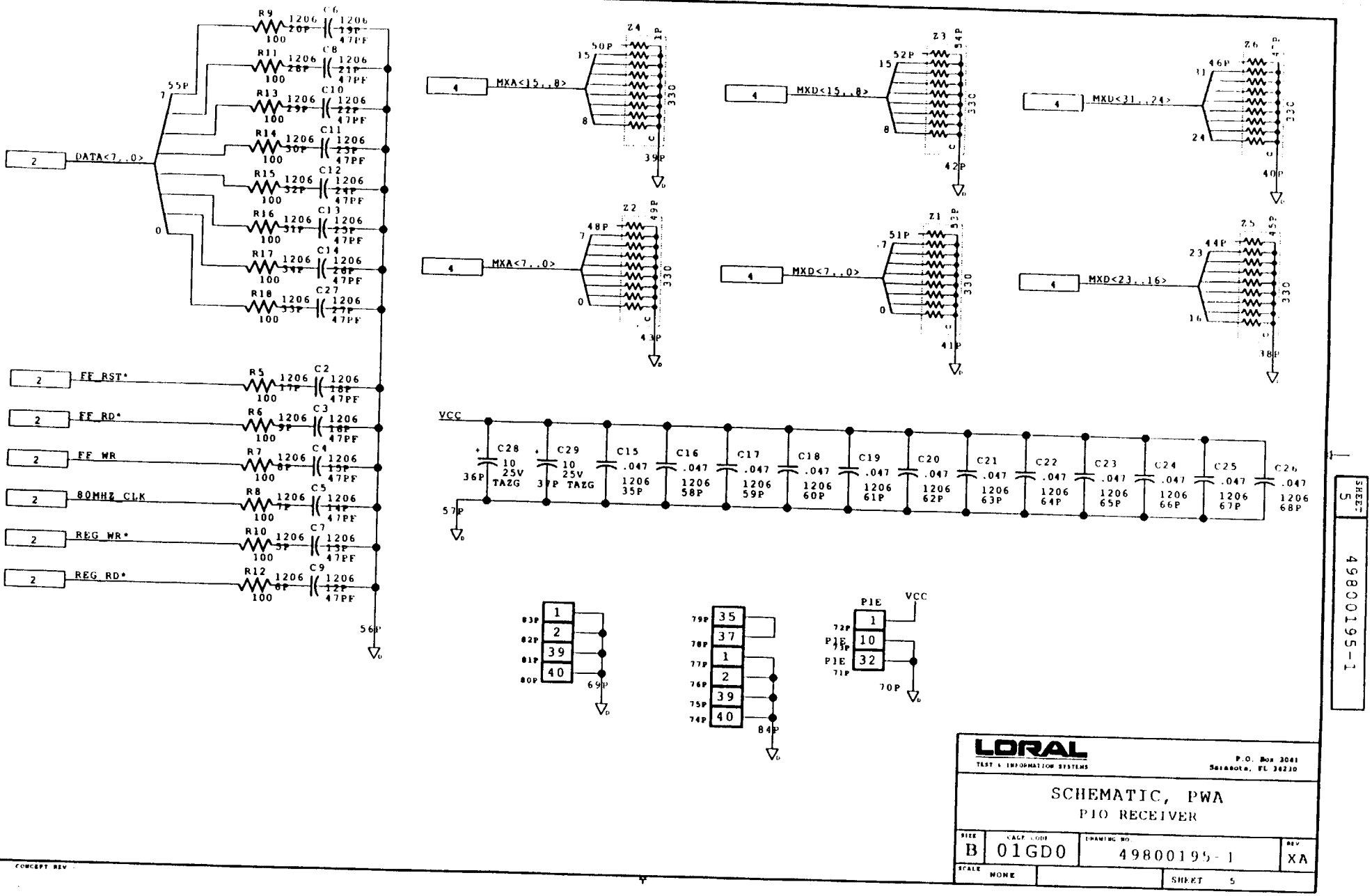
SCHEMATIC, PWA
PIO RECEIVER

| SIZE | CAGE CODE | DRAWING NO. | REV |
|---|---|---|---|
| B | 01GD0 | 49800195-1 | XA |
| SCALE NONE | | SHEET 3 | |

SHEET 3

49800195-1

CONCEPT REV




LORAL
TEST & INFORMATION SYSTEMS
P.O. Box 3041
Sarasota, FL 34230

SCHEMATIC, PWA
PIO RECEIVER

| SIZE | CAGE CODE | DRAWING NO | REV |
|---|---|---|---|
| B | 01GD0 | 49800195-1 | XA |

SCALE NONE | SHEET 5

SHEET 5

49800195-1

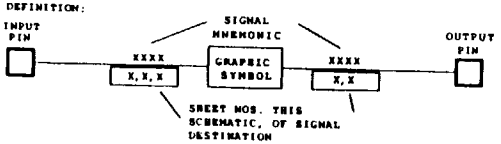
CONCEPT REV

| COMPONENT CHART | |
|---|---|
| LAST NO. USED | UNUSED NUMBER |
| C | |
| R | |
| E | |
| T | |
| L | |
| P | |
| Q | |
| K | |
| S | |
| T | |
| TP | |
| U | |

| REVISIONS | | | | |
|---|---|---|---|---|
| SYM | DESCRIPTION | APPR. ENGR. | DATE | APPROVED |
| - | - | | | |

5. INFORMATION FOR THIS DRAWING IS CONTAINED IN CADD DATABASE 899-XXXXX-00.

4. ADDRESS DEFINITION:




3. CIRCUIT RETURN SYMBOLS:


2. FOR TOLERANCES AND RATINGS SEE PARTS LIST.

1. RESISTOR VALUES ARE IN OHMS, CAPACITOR VALUES ARE IN MICROFARADS.

UNLESS OTHERWISE SPECIFIED:
NOTES:

DRAWING

TITLE=PIOXMTR
ABBREV=PIOXMTR

LAST_MODIFIED=Tue Sep 26 09:53:53 1995

| | | | |
|---|---|---|---|
| | -1 | - | 550 |
| | CONFIG. | NEXT ASSY. NO. | USED ON |
| SIMILAR TO | APPLICATION | | |



| | | DATE |
|---|---|---|
| DRAWN BY | - | |
| DESIGNER | - | |
| CHECKED | - | |
| DESIGN ENGINEER | - | |
| PROJECT ENGINEER | - | |
| APPROVED | - | |
| APPROVED | - | |
| APPROVED | - | |

LORAL
TEST & INFORMATION SYSTEMS
P.O. Box 3041
Sarasota, FL 34230

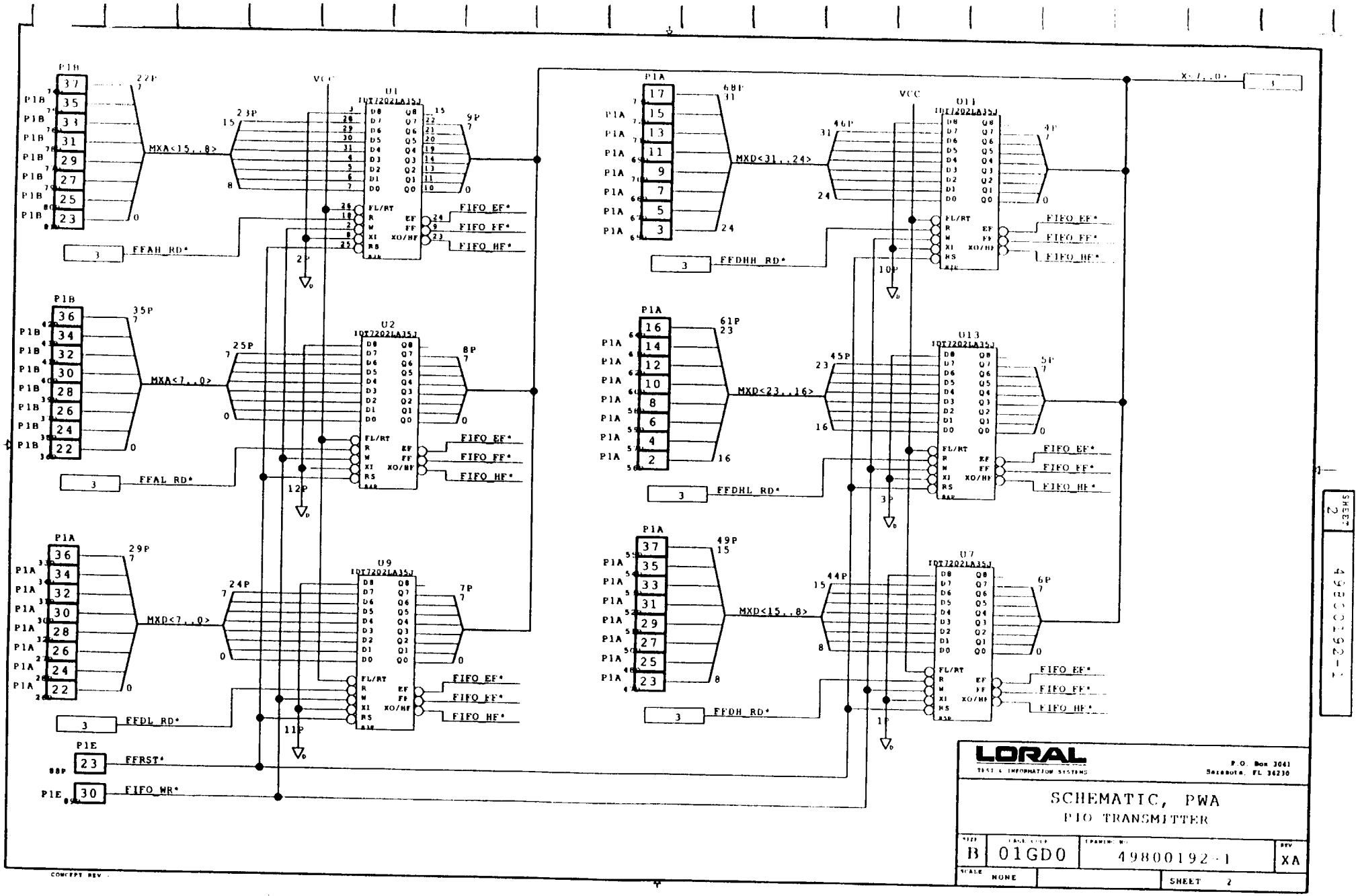
# SCHEMATIC, PWA
## PIO TRANSMITTER

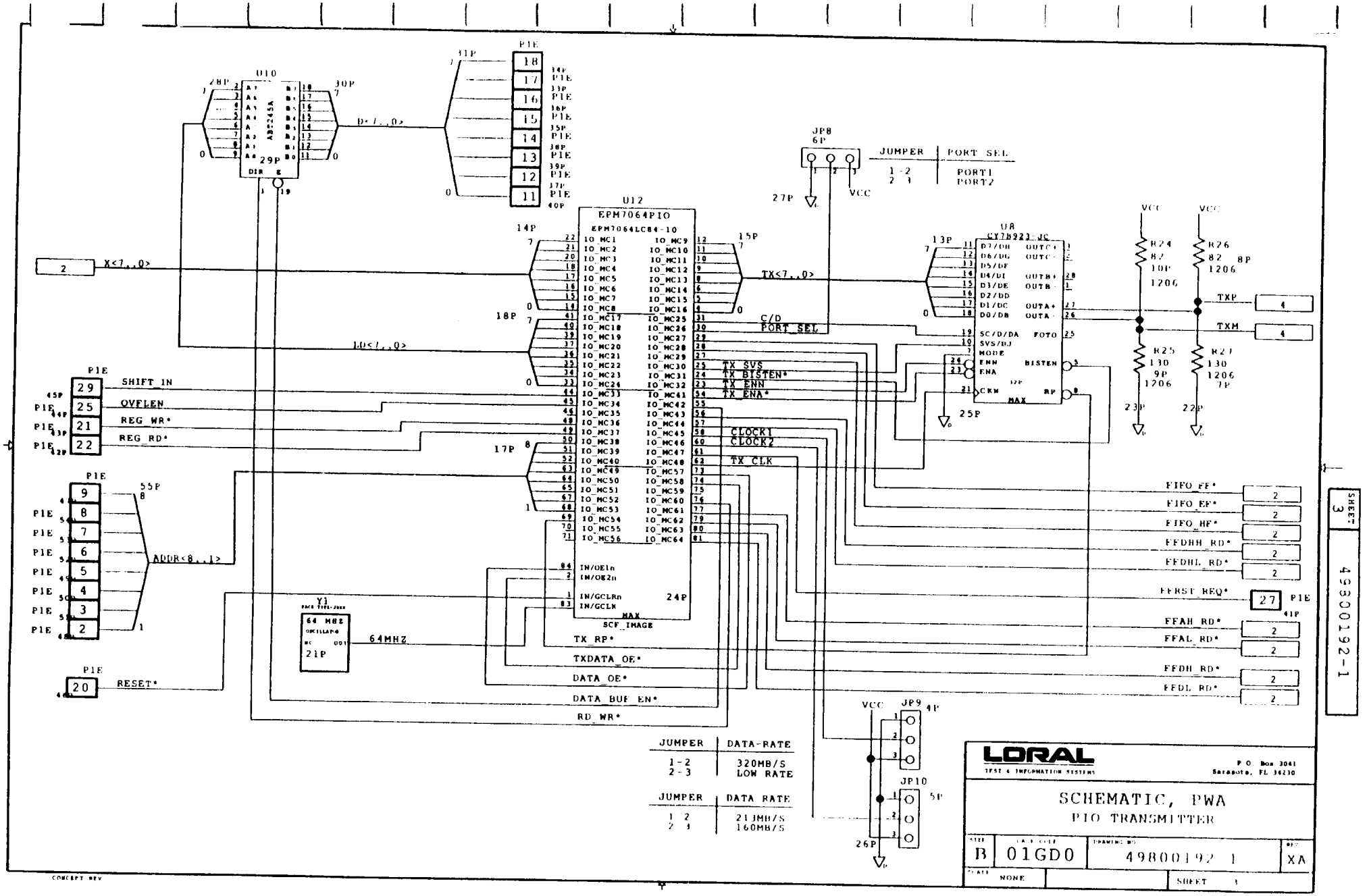
| SIZE | CAGE CODE | DRAWING NO. | REV |
|---|---|---|---|
| B | 01GD0 | 49800192 1 | XA |
| SCALE NONE | | SHEET 1 OF 5 | |

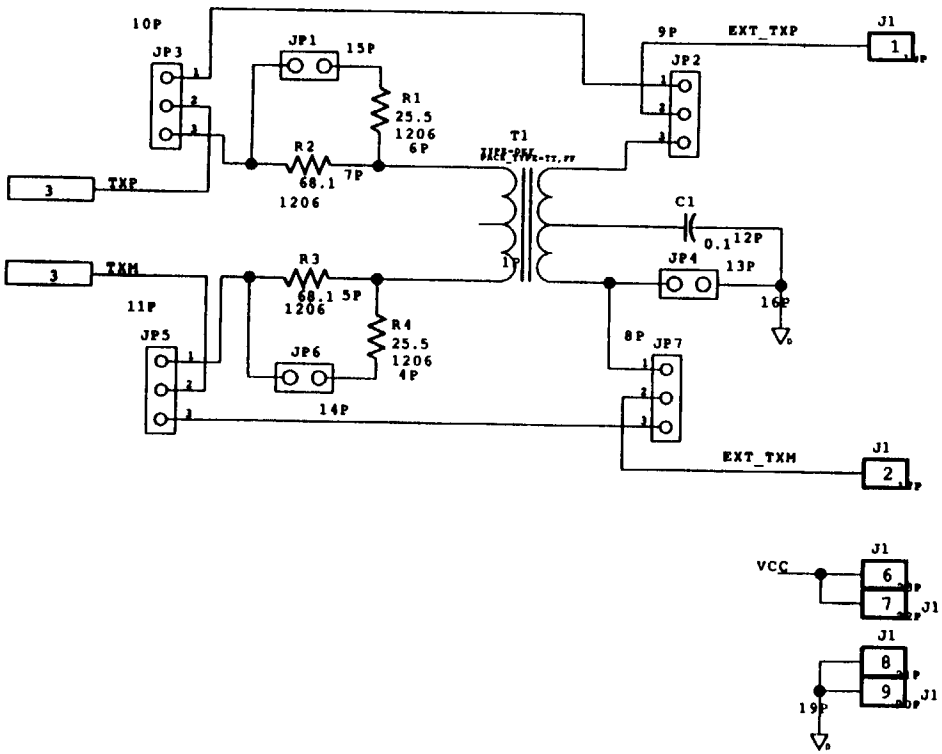
CONCEPT REV

SHEET 1

49800192-1


P1B
P1A
P1E
MXA<15..8>
MXA<7..0>
MXD<31..24>
MXD<23..16>
MXD<15..8>
MXD<7..0>
FFAH_RD*
FFAL_RD*
FFDHH_RD*
FFDHL_RD*
FFDH_RD*
FFDL_RD*
FFRST*
FIFO_WR*
FIFO_EF*
FIFO_FF*
FIFO_HF*
U1
U2
U3
U7
U9
U11
U13
IDT7202LA35J
VCC
LORAL
TEST & INFORMATION SYSTEMS
P.O. Box 3041
Sarasota, FL 34230
SCHEMATIC, PWA
PIO TRANSMITTER
B
01GD0
49800192-1
XA
NONE
SHEET 2
SHEET 2
49800192-1


U10
AB245A
U12
EPM7064PIO
EPM7064LC84-10
U8
CY7B921-JC
MAX
SCF_IMAGE
X<7..0>
D<7..0>
LD<7..0>
TX<7..0>
C/D
PORT_SEL
SHIFT_IN
OVFLEN
REG_WR*
REG_RD*
ADDR<8..1>
RESET*
64MHZ
TX_SVS
TX_BISTEN*
TX_ENN
TX_ENA*
CLOCK1
CLOCK2
TX_CLK
TX_RP*
TXDATA_OE*
DATA_OE*
DATA_BUF_EN*
RD_WR*
FIFO_FF*
FIFO_EF*
FIFO_HF*
FFDHH_RD*
FFDHL_RD*
FFRST_REQ*
FFAH_RD*
FFAL_RD*
FFDH_RD*
FFDL_RD*
TXP
TXM
JP8
JUMPER | PORT SEL
1-2 | PORT1
2-3 | PORT2
JP9
JP10
JUMPER | DATA-RATE
1-2 | 320MB/S
2-3 | LOW RATE
JUMPER | DATA RATE
1 2 | 213MB/S
2 3 | 160MB/S
LORAL
TEST & INFORMATION SYSTEMS
P.O. Box 3041
Sarasota, FL 34230
SCHEMATIC, PWA
PIO TRANSMITTER
SIZE B
CAGE CODE 01GD0
DRAWING NO 49800192 1
REV XA
SHEET 3
SHEET 3
49800192-1

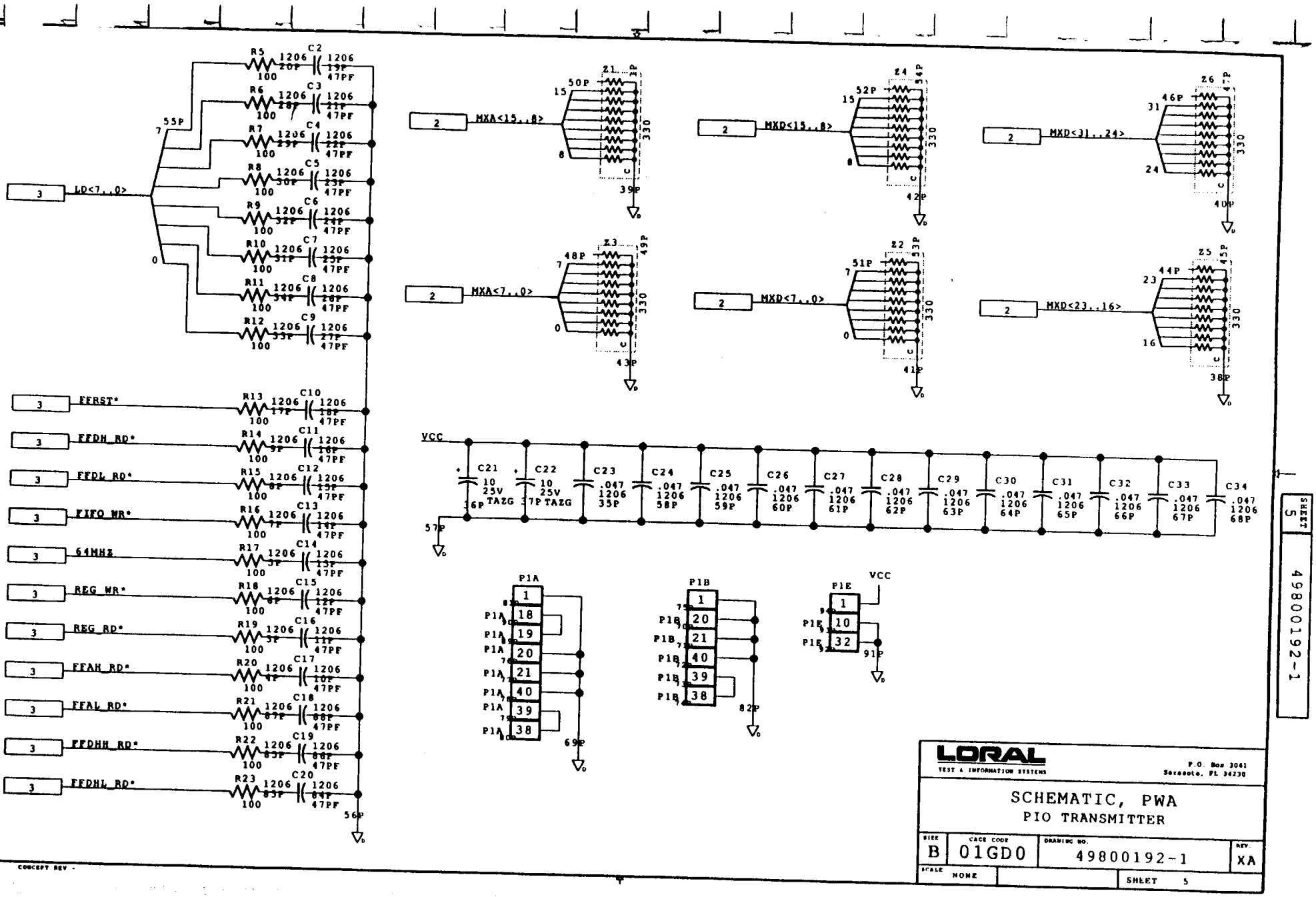



| | | | |
|---|---|---|---|
| LORAL TEST & INFORMATION SYSTEMS | | P.O. Box 3041 Sarasota, FL 34230 | |
| SCHEMATIC, PWA<br>PIO TRANSMITTER | | | |
| SIZE B | CAGE CODE 01GD0 | DRAWING NO. 49800192-1 | REV. XA |
| SCALE NONE | | SHEET 4 | |

SHEET 4

49800192-1

CONCEPT REV -


R5 1206 100 20P C2 1206 47PF
R6 1206 100 C3 1206 47PF
R7 1206 100 25P C4 1206 47PF
R8 1206 100 30P C5 1206 47PF
R9 1206 100 32P C6 1206 47PF
R10 1206 100 31P C7 1206 47PF
R11 1206 100 34P C8 1206 47PF
R12 1206 100 33P C9 1206 47PF
3 LD<7..0>
7 55P
0
R13 1206 100 17P C10 1206 47PF
R14 1206 100 9P C11 1206 47PF
R15 1206 100 8P C12 1206 47PF
R16 1206 100 7P C13 1206 47PF
R17 1206 100 3P C14 1206 47PF
R18 1206 100 6P C15 1206 47PF
R19 1206 100 5P C16 1206 47PF
R20 1206 100 4P C17 1206 47PF
R21 1206 100 87P C18 1206 47PF
R22 1206 100 83P C19 1206 47PF
R23 1206 100 83P C20 1206 47PF
3 FFRST*
3 FFDH_RD*
3 FFDL_RD*
3 FIFO_MR*
3 64MHZ
3 REG_WR*
3 REG_RD*
3 FFAH_RD*
3 FFAL_RD*
3 FFDHH_RD*
3 FFDHL_RD*
56P
Z1 50P 15 8 330 39P
Z4 52P 15 8 330 42P
Z6 46P 31 24 330 40P
2 MXA<15..8>
2 MXD<15..8>
2 MXD<31..24>
Z3 48P 7 0 330 43P
Z2 51P 7 0 330 41P
Z5 44P 23 16 330 38P
2 MXA<7..0>
2 MXD<7..0>
VCC
C21 10 25V TAZG 16P
C22 10 25V TAZG 37P
C23 .047 1206 35P
C24 .047 1206 58P
C25 .047 1206 59P
C26 .047 1206 60P
C27 .047 1206 61P
C28 .047 1206 62P
C29 .047 1206 63P
C30 .047 1206 64P
C31 .047 1206 65P
C32 .047 1206 66P
C33 .047 1206 67P
C34 .047 1206 68P
57P
P1A 1 18 19 20 21 40 39 38 69P
P1B 1 20 21 40 39 38 82P
P1E 1 10 32 91P
VCC
CONCEPT REV .
LORAL
VEST & INFORMATION SYSTEMS
P.O. Box 3041 Sarasota, FL 34230
SCHEMATIC, PWA
PIO TRANSMITTER
SIZE B
CAGE CODE 01GD0
DRAWING NO. 49800192-1
REV. XA
SCALE NONE
SHEET 5
SHEET 5
49800192-1

# ADAS MILESTONES (TRDA 410 / LMTI SO 22049)

1. 03/30/96 - Complete — Complete the ordering of the materials for the Input Card manufacturing and testing based on 90% P.L. Input design package to LMTI.

   STATUS 10/30/96: All parts for the Input Card have been purchased and received by LMTI.

2. 09/29/95 - Complete — Complete the CAD Schematic Design of the Input Card.

   STATUS 10/30/96: Schematics have been completed.

3. 04/30/96 - Complete — Complete the Input Card PC Board Fabrication.

   STATUS 10/30/96: The fabrication of the Input Cards has been completed, and 2 units have been delivered.

4. 09/29/95 - Complete — Complete CAD Schematic Design of the Output Card.

   STATUS 10/30/96: The Schematics have been completed.

5. 10/29/96 - Complete — Complete the Output Card PC Board Fabrication.

   STATUS 10/30/96: The fabrication of the Output Card has been completed, and the card has been delivered.

6. 10/30/96 - Complete — ADAS System Test. In conjunction with NASA-KSC, Complete the final design, testing and acceptance of the total ADAS.

   STATUS 10/30/96: System integration and test has been completed.

# TRDA /Brevard Contracts Status

- **All items on both contracts have been completed**
  - ≈ ***Pilot Production USCA's delivered to NASA***
  - ≈ ***Engineering development completed and released to production***
  - ≈ ***USCA 5200R***
  - ≈ ***Tag Ram***
  - ≈ ***Universal Input Module***
  - ≈ ***PIO with Hot Link fiber optic Interface***
  - ≈ ***ADAS 5000 System with IRIG***
  - ≈ ***ACA Software Control Package***

# TRDA / Brevard Contract Status

- USCA's
- Manufactured in Florida
- Assembled and Tested in Florida
- Shipped to San Diego for Final Integration and test
- 50 USCA 5200R units delivered to NASA
  - ≈ *In test at the Launch Equipment Test Facility*
- LMTI received orders for 250 USCA 5200R from NASA - Option for additional 800 USCA's
  - ≈ *Qualification Testing in process at Launch Equipment Test Facility*

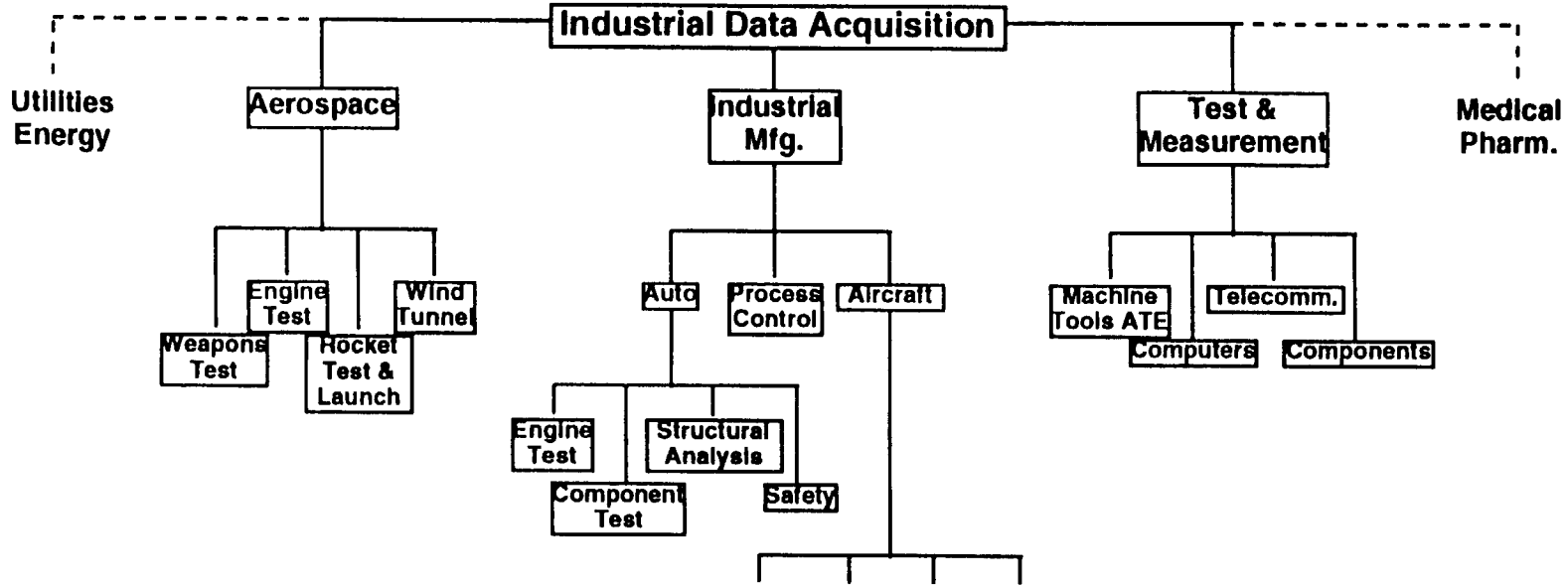
# Commercial Product Status

- **AEDC - Sverdrup Purchased 1 unit for evaluation**
  - ≈ ***Test Cell Upgrade Program***
  - ≈ ***Possible 7000 Units over 5 years***
  - ≈ ***Funding - October '97***

# Commercial Product Status

- **Marketing Survey**
  - ≈ *Reduce Life Cycle Costs*
  - ≈ *Reduce maintenance costs*
  - ≈ *Large number of channels*
  - ≈ *Real Time Data Acquisition*
- **Conjoint Analysis - In Process**
- **Applications - Aerospace Focus**
  - ≈ *Launch Operations* - *Environmental Test*
  - ≈ *Wind Tunnels* - *Engine Test*
  - ≈ *Vibration* - *Acoustic Test Cells*

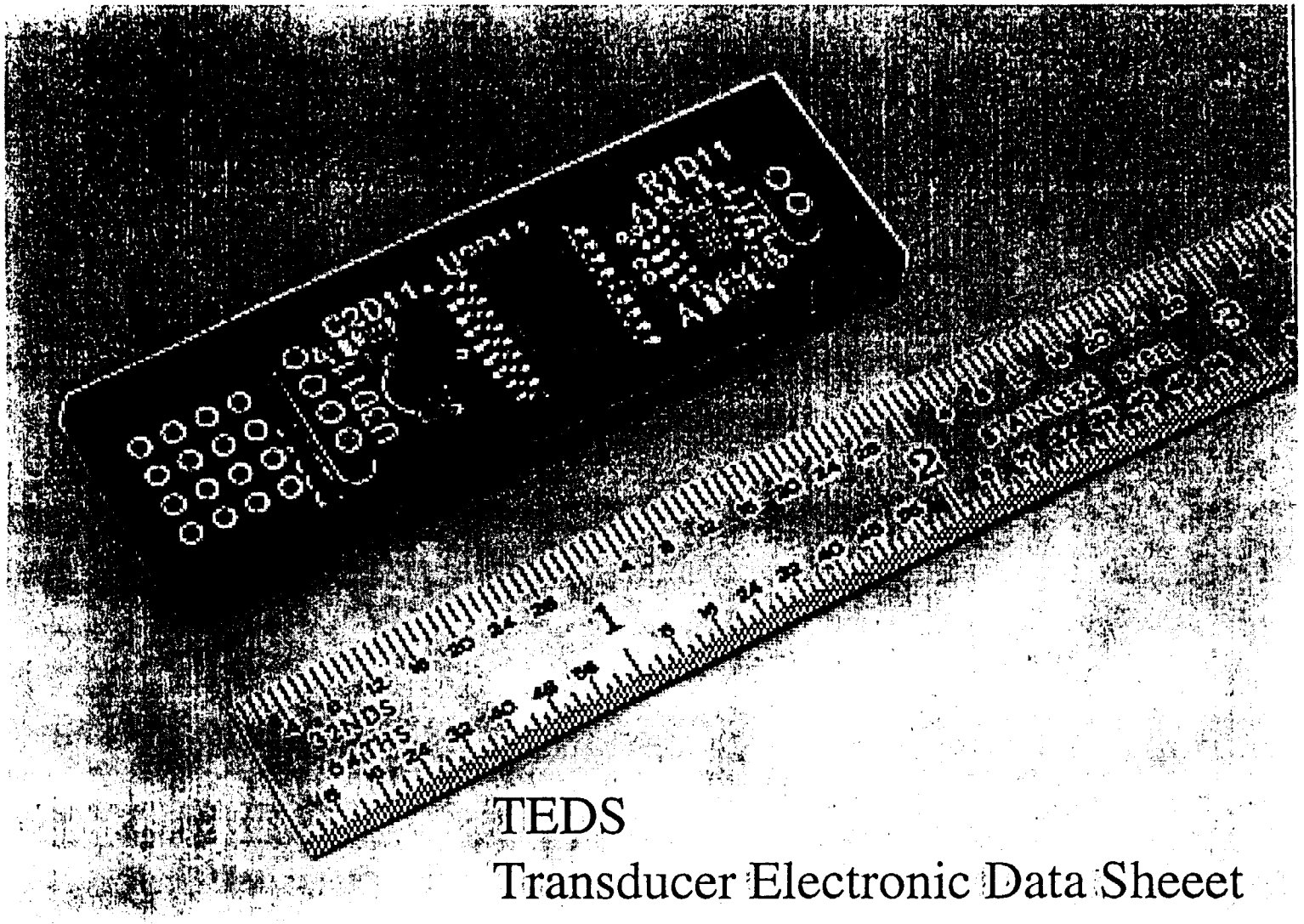
# Market Segments




| | | | | | | | |
|---|---|---|---|---|---|---|---|
| ***Turnkey:*** *40 companies HP = 23% Daytronic Kinetics* | **$20M** | + | **$90M** | + | **$35M** | ⇨ | **$145M** |
| ***Loral Target*** | ○ | | ⊘ | | ⊘ | | |
| ***Front Ends:*** *(Sig. Cond.) VME – 60 companies VXI – 10 companies (HP = 50%)* | **$60M** | + | **$80M** | + | **$30M** | ⇨ | **$170M** |
| ***Loral Target*** | ○ | | ⊘ | | ⊘ | | |

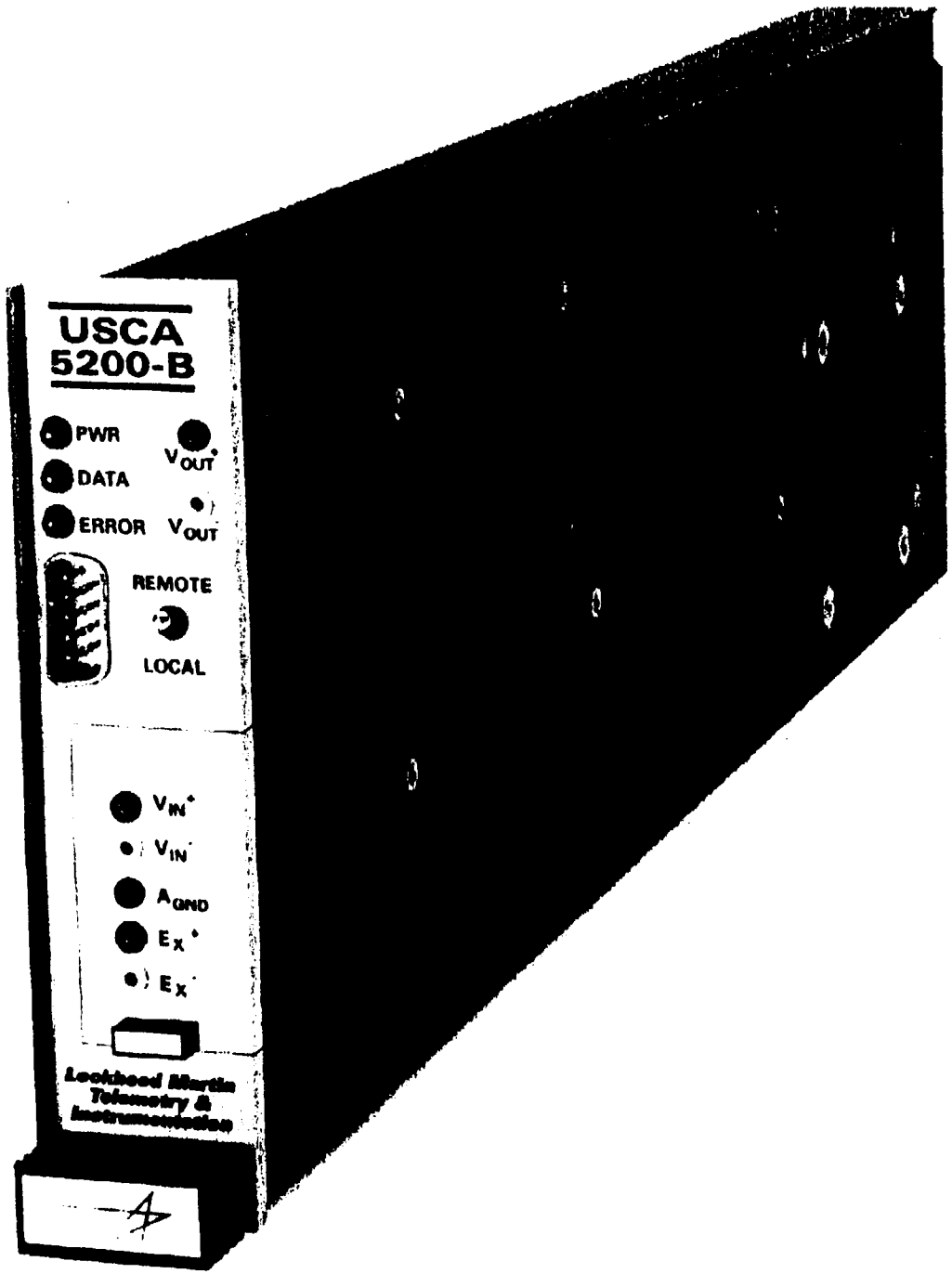
# Commercial Product Status

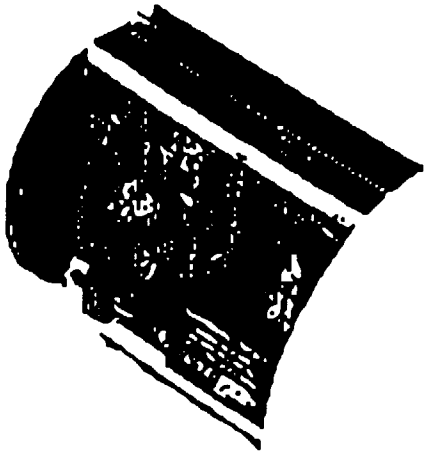
- **Integrated Product Solution**
  - ≈ *End to End Data Acquisition*
  - ≈ *Rack Mount System*
  - ≈ *Lower Cost Per Channel*
  - ≈ *Multiple Inputs*
  - ≈ *6U VME Version*
- **ADAS 5000 Product Line**
  - ≈ *Brochures / Literature Released*
  - ≈ *Price List Established*
  - ≈ *Introduced at Sensors and ITC Shows -- October '96*

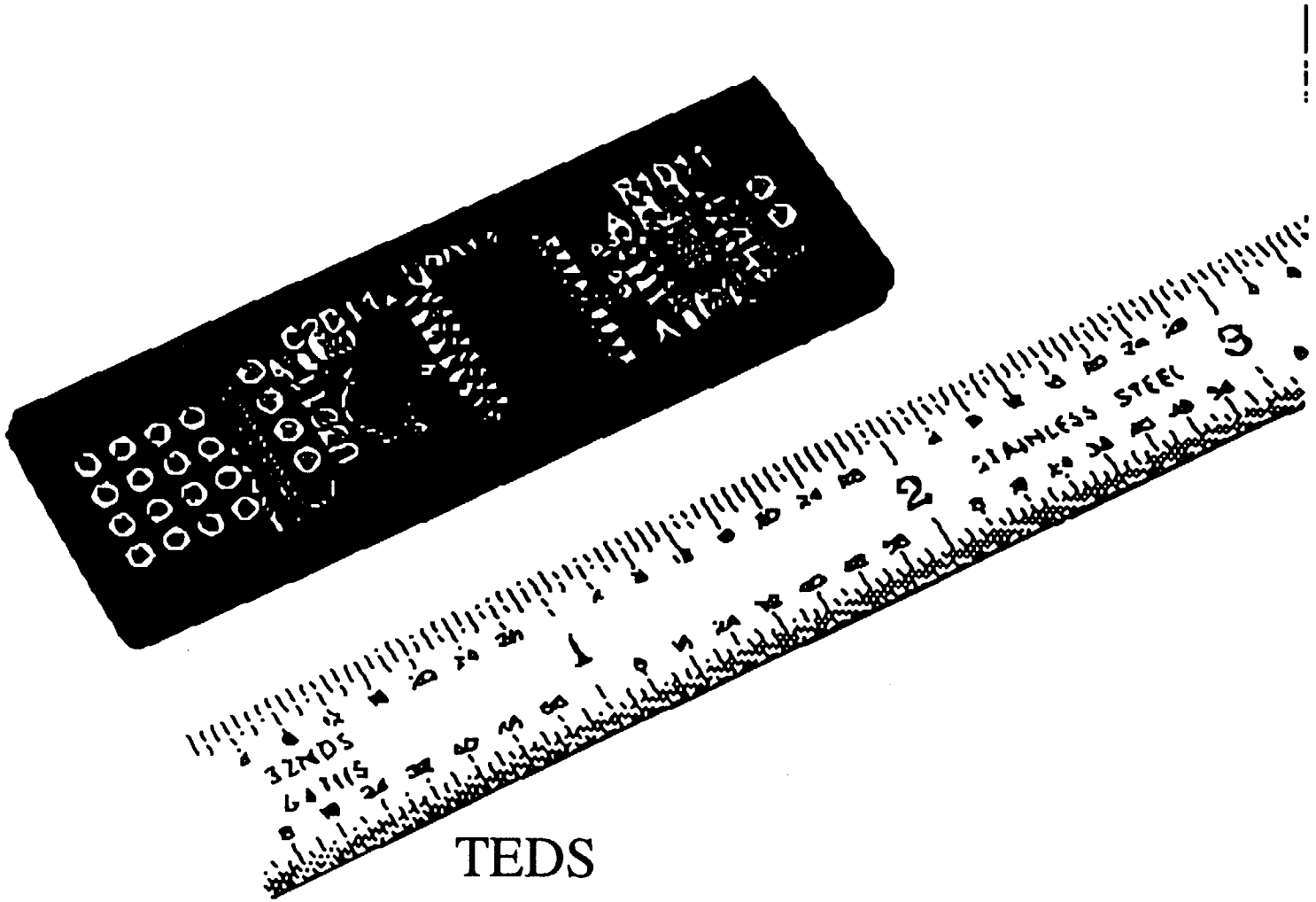


# TEDS

## Transducer Electronic Data Sheeet


USCA
5200-B
PWR
DATA
ERROR
$V_{OUT}^{+}$
$V_{OUT}^{-}$
REMOTE
LOCAL
$V_{IN}^{+}$
$V_{IN}^{-}$
$A_{GND}$
$E_X^{+}$
$E_X^{-}$
Lockheed Martin
Telemetry &
Instrumentation






# TEDS
# Transducer Electronic Data Sheet

# Commercialization

- **Board Level USCA USCA 5200B**
  - ≈ *Rack Mount System*
  - ≈ *Mode Card for Bridge Completion*
  - ≈ *DEMO System - May '97*
  - ≈ *ISA Orlando, May 1997*
  - ≈ *Sensors Show Boston, May 1997*
- **Other Improvements**
  - ≈ *Filters, A/D Sample Rate Selections*
  - ≈ *Local Control and Setup through Front Panel*
  - ≈ *Sigma Delta A/D*
  - ≈ *New GUI*

# Marketing - Opportunities

- **Titan Centaur Launch Pad Upgrade**
  - ≈ *Vertical Integration Building*
  - ≈ *Launch Pad*
  - ≈ *Systems Integration Lab*
  - ≈ *300 measurements*
- **EELV Program** expendable heavy launch vehicle
- **NASA MSFC Engine Test Facility**

# SUMMARY

- **Program has taken longer than expected**
  - ≈ ***Design problems and some manufacturing startup problems***
- **Now in Full Production**
- **Excellent potential for the commercial version**
- **Commercial Product Forecast**
  - ≈ ***1997 - $2M***
  - ≈ ***1998 - $5M***
- **Presentation with Brevard and NASA**

# Commercialization of NASA Technology — Universal Signal Conditioning Amplifier (USCA)

## Final Report


## Lockheed Martin Telemetry & Instrumentation

for

Technological Research and Development Authority of Florida

and

Brevard Community College



Reference
BCC PO # 610, TRDA Grant 410
BCC PO # 433, TRDA Grant 405

# General

Lockheed Martin Telemetry & Instrumentation (LMTI) is pleased to report the successful conclusion of the referenced contracts to commercialize a new technology developed by NASA Kennedy Space Center (KSC) that was coupled with existing LMTI products. All contract items have been satisfied.

# Background

LMTI entered a partnership with KSC to transfer NASA technology for the Universal Signal Conditioning Amplifier (USCA) to the commercial sector. Funding for the project was provided jointly by the Technological Research and Development Authority (TRDA) of Florida, Brevard Community College (BCC), NASA, and LMTI. Under the contract with BCC and the TRDA, LMTI was to:

- Provide the resources and perform the commercialization of the USCA prototype developed by NASA KSC
- Provide the resources to adapt the government prototype to a commercially manufactured product
- Produce the government version and incorporate the resulting product into our standard product catalog
- Determine the extent of the USCA market, adapt the prototype design to targeted markets, and develop marketing and manufacturing plans
- Perform a design-to-cost analysis to develop a commercial product manufacturable within the budget constraints of the target market
- Develop and market the resulting commercial product worldwide

An additional underlying goal was to successfully transfer NASA technology to the commercial sector and generate additional business for the people of the state of Florida.

# Status

***Hardware Deliverables***

**BCC PO # 433, TRDA Grant 405**

Develop and deliver USCA prototype per proposal

*Completed 9-28-95*

**BCC PO # 610, TRDA Grant 410**

Develop and deliver Automated Data Acquisition System (ADAS) per proposal including:

- USCA Pilot Production
- Tag RAM Programmer
- USCA Interface Module
- PIO Module
- Hot Link Transmitter and Receiver Modules
- ADAS Integration and Test

*Completed October 30, 1996*

***Commercialization***

The commercial government version of the rugged USCA (LMTI model USCA 5200R) is complete and in production.

Twenty pilot production units have been delivered to NASA KSC, and integration and test is currently being conducted by NASA engineers. LMTI has received orders from NASA for 250 USCA 5200R units with an option for an additional 800 units over the next five years. The first 100 USCA 5200Rs are being manufactured and delivered.

As part of the production release process, LMTI surveyed several Florida manufacturers and selected three vendors for the commercial USCA. These are:

| | |
|---|---|
| V.A.W. of America<br>P.O. Box 3887<br>St. Augustine, FL 32085<br>(904) 794-1500 | Fabrication of the aluminum chassis |
| Advanced Quick Circuits<br>245 East Drive<br>Melbourne, FL 32904<br>(407) 752-8854 | Manufacture of the printed wiring boards |
| Spatron Technologies (STI)<br>285A North Drive<br>Melbourne, FL 32934<br>(407) 242-1249 | SMT board assembly and test |

LMTI has contracted with its Florida division for on-site inspection and acceptance at each of the vendor's facilities. In addition, all follow-on maintenance and support will come from our Sarasota and Melbourne offices.

LMTI also has contracted other work unrelated to USCA with the above companies. As a result, and due to their favorable rates, LMTI has placed additional orders with them.

# Marketing

LMTI is in the process of marketing and introducing the USCA and ADAS to the commercial marketplace. Market studies and surveys have resulted in the segmentation of the market as shown in Figure 1. As can be seen, there are significant business opportunities for data acquisition.

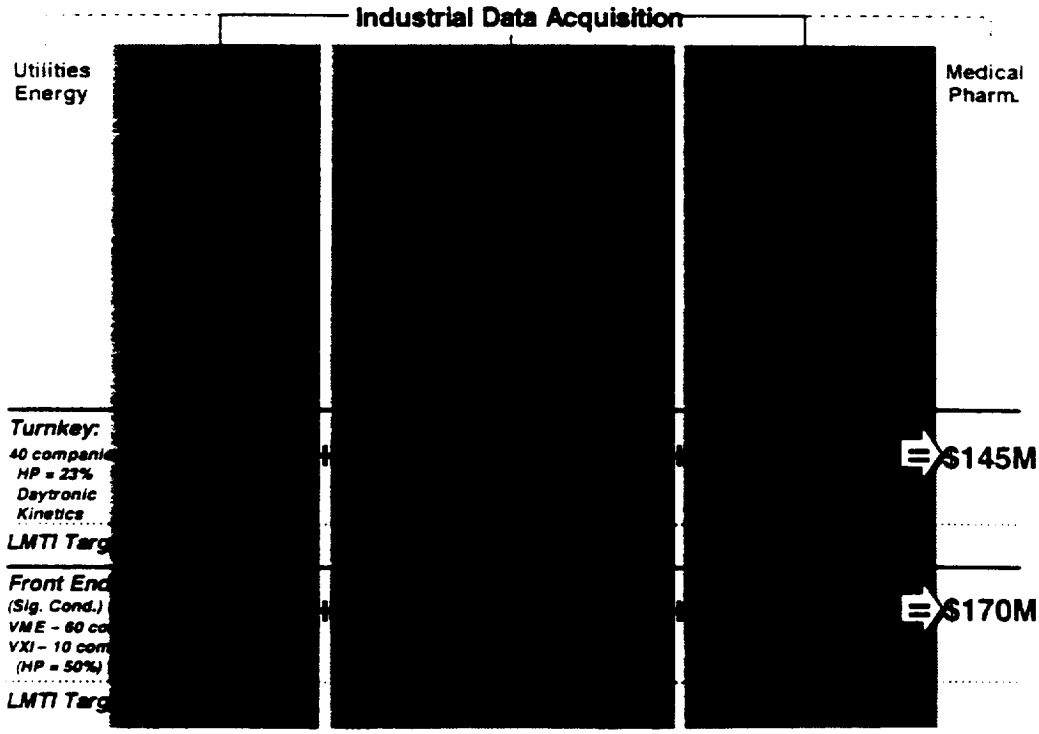



**Figure 1. Market Segments**

A conjoint analysis currently underway will further test our market assumptions and identify areas of particular importance to our customers.

### *Product Development*

Our marketing surveys indicate that USCA / ADAS technology is best applied to applications and customers that require:

- Lower life cycle costs
- Reduced maintenance costs
- 100 or more channels
- High accuracy (12 bits or 0.01%)
- Real-time data analysis
- Frequent reconfiguration
- Frequent calibration

Based on our current areas of expertise and the above requirements, we have identified the following applications for our initial marketing efforts.

- Launch operations
- Wind tunnels
- Vibration analysis
- Environmental test cells
- Engine test cells
- Acoustic test chambers

These application areas are best served by an integrated product solution, which is why we decided to market the USCA as part of a complete turnkey system called the Automated Data Acquisition System (ADAS) 5000.

The ADAS 5000 consists of all the hardware and software needed for complete end-to-end data acquisition. Since the ADAS 5000 is an entirely new product line, we designed a new product logo, assigned model numbers for the various product components, established prices, and published a commercial ADAS price list. We also created a literature package that includes a high-level ADAS brochure and supporting data sheets for each system component (see enclosure).

### *Market Introduction*

The ADAS 5000 was introduced at two trade shows in October 1995: the Sensors show in Philadelphia, PA, and the International Telemetry Conference in San Diego, CA.

LMTI presented working demonstration equipment at both shows. In addition, technical papers were written and presented in technical meetings at each show explaining our new approach to data acquisition.

Overall, the response from these shows was excellent. At the Sensors show, we attended a press conference and generated a great deal of media interest. We also generated a number of sales leads (at least three opportunities resulted directly from our presence at the shows).

To build on last year's momentum, we will attend four additional trade shows in 1997 which will each require technical paper presentations, press conferences, and demonstration equipment.

***Current Status***

We recently redesigned the government version of the USCA to adapt it to a laboratory environment suitable for the commercial marketplace. This new USCA 5200B board-level configuration is shown in Figure 2. A rack-mount chassis is being designed to accept the new USCA model.

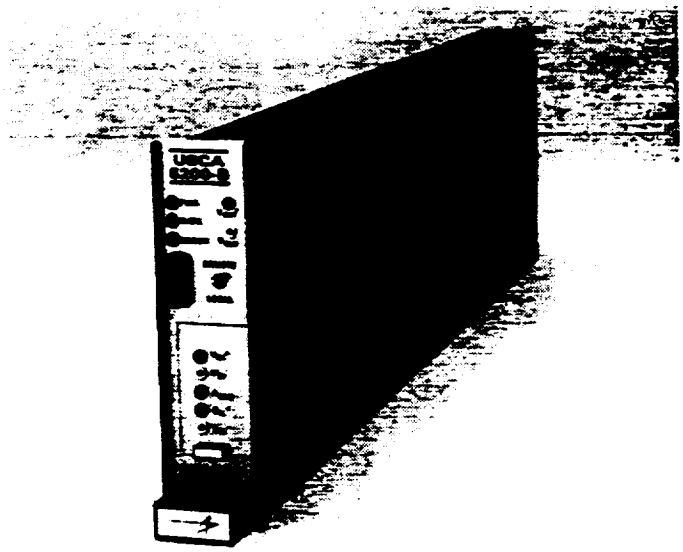


**Figure 2. USCA 5200B**

Upgrades to the USCA 5200B are underway as we add a Sigma Delta A/D converter to increase its sample rate and improve the filtering process. We are also adding more selections for filters and sample rates, new software to improve performance and make the product marketable to a wider set of customers, and an option for a "Mode" card that will provide bridge completion and other functions as required.

***Pending Sales***

LMTI has been working with a major prime contractor over the past year. The company purchased a single USCA for evaluation, which was delivered in December 1996. If their evaluation is successful, they may purchase up to 7,000 USCAs over a 5-year period.

# Program Results

LMTI and NASA KSC, in partnership and under a grant from the Florida Technological Research and Development Authority and Brevard Community College, have successfully completed a transfer of NASA technology to a commercial manufacturing environment.

Commercial products are currently being produced and delivered to NASA by LMTI. Additional business has been created for several Florida companies. And LMTI has adapted the technology to a new commercially viable product for general industry.

LMTI has introduced the product to the commercial marketplace through trade shows, direct mail, and other means of advertising. While the product launch is still in its infancy, marketplace reaction is very encouraging.

# Summary

Although the USCA dual-use program was more expensive and took longer than originally planned, LMTI is very pleased with the results. Design problems and initial manufacturing startup problems caused delays in the program. However, from the outset, LMTI firmly believed in the business potential of the NASA technology and therefore invested heavily in the program to guarantee its success.

Market feedback on the technology is overwhelmingly positive. LMTI has every reason to believe our new ADAS 5000 product line will become a significant part of our business in the near future.

# REPORT OF NEW TECHNOLOGY/INVENTIONS
(Required by New Technology or Patent Rights Clause)

1. Name and Address of Contractor:

**Technological Research & Development Authority**
**6770 South Highway U.S. 1**
**Titusville, FL 32780**

2. Contract/Grant Number: NCC10-0028

3. List each New Technology/Invention by Title and Innovator's Name.

**NOTE: A separate detailed description (including drawings) must also be provided for each New Technology/Invention listed.**

4. List each New Technology/Invention on which Contractor elects to retain title.

5. List subcontracts containing New Technology or Patent Rights Clause (if "None", so state). Provide name, address and subcontract number.

6. Certification is hereby made to the following (check "a" or "b")

____a. New Technology/Inventions listed above are all of the items required to be reported

__X__b. No New Technology/Inventions were made under the contract/grant identified above

W. A. Deputo
Director of Contracts
Name & Title of Authorized Contractor Official

Signature

Date: March 31, 1997

FNe 1002

# REPORT OF NEW TECHNOLOGY/INVENTIONS

(Required by New Technology or Patent Rights Clause)

1. Name and Address of Contractor -

**Technological Research & Development Authority**
**6770 South Highway U.S. 1**
**Titusville, FL 32780**

2. Contract/Grant Number - **NCC10-0008**

3. List each New Technology/Invention by Title and Innovator's Name.

**NOTE: A separate detailed description (including drawings) must also be provided for each New Technology/Invention listed.**

4. List each New Technology/Invention on which Contractor elects to retain title.

5. List subcontracts containing New Technology or Patent Rights Clause (if "None", so state). Provide name, address and subcontract number.

6. Certification is hereby made to the following: (check "a" or "b")

____a. New Technology/Inventions listed above are all of the items required to be reported.

__X__b. No New Technology/Inventions were made under the contract/grant identified above.

Matthew D. LaVigne
Business Manager

Name & Title of Authorized Contractor Official

Signature

Date: April 4, 1997

File 1002