Ask The Application Engineer—32

Practical Techniques to Avoid Instability Due to Capacitive Loading

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Q: *ADI has published a lot of information on dealing with capacitive loading and other stability issues in books, such as the amplifier seminar series, in earlier issues of Analog Dialogue, and in some design tools. But, I need a refresher—NOW.*

A: OK. Here goes!

Capacitive loads often give rise to problems, in part because they can reduce the output bandwidth and slew rate, but mainly because the phase lag they produce in the op amp's feedback loop can cause instability. Although some capacitive loading is inevitable, amplifiers are often subjected to sufficient capacitive loading to cause overshoots, ringing, and even oscillation. The problem is especially severe when large capacitive loads, such as LCD panels or poorly terminated coaxial cables, must be driven—but unpleasant surprises in precision low-frequency and dc applications can result as well.

As will be seen, the op amp is most prone to instability when it is configured as a unity-gain follower, either because (a) there is no attenuation in the loop, or (b) large common-mode swings, though not substantially affecting accuracy of the signal gain, can modulate the loop gain into unstable regions.

The ability of an op amp to drive capacitive loads is affected by several factors:

1. the amplifier's internal architecture (for example, output impedance, gain and phase margin, internal compensation circuitry)
2. the nature of the load impedance
3. attenuation and phase shift of the feedback circuit, including the effects of output loads, input impedances, and stray capacitances.

Among the parameters cited above, the amplifier output impedance, represented by the output resistance, R_O, is the one factor that most affects performance with capacitive loads. Ideally, an otherwise stable op amp with $R_O = 0$ will drive any capacitive load without phase degradation.

To avoid sacrificing performance with light loads, most amplifiers are not heavily compensated internally for substantial capacitive loads, so external compensation techniques must be used to optimize those applications in which a large capacitive load at the output of the op amp must be handled. Typical applications include sample-and-hold amplifiers, peak detectors, and driving unterminated coaxial cables.

Capacitive loading, as shown in Figures 1 and 2, affects the *open-loop* gain in the same way, regardless of whether the active input is at the noninverting or the inverting terminal: the load capacitance, C_L, forms a pole with the open-loop output resistance, R_O. The loaded gain can be expressed as follows:

$$A_{loaded} = A\left(\frac{1}{1+j\frac{f}{f_p}}\right), \text{where } f_p = \frac{1}{2\pi R_O C_L}$$

and A is the unloaded open-loop gain of the amplifier.

The –20 dB/decade slope and 90° lag contributed by the pole, added to the –20 dB slope and 90° contributed by the amplifier (plus any other existing lags), results in an increase in the rate of closure (ROC) to a value of at least 40 dB per decade, which, in turn, causes instability.

This note discusses typical questions about the effects of capacitive loads on the performance of some amplifier circuits, and suggests techniques to solve the instability problems they raise.

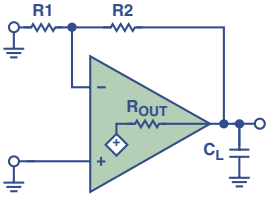

Figure 1. A simple op amp circuit with capacitive load.

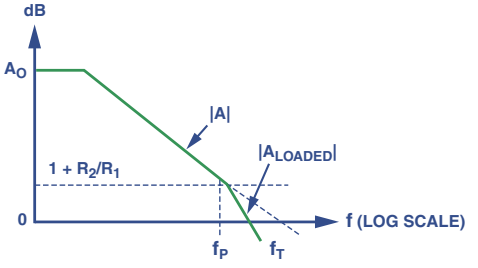

Figure 2. Bodé plot for the circuit of Figure 1.

Q: *So, different circuits call for different techniques?*

A: Yes, absolutely! You'll choose the compensation technique that best suits your design. Some examples are detailed below. For example, here's a compensation technique that has the added benefit of filtering the op amp's noise via an RC feedback circuit.

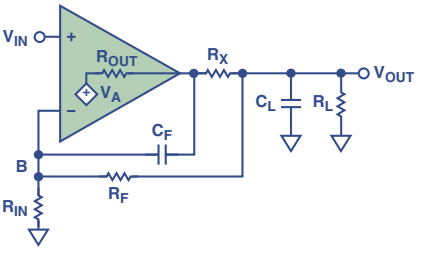

Figure 3. In-the-loop compensation circuit.

Figure 3 shows a commonly used compensation technique, often dubbed *in-the-loop* compensation. A small series resistor, R_x, is used to decouple the amplifier output from C_L; and a small capacitor, C_f, inserted in the feedback loop, provides a high frequency bypass around C_L.

To better understand this technique, consider the redrawn feedback portion of the circuit shown in Figure 4. VB is connected to the amplifier's minus input.

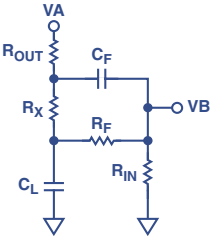

Figure 4. Feedback portion of the circuit.

Think of the capacitors, C_f and C_L, as open circuits at dc, and shorts at high frequencies. With this in mind, and referring to the circuit in Figure 4, let's apply this principle to one capacitor at a time.

Case 1 (Figure 5a):
With C_f shorted, $R_x << R_f$, and $R_o << R_{in}$, the pole and zero are functions of C_L, R_o, and R_x.

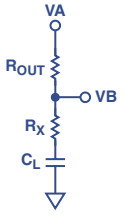

Figure 5a. C_f short-circuited.

Thus,

$$Pole\ Frequency = \frac{1}{2\pi(R_O + R_X)C_L}$$

and

$$Zero\ Frequency = \frac{1}{2\pi R_X C_L}$$

Case 2. (Figure 5b)
With C_L open, the pole and zero are a function of C_f.

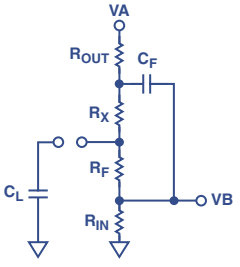

Figure 5b. C_L open-circuited.

Thus,

$$Pole\ Frequency = \frac{1}{2\pi\left[\left(R_X + R_f\right) \| \left(R_O + R_{in}\right)C_f\right]}$$

$$Zero\ Frequency = \frac{1}{2\pi\left(R_X + R_f\right)C_f}$$

By equating the pole in Case 1 to the zero in Case 2, and the pole in Case 2 to the zero in Case 1, we derive the following two equations:

$$R_X = \frac{R_O R_{in}}{R_f} \text{ and}$$

$$C_f = \left(1 + \frac{1}{|A_{cl}|}\right)\left(\frac{R_f + R_{in}}{R_f{}^2}\right)C_L R_O$$

The formula for C_f includes the term, A_{cl} (amplifier closed-loop gain, $1+R_f/R_{in}$). By experimenting, it was found that the $1/A_{cl}$ term needed to be included in the formula for C_f. For the above circuit, these two equations alone will allow compensation for any op amp with any applied capacitive load.

Although this method helps prevents oscillation when heavy capacitive loads are used, it reduces the closed-loop circuit bandwidth drastically. The bandwidth is no longer determined by the op amp, but rather by the external components, C_f and R_f, producing a closed-loop bandwidth of: $f_{-3\ dB} = 1/(2\pi C_f R_f)$.

A good, practical example of this compensation technique can be seen with the AD8510, an amplifier that can safely drive up to 200 pF while still preserving a 45° phase margin at unity-gain crossover. With the AD8510 in the circuit of Figure 3, configured for a gain of 10, with a 1-nF load capacitance at the output and a typical output impedance of 15 ohms, the values of R_x and C_f, computed using the above formulas, are 2 ohms and 2 pF. The square wave responses of Figures 6 and 7 show the fast response with uncompensated ringing, and the slower, but monotonic corrected response.

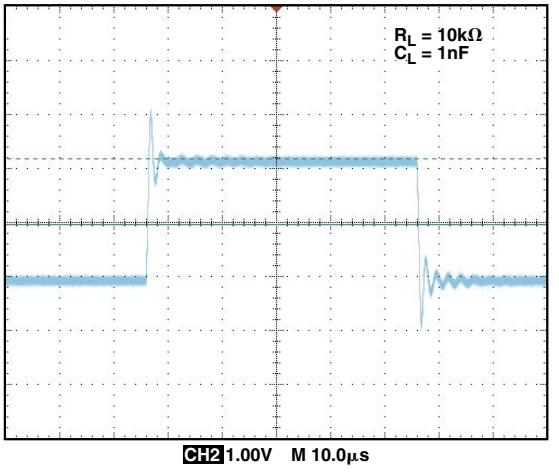

Figure 6. AD8510 output response without compensation.

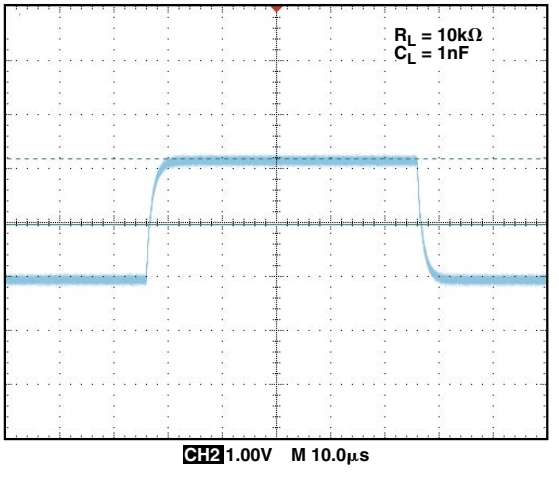

Figure 7. AD8510 output response with compensation.

In Figure 7, note that, because R_x is inside the feedback loop, its presence does not degrade the dc accuracy. However, R_x should always be kept suitably small to avoid excessive output swing reduction and slew-rate degradation.

Caution: The behaviors discussed here are typically experienced with the commonly used *voltage-feedback amplifiers*. Amplifiers that use *current feedback* require different treatment—beyond the scope of this discussion. If these techniques are used with a current feedback amplifier, the integration inherent in C_f will cause instability.

Out-of-the-Loop Compensation

Q: *Is there a simpler compensation scheme that uses fewer components?*

A: Yes, the easiest way is to use a single external resistor in series with the output. This method is effective but costly in terms of performance (Figure 8).

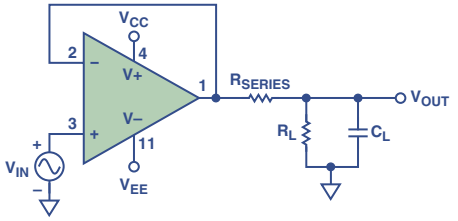

Figure 8. External R_{series} isolates the amplifier's feedback loop from the capacitive load.

Here a resistor, R_{series}, is placed between the output and the load. The primary function of this resistor is to isolate the op-amp output and feedback network from the capacitive load. Functionally, it introduces a zero in the transfer function of the feedback network, which reduces the loop phase shift at higher frequencies. To ensure a good level of stability, the value of R_{series} should be such that the zero added is at least a decade below the unity-gain crossover bandwidth of the amplifier circuit. The required amount of series resistance depends primarily on the output impedance of the amplifier used; values ranging from 5 ohms to 50 ohms are usually sufficient to prevent instability. Figure 9 shows the output response of the OP1177 with a 2-nF load and a 200-mV peak-peak signal at its positive input. Figure 10 shows the output response under the same conditions, but with a 50-ohm resistor in the signal path.

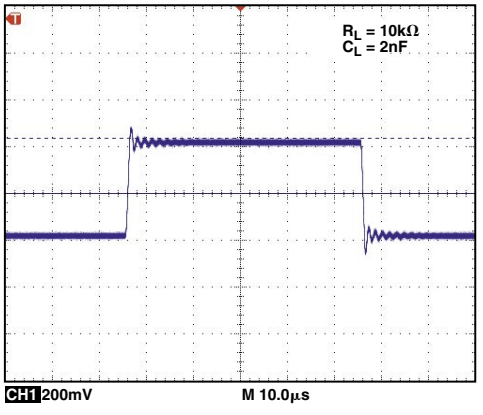

Figure 9. Output response of follower-connected OP1177 with capacitive load. Note high frequency ringing.

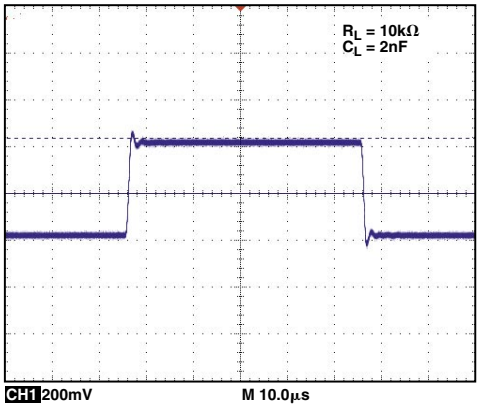

Figure 10. OP1177 output response with 50-ohm series resistance. Note reduced ringing.

The output signal will be attenuated by the ratio of the series resistance to the total resistance. This will require a wider amplifier output swing to attain full-scale load voltage. Nonlinear or variable loads will affect the shape and amplitude of the output signal.

Snubber Network

Q: *If I'm using a rail-to-rail amplifier, can you suggest a stabilizing method that will preserve my output swing and maintain gain accuracy?*

A: Yes, with an R-C series circuit from output to ground, the *snubber* method is recommended for lower voltage applications, where the full output swing is needed (Figure 11).

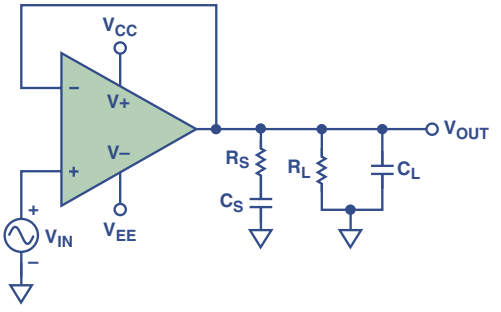

Figure 11. The R_S-C_S load forms a snubber circuit to reduce the phase shift caused by C_L.

Depending on the capacitive load, application engineers usually adopt empirical methods to determine the correct values for R_s and C_s. The principle here is to resistively load down the output of the amplifier for frequencies in the vicinity at which peaking occurs—thus snubbing down the amplifier's gain, then use series capacitance to decrease the loading at lower frequencies. So, the procedure is to: check the amplifier's frequency response to determine the peaking frequency; then, experimentally apply values of resistive loading (R_s) to reduce peaking to a satisfactory value; then, compute the value of C_s for a break frequency at about 1/3 the peak frequency. Thus, $C_s = 3/(2\pi f_p R_s)$, where f_p is the frequency at which peaking occurs.

These values can also be determined by trial and error while looking at the transient response (with capacitive loading) on an oscilloscope. The ideal values for R_s and C_s will yield minimum overshoot and undershoot. Figure 12 shows the output response of the AD8698 with a 68-nF load in response to a 400-mV signal at its positive input. The overshoot here is less than 25% without any external compensation. A simple snubber network reduces the overshoot to less than 10%, as seen in Figure 13. In this case, R_s and C_s are 30 ohms and 5 nF, respectively.

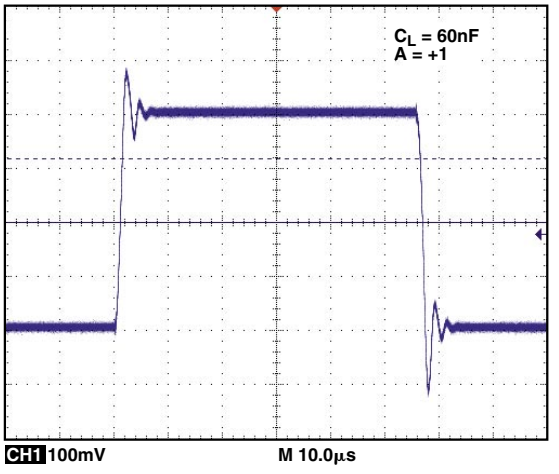

Figure 12. AD8698 output response without compensation.

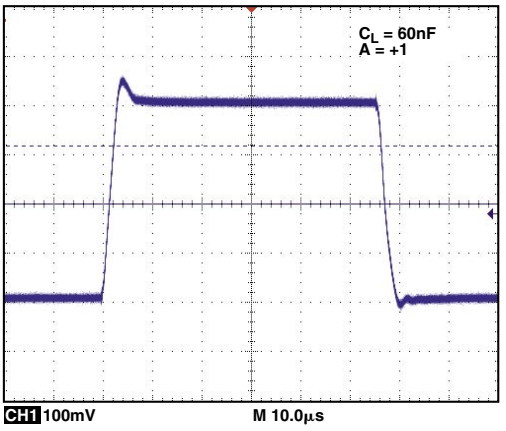

Figure 13. AD8698 output response with snubber network.

Q: *OK. I understand these examples about dealing with capacitive loading on the amplifier output. Now, is capacitance at the input terminals also of concern?*

A: Yes, capacitive loading at the inputs of an op amp can cause stability problems. We'll go through a few examples.

A very common and typical application is in current-to-voltage conversion when the op amp is used as a buffer/amplifier for a current-output DAC. The total capacitance at the input consists of the DAC output capacitance, the op amp input capacitance, and the stray wiring capacitance.

Another popular application in which significant capacitance may appear at the inputs of the op amp is in filter design. Some engineers may put a large capacitor across the inputs (often in series with a resistor) to prevent RF noise from propagating through the amplifier—overlooking the fact that this method can lead to severe ringing or even oscillation.

To better understand what is going on in a representative case, we analyze the circuit of Figure 14, unfolding the equivalent of its feedback circuit (input, V_{in}, grounded) to derive the feedback transfer function:

$$\frac{V_B}{V_A}(=\beta)=\frac{R_1}{(R_O+R_2)(1+sR_1C_1)+R_1}$$

which gives a pole located at

$$f_p=\frac{R_1+R_2+R_O}{2\pi R_1C_1(R_2+R_O)}$$

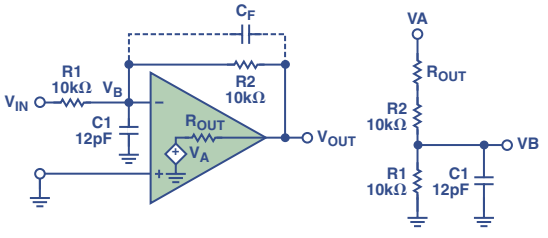

Figure 14. Capacitive loading at the input—inverting configuration.

This function indicates that the *noise gain* (1/β) curve rises at 20 dB/decade above the *break frequency*, f_p. If f_p is well below the open-loop unity-gain frequency, the system becomes unstable. This corresponds to a rate of closure of about 40 dB/decade. The rate of closure is defined as the magnitude of the difference between slopes of the open-loop gain (dB) plot (–20 dB/decade at most frequencies of interest) and that of 1/β, in the neighborhood of the frequency at which they cross (loop gain = 0 dB).

To cure the instability induced by C_1, a capacitor, C_f, can be connected in parallel with R_2, providing a zero which can be matched with the pole, f_p, to lower the rate of closure, and thus increase the phase margin. For a phase margin of 90°, pick $C_f=(R_1/R_2)C_1$.

Figure 15 shows the frequency response of the AD8605 in the configuration of Figure 14.

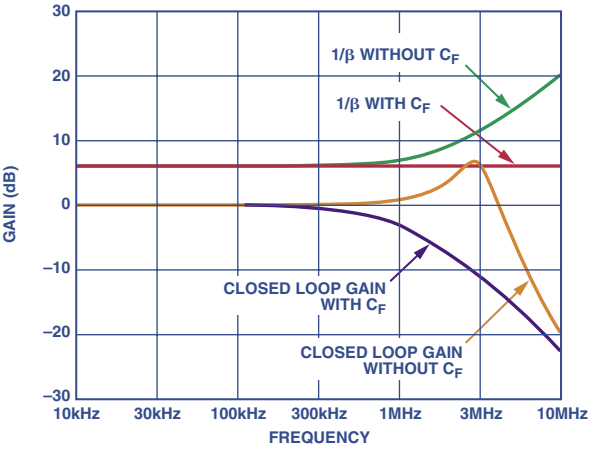

Figure 15. Frequency response of Figure 14.

Q: *Can I predict what the phase margin would be, or how much peaking I should expect?*

A: Yes, here's how:

You can determine the amount of uncompensated peaking using the following equation:

$$Q=\sqrt{\frac{f_u}{f_z}},\ \text{where}\ f_z=\frac{1}{2\pi\left(R_1\|R_2\right)C_1}$$

where f_u is the unity gain bandwidth, f_z is the breakpoint of the 1/β curve, and C_1 is the total capacitance—internal and external—including any parasitic capacitance.

The phase margin (Φ_m) can be determined with the following equation:

$$\Phi_m=\cos^{-1}\left(\sqrt{1+\frac{1}{4Q^4}}-\frac{1}{2Q^2}\right)$$

The AD8605 has a total input capacitance of approximately 7 pF. Assuming the parasitic capacitance is about 5 pF, the closed-loop gain will have a severe peaking of 5.5 dB, using the above equation. In the same manner, the phase margin is about 29°, a severe degradation from the op amp's natural phase response of 64°.

Q: *How can I make sure the op amp circuit is stable if I want to use an RC filter directly at the input?*

A: You can use a similar technique to that described above. Here's an example:

It is often desirable to use capacitance to ground from an amplifier's active input terminals to reduce high-frequency interference, RFI and EMI. This filter capacitor has a similar effect on op amp dynamics as increased stray capacitance. Since not all op amps behave in the same way, some will tolerate less capacitance at the input than others. So, it is useful in any event, to introduce a feedback capacitor, C_f, as compensation. For further RFI reduction, a small series resistor at the amplifier terminal will combine with the amplifier's input capacitance for filtering at radio frequencies. Figure 16 shows an approach (at left), that will have difficulty maintaining stability, compared with a considerably

improved circuit (at right). Figure 17 shows their superimposed square wave responses.

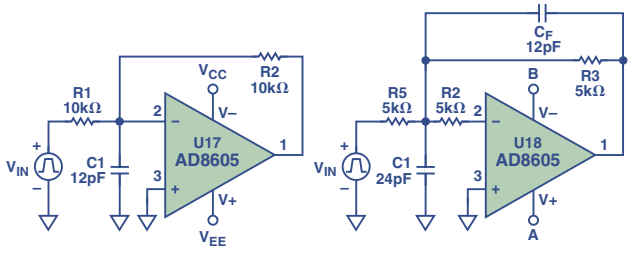

Figure 16. Input filter without (at left), and with (at right) compensation and lower impedance levels.

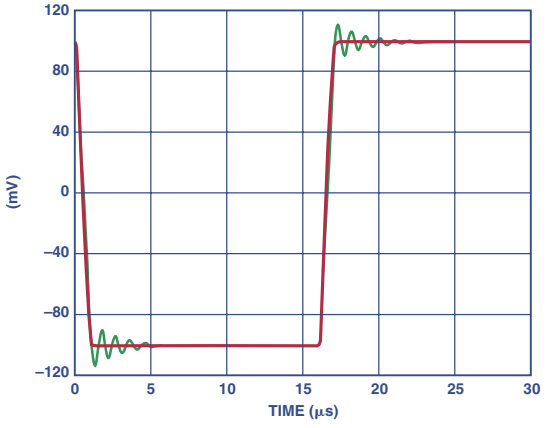

Figure 17. Comparison of output responses of the circuits in Figure 16. The circuit at left resulted in the oscillatory response.

Q: *You mentioned earlier that stray capacitance is added to the total input capacitance. How important is stray capacitance?*

A: Unsuspected stray capacitance can have a detrimental impact on the stability of the op amp. It is very important to anticipate and minimize it.

The board layout can be a major source of stray input capacitance. This capacitance occurs at the input traces to the summing junction of the op amp. For example, one square centimeter of a PC board, with a ground plane surrounding it, will produce about 2.8 pF of capacitance (depending on the thickness of the board).

To reduce this capacitance: Always keep the input traces as short as possible. Place the feedback resistor and the input source as close as possible to the op amp input. Keep the ground plane away from the op amp, especially the inputs, except where it is needed for the circuit and the noninverting pin is grounded. When ground is really needed, use a wide trace to ensure a low resistance path to ground.

Q: *Can op amps that aren't unity-gain stable be used at unity-gain? The OP37 is a great amplifier, but it must be used in a gain of at least 5 to be stable.*

A: You can use such op amps for lower gains by *tricking* them. Figure 18 shows a useful approach.

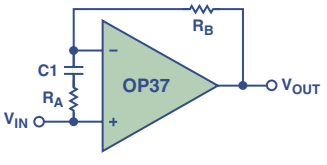

Figure 18. Unity-gain follower using an input series R-C to stabilize an amplifier that is not stable at unity-gain.

In Figure 18, R_B and R_A provide enough closed-loop gain at high frequencies to stabilize the amplifier, and C_1 brings it back to unity at low frequencies and dc. Calculating the values of R_B and R_A is fairly straightforward, based on the amplifier's minimum stable gain. In the case of the OP37, the amplifier needs a closed-loop gain of at least 5 to be stable, so $R_B = 4R_A$ for $\beta = 1/5$. For high frequencies, where C_1 behaves like a direct connection, the op amp *thinks* it's operating at a closed-loop gain of 5, and is therefore stable. At dc and low frequencies, where C_1 behaves like an open circuit, there is no attenuation of negative feedback, and the circuit behaves like a unity-gain follower.

The next step is to calculate the value of capacitance, C_1. A good value for C_1 should be picked such that it will provide a break frequency at least a decade below the circuit's corner frequency ($f_{-3\,dB}$).

$$C_1 = \frac{1}{2\pi R_A\left(\frac{f_c}{10}\right)}$$

Figure 19 shows the output of the OP37 in response to a 2-V p-p input step. The values of the compensation components are chosen using the equations above, with f_c = 16 MHz

$$R_B = 10k\Omega$$
$$R_A = R_B/4 = 2.k\Omega$$
$$C_1 = 1/\left(2\pi \times 2.5E3 \times 16E6/10\right) = 39\,pF$$

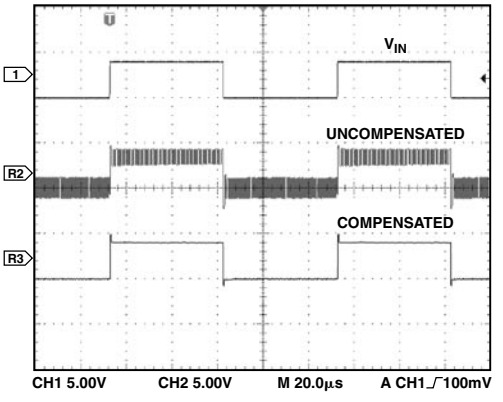

Figure 19. Unity-gain response of the OP37 with and without compensation.

Q: *Can this approach also be used for the inverting configuration? Can I still use the same equations?*

A: For the inverting configuration, the analysis is similar, but the equations for the closed-loop gain are slightly different. Remember that the input resistor to the inverting terminal of the op amp is now in parallel with R_A at high frequencies. This parallel combination is used to calculate the value of R_A for minimum stable gain. The capacitance value, C_1, is calculated in the same way as for the noninverting case.

Q: *Are there drawbacks to using this technique?*

A: Indeed, there are. Increasing the noise gain will increase the output noise level at higher frequencies, which may not be tolerable in some applications. Care should be used in wiring, especially with high source impedance, in the follower configuration. The reason is that positive feedback via capacitance to the amplifier's noninverting input at frequencies where the gain is greater than unity, can invite instability, as well as increased noise.

This article can be found at http://www.analog.com/library/analogDialogue/archives/38-06/capacitive_loading.html

PRODUCT INTRODUCTION—New DigiTrim™ Amplifiers

Many of today's most popular electronics applications such as digital cameras and mobile phones are migrating to lower operating voltages, reducing error budgets and increasing component accuracy requirements. At the same time, volume for these products continues to grow, putting additional pressure on suppliers to reduce component costs. This is especially true for the amplifiers used in these applications.

The key amplifier parameter for system accuracy is input offset voltage. Various techniques including laser trim and zener-zapping have been used to adjust amplifier offset voltage and other parameters. Indeed, offset-trimming techniques have enabled the entire class of precision amplifiers to exist today. However, offset trimming and the improved accuracy it creates has not, for the most part, found its way into the high volume, low-cost CMOS amplifier segment—until now. Analog Devices has developed a novel, patented trimming process that delivers the required accuracy and performance at a very low cost. The DigiTrim technique allows production of precision CMOS amplifiers at costs up to 30% lower than competitive solutions and with higher accuracy.

DigiTrim—*Digital control of adjustment currents through logic circuits and weighted current sources.*

DigiTrim adjusts circuit performance by programming digitally weighted current sources. In this patented new trim method, the trim information is entered through existing analog pins using a special digital keyword sequence. The adjustment values can be temporarily programmed, evaluated, and readjusted for optimum accuracy before permanent adjustment is performed. After the trim is completed, the trim circuit is locked out to prevent the possibility of any accidental re-trimming by the end user.

The physical trimming, achieved by blowing polysilicon fuses, is very reliable. No extra pads or pins are required for this trim method, and no special test equipment is needed to perform the trimming. The trims can be done after packaging so that assembly-related shifts may be eliminated. No testing is required at the wafer level, and no special wafer fabrication process is required, so circuits can even be produced by our foundry partners. The trim circuitry scales with the process features so that as the process—and thus the amplifier circuit—shrink, the trim circuit also shrinks proportionally. The trim circuits are considerably smaller than the amplifier circuits, so their contribution to die cost is minimal. The trims are discrete, but the required accuracy is easily achieved at a very small cost increase over an untrimmed part. A simplified representation of an amplifier with DigiTrim is shown in Figure 1.

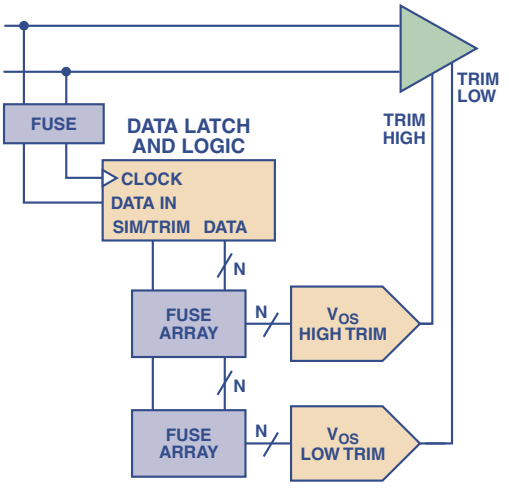

Figure 1. Simplified drawing

DigiTrim Amplifiers

The first part used in this new scheme was the AD8602 dual, low-cost, rail-to-rail CMOS amplifier. The offset voltage, trimmed for both high and low common-mode voltage conditions, is under 500 μV over the full common-mode input voltage range. With an 8-MHz bandwidth, 5 V/μs slew rate and 640 μA per amplifier current consumption, this part supports a variety of high volume, cost-sensitive applications from bar code scanners to GSM phones. Three new DigiTrim amplifiers have recently been introduced:

The AD8615/AD8616/AD8618 single/dual/quad op amps use ADI's patented DigiTrim technology to achieve 65-μV maximum offset voltage and 7-μV/°C maximum offset drift without laser trimming. The CMOS process provides ultralow input bias current (1 pA max), input offset current (0.5 pA max), and current noise density (0.05 pA/$\sqrt{\text{Hz}}$). Other features include 24-MHz gain-bandwidth product, rail-to-rail inputs and outputs, 100-dB common-mode rejection, 90-dB power supply rejection, 6-nV/$\sqrt{\text{Hz}}$ voltage noise, 1500-V/mV open-loop gain, and ±150-mA output current. This combination of features makes the AD8615/AD8616/AD8618 ideal for filters, photodiode amplifiers, buffering multiplexed inputs to ADCs, and audio applications. Specified from –40°C to +125°C, they operate on a single 2.7-V to 5.5-V supply, consuming only 1.7 mA per amplifier. The AD8515 is available in a 5-lead SOT-23 package; the AD8616 is available in 8-lead MSOP and SOIC packages; and the AD8618 is available in 14-lead TSSOP and SOIC packages.

Figures 2 and 3 show typical applications for the AD8616 and AD8618. Additional information on DigiTrim technology can be found at http://www.analog.com/DigiTrim.

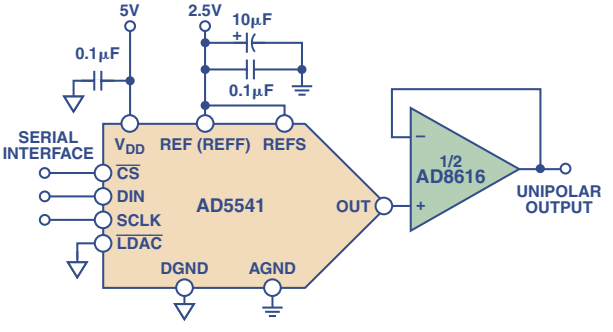

Figure 2. DAC buffer

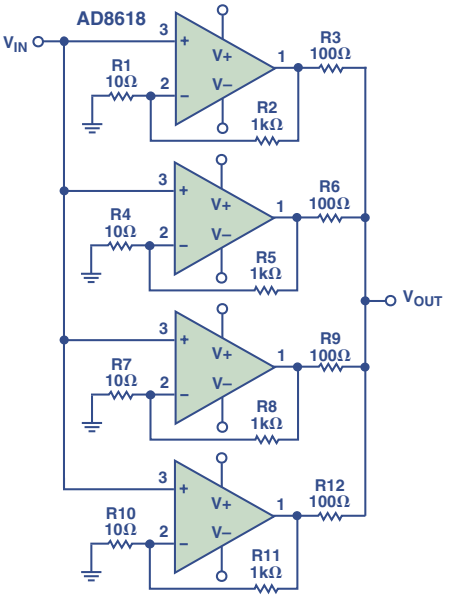

Figure 3. Noise reduction using multiple parallel paths