Application Brief

SIMPLE RULES FOR CHOOSING RESISTOR VALUES IN ADDER-SUBTRACTOR CIRCUITS

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THE PROBLEM

I want to take a linear combination of analog voltages with both positive and negative coefficients, using a single operational amplifier. In Figure 1, for example:

$$Z = 3\,x_1 + 0.15\,x_2 - 2.9\,y_1 \text{*} \qquad (1)$$

To minimize offset-current error, I want to keep the equivalent parallel resistance on both sides equal. How do I choose the nominal resistance values, given a specified value of parallel resistance, and fit within all the constraints without indulging in a lot of hairy network analysis?

In general, one must be concerned with: the effect of the resistance values on the subtractive side on gain for signals on the positive side, interaction among the inputs on the positive side, and the equal-parallel-resistance constraint. A loading resistor to ground from one of the two summing points provides a necessary degree of freedom.

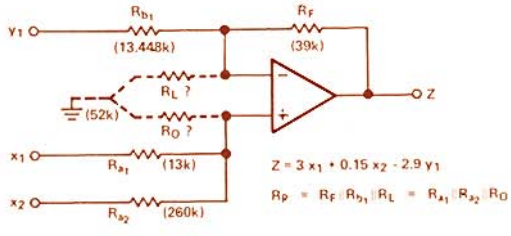

Figure 1. Typical adder-subtractor problem.

A SOLUTION[1]

This is a mechanized procedure for computing all the required values. *It works in all practical cases, for any number of inputs on either side, whether the circuit is inverting-only, non-inverting only, or an adder-subtractor, and for all reasonable values of gain or attenuation.*

Grouping the positive and negative coefficients, we label each positive coefficient a_i, the corresponding input x_i, and the corresponding input resistor R_{a_i}. Corresponding quantities for each inverted gain are b_j, y_j, and R_{b_j}. In the example of Figure 1, a_1 is 3.00, a_2 is 0.15, and b_1 is 2.90. We want to compute the values of R_{a_1}, R_{a_2}, R_{b_1}, the feedback resistance R_F, and the value and disposition (to the + or the - input?) of the grounded loading resistor (R_O or R_L), in order to keep the effective parallel resistance on both sides equal to a specified value, R_p – for example, 10kΩ.

* Expressed in general and compact form,

$$Z = \sum_{i=1}^{m} a_i x_i - \sum_{j=1}^{n} b_j y_j$$

[1] An earlier exposition of this technique by the author, with additional examples, may be found in *Electronics*, June 12, 1975, page 125.

Here are the rules:

1. *Add up the positive coefficients,* Σa.
   In this example, $\Sigma a = 3 + 0.15 = 3.15$.
2. *Add up the magnitudes of the negative coefficients,* Σb, *and add 1.00.*
   In this example, $1 + \Sigma b = 1 + 2.9 = 3.9$.
3. *Subtract* Σa *from* $(1 + \Sigma b)$ *to get the difference,* Δ. *If* Δ *is positive, a resistance* R_O *will be required between the amplifier's + input and ground; if negative, a resistance* R_L *will be required between the - input and ground.*
   In this example, $\Delta = 3.9 - 3.15 = +0.75$, calling for a resistance R_O from the + input to ground.
4. *Calculate* R_F. *It is simply equal to the product of* R_p *and the larger of the two sums.*
   In this case, since $3.9 > 3.15$, $R_F = 3.9 \times 10k\Omega = 39k\Omega$.
5. *Calculate* R_O *(or* $-R_L$*). It is equal to* R_F/Δ.
   Here, $R_O = 39k\Omega/(+0.75) = 52k\Omega$.
6. *Calculate each of the input resistances,* R_{a_i} *and* R_{b_j}. *Simply divide* R_F *by each coefficient* (a_i, b_j) *in turn.*
   In this case, $R_{a_1} = 39k\Omega/3.00 = 13k\Omega$,
   $R_{a_2} = 39k\Omega/0.15 = 260k\Omega$, and
   $R_{b_1} = 39k\Omega/2.9 = 13.448k\Omega$.

That's all, folks!

You'll find it harder to check the results from first principles than it was to execute the algorithm. The first step is to check the parallel resistances on both sides. In the example, the parallel resistance on the – side is $1/(1/39 + 1/13.448) = 10.00k\Omega$. On the + side, it is $1/(1/13 + 1/260 + 1/52) = 10.00k\Omega$. If you wish, you may satisfy yourself that the individual gain criteria are also met.

A note on implementing the circuits: Interaction among the R_{a_i} values makes dynamic trimming of the whole circuit difficult. For this reason, the resistance ratios should be trimmed *before* the network is connected to its circuit. If a final trim is needed, R_F is first tweaked to optimize overall gain accuracy for the subtracted inputs, then R_O (or R_L) for the + inputs. The amplifier's contribution to common-mode and gain errors can be minimized if it has high gain, high CMR, low E_{OS}, low I_{OS}, and low tempcos, e.g., the AD510.† If many identical networks are to be used, a cost-effective approach is to design a thin- or thick-film network, with resistors that accurately track one another with temperature and are initially set to within the required relative tolerances.† (Absolute accuracy is unnecessary.)

If many similar networks with differing gains are to be designed, the Reader may be interested in an HP-25 program that will provide fast and accurate implementation of the above procedure for up to 3 inputs on each side. It appears on page 18. ▶▶▶

†For information on the AD510 and custom R-networks, use reply card.