Chapter 8

Current-Feedback Op Amp Analysis

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8.1 Introduction

Current-feedback amplifiers (CFA) do not have the traditional differential amplifier input structure, thus they sacrifice the parameter matching inherent to that structure. The CFA circuit configuration prevents them from obtaining the precision of voltage-feedback amplifiers (VFA), but the circuit configuration that sacrifices precision results in increased bandwidth and slew rate. The higher bandwidth is relatively independent of closed-loop gain, so the constant gain-bandwidth restriction applied to VFAs is removed for CFAs. The slew rate of CFAs is much improved from their counterpart VFAs because their structure enables the output stage to supply slewing current until the output reaches its final value. In general, VFAs are used for precision and general purpose applications, while CFAs are restricted to high frequency applications above 100 MHz.

Although CFAs do not have the precision of their VFA counterparts, they are precise enough to be dc-coupled in video applications where dynamic range requirements are not severe. CFAs, unlike previous generation high-frequency amplifiers, have eliminated the ac coupling requirement; they are usually dc-coupled while they operate in the GHz range. CFAs have much faster slew rates than VFAs, so they have faster rise/fall times and less intermodulation distortion.

8.2 CFA Model

The CFA model is shown in Figure 8–1. The noninverting input of a CFA connects to the input of the input buffer, so it has very high impedance similar to that of a bipolar transistor noninverting VFA input. The inverting input connects to the input buffer's output, so the inverting input impedance is equivalent to a buffer's output impedance, which is very low. Z_B models the input buffer's output impedance, and it is usually less than 50 Ω. The input buffer gain, G_B, is as close to one as IC design methods can achieve, and it is small enough to neglect in the calculations.

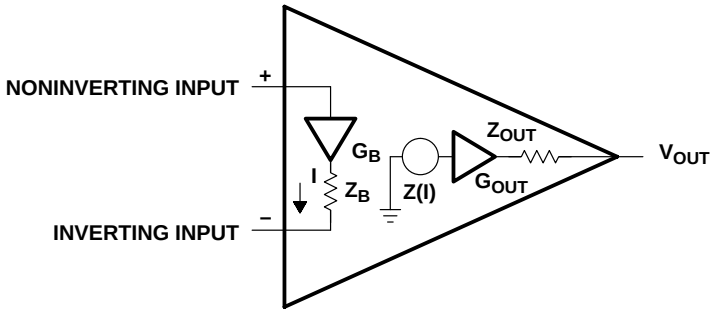

Figure 8–1. Current-Feedback Amplifier Model

The output buffer provides low output impedance for the amplifier. Again, the output buffer gain, G_{OUT}, is very close to one, so it is neglected in the analysis. The output impedance of the output buffer is ignored during the calculations. This parameter may influence the circuit performance when driving very low impedance or capacitive loads, but this is usually not the case. The input buffer's output impedance can't be ignored because affects stability at high frequencies.

The current-controlled current source, Z, is a transimpedance. The transimpedance in a CFA serves the same function as gain in a VFA; it is the parameter that makes the performance of the op amp dependent only on the passive parameter values. Usually the transimpedance is very high, in the MΩ range, so the CFA gains accuracy by closing a feedback loop in the same manner that the VFA does.

8.3 Development of the Stability Equation

The stability equation is developed with the aid of Figure 8–2. Remember, stability is independent of the input, and stability depends solely on the loop gain, Aβ. Breaking the loop at point *X*, inserting a test signal, V_{TI}, and calculating the return signal V_{TO} develops the stability equation.

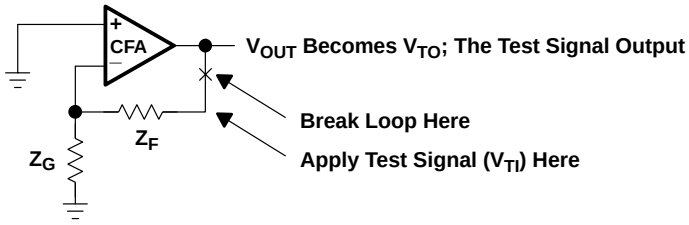

Figure 8–2. Stability Analysis Circuit

The circuit used for stability calculations is shown in Figure 8–3 where the model of Figure 8–1 is substituted for the CFA symbol. The input and output buffer gain, and output buffer

output impedance have been deleted from the circuit to simplify calculations. This approximation is valid for almost all applications.

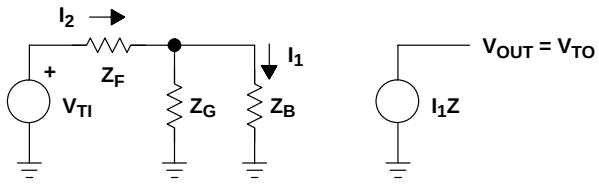

Figure 8–3. Stability Analysis Circuit

The transfer equation is given in Equation 8–1, and the Kirchoff"s law is used to write Equations 8–2 and 8–3.

$$V_{TO} = I_1 Z \tag{8–1}$$

$$V_{TI} = I_2\left(Z_F + Z_G \parallel Z_B\right) \tag{8–2}$$

$$I_2\left(Z_G \parallel Z_B\right) = I_1 Z_B \tag{8–3}$$

Equations 8–2 and 8–3 are combined to yield Equation 8–4.

$$V_{TI} = I_1\left(Z_F + Z_G \parallel Z_B\right)\left(1 + \frac{Z_B}{Z_G}\right) = I_1 Z_F\left(1 + \frac{Z_B}{Z_F \parallel Z_G}\right) \tag{8–4}$$

Dividing Equation 8–1 by Equation 8–4 yields Equation 8–5, and this is the open loop transfer equation. This equation is commonly known as the loop gain.

$$A\beta = \frac{V_{TO}}{V_{TI}} = \frac{Z}{\left(Z_F\left(1 + \frac{Z_B}{Z_F \parallel Z_G}\right)\right)} \tag{8–5}$$

8.4 The Noninverting CFA

The closed-loop gain equation for the noninverting CFA is developed with the aid of Figure 8–4, where external gain setting resistors have been added to the circuit. The buffers are shown in Figure 8–4, but because their gains equal one and they are included within the feedback loop, the buffer gain does not enter into the calculations.

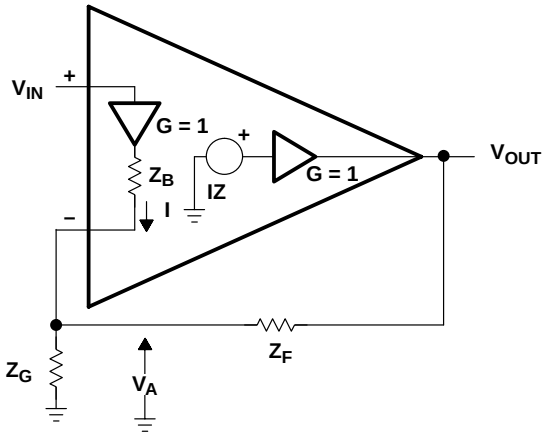

Figure 8–4. Noninverting CFA

Equation 8–6 is the transfer equation, Equation 8–7 is the current equation at the inverting node, and Equation 8–8 is the input loop equation. These equations are combined to yield the closed-loop gain equation, Equation 8–9.

$$V_{OUT} = IZ \tag{8–6}$$

$$I = \left(\frac{V_A}{Z_G}\right) - \left(\frac{V_{OUT} - V_A}{Z_F}\right) \tag{8–7}$$

$$V_A = V_{IN} - IZ_B \tag{8–8}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{\dfrac{Z\left(1 + \dfrac{Z_F}{Z_G}\right)}{Z_F\left(1 + \dfrac{Z_B}{Z_F \| Z_G}\right)}}{1 + \dfrac{Z}{Z_F\left(1 + \dfrac{Z_B}{Z_F \| Z_G}\right)}} \tag{8–9}$$

When the input buffer output impedance, Z_B, approaches zero, Equation 8–9 reduces to Equation 8–10.

$$\frac{V_{OUT}}{V_{IN}} = \frac{\frac{Z\left(1+\frac{Z_F}{Z_G}\right)}{Z_F}}{1+\frac{Z}{Z_F}} = \frac{1+\frac{Z_F}{Z_G}}{1+\frac{Z_F}{Z}} \qquad (8\text{–}10)$$

When the transimpedance, Z, is very high, the term Z_F/Z in Equation 8–10 approaches zero, and Equation 8–10 reduces to Equation 8–11; the ideal closed-loop gain equation for the CFA. The ideal closed-loop gain equations for the CFA and VFA are identical, and the degree to which they depart from ideal is dependent on the validity of the assumptions. The VFA has one assumption that the direct gain is very high, while the CFA has two assumptions, that the transimpedance is very high and that the input buffer output impedance is very low. As would be expected, two assumptions are much harder to meet than one, thus the CFA departs from the ideal more than the VFA does.

$$\frac{V_{OUT}}{V_{IN}} = 1 + \frac{Z_F}{Z_G} \qquad (8\text{–}11)$$

8.5 The Inverting CFA

The inverting CFA configuration is seldom used because the inverting input impedance is very low ($Z_B||Z_F + Z_G$). When Z_G is made dominant by selecting it as a high resistance value it overrides the effect of Z_B. Z_F must also be selected as a high value to achieve at least unity gain, and high values for Z_F result in poor bandwidth performance, as we will see in the next section. If Z_G is selected as a low value the frequency sensitive Z_B causes the gain to increase as frequency increases. These limitations restrict inverting applications of the inverting CFA.

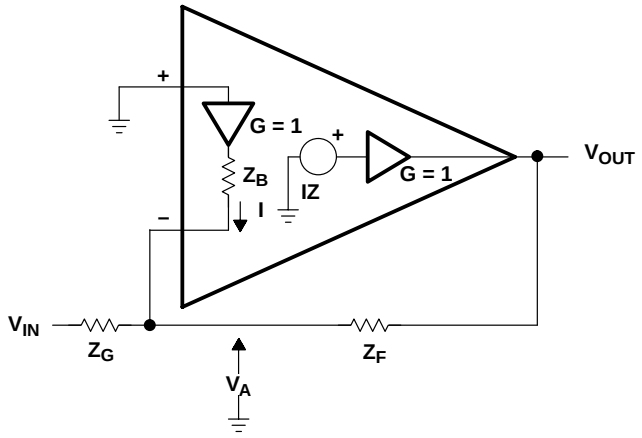

Figure 8–5. Inverting CFA

The current equation for the input node is written as Equation 8–12. Equation 8–13 defines the dummy variable, V_A, and Equation 8–14 is the transfer equation for the CFA. These equations are combined and simplified leading to Equation 8–15, which is the closed-loop gain equation for the inverting CFA.

$$I + \frac{V_{IN} - V_A}{Z_G} = \frac{V_A - V_{OUT}}{Z_F} \tag{8–12}$$

$$IZ_B = -V_A \tag{8–13}$$

$$IZ = V_{OUT} \tag{8–14}$$

$$\frac{V_{OUT}}{V_{IN}} = -\frac{\dfrac{Z}{Z_G\left(1 + \dfrac{Z_B}{Z_F \| Z_G}\right)}}{1 + \dfrac{Z}{Z_F\left(1 + \dfrac{Z_B}{Z_F \| Z_G}\right)}} \tag{8–15}$$

When Z_B approaches zero, Equation 8–15 reduces to Equation 8–16.

$$\frac{V_{OUT}}{V_{IN}} = -\frac{\dfrac{1}{Z_G}}{\dfrac{1}{Z} + \dfrac{1}{Z_F}} \tag{8–16}$$

When Z is very large, Equation 8–16 becomes Equation 8–17, which is the ideal closed-loop gain equation for the inverting CFA.

$$\frac{V_{OUT}}{V_{IN}} = -\frac{Z_F}{Z_G} \tag{8–17}$$

The ideal closed-loop gain equation for the inverting VFA and CFA op amps are identical. Both configurations have lower input impedance than the noninverting configuration has, but the VFA has one assumption while the CFA has two assumptions. Again, as was the case with the noninverting counterparts, the CFA is less ideal than the VFA because of the two assumptions. The zero Z_B assumption always breaks down in bipolar junction transistors as is shown later. The CFA is almost never used in the differential amplifier configuration because of the CFA's gross input impedance mismatch.

8.6 Stability Analysis

The stability equation is repeated as Equation 8–18.

$$A\beta = \frac{V_{TO}}{V_{TI}} = \frac{Z}{\left(Z_F\left(1 + \frac{Z_B}{Z_F \| Z_G}\right)\right)} \tag{8–18}$$

Comparing Equations 8–9 and 8–15 to Equation 8–18 reveals that the inverting and noninverting CFA op amps have identical stability equations. This is the expected result because stability of any feedback circuit is a function of the loop gain, and the input signals have no affect on stability. The two op amp parameters affecting stability are the transimpedance, Z, and the input buffer's output impedance, Z_B. The external components affecting stability are Z_G and Z_F. The designer controls the external impedance, although stray capacitance that is a part of the external impedance sometimes seems to be uncontrollable. Stray capacitance is the primary cause of ringing and overshoot in CFAs. Z and Z_B are CFA op amp parameters that can't be controlled by the circuit designer, so he has to live with them.

Prior to determining stability with a Bode plot, we take the log of Equation 8–18, and plot the logs (Equations 8–19 and 8–20) in Figure 8–6.

$$20 \text{ LOG } |A\beta| = 20 \text{ LOG } |Z| - 20 \text{ LOG } \left|Z_F\left(1 + \frac{Z_B}{Z_F \| Z_B}\right)\right| \tag{8–19}$$

$$\phi = \text{TANGENT}^{-1}(A\beta) \tag{8–20}$$

This enables the designer to add and subtract components of the stability equation graphically.

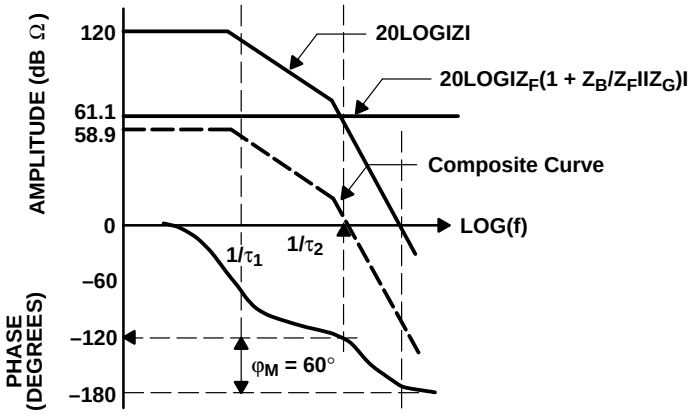

Figure 8–6. Bode Plot of Stability Equation

The plot in Figure 8–6 assumes typical values for the parameters:

$$Z = \frac{1M\Omega}{(1 + \tau_1 S)(1 + \tau_2 S)} \tag{8–21}$$

$$Z_B = 70\Omega \tag{8–22}$$

$$Z_G = Z_F = 1k\Omega \tag{8–23}$$

The transimpedance has two poles and the plot shows that the op amp will be unstable without the addition of external components because 20 LOG|Z| crosses the 0-dB axis after the phase shift is 180°. Z_F, Z_B, and Z_G reduce the loop gain 61.1 dB, so the circuit is stable because it has 60°-phase margin. Z_F is the component that stabilizes the circuit. The parallel combination of Z_F and Z_G contribute little to the phase margin because Z_B is very small, so Z_B and Z_G have little effect on stability.

The manufacturer determines the optimum value of R_F during the characterization of the IC. Referring to Figure 8–6, it is seen that when R_F exceeds the optimum value recommended by the IC manufacturer, stability increases. The increased stability has a price called decreased bandwidth. Conversely, when R_F is less than the optimum value recommended by the IC manufacturer, stability decreases, and the circuit response to step inputs is overshoot or possibly ringing. Sometimes the overshoot associated with less than optimum R_F is tolerated because the bandwidth increases as R_F decreases. The peaked response associated with less than optimum values of R_F can be used to compensate for cable droop caused by cable capacitance.

When $Z_B = 0\ \Omega$ and $Z_F = R_F$ the loop gain equation is; $A\beta = Z/R_F$. Under these conditions Z and R_F determine stability, and a value of R_F can always be found to stabilize the circuit. The transimpedance and feedback resistor have a major impact on stability, and the input buffer's output impedance has a minor effect on stability. Since Z_B increases with an increase in frequency, it tends to increase stability at higher frequencies. Equation 8–18 is rewritten as Equation 8–24, but it has been manipulated so that the ideal closed-loop gain is readily apparent.

$$A\beta = \frac{Z}{Z_F + Z_B\left(1 + \frac{R_F}{R_G}\right)} \tag{8–24}$$

The closed-loop ideal gain equation (inverting and noninverting) shows up in the denominator of Equation 8–24, so the closed-loop gain influences the stability of the op amp. When Z_B approaches zero, the closed-loop gain term also approaches zero, and the op amp becomes independent of the ideal closed-loop gain. Under these conditions R_F determines stability, and the bandwidth is independent of the closed-loop gain. Many people claim that the CFA bandwidth is independent of the gain, and that claim's validity is dependent on the ratios Z_B/Z_F being very low.

Z_B is important enough to warrant further investigation, so the equation for Z_B is given below.

$$Z_B \cong h_{ib} + \frac{R_B}{\beta_0 + 1}\left(\frac{1 + \frac{s\beta_0}{\omega_T}}{1 + \frac{S\beta_0}{(\beta_0+1)\omega_T}}\right) \quad (8\text{–}25)$$

At low frequencies $h_{ib} = 50\ \Omega$ and $R_B/(\beta_0+1) = 25\ \Omega$, so $Z_B = 75\ \Omega$. Z_B varies in accordance with Equation 8–25 at high frequencies. Also, the transistor parameters in Equation 8–25 vary with transistor type; they are different for NPN and PNP transistors. Because Z_B is dependent on the output transistors being used, and this is a function of the quadrant the output signal is in, Z_B has an extremely wide variation. Z_B is a small factor in the equation, but it adds a lot of variability to the current-feedback op amp.

8.7 Selection of the Feedback Resistor

The feedback resistor determines stability, and it affects closed-loop bandwidth, so it must be selected very carefully. Most CFA IC manufacturers employ applications and product engineers who spend a great deal of time and effort selecting R_F. They measure each noninverting gain with several different feedback resistors to gather data. Then they pick a compromise value of R_F that yields stable operation with acceptable peaking, and that value of R_F is recommended on the data sheet for that specific gain. This procedure is repeated for several different gains in anticipation of the various gains their customer applications require (often G = 1, 2, or 5). When the value of R_F or the gain is changed from the values recommended on the data sheet, bandwidth and/or stability is affected.

When the circuit designer must select a different R_F value from that recommended on the data sheet he gets into stability or low bandwidth problems. Lowering R_F decreases stability, and increasing R_F decreases bandwidth. What happens when the designer needs to operate at a gain not specified on the data sheet? The designer must select a new value of R_F for the new gain, but there is no guarantee that new value of R_F is an optimum value. One solution to the R_F selection problem is to assume that the loop gain, $A\beta$, is a linear function. Then the assumption can be made that $(A\beta)_1$ for a gain of one equals $(A\beta)_N$ for a gain of N, and that this is a linear relationship between stability and gain. Equations 8–26 and 8–27 are based on the linearity assumption.

$$\frac{Z}{Z_{F1} + Z_B\left(1 + \frac{Z_{F1}}{Z_{G1}}\right)} = \frac{Z}{Z_{FN} + Z_B\left(1 + \frac{Z_{FN}}{Z_{GN}}\right)} \quad (8\text{–}26)$$

$$Z_{FN} = Z_{F1} + Z_B\left(\left(1 + \frac{Z_{F1}}{Z_{G1}}\right) - \left(1 + \frac{Z_{FN}}{Z_{GN}}\right)\right) \quad (8\text{–}27)$$

Equation 8–27 leads one to believe that a new value for Z_F can easily be chosen for each new gain. This is not the case in the real world; the assumptions don't hold up well enough to rely on them. When you change to a new gain not specified on the data sheet, Equation 8–27, at best, supplies a starting point for R_F, but you must test to determine the final value of R_F.

When the R_F value recommended on the data sheet can't be used, an alternate method of selecting a starting value for R_F is to use graphical techniques. The graph shown in Figure 8–7 is a plot of the typical 300-MHz CFA data given in Table 8–1.

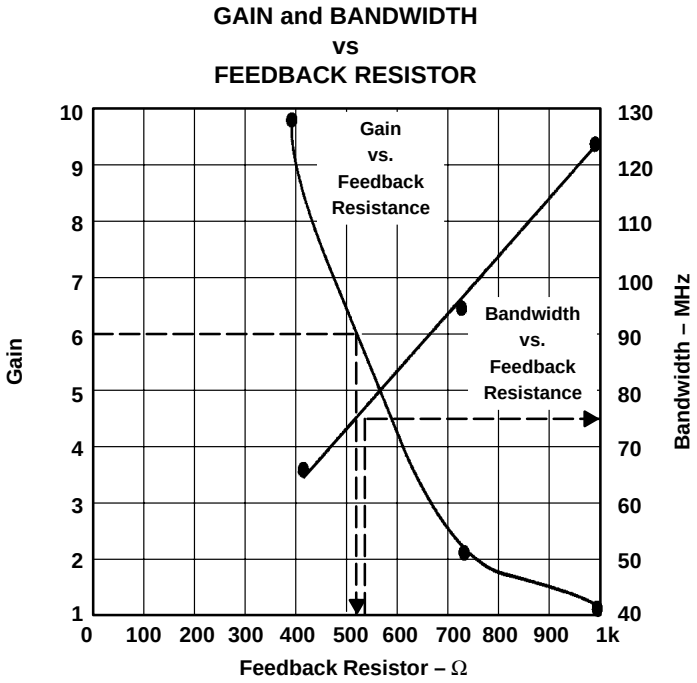

Figure 8–7. Plot of CFA R_F, G, and BW

Table 8–1. Data Set for Curves in Figure 8–7

GAIN (A_{CL})	R_F (Ω)	BANDWIDTH (MHz)
+ 1	1000	125
+ 2	681	95
+ 10	383	65

Enter the graph at the new gain, say A_{CL} = 6, and move horizontally until you reach the intersection of the gain versus feedback resistance curve. Then drop vertically to the resistance axis and read the new value of R_F (500 Ω in this example). Enter the graph at the new value of R_F, and travel vertically until you intersect the bandwidth versus feedback resistance curve. Now move to the bandwidth axis to read the new bandwidth (75 MHz in this example). As a starting point you should expect to get approximately 75 MHz BW with a gain of 6 and R_F = 500 Ω. Although this technique yields more reliable solutions than Equation 8–27 does, op amp peculiarities, circuit board stray capacitances, and wiring make extensive testing mandatory. The circuit must be tested for performance and stability at each new operating point.

8.8 Stability and Input Capacitance

When designer lets the circuit board introduce stray capacitance on the inverting input node to ground, it causes the impedance Z_G to become reactive. The new impedance, Z_G, is given in Equation 8–28, and Equation 8–29 is the stability equation that describes the situation.

$$Z_G = \frac{R_G}{1 + R_G C_G s} \tag{8–28}$$

$$A\beta = \frac{Z}{Z_B + \dfrac{Z_F}{Z_G^2 + Z_B Z_G}} \tag{8–29}$$

$$A\beta = \frac{Z}{R_F\left(1 + \dfrac{R_B}{R_F \| R_G}\right)\left(1 + R_B \parallel R_F \parallel R_G C_G s\right)} \tag{8–30}$$

Equation 8–29 is the stability equation when Z_G consists of a resistor in parallel with stray capacitance between the inverting input node and ground. The stray capacitance, C_G, is a fixed value because it is dependent on the circuit layout. The pole created by the stray capacitance is dependent on R_B because it dominates R_F and R_G. R_B fluctuates with manufacturing tolerances, so the $R_B C_G$ pole placement is subject to IC manufacturing tolerances. As the $R_B C_G$ combination becomes larger, the pole moves towards the zero fre-

quency axis, lowering the circuit stability. Eventually it interacts with the pole contained in Z, $1/\tau_2$, and instability results.

The effects of stray capacitance on CFA closed-loop performance are shown in Figure 8–8.

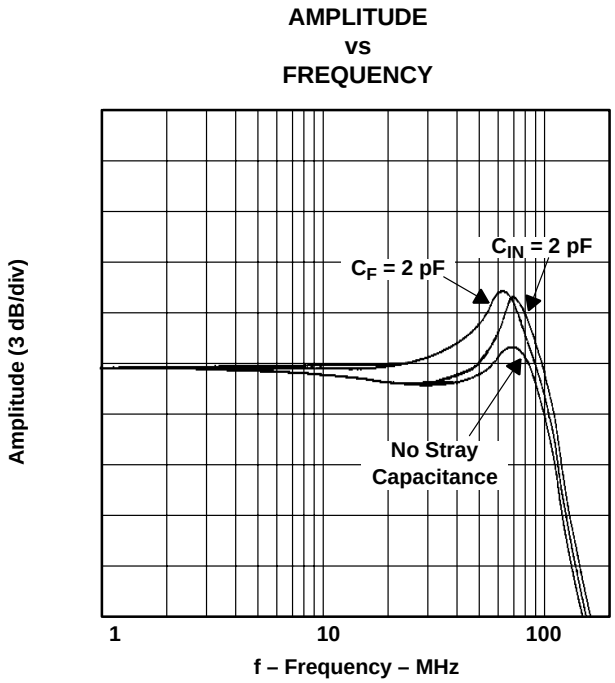

Figure 8–8. Effects of Stray Capacitance on CFAs

Notice that the introduction of C_G causes more than 3 dB peaking in the CFA frequency response plot, and it increases the bandwidth about 18 MHz. Two picofarads are not a lot of capacitance because a sloppy layout can easily add 4 or more picofarads to the circuit.

8.9 Stability and Feedback Capacitance

When a stray capacitor is formed across the feedback resistor, the feedback impedance is given by Equation 8–31. Equation 8–32 gives the loop gain when a feedback capacitor has been added to the circuit.

$$Z_F = \frac{R_F}{1 + R_F C_F s} \tag{8–31}$$

$$A\beta = \frac{Z\left(1 + R_F C_F s\right)}{R_F\left(1 + \frac{R_B}{R_F \| R_G}\right)\left(1 + R_B \| R_F \| R_G C_F s\right)} \tag{8–32}$$

This loop gain transfer function contains a pole and zero, thus, depending on the pole/zero placement, oscillation can result. The Bode plot for this case is shown in Figure 8–9. The original and composite curves cross the 0-dB axis with a slope of –40 dB/decade, so either curve can indicate instability. The composite curve crosses the 0-dB axis at a higher frequency than the original curve, hence the stray capacitance has added more phase shift to the system. The composite curve is surely less stable than the original curve. Adding capacitance to the inverting input node or across the feedback resistor usually results in instability. R_B largely influences the location of the pole introduced by C_F, thus here is another case where stray capacitance leads to instability.

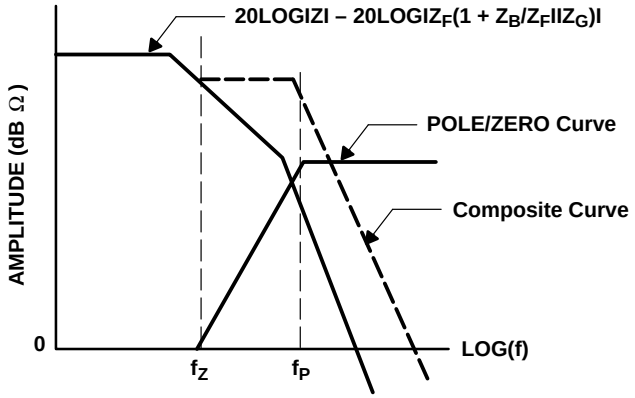

Figure 8–9. Bode Plot with C_F

Figure 8–8 shows that C_F = 2 pF adds about 4 dB of peaking to the frequency response plot. The bandwidth increases about 10 MHz because of the peaking. C_F and C_G are the major causes of overshoot, ringing, and oscillation in CFAs, and the circuit board layout must be carefully done to eliminate these stray capacitances.

8.10 Compensation of C_F and C_G

When C_F and C_G both are present in the circuit they may be adjusted to cancel each other out. The stability equation for a circuit with C_F and C_G is Equation 8–33.

$$A\beta = \frac{Z\left(1 + R_F C_F s\right)}{R_F\left(1 + \frac{R_B}{R_F \| R_G}\right)\left(R_B \| R_F \| R_G \left(C_F + C_G\right) s + 1\right)} \quad (8\text{–}33)$$

If the zero and pole in Equation 8–33 are made to cancel each other, the only poles remaining are in Z. Setting the pole and zero in Equation 8–33 equal yields Equation 8–34 after some algebraic manipulation.

$$R_F C_F = C_G\left(R_G \| R_B\right) \quad (8\text{–}34)$$

R_B dominates the parallel combination of R_B and R_G, so Equation 8–34 is reduced to Equation 8–35.

$$R_F C_F = R_B C_G \quad (8\text{–}35)$$

R_B is an IC parameter, so it is dependent on the IC process. R_B it is an important IC parameter, but it is not important enough to be monitored as a control variable during the manufacturing process. R_B has widely spread, unspecified parameters, thus depending on R_B for compensation is risky. Rather, the prudent design engineer assures that the circuit will be stable for any reasonable value of R_B, and that the resulting frequency response peaking is acceptable.

8.11 Summary

Constant gain-bandwidth is not a limiting criterion for the CFA, so the feedback resistor is adjusted for maximum performance. Stability is dependent on the feedback resistor; as R_F is decreased, stability is decreased, and when R_F goes to zero the circuit becomes unstable. As R_F is increased stability increases, but the bandwidth decreases.

The inverting input impedance is very high, but the noninverting input impedance is very low. This situation precludes CFAs from operation in the differential amplifier configuration. Stray capacitance on the inverting input node or across the feedback resistor always leads to peaking, usually to ringing, and sometimes to oscillations. A prudent circuit designer scans the PC board layout for stray capacitances, and he eliminates them. Breadboarding and lab testing are a must with CFAs. The CFA performance can be improved immeasurably with a good layout, good decoupling capacitors, and low inductance components.