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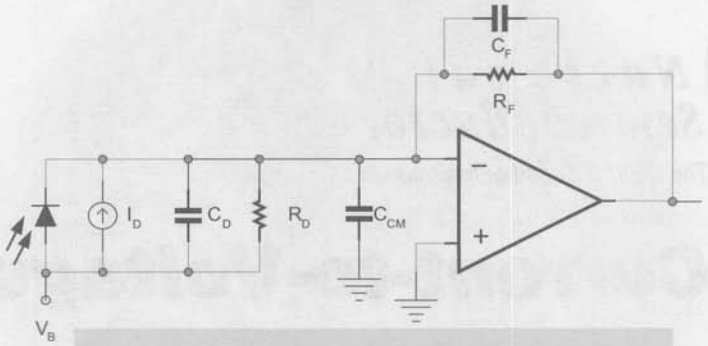
The Sight & Sound of Information

Current-to-Voltage or Transimpedance

Photodiode I-V Converters



- $100K < R_D < 100Gohm$ It halves every 10deg. C
- $10pF < C_D < 500pF$
- V_B (negative polarity) would reduce C_D
- $C_{IN} = C_D + C_{CM}$ where C_{CM} is the Op Amp Common Mode input capacitance, $1pF < C_{CM} < 10pF$ for most Op Amp's
- C_F = parasitic cap across R_F (~0.5pF) + Compensation Cap.
- C_{CM} = Op Amp Common Mode input capacitance $1pF < C_{CM} < 10pF$ for most Op Amp's

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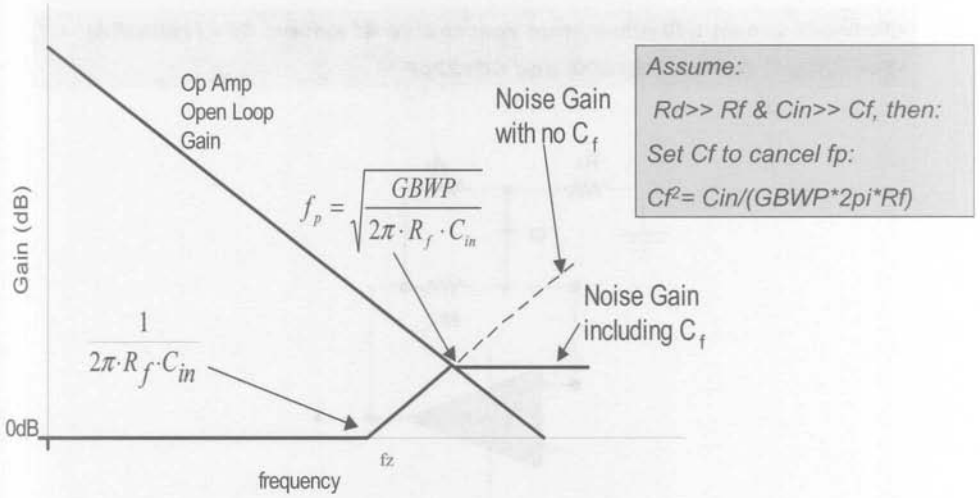
The Art of Analog 60

There are many applications which use photo diode to detect the intensity of the incident light. Examples would be: Barcode scanners, light meters, fiber optic receivers, industrial sensors, etc. The diode has a nearly linear output current for a very large range of light intensity. The voltage across the diode is held constant in order to minimize non-linearities.

Here is a schematic of a typical circuit used to convert the diode current into a voltage, along with the parasitic components of the diode and the amplifier. The op amp is an ideal candidate to do this since it has minimal input current and its high open loop gain will eliminate voltage variations at the Cathode. The higher speed applications could tie the Anode side to a negative potential in order to reduce the diode capacitance. As we shall see later, this capacitance is troublesome in two ways: It reduces the achievable bandwidth and necessitates stability compensation. Also, it tends to increase noise gain, as will be shown later. More sensitive diodes will tend to be of bigger area and will subsequently exhibit a higher capacitance. Rf determines the overall circuit sensitivity. So, one obvious tradeoff would be between raising the value of Rf (with resulting higher noise and lower BW) vs. increasing the diode area and having a larger Cd. In this schematic, Cin, the op amp's input capacitance is also included since it cannot be ignored in most cases.

Bode Plot Illustrating C_F Selection



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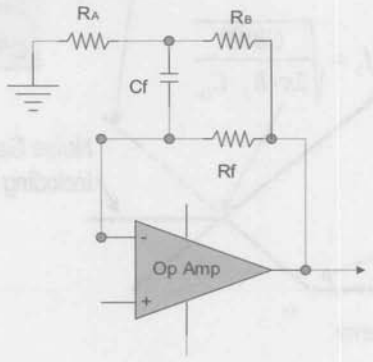
One interesting aspect of this type of amplifiers, also know as I-V converters, is that in almost all cases the frequency response needs to "shaped" or otherwise the circuit will oscillate. The high capacitance of the diode (including the op amp input capacitance), along with large Rf needed to get reasonable trans-impedance gain, will create enough phase shift around the loop that necessitates steps be taken to avoid oscillations.

As can be seen here, if Cf were not included, the noise gain plot would intersect the op amp open loop gain plot at a rate of closure of 40dB/decade. The noise gain is inverse of the feedback factor function. A zero in the noise gain corresponds to a pole in the feedback factor. Therefore, with no Cf, at the intersection point there is 180 degrees of phase shift and thereby oscillation would set in.

In order to operate properly, Cf would need to be chosen properly to set the noise gain pole to coincide with the op amp open loop gain plot as shown. This leads to a closed loop phase margin of 45 degrees. Under these conditions, the noise gain pole would be at the frequency shown (fp). This would be the BW of the I-V converter as well. If Cf is any larger, then the BW is excessively reduced.

Realistic Values

- ***Network shown will allow more reasonable Cf values: Cf'= (1+RB/RA)* Cf***
- ***For Cf=2pF, RA=50, RB=500, and Cf'=22pF***

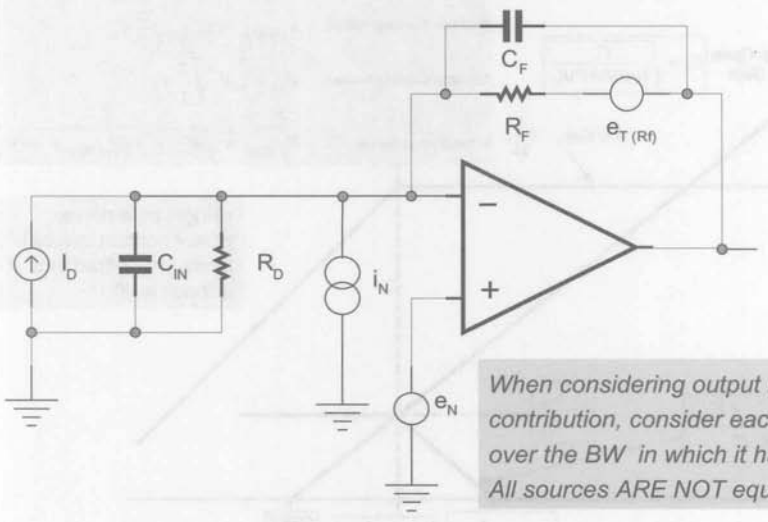


Often, the required Cf would be very small (<5pF), especially for the higher speed applications. In these cases, its often more practical to use the circuit above in order to allow more reasonable values.
The new value of Cf'= (1+RB/RA)* Cf
This relationship holds true as long as RA<<Rf.

As an example, if Cf=2pF, , select RA=50ohm,and RB=500ohm.
Therefore, Cf'=(1+500/50)*2pF= ~22pF
which is a much more practical component value.

This value needs to be "fine tuned" in the real application for proper step response.

The Noise Model



When considering output noise contribution, consider each source over the BW in which it has an effect. All sources ARE NOT equally weighted

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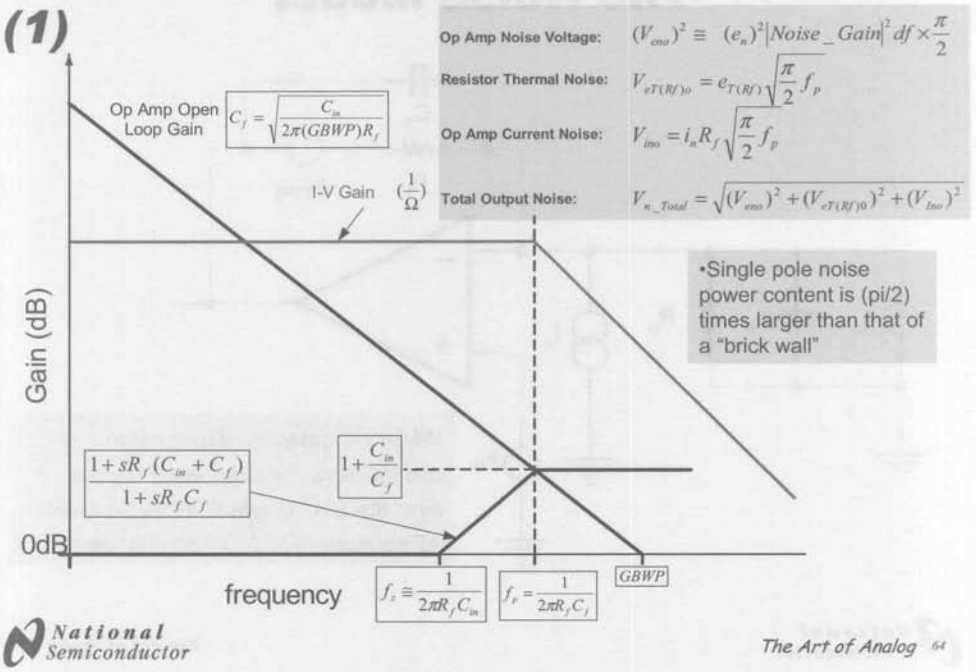
Here is the noise model for the I-V converter. When doing noise analysis, as always, all noise sources can be assumed to be independent of each other thereby allowing the response to be calculated by considering one noise source at the time. The final output noise would be the RMS (root mean square) of the individual noise sources contributions to the output voltage.

Input capacitances have been combined into a single Cin. The noise current on the non-inverting input has been ignored since it won't contribute to any noise at the output.

The thermal noise voltage of any resistor is 4nV* √[R(Kohm)]. Therefore, a 100Kohm resistor would have 40nV/√Hz of noise at 25°C. This noise would increase at the rate of √[Temp(K)]. So, going from 300°K to 400°K increases the noise by a factor of 1.15.

Noise Gain and Frequency Response (1)



When analyzing the noise at the output of the I-V converter, its important to note that the various noise sources (i.e. op amp noise voltage, feedback resistor thermal noise, input noise current, etc.) do not all operate the same frequency band. Therefore, when the noise at the output is calculated, this should be taken into account. Namely, the op amp noise voltage will be gained up in the region between the noise gain's "zero" and its "pole". The higher the value of Rf and Cin, the sooner the noise gain peaking starts and the larger would be it's contribution to the total output noise. Therefore, its obvious to note that its advantageous to minimize Cin (e.g. by proper choice of op amp, by applying a reverse bias across the diode at the expense of excess dark current and noise). Unfortunately, most low noise op amps have a higher input capacitance compared to ordinary ones.
The "π/2" factor within the square root will account for the single pole response.
For the op amp noise voltage, the calculation is slightly more complicated since the total noise contribution would involve an integration as the noise gain varies with frequency.
To maximize the I-V bandwidth for a given trans-impedance gain and photodiode, one would choose an Op Amp with high GBWP and low input capacitance. However, the input capacitance for an Op Amp is not always readily available on the data sheet.

Noise Gain and Frequency Response (2) An Example

$e_n = 10nV/\sqrt{Hz}$ $\quad i_n = 3pA/\sqrt{Hz}$

$f_z = 100KHz$ $\quad f_p = 1MHz$

C_{in}=50pF, C_F=5pF, R_F=32K

- The low frequency portion of the voltage noise contribution is negligible
- Between f_z and f_p, the Noise Gain is approximated by a +20dB/decade response having a "zero" at f_z: [Noise Gain (f)]^2=1+f ^{2} / f_z ^{2}

$$(V_{eno}')^2 = [10(\frac{nV}{\sqrt{Hz}})]^2 . \{ \int_{f_1}^{f_p} (1+\frac{f^2}{f_z^2}) df + 100(KHz) \}$$

$$= 100e-18 . \{ \int_{100KHz}^{1MHz} (1+\frac{f^2}{(100KHz)^2}) df + 100e3 \}$$

$$= 100e-18 . \{ [f + \frac{f^3}{3\times(10e9)}]_{100KHz}^{1MHz} + 100e3 \}$$

$$= 100e-18\times\{34.2e6+100e3\} \cong 100e-18\times34.2e6 = 3.43e-9(V^2)$$

$$V_{eno} = V_{eno}' \times \sqrt{\frac{\pi}{2}} = 73.4(\mu V)$$

$$V_{eF(RF)} = e_{F(RF)} \times \sqrt{\frac{\pi}{2}\times f_p} = 4(\frac{nV}{\sqrt{Hz}}) \times \sqrt{32} \sqrt{\frac{\pi}{2}\times 1e6} = 28.4(\mu V)$$

$$V_{ino} = i_n \times R_f \times \sqrt{\frac{\pi}{2}\times f_p} = 3(\frac{pA}{\sqrt{Hz}}) \times (32e3) \sqrt{\frac{\pi}{2}\times 1e6} = 120(\mu V)$$

$$V_{n\_Total} = \sqrt{V_{eno}^2 + V_{eF(RF)}^2 + V_{ino}^2} = \sqrt{(73.4)^2 + (28.4)^2 + (120)^2}(\mu V) = 144(\mu V)$$

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Here are the calculations based on an example to show how the noise is integrated over the noise gain. Here, the noise gain is assumed to have a single zero at 100KHz and the pole at 1MHz is ignored for simplicity. The noise density (nV/√Hz) function is multiplied by the noise gain magnitude and then squared before being integrated over the total range (0Hz to 1MHz).

The other simplifying assumption made is that the op amp noise voltage is constant over the entire range. This is not a bad assumption since the contribution of the 1/f region of the op amp is negligible in a situation like this where BW reaches into the MHz region.

As far as the input noise current (in) is concerned, there is only a single pole located at fp. The same is true for the RF noise voltage which sees a single rolloff at fp .

The resultant noise voltage from all sources is then summed together in a square root of the sum of the squares fashion before arriving at the total rms output noise (V).

It turns out that the dominant noise source would be the op amp input noise current. The op amp input noise current is given by: √(2qIb), where Ib is the input bias current. Therefore, it's obvious that choosing a device with minimal input bias current would be advantageous in terms of noise.

Optimization Guidelines

•Op Amp: the voltage noise and the current noise times Z_D should both be as small as you can get. If one of these noises is much larger than the other, then you're probably far off optimum. Lower input capacitance also helps to reduce the noise gain peaking effect. Noise is reduced by the square root of the BW.

•Photodiode: If you have a choice, choose one with low capacitance (at the expense of sensitivity). This would reduce noise gain peaking.

•R_F: A lower resistor value decreases resistor noise as a function of $\sqrt{(R)}$, but it also lowers the desired I-V gain as a direct function of R. Therefore, lowering R reduces the SNR at the output. The feedback resistor should be as large as possible to maximize SNR.

C_F: The noise contribution due to R_F can be decreased by raising the value of C_F (lowering f_p) but this reduces signal bandwidth.

For the op amp noise voltage, the highest noise contribution comes at the highest frequency ranges. Therefore, to calculate Zd (diode impedance), use the highest frequency of interest. As Zd decreases, the voltage noise becomes more dominant and vice versa. Therefore, the voltage and current noises can be conveniently and simply compared in this fashion.

As far as the diode capacitance is concerned, it is interesting to observe that if Cd is lowered, the noise gain peaking effect is reduced. This could have a very significant effect on the overall noise without effecting the BW. That is precisely why it's important to keep the total input capacitance low. On the other hand, increasing Cf would counteract the noise gain peaking at the expense of BW. The value of Cf is often times a compromise between the required BW and the noise gain.

List of Suitable Op Amps for I-V Conversion

Device	Input Noise Voltage (nV/RtHz)	Input Noise Current (pA/RtHz)	Input Capacitance (pF)	I_{bias} (max)	GBWP (MHz)	GBWP/C_{in} (MHz/pF)
LMH6628	2	2	1.5	20µA	200	133
LMH6626*	1.0	1.8	0.9	20µA	500	556
LMH6624*	0.92	2.3	0.9	20µA	500	556
LMH6622	1.6	1.5	0.9	10µA	200	222
LMH6654 /6655	4.5	1.7	1.8	12µA	150	83
LMH6672	4.5	1.7	2	14µA	100	50
LF411A	25	0.01	4	200pA	4	1
LMV751	7	0.005	5	100pA	5	1
LMC662	22	0.0002	4	0.01pA (typical)	1.4	0.3
LMV771	8	0.001	4	100pA	4	1

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*:Not Unity Gain Stable

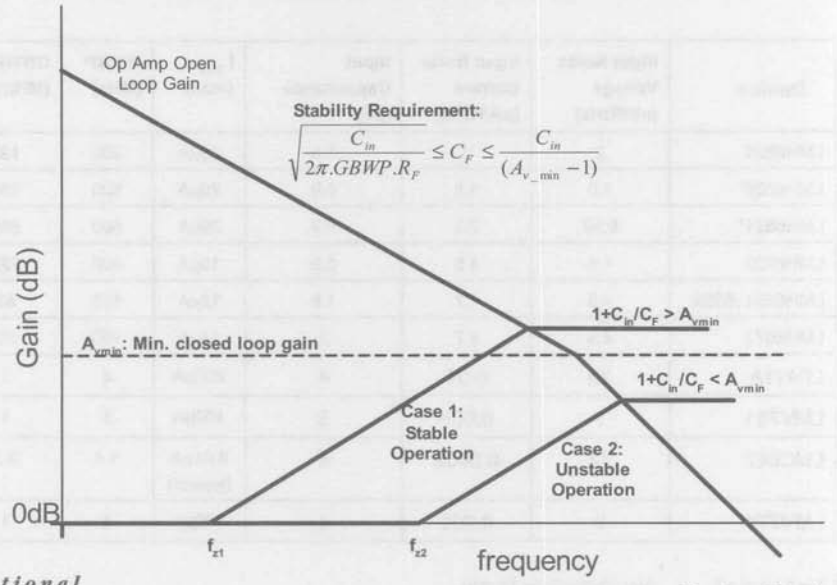
For current feedback Op Amps, the inverting current noise is usually much higher than that of the non-inverting input. Therefore, as far as noise is concerned, the CFA is not the best choice. All devices listed here are of the voltage feedback topology.

When considering the choice of device to be used, a rough measure of max possible I-V bandwidth would be the ratio of GBWP/Cin.

If ultra low noise and maximum DC accuracy are important in your application, you could use some of the amplifiers shown here with input bias currents in the pA range (last 4 devices from the bottom). As you can see, reducing the input bias current means an automatic improvement in input current noise as well. So, you gain higher DC accuracy and reduced noise at the same time!

In addition, the LMC662, LMV751, & LMV771 also allow input common mode voltage to extend below V-; this makes for easier interface to the Photo diode and could allow easy adoption to single supply use. The LMV751 & LMV771 could also allow usage down to very low supply voltages (2.7V).

Non-Unity Gain Stable Op Amp (Additional Constraint)



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Devices which have a minimum closed loop gain requirement (i.e. LMH6624 & LMH6626) need special considerations when it comes to stability. These devices are optimized to provide maximum possible speed for the amount of power they use. In the case of the LMH6624 & LMH6626, the minimum closed loop configuration is 10V/V (20dB). In the I-V converter configuration, there is the additional constraint of increasing Noise Gain which gives rise to further phase shift which must be accounted for.

To ensure stability, the following must hold true:

$1+C_{in}/C_F >= 10$ (this is dictated by the op amp's minimum closed loop gain). This can be simplified to $C_F <= C_{in}/9$

$C_F >= \sqrt{[C_{in}/(2\pi.GBWP.R_f)]}$ (this is dictated by the feedback characteristics discussed earlier).

IF the conditions above can be met simultaneously, the preferred value for C_F from a BW point of view would be the smaller of the two which is dictated by the feedback function (C_{in}, R_F, GBWP).

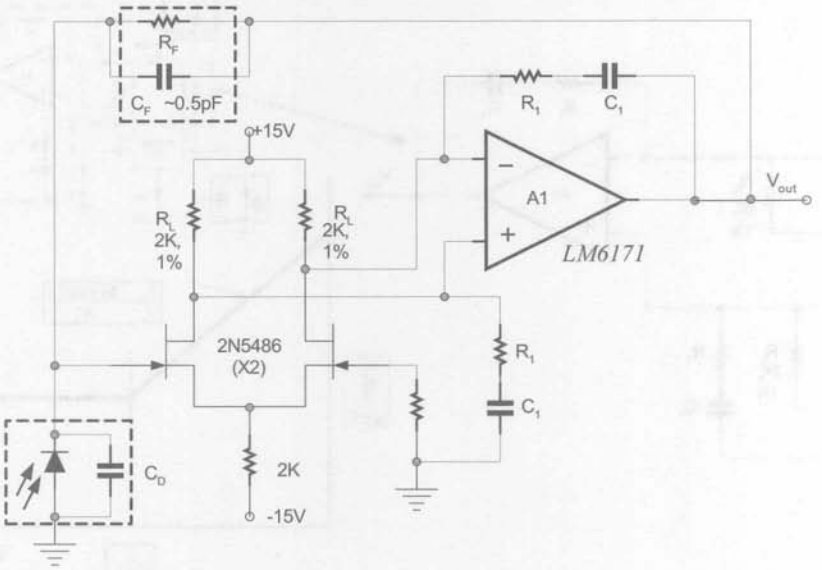
Therefore:

$\sqrt{[C_{in}/(2\pi.GBWP.R_f)]} < C_F < (C_{IN}/9)$

For the specific case of the LMH6624 & LMH6626, because of the large GBWP of these two devices, in almost all cases the solution exists. There will be a value of C_F which satisfies both conditions as long as:

$C_{in} >= 25.8e\text{-}9/ R_F$. In other words, with a nominal value of 20pF for C_{in}, the minimum trans-impedance gain would be 1200V/A or else the circuit would be unstable.

Composite I-V Converter



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As we found earlier, the input noise current could have a profound effect on overall noise, especially with large Rf. Here is a neat way to optimize the I-V converter.

The choice of good low-noise JFET's on the input eliminate input noise current as a contributing factor.

Here are the advantages of this composite amplifier over a simple op amp circuit:

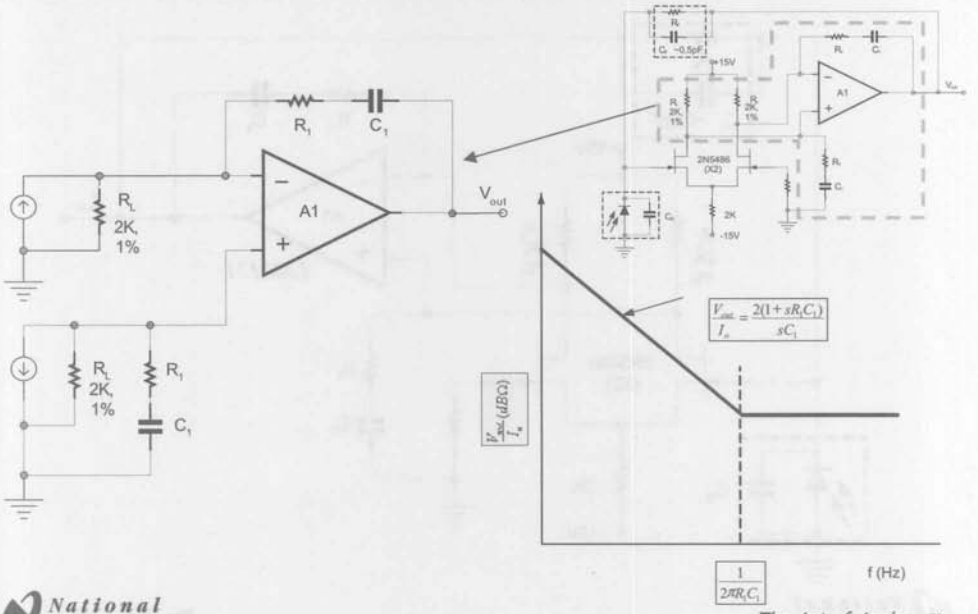
-Input differential pair tail current can be substantially increased to reduce input noise voltage.

-Input noise current would reduce significantly because of the FET's extremely low bias current

-By proper selection of compensation components R1 and C1, one could alter the open loop response to ensure stability. This is in contrast to the method discussed earlier which required increasing R_F, since this method would ultimately limit BW but R1, C1 setting won't.

When configured as shown, the noise requirements on the A1 are eased. The differential pair on the pair becomes the dominant factor in the overall noise. A good general purpose Op Amp such as the LM6171 would work well here allowing operation with +/-15V supplies thereby getting maximum dynamic range.

Composite I-V Converter Analysis



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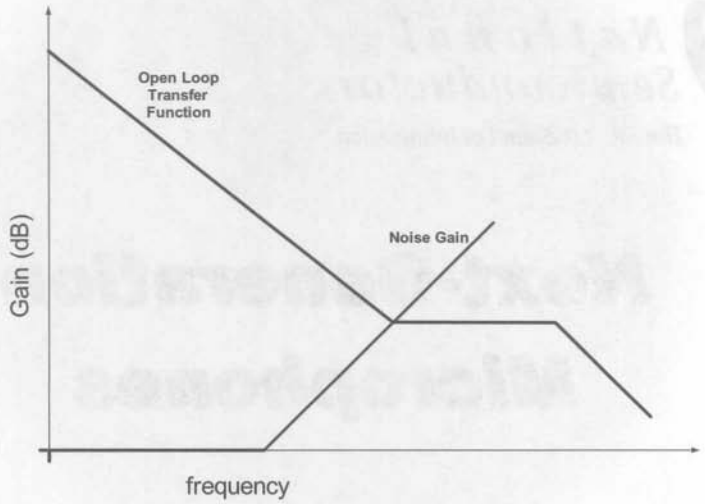
This is the schematic of the gain stage inside the composite amplifier shown on the previous slide. The schematic of the shaded area is isolated and shown on the left hand side. The current out of the JFET differential pair is shown as I_o. To the right is the bode plot of the transfer function to Vout.
In contrast to what has been discussed so far, this amplifier configuration allows the open loop gain response to be reshaped as opposed to the feedback factor (ie using C_F across R_F). The open loop gain of the previous page's schematic is shaped using the R1, & C1 placed inside the loop. Using 1% precision load resistors for the two load resistors (2Kohm), the open loop gain becomes a function of R1, & C1 only.

Shaping the Open Loop Gain Curve



The composite amplifier just discussed could be made to have an open loop response resembling that shown here by the proper selection of R1, and C1. As can be observed on this plot, the noise gain and the X curves intersect each other at a point where the phase shift around the loop is 135 degrees (Phase margin of 45 degrees). Note that the useable BW did not have to be sacrificed to ensure adequate phase margin in this case.

At the point of intersection, that is when loop gain is 0dB, the signal has already gone through 180 degrees of phase shift had there not been a zero in the open loop transfer function. The presence of this zero adds 45 degrees of phase lead around the loop resulting in 45 degrees of phase margin.