New Design Techniques for FET Op Amps

National Semiconductor
Application Note 63

INTRODUCTION

The LH0052, LH0042 and LH0022 series operational amplifiers are "monobrid" integrated circuits consisting of a monolithic dual junction field effect transistor followed by a special linear integrated circuit amplifier chip. Each device features very closely matched input characteristics, very high input impedance, and ultra low input currents with no compromise in noise, common mode rejection ratio, open loop gain or slew rate. The LH0052 is internally laser nulled and features offset current of 100 femtoamps max at 25°C (100 pA at +125°C), offset voltage of 100 microvolts max and offset drift of 5 μV/°C max. Unlike most module FET op amps, this series of op amps does not require "grading" of electrical performance at final test. Different die types are used in each member of the family to assure availability and lowest possible cost. The amplifiers are internally compensated to be unity gain stable and require no external parts for operation with the exception of feedback and input impedances as dictated by the application. Amplifiers are available in TO-99, (TO-5 metal can) or 14-lead cavity dual-in-line package and are specified either for the full military temperature range of −55°C to +125°C or for an expanded commercial temperature range of −25°C to +85°C. Operation is specified for power supply voltages between 10V (±5V) and 44V (±22V). Table I below, and Typical Performance Characteristics (last page) give a summary of other major parameters illustrating similarities and differences of members of the series. See individual data sheets for complete specifications.

WHY FETs?

The virtue of super gain bipolar transistors as the input stage to operational amplifiers is well known[1,2] and widely used in such amplifiers as the LM108, LM112, and LM216. These amplifiers attain very low input bias currents by special processing that allows the first stage to run at very low emitter currents while achieving current gains of 1500. This results in relatively constant bias and offset currents with temperature tending to increase at low temperatures where transistor gain is lowest. (*Figure 1.*)

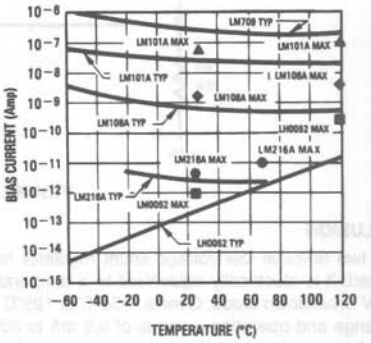

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FIGURE 1. Typical I_b vs. Temperature for Several Op Amps

TABLE I. Performance Comparison of LH0052/LH0022/LH0042 FET Op Amp Family

Parameter (T_A = 25°C)	LH0052	LH0022	LH0042	Units
Offset Voltage (Max)	0.5	4	20	mV
Offset Voltage Drift (Typ)	2	5	5	μV/°C
Offset Current (Max)	2.5	2.0	5.0	pA
Bias Current (Max)	1.0	10	25	pA
Open Loop Gain (Min)	100	100	50	V/mV
Bandwidth (Typ)	1	1	1	MHz
Slew Rate (Typ)	3	3	3	V/μs
Output Current Drive (Min)	±10	±10	±10	mA
Min Supply Voltage	±5	±5	±5	V
Max Supply Voltage	±22	±22	±22	V
Input Voltage Range (Min)	±12	±12	±12	V
CMRR (Min)	80	80	70	dB
Compensation Components	0	0	0	
Output Current Limit	Yes	Yes	Yes	
Simple Offset Null	Yes	Yes	Yes	
Package Types	TO-5	DIP, TO-5	DIP, TO-5	

The low emitter current available in the typical super gain amplifier severely limits the slew rate attainable, the devices that have input currents in the same area as the LH0052 family normally have slew rates in the neighborhood of a few tenths of a volt per microsecond. As long as a FET is operated in its normal linear region, its input current is not materially affected by the channel current. The LH0052 family, therefore, runs more input stage current and thus attains a typical slew rate of three volts per microsecond. A soon-to-be announced device (LH0062) has demonstrated slew rates greater than 50 V per μs with the same input characteristics as the LH0052 family.

FET's FEATURE SUPERIOR NOISE AT HIGH SOURCE RESISTANCES

Figure 2 is a plot of total amplifier noise at 100 Hz (1 Hz bandwidth) vs source resistance for the LH0052 family of FET amplifiers and the LM108, representative of the best super-gain bipolar amplifiers. Thermal noise contributed by the source resistance is also plotted. Note that at low source resistances the LM108 is lower noise; at high source resistance the LH0052 series is superior.

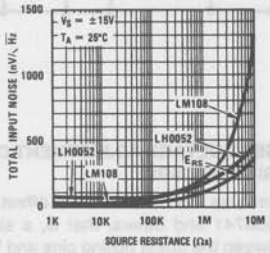

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FIGURE 2. Total Equivalent Input Noise Voltage

A useful noise model applicable to operational amplifiers in general is shown in *Figure 3*. It consists of an ideal noiseless amplifier preceded by a number of noise sources. Amplifier voltage noise, E_N, appears directly in series with one of the inputs. Current noise from the amplifier develops an additional noise voltage across the source resistance. The RMS value of thermal noise from the source resistances can be calculated from the equation $E_{rs} = \sqrt{4kT(BW)R_s}$ which simplifies to $E_{rs} = \sqrt{R_s}\ nV/\sqrt{Hz}$ for room temperature calculations and resistor values in kΩ.

The total spot noise present at the input to the ideal amplifier may be found by summing the RMS values of the three noise voltage sources as follows:

$$E_T = \sqrt{E_N^2 + 2\,(R_S I_N)^2 + 2E_{rs}^2}$$

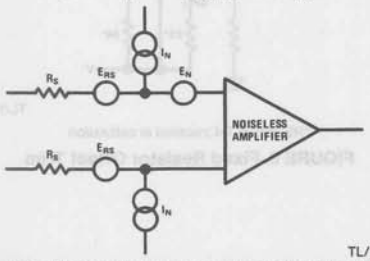

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FIGURE 3. Noise Model of an Operational Amplifier

E_N comes directly from data of the type plotted in the figure by looking at the flat portion of the curve below 10k and assuming that the current noise is insignificant in this area. For the LH0052 and LM108 E_N, at 100 Hz, 1 Hz bandwidth, is 70 $nV/\sqrt{Hz}$ and 35 $nV/\sqrt{Hz}$ respectively. I_N may be computed from a total noise measurement at high source resistance by using a calculated value of E_{rs} and the previously measured value of E_N.

$$I_N = \sqrt{(E_T^2 - E_N^2 - 2E_{rs}^2)/2R_s^2}$$

For the LH0052 family and the LM108, I_N is 10 $fA/\sqrt{Hz}$ and 100 $fA/\sqrt{Hz}$ respectively.

One way to illustrate the importance of noise current in deciding which of two amplifier types will be better in a given situation is to set the total noise equal for the two cases and solve for the value R_s at which this occurs. The amplifier with the lower noise voltage will be superior at source resistances lower than this value; the one with lower current noise will be better at higher resistances. Note that this is merely calculating the intersection of the curves of *Figure 2*. The intersection will normally lie near 150k when comparing the LH0052 family with the best of the presently available bipolar amplifiers.

LOW OFFSET VOLTAGE IS NO PROBLEM WITH MODERN JFETs

FETs have a reputation for poor control of voltage matching characteristics that developed from behavior of the early matched dual discrete devices. These were invariably a pair of separate FET chips mounted on the same header tested for gate to source voltage match at some specified current at room temperature. Devices constructed in this manner tracked rather poorly over temperature due to G_{fs} mismatch and temperature gradients across the header.

The monolithic dual FETs of the FM1100 series interweave the channels of the two halves of the device and achieve a match not only of V_{gs} but of all other parameters. Further, the V_{gs} match is preserved over a wide range of drain currents, drain to source voltage, and temperature. The voltage drift attainable with this technique is exceeded only by the very best bipolar devices.

It is possible to fabricate FETs and bipolar transistors on the same wafer at the same time. Why not build a single monolithic FET/bipolar amplifier utilizing each where it is best suited? It would seem at first glance that this would necessarily result in a cheaper, more reliable product. At the present state of the art, severe compromises are necessary to both the FET and bipolar devices so constructed as exemplified by the 740 and 536 with the net result that specifications must be relaxed and/or a yield loss suffered. The two chip "monobrid" approach taken with the LH0052 family maximizes performance while allowing lower cost.

CIRCUIT DESCRIPTION

Figure 4 is a simplified schematic typical of all of the amplifiers in the family. The input FET (Q_1, Q_2) is a monolithic dual similar in construction to the discrete FM1100 series device. The stage is operated as a source follower with V^+ applied directly to the drains for the maximum possible common mode range.

A differential common base PNP stage (Q_3, Q_4) serves as the load for the input FETs. The bases of this stage form the bias point for the backside gate of the monolithic input FET[3]. To obtain high voltage gain from the PNP common base stage, the output resistances of Q_5 and Q_6 are used

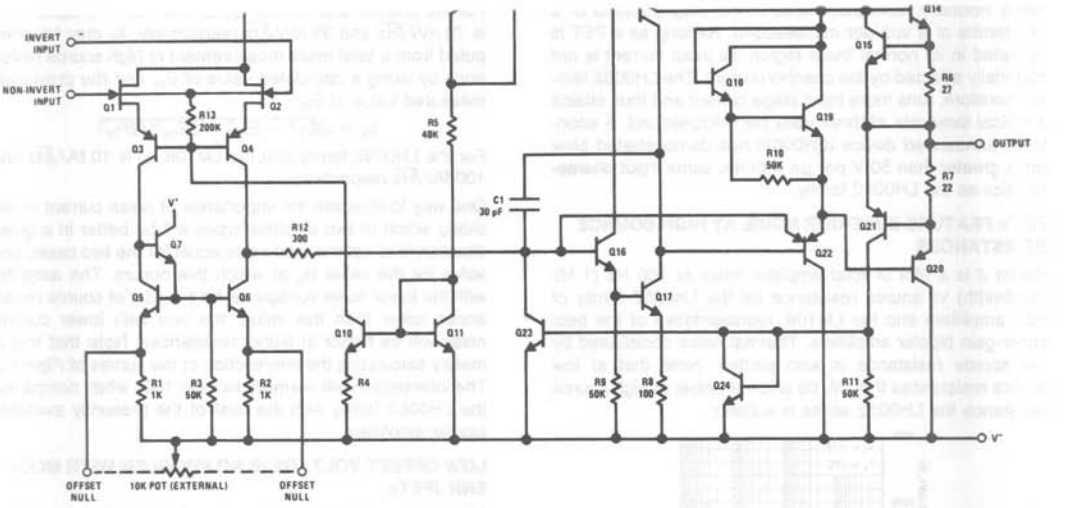

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FIGURE 4. Internal Schematic

as loads, giving effective values of about 2 mΩ while at the same time converting the differential current signal into a single ended voltage. The operating drain current for the input stage is determined by the bias network composed of the current source Q_{10} and the diodes Q_{11} and Q_{12}; target current is 40 μA per side.

A Darlington driver (Q_{16}, Q_{17}) is used to avoid loading the first stage output. The output stage uses a conventional complementary symmetry design with a bias current of about 60 μA through Q_{14} to Q_{20} to minimize crossover distortion. Output current is limited to about ±25 mA at 25°C ambient decreasing to about ±17 mA at +125°C. The output characteristics are similar to those of conventional amplifiers.

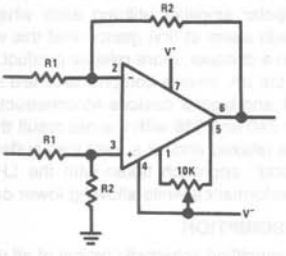

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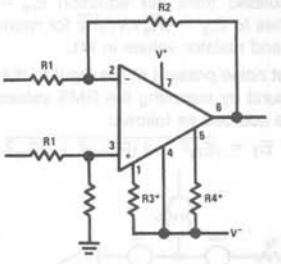
FIGURE 5. Trimpot Offset Trim

SIMPLE OFFSET VOLTAGE ADJUSTMENT DOES NOT DEGRADE DRIFT OF CMRR

These amplifiers use the same internal offset nulling technique as the LM741 and others, that is, a single 10k pot connected between the offset nulling pins and V⁻ as shown in *Figure 5*. Adjustment of this pot will always produce offset null. With the premium devices of the series, it may be desirable to restrict the range of adjustment to increase the precision of the null. This may be done by inserting a resistor of about 100k in series with the wiper of the pot. This technique provides a method of externally nulling offset voltage of the amplifiers to zero with virtually no effect on the offset voltage drift or CMRR.



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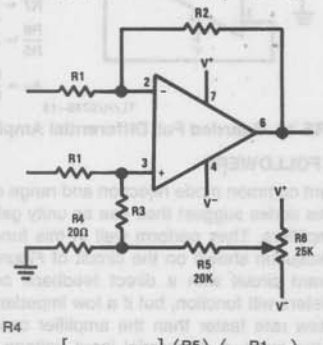
*R3 and/or R4 installed at calibration

FIGURE 6. Fixed Resistor Offset Trim

By definition, offset voltage is that voltage which must be applied between the input terminals to obtain zero output voltage. This suggests a straight-forward and practical "universal"[4] system to null the offset in an operating circuit. *Figure 7* illustrates one way that an adjustable voltage in the millivolt range may be connected in series with the input signal to subtract the amplifier offset. If this technique of offset nulling at the inputs of the amplifier is used, the TO-5 devices of the series will be pin compatible with virtually all of the 8-pin TO-5 amplifiers on the market today, bipolar or FET.

CAREFUL PC BOARD LAYOUT MUST BE OBSERVED

In order to realize the full low input current capabilities of these amplifiers, considerable care must be exercised in the design of the input circuitry and in the selection of materials contacting the input conductors. A leakage impedance of even $10^{12}\Omega$ to 15V produces a leakage current of 15 pA, much higher than amplifier input current. This level of leakage may be inadvertently produced by socket leakage, poor quality or imperfectly cleaned printed circuit boards, or improperly cured protective coatings. Sockets are to be avoided if possible; they can not only degrade leakage current, but may cause other unsuspected erratic behavior when used in severe environments. (IF absolutely unavoidable, they should be high quality, preferably Teflon.) Printed circuit board material should be judged both on initial resistivity and on the likelihood of degradation by outside influences. Teflon and polycarbonate are particularly recommended; glass epoxy may be used if it is protected with a silicone or epoxy coating to prevent moisture absorption. If operation at high humidities is required, this coating will be desirable anyway to control surface leakage. All residues of previous operations, such as soldering flux, inks, and resists, must of course be thoroughly removed before coating.



$R2 = R3 + R4$

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$$\text{Adjustment Range} \approx \left[(V^+) - (V^-)\right]\left(\frac{R5}{R4}\right)\left(\frac{R1}{R1 + R3}\right)$$

$$\text{Voltage Gain} = \frac{R2}{R1}$$

FIGURE 7. Universal Offset Trim

Another approach which has been successfully used with the TO-5 amplifiers is to terminate all critical connections on Teflon standoff insulators. These may be interconnected as required with Teflon insulated wire, keeping connections as short as possible to minimize noise pick-up. A short length of Teflon tubing slipped over the wire from the amplifier prevents contact with the oversize hole in the mounting board. The remainder of the amplifier connections may be terminated conventionally, either to printed circuit lands or to other standoff insulators.

INPUT GUARDING IMPROVES SYSTEM PERFORMANCE

Even with properly cleaned and coated printed circuit boards, leakage currents can limit the circuit performance under severe environmental conditions. In most cases with the LH0052 family devices, leakage will be primarily to V^- as the inputs are between the offset null pin (which in normal operation runs at a voltage very near V^-) and the V^- pin itself. This would seem to predict that leakage into the inverting and non-inverting inputs should at least be of the same polarity, but the effects are too unpredictable to make much use of the cancellation which should occur.

These currents may be intercepted before they reach the amplifier inputs by a guard conductor in the leakage path operating at the same potential as the inputs. Resistance between the inputs and the guard will cause little current to flow because of the premise that the guard voltage equals the input voltage. Suggested board layouts for the various package types are shown in *Figures 8* through *11*.

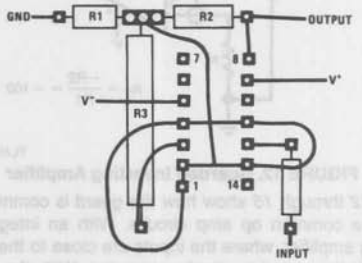

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FIGURE 8. DIP Non-Inverting Amplifer PC Layout

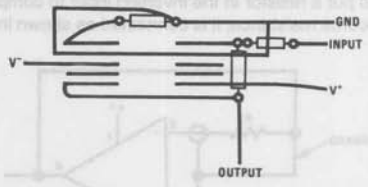

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FIGURE 9. Flat Pack Inverting Amplifier PC Layout

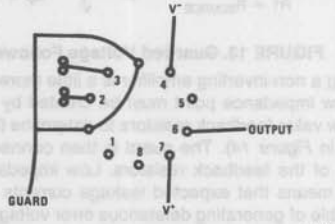

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FIGURE 10. TO-5—10 Pin Pattern PC Layout

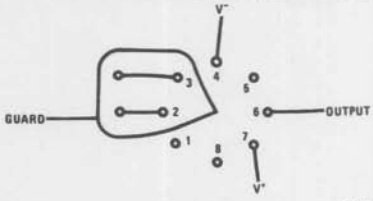

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FIGURE 11. TO-5—8 Lead Pattern

The flat pack and dual-in-line packages have an unconnected pin on either side of the inputs. These may be used as shown, both to continue the guard into the package and as a convenient method of surrounding the inputs with a guard conductor without running a line between device pins. The eight lead TO-5 package has only one spare pin, so the leads must either be formed into a 10 lead circle with two gaps, or the pin circle expanded sufficiently to allow a conductor to pass between device pins. If the board is double sided or multilayer, the guard pattern should be repeated on all conductor planes.

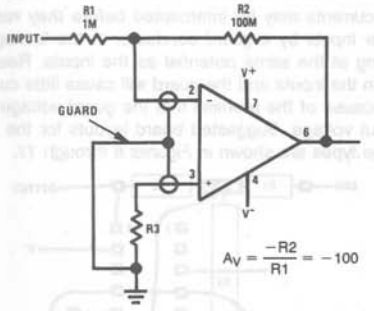

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FIGURE 12. Guarded Inverting Amplifier

Figure 12 through *15* show how the guard is committed on the more common op amp circuits. With an integrator or inverting amplifier, where the inputs are close to the ground potential, the guard is simply grounded. With the voltage follower, the guard is bootstrapped to the output. If it is desirable to put a resistor in the inverting input to compensate for the source resistance, it is connected as shown in *Figure 13.*

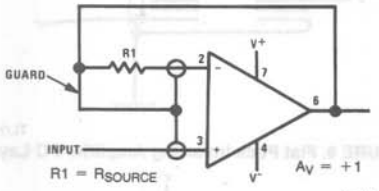

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FIGURE 13. Guarded Voltage Follower

Guarding a non-inverting amplifier is a little more complicated. A low impedance point must be created by using relatively low value feedback resistors to determine the gain (R_1 and R_2 in *Figure 14*). The guard is then connected to the junction of the feedback resistors. Low impedance in this context means that expected leakage currents should not be capable of generating deleterious error voltages. A resistor, R_3, may be added to balance the source resistance and thus cancel the effect of bias current.

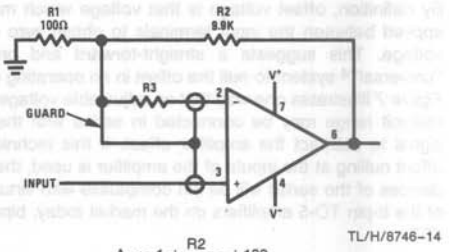

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FIGURE 14. Guarded Non-Inverting Amplifier

The general case of a full differential configuration may require the use of a guard driver amplifier A_2 as shown in *Figure 15.* Resistors R_5 and R_6 develop the proper voltage for the guard at their junction, but it will normally be impractical to make them low enough resistance due to source loading. R_7 is included to balance the effect of R_5 plus R_6 and thus not degrade the closed loop common mode rejection.

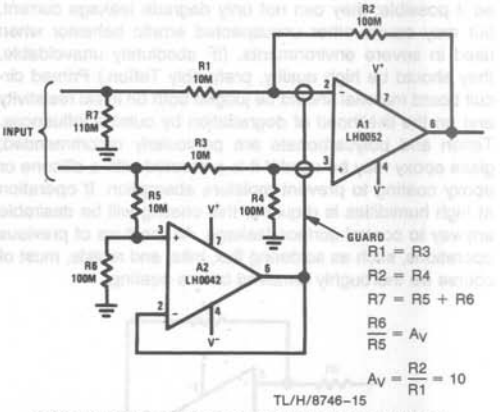

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FIGURE 15. Guarded Full Differential Amplifier

VOLTAGE FOLLOWERS

The excellent common mode rejection and range of the amplifiers in this series suggest their use as unity gain voltage follower amplifiers. They perform well in this function with the one precaution shown on the circuit of *Figure 16.* The straightforward circuit with a direct feedback connection and no resistors will function, but if a low impedance signal having a slew rate faster than the amplifier can follow is applied to the input, a differential input voltage might be developed in excess of the absolute maximum. R_1 limits the current under these conditions to a safe value of 200 μA. R_2 is included to cancel the error voltage due to bias current and should in general be equal to the source resistance plus R_1.

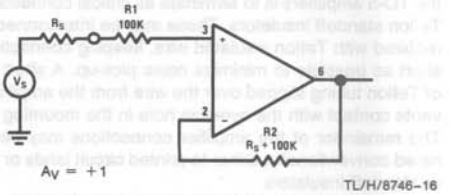

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FIGURE 16. Unity Gain Voltage Follower

For applications requiring voltage gain as well as high input impedance, a voltage divider may be included in the feedback path as-in *Figure 17*. The voltage gain of this circuit is approximately $1 + R_2/R_3$ (neglecting amplifier open loop gain).

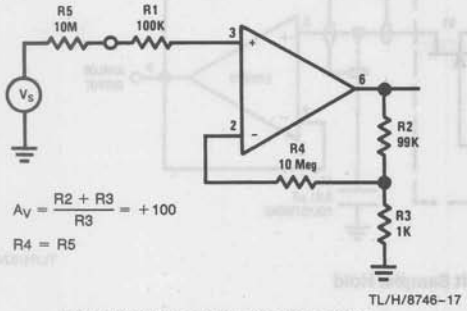

FIGURE 17. Non-Inverting Amplifier

R_4 is included as a convenient variable to equalize resistances in the two amplifier inputs: R_4 in series with the parallel combination of R_2 and R_3 should be set equal to the source resistance plus R_1. Note that all of these resistors may not be necessary depending on the required voltage gain, source impedance, accuracy requirement, temperature range, and amplifier selected.

PRECISION INTEGRATOR

The low input bias currents attainable with amplifiers of this series make them a natural choice for integrator applications requiring long time constants. *Figure 18* illustrates a typical practical circuit. R_1 should be selected so that the total leakage current at the summing node is smaller than the signal current (V_1/R_1) by a margin sufficient to insure the required accuracy, i.e., $V_1/R_1 \geqslant I_{b1}$. C_1 should be chosen for low leakage, stability, accuracy, and low voltage coefficient. Polystyrene or polycarbonate dielectric is the best choice for capacitances up to about 1 μF. Teflon is good for the lower values.

R_2 is included to protect the input circuit during the reset transient, although many low speed applications will not require it at all. If the resistance of the reset switch is 100Ω, the maximum current that could flow in C_1 is 10V/100 = 0.1 amp. In reality this may well be limited to a lower value by I_{DSS}, if the reset switch is an FET. Then the rate of change of voltage cannot exceed 0.1 amp/1 μF = 0.1 V/μs which is well within the slew rate capability of the amplifier. R_3, used to balance the resistance in the inputs, should be made equal to the sum of R_2 and the reset switch resistance.

SAMPLE/HOLD AMPLIFIERS

The LH0052 family of amplifiers is well suited for use as a buffer amplifier in long hold-time sample/hold circuits. They may be used in any of the common configurations where improved hold performance is required. *Figure 19a* illustrates one circuit taking advantage of the low bias currents attainable. R_1 serves to bootstrap the connection between analog switch S_1 and S_2 so that there is essentially no voltage across S_1 in the hold mode. When S_1 and S_2 are closed to enter the sample mode, the effect of R_1 is slight as it is much higher resistance than the switches. After a long enough time, C_1 will charge to the input voltage, the amplifier will buffer it to the output, and both ends of R_1 will be at the input potential so it will have no effect at all after the transient. *Figure 19b* illustrates an alternate circuit configuration with input buffer amplifier.

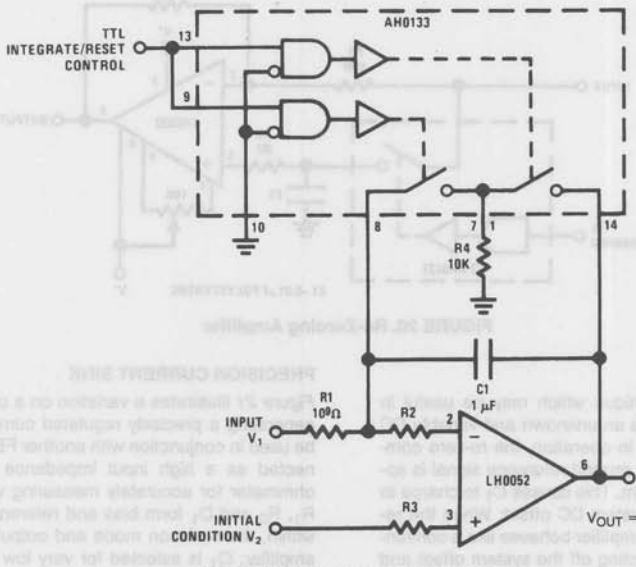

FIGURE 18. Precision Integrator

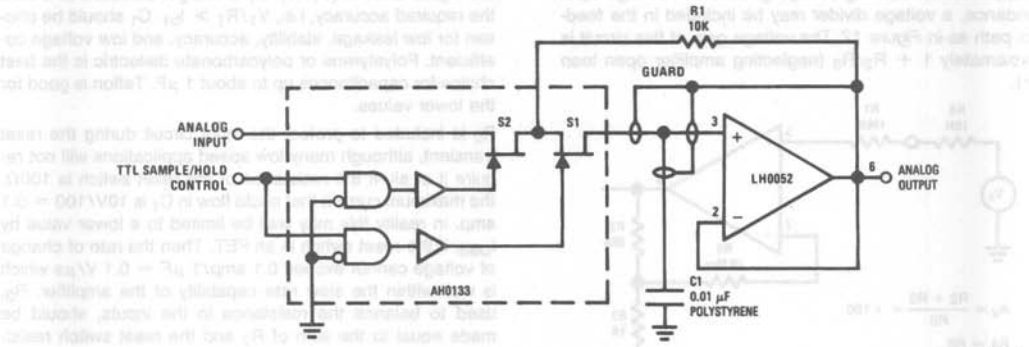

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FIGURE 19a. Low Drift Sample/Hold

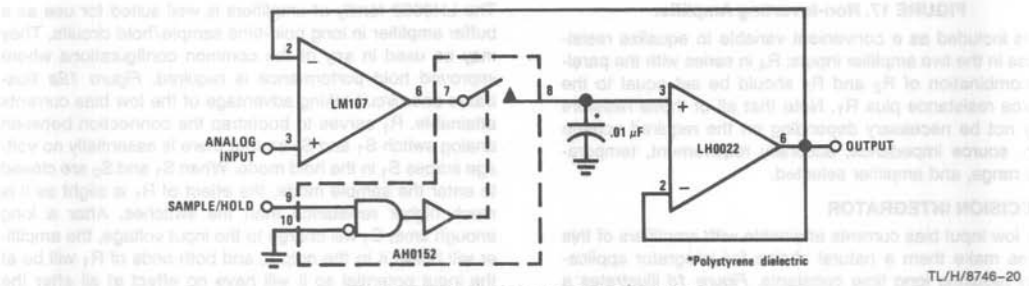

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FIGURE 19b. Precision Sample and Hold

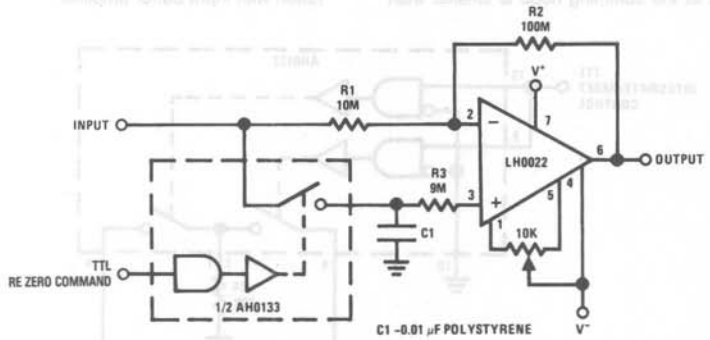

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FIGURE 20. Re-Zeroing Amplifier

RE-ZEROING AMPLIFIER

Figure 20 illustrates a technique which may be useful in situations where a signal has an unknown and variable DC offset, such as in telemetry. In operation, the re-zero command line is enabled while a ground reference signal is applied to the input of the system. This causes C_1 to charge to a level proportional to the system DC offset. When the re-zero line is deactivated, the amplifier behaves like a conventional inverting stage, subtracting off the system offset and giving a true ground referenced output.

If the total worst case leakage at the capacitor node is 1 nA, and if $C_1 = 0.01\ \mu F$, then the drift rate is $10^{-9}/0.01 \times 10^{-6} = 0.1$ V/s. For a 10V full scale system requiring an accuracy of 0.1% (10 mV), the amplifier would need re-zeroing reference every 100 ms.

PRECISION CURRENT SINK

Figure 21 illustrates a variation on a common technique for generating a precisely regulated current. This circuit could be used in conjunction with another FET input amplifier connected as a high input impedance follower to form an ohmmeter for accurately measuring very high resistances. R_1, R_2 and D_1 form bias and reference voltages near, but within, the common mode and output voltage limits of the amplifier. Q_1 is selected for very low gate leakage so that the current in its source will be nearly identical to the feedback current in its drain. In operation, the amplifier output will cause the gate of Q_1 to be cut off however much is necessary to keep the voltage across R_3 equal to 1.220V, the breakdown voltage of D_1. The LM113 diode is available to an initial voltage accuracy of 1% (12.2 mV) and is guaran-

teed to drift less than 15 mV over the temperature range, thus by specifying the LH0052 amplifier and a 1% resistor, a current sink can be designed for a worst case initial accuracy near 2% and a drift over the temperature range of less than 2%. The technique may be applied over a wide range of currents by properly scaling R_3 and its balancing resistor R_4; a mirror image current source is possible using a P channel FET for Q_1.

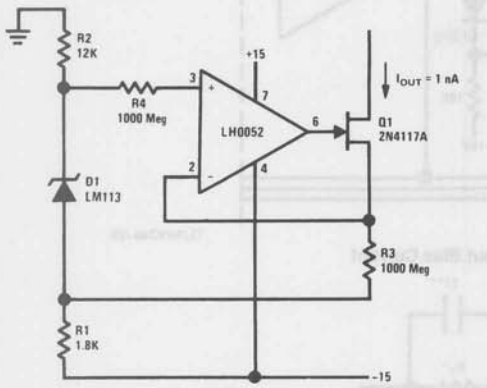

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FIGURE 21. Precision Current Sink

PRECISION COMPARATOR

FET amplifiers have a significant advantage over bipolar in precision voltage comparator applications: the input current is nearly independent of input voltage. With a bipolar input stage, input current is $1/\beta$ of the emitter current, but the emitter current can vary from zero when the stage is cut off to twice the nominal value when fully conducting. Furthermore, the inputs are often internally clamped to a diode drop for protection of the emitter base junctions.

As long as the input and reference signals are no more than 4V apart in the circuit of *Figure 22,* the input currents remain low and constant. This is an adequate signal range for many applications, especially in view of the offset voltage performance available in the top of the line amplifiers. If wider signal range is required, resistors R_1 and R_2 should be included to limit the input current to a safe value. Internal zener junctions will limit the differential input voltage to a safe value if the input current is limited 200 μA.

The output clamp circuit shown in *Figure 22* will drive 3 standard TTL loads or 30 National low power TTL loads. Considerable power may be saved by increasing R_3 if full fan-out is not required. If only 2 low power loads are to be driven, the required low state output current is 360 μA, so R_3 = 10V/360 μA = 27k.

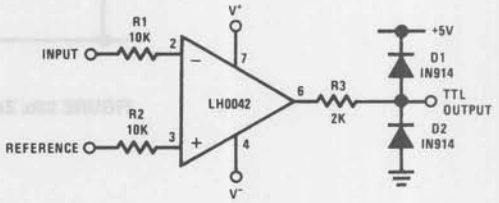

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FIGURE 22. Precision Voltage Comparator

TRUE INSTRUMENTATION AMPLIFIER

Figure 23a illustrates an instrumentation amplifier that features high differential and common mode input resistance ($10^{12}\Omega$), ±10V common mode and differential mode input range, 0.01% gain accuracy at A_V = 1000, and 110 dB CMRR with 1 kΩ imbalance in bridge source resistance. Input current is less than 1 pA and offset drift is less than 5 μV/°C. R_1 provides a simple means of adjusting gain over a wide range without degrading CMRR. R_2 is an initial trim used to maximize CMRR without using super precision

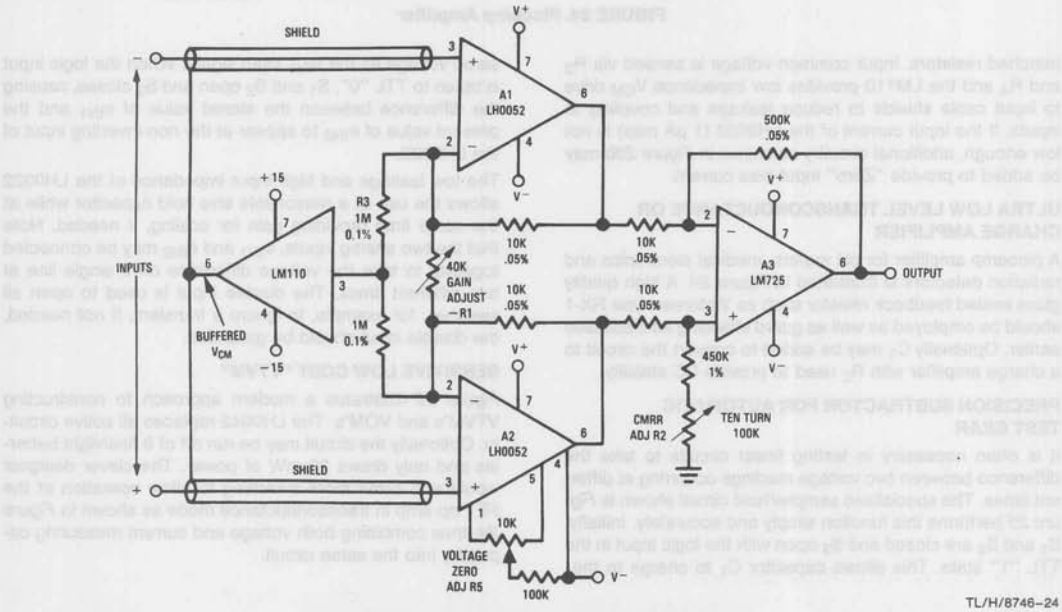

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FIGURE 23a. True Instrumentation Amplifier

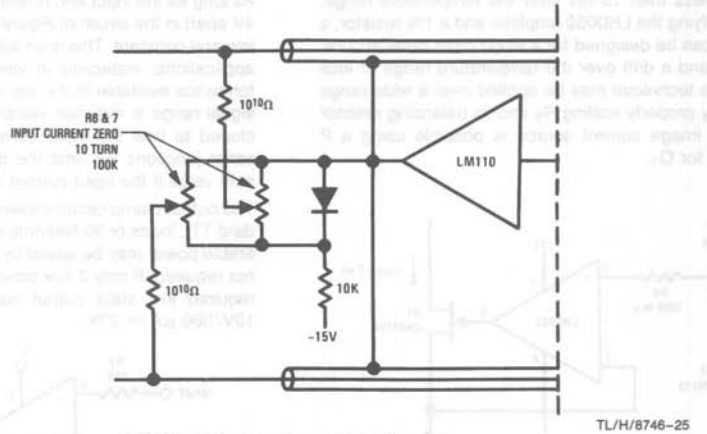

FIGURE 23b. Zero Input Bias Current

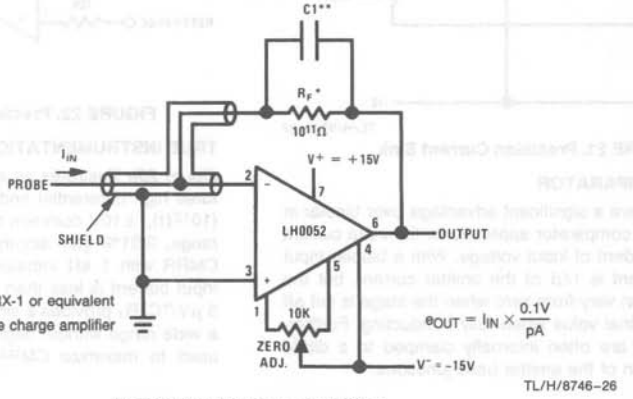

FIGURE 24. Picoamp Amplifier

matched resistors. Input common voltage is sensed via R_3 and R_4 and the LM110 provides low impedance V_{CM} drive to input cable shields to reduce leakage and coupling to inputs. If the input current of the LH0052 (1 pA max) is not low enough, additional circuitry as shown in *Figure 23b* may be added to provide "Zero" input bias current.

ULTRA LOW LEVEL TRANSCONDUCTANCE OR CHARGE AMPLIFIER

A picoamp amplifier for pH meters, medical electronics and radiation detectors is illustrated in *Figure 24*. A high quality glass sealed feedback resistor such as Victoreen type RX-1 should be employed as well as guard shielding as discussed earlier. Optionally C_1 may be added to convert the circuit to a charge amplifier with R_L used to provide DC stability.

PRECISION SUBTRACTOR FOR AUTOMATIC TEST GEAR

It is often necessary in testing linear circuits to take the difference between two voltage readings occurring at different times. The specialized sample/hold circuit shown is *Figure 25* performs this function simply and accurately. Initially, S_1 and S_2 are closed and S_3 open with the logic input in the TTL "1" state. This allows capacitor C_1 to charge to the same voltage as the e_{IN1} input signal. When the logic input is taken to TTL "0", S_1 and S_2 open and S_3 closes, causing the difference between the stored value of e_{IN1} and the present value of e_{IN2} to appear at the non-inverting input of the LH0022.

The low leakage and high input impedance of the LH0022 allows the use of a reasonable size hold capacitor while at the same time providing gain for scaling, if needed. Note that the two analog inputs, e_{IN1} and e_{IN2} may be connected together to take the voltage difference on a single line at two different times. The disable input is used to open all switches, for example, to ignore a transient. If not needed, the disable input should be grounded.

SENSITIVE LOW COST "VTVM"

Figure 26 illustrates a modern approach to constructing VTVM's and VOM's. The LH0042 replaces all active circuitry. Optionally the circuit may be run off of 8 flashlight batteries and only draws 20 mW of power. The clever designer would add some more switching to allow operation of the FET op amp in transconductance mode as shown in *Figure 24*, thus combining both voltage and current measuring capability into the same circuit.

HOW TO BUILD A FET OP AMP "MODULE"

The LH0052 series when compared spec for spec with modules usually offers superior performance and significantly lower cost. What's the difference between modules and these integrated circuit amplifiers? In most cases the answer is nothing but two 0.01 μF power supply decoupling capacitors. To make your own module merely build a small 1¼ x 1¼ printed circuit board that adapts the pin-out of the LH0052 to your module requirement. No need to pot the assembly in epoxy, the LH0052 family is completely hermetic and does not absorb moisture. Some modules specify higher output current capability than the ±10 mA of the LH0052. To build a ±100 mA output "module" FET op amp, simply add a LH0002 buffer as shown in *Figure 27.*

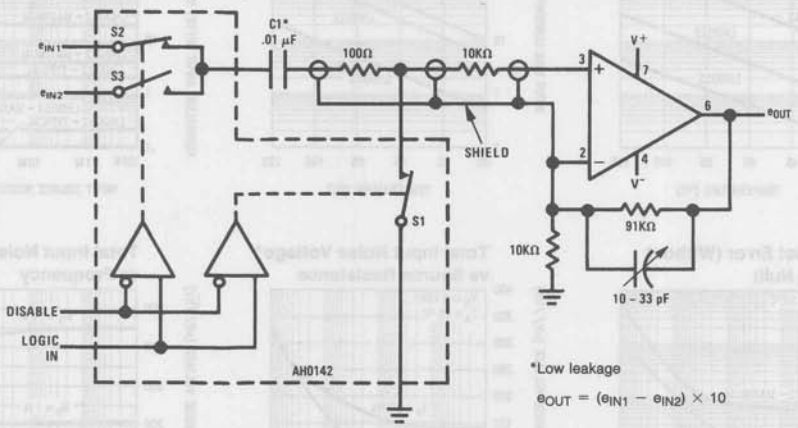

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FIGURE 25. Precision Subtractor for Automatic Test Gear

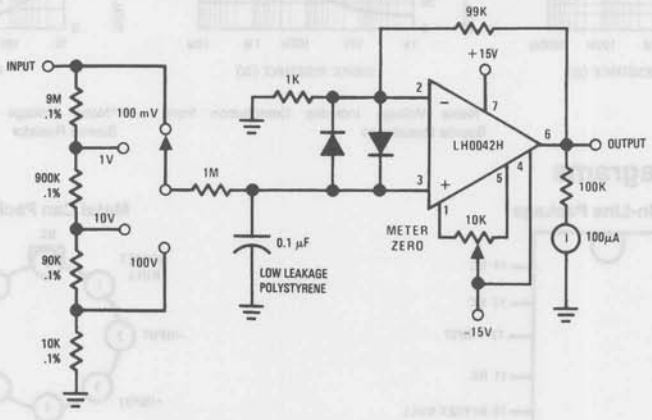

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FIGURE 26. Sensitive Low Cost "VTVM"

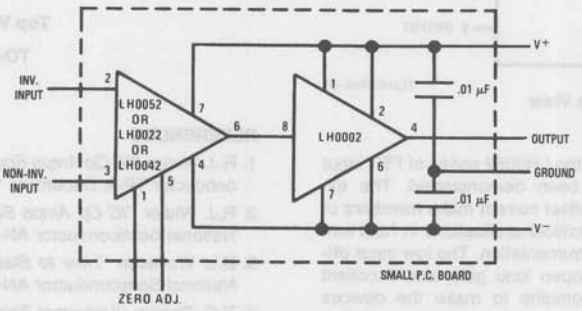

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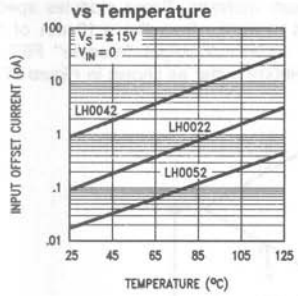
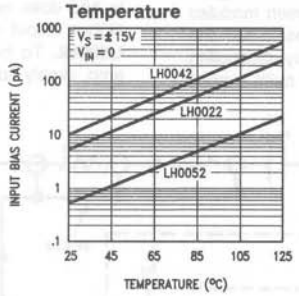
FIGURE 27. 100 mA Output FET Op Amp "Module"

Typical Performance Characteristics

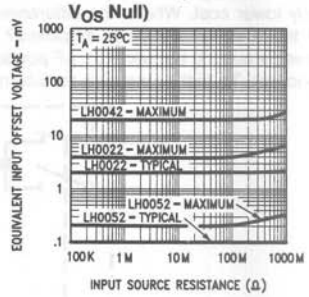
Input Offset Current vs Temperature



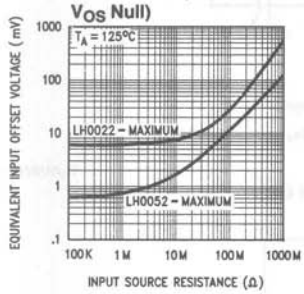
Input Bias Current vs Temperature



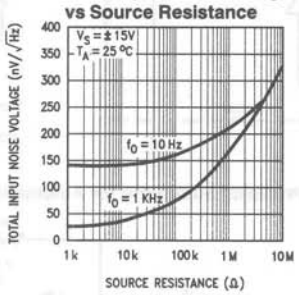
Offset Error (Without V_{OS} Null)



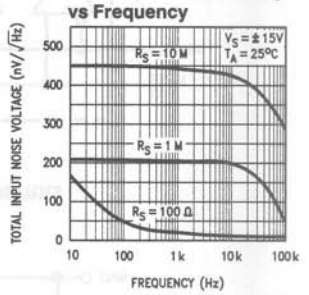
Offset Error (Without V_{OS} Null)



Total Input Noise Voltage* vs Source Resistance



Total Input Noise Voltage* vs Frequency



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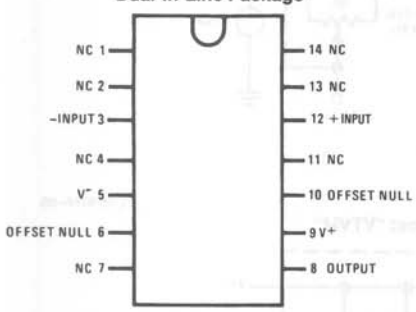
*Noise Voltage Includes Contribution from Source Resistance

*Noise Voltage Includes Contribution from Source Resistor

Connection Diagrams

Dual-In-Line Package



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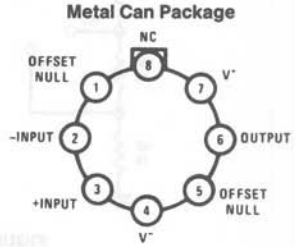
Top View

Metal Can Package



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Top View

TO-5

CONCLUSION

The practical advantages of the LH0052 series of FET input operational amplifiers has been demonstrated. The extremely low input bias and offset current make members of the family ideal choices for critical applications in hold amplifiers, active filters and instrumentation. The low input offset voltage and drift, high open loop gain, and excellent common mode rejection combine to make the devices equally well suited for general purpose applications including summers, subtractors, and oscillators.

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