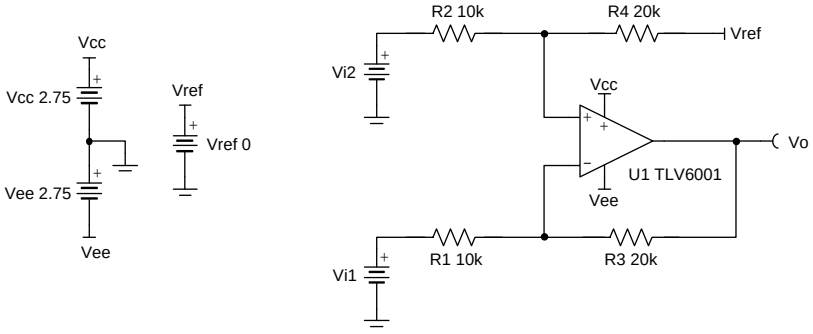
Difference amplifier (subtractor) circuit

Design Goals

Input (V_{i2}-V_{i1})		Output		CMRR (min)	Supply		
$V_{idiffMin}$	$V_{idiffMax}$	V_{oMin}	V_{oMax}	dB	V_{cc}	V_{ee}	V_{ref}
–1.25V	1.25V	–2.5V	2.5V	50	2.75V	–2.75V	0V

Design Description

This design inputs two signals, V_{i1} and V_{i2}, and outputs their difference (subtracts). The input signals typically come from low-impedance sources because the input impedance of this circuit is determined by the resistive network. Difference amplifiers are typically used to amplify differential input signals and reject common-mode voltages. A common-mode voltage is the voltage common to both inputs. The effectiveness of the ability of a difference amplifier to reject a common-mode signal is known as common-mode rejection ratio (CMRR). The CMRR of a difference amplifier is dominated by the tolerance of the resistors.



Design Notes

1. Use the op amp in a linear operating region. Ensure that the inputs of the op amp do not exceed the common-mode range of the device. Linear output swing is usually specified under the A_{OL} test conditions.
2. The input impedance is determined by the input resistive network. Make sure these values are large when compared to the output impedance of the sources.
3. Using high-value resistors can degrade the phase margin of the circuit and introduce additional noise in the circuit.
4. Avoid placing capacitive loads directly on the output of the amplifier to minimize stability issues.
5. Small-signal bandwidth is determined by the noise gain (or non-inverting gain) and op amp gain-bandwidth product (GBP). Additional filtering can be accomplished by adding a capacitors in parallel to R_3 and R_4. Adding capacitors in parallel with R_3 and R_4 will also improve stability of the circuit if high-value resistors are used.
6. Large signal performance may be limited by slew rate. Therefore, check the maximum output swing versus frequency plot in the data sheet to minimize slew-induced distortion.
7. For more information on op amp linear operating region, stability, slew-induced distortion, capacitive load drive, driving ADCs, and bandwidth please see the Design References section.

Design Steps

The complete transfer function for this circuit is shown below.

$$V_o = V_{i1} \times \left(-\frac{R_3}{R_1}\right) + V_{i2} \times \left(\frac{R_4}{R_2+R_4}\right) \times \left(1+\frac{R_3}{R_1}\right) + Vref \times \left(\frac{R_2}{R_2+R_4}\right) \times \left(1+\frac{R_3}{R_1}\right)$$

If $R_1 = R_2$ and $R_3 = R_4$ the transfer function for this circuit simplifies to the following equation.

$$V_o = (V_{i2} - V_{i1}) \times \frac{R_3}{R_1} + Vref$$

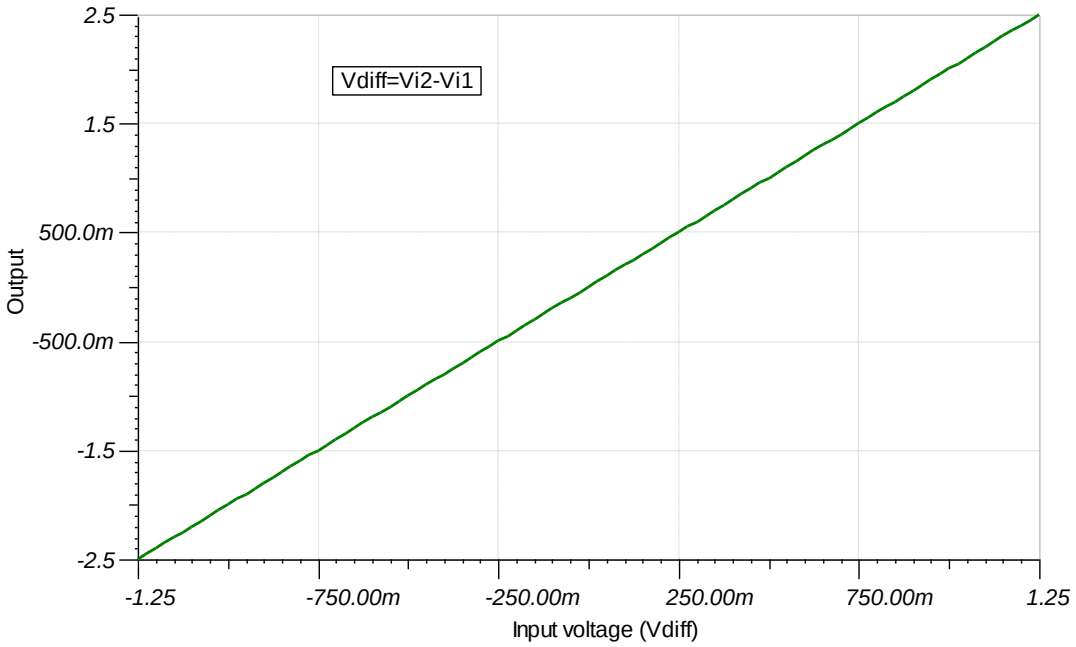
- Where the gain, G, is R_3/R_1.

1. Determine the starting value of R_1 and R_2. The relative size of R_1 and R_2 to the signal impedance of the source affects the gain error.
   $$R_1 = R_2 = 10k\Omega$$
2. Calculate the gain required for the circuit.
   $$G = \frac{V_{oMax} - V_{oMin}}{V_{idiffMax} - V_{idiffMin}} = \frac{2.5V-(-2.5V)}{1.25V-(-1.25V)} = 2\frac{V}{V} = 6.02dB$$
3. Calculate the values for R_3 and R_4.
   $$G = 2\frac{V}{V} = \frac{R_3}{R_1} \rightarrow 2 \times R_1 = R_3 = R_4 = 20k\Omega$$
4. Calculate resistor tolerance to meet the minimum common-mode rejection ratio (CMRR). For minimum (worst-case) CMRR, α = 4. For a more probable, or typical value of CMRR, α = 0.33.
   $$CMRR_{dB} \cong 20\log10\left(\frac{1+G}{\alpha \times \varepsilon}\right)$$
   ( ) ( )
   $$\varepsilon = \frac{1+G}{\alpha \times 10^{\frac{CMRR_{dB}}{20}}} = \frac{3}{4 \times 10^{\frac{50}{20}}} = 0.024 = 0.24\% \rightarrow \text{Use } 0.1 \text{ \% resistors}$$
5. For quick reference, the following table compares resistor tolerance to minimum and typical CMRR values assuming G = 1 or G = 2. As shown above, as gain increases so does CMRR.

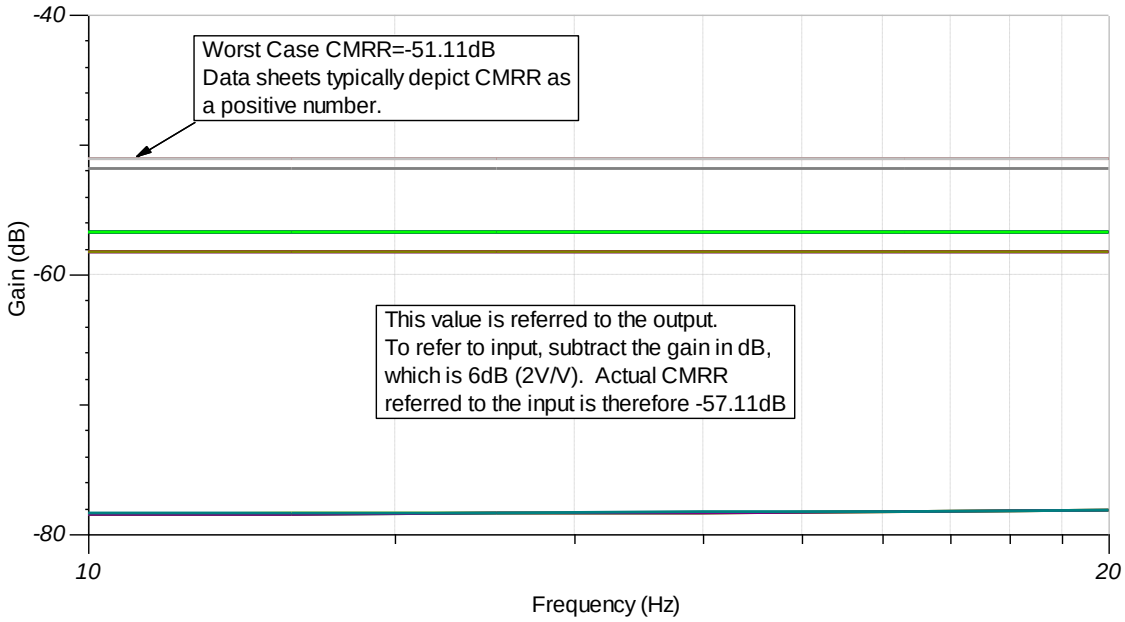
Tolerance	G=1 Minimum (dB)	G=1 Typical (dB)	G=2 Minimum (dB)	G=2 Typical (dB)
0.01%=0.0001	74	95.6	77.5	99.2
0.1%=0.001	54	75.6	57.5	79.2
0.5%=0.005	40	61.6	43.5	65.2
1%=0.01	34	55.6	37.5	59.2
5%=0.05	20	41.6	23.5	45.2

Design Simulations

DC Simulation Results



CMRR Simulation Results



Design References

See Analog Engineer's Circuit Cookbooks for TI's comprehensive circuit library.

See circuit SPICE simulation file SBOC495.

For more information on many op amp topics including common-mode range, output swing, bandwidth, and how to drive an ADC please visit TI Precision Labs. For more information on difference amplifier CMRR, please read Overlooking the obvious: the input impedance of a difference amplifier .

Design Featured Op Amp

TLV6001	
V_{ss}	1.8V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	750µV
I_q	75µA
I_b	1pA
UGBW	1MHz
SR	0.5V/µs
#Channels	1, 2, 4
www.ti.com/product/tlv6001	

Design Alternate Op Amp

OPA320	
V_{ss}	1.8V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	40µV
I_q	1.5mA
I_b	0.2pA
UGBW	20MHz
SR	10V/µs
#Channels	1, 2
www.ti.com/product/opa320	

Revision History

Revision	Date	Change
A	January 2019	Downscale title. Added link to circuit cookbook landing page.