A 10-BIT MONOLITHIC CMOS D/A CONVERTER THAT CAN BE USED FOR 4-QUADRANT MULTIPLICATION

by Jim Cecil and Jerry Whitmore

The AD7520* is a 10-bit multiplying digital-to-analog converter constructed on a single silicon chip. It consists of 10 CMOS (complementary metal-oxide-semiconductor) switches and a thin-film-on-CMOS R-2R ladder network. The digital input, which responds to the wide voltage swings of CMOS logic, is also compatible with TTL/DTL logic levels. Two complementary current outputs are available for use with inverting operational amplifiers.

Besides the 10-bit resolution, the AD7520 family has maximum nonlinearities as low as ±0.05% of V_{REF}, nonlinearity temperature-coefficient of 2ppm/°C, and maximum feedthrough error of ½ least-significant bit (LSB = 0.1%) at 100kHz. Typical settling time following a full-scale digital input change is 500ns.

In addition to a constant or variable reference (current or voltage), of either positive or negative polarity, the AD7520 requires one external operational amplifier for unipolar digitally-set gains (2-quadrant multiplication) or two amplifiers for bipolar gains (4-quadrant multiplication).

The 74 x 96 mil (1.88 x 2.44mm) chip, normally housed in a 16-pin hermetically-sealed ceramic dual in-line package, can also be made available in a flatpack or plastic DIP. It will operate from a single +5 or +15V power supply, and it dissipates only 20mW, including the ladder network.

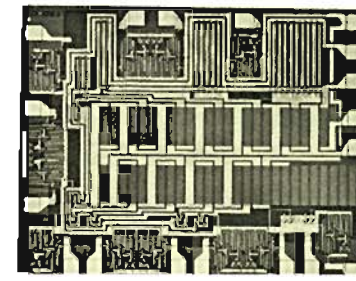
It can be used for D/A and A/D conversion, multiplication and division, programmable power supplies, digitally-programmed filters, and digital-analog function generation. Besides unipolar conversion (of either polarity), offset-binary, two's-complement, and sign-magnitude bipolar operation can also be implemented.

ADVANTAGES OF CMOS D/A CONVERSION

Commercially-available monolithic D/A converters have been, as of this writing, principally processed by conventional bipolar linear processing by conventional bipolar linear processing techniques. While 6- and 8-bit converters have been easily achievable, 10-bit conversion has been more difficult to obtain with good yields (and low cost) because of the finite β of the switching devices, the V_{BE}-matching requirement, the matching and tracking requirements on the resistance ladders, and the tracking limitations caused by the thermal gradients produced by high internal power dissipation.

All of these problems can be solved or avoided with CMOS devices. They have nearly-infinite current gain, eliminating β problems. There is no equivalent in CMOS circuitry to a bipolar transistor's V_{BE} drop; instead, a CMOS switch in the *on* condition is almost purely resistive, with the resistance value controllable by device geometry. The temperature-tracking problems of diffused resistors were solved easily: they weren't used.

*For complete information on the AD7520, use the reply card. Request **L1**.



The R-2R ladder is composed of 2kΩ/square silicon-chromium resistors (a 10kΩ resistor has a very manageable length/width of 5:1), deposited on the CMOS die. While the absolute temperature coefficient of these resistors is 150ppm/°C, their tracking with temperature is better than 1ppm/°C. The feedback resistor for the output amplifier is also provided on the chip, to ensure that the DAC's gain-temperature coefficient is better than 10ppm/°C by compensating for the absolute temperature coefficient of the network.

Finally, the low on-chip dissipation of only 20mW (including the dissipation of the ladder network), in conjunction with the excellent tracking capabilities of the thin-film resistors, minimizes linearity-drift problems caused by internally-generated thermal gradients. It also helps to minimize the power and cooling requirements for circuitry that the AD7520 is used in.

(continued on p. 4)

IN THIS ISSUE

Volume 8, No. 1, 1974

Figure 1 shows a functional diagram of the D/A converter, which employs an inverted R-2R ladder.[1] Binary-weighted currents flow continuously in the shunt arms of the network; with 10V applied at the reference input, 0.5mA flows in the first, 0.25mA in the second, 0.125mA in the third, and so on. The I_{OUT_1} and I_{OUT_2} output busses are maintained at ground potential, either by operational-amplifier feedback, or by a direct connection to common.

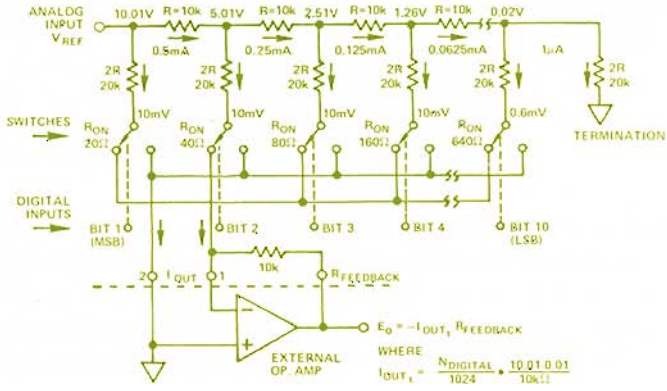


Figure 1. Functional diagram of the AD7520 D/A converter, with V_{REF} = 10.01V. Bits 5-9 are omitted for clarity.

The switches steer the current to the appropriate output lines in response to the individually-applied logic levels. For example, a "high" digital input to SW1 will cause the 0.5mA of the most-significant bit (MSB) to flow through I_{OUT_1}. When the digital input is "low," the current will flow through I_{OUT_2}. If I_{OUT_1} flows through the summing point of an operational amplifier and I_{OUT_2} flows to ground, then "high" logic will cause the nominal output voltage of the op amp to be - (0.5mA) x (10kΩ) = -5V, for a positive reference voltage of 10V, while "low" logic will make the contribution of Bit 1 zero. With all bits *on* (i.e., "high"), the nominal output will be -9.99V. With all bits *off*, the output will be zero.

Linearity errors, and – more important – their variation with temperature, are affected by variations of resistance in both the resistors and the switches. As we have seen, the resistor-network tracking is excellent. However, it is natural to expect that the switches, while tracking one another, will not track the resistance network. With identical switches having realistic resistance values (say 100Ω), one would expect that, as temperature changed, the variation of resistance in the series legs would transform the network into an R-*n*R network, with *n* sufficiently different from 2 to destroy the binary character of the network and cause the converter to become non-monotonic.

The key to the linearity of the AD7520 is that the geometries of the switches are tapered so as to obtain *on* resistances that are related in binary fashion, for the first 6 bits. Thus, the nominal values of switch resistance range from 20Ω for the first bit, 40Ω for the second bit, through 640Ω for the last 5 bits. The effect is, as can be seen in Figure 1, to provide equal voltages at the ends of the 6 most-significant arms of the ladder (0.5mA x 20Ω = 0.25mA x 40Ω, etc. = 10mV). Since this drop is, in effect, in series with the reference, it causes an initial 0.1% scale-factor ("gain") error, which is well within the specifications, but does not affect the linearity. Since the switches tend to track one another with temperature, linearity is essentially unaffected by temperature changes, and the gain error is held to within the 10ppm/°C specification.

Ten-bit linearity could, of course, have been obtained by scaling the *on* resistance of all the switches to a negligible value, say 10Ω, but the switches would have required very large geometries, which would result in a 30% to 50% larger chip, at a substantial increase in cost.

Figure 2 illustrates one of the 10 current switches and its associated internal drive circuitry. The geometries of the input devices 1 & 2 are scaled to provide a switching threshold of 1.4V, which permits the digital inputs to be compatible with TTL, DTL, and CMOS. The input stage drives two inverters (4, 5, 6, & 7), which in turn drive the N-channel output switches.

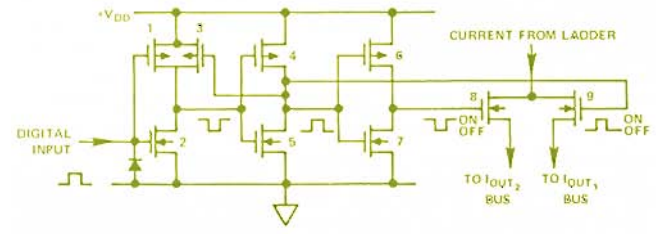


Figure 2. CMOS switch used in the AD7520. Digital input levels may be DTL, TTL, or CMOS.

EQUIVALENT CIRCUIT

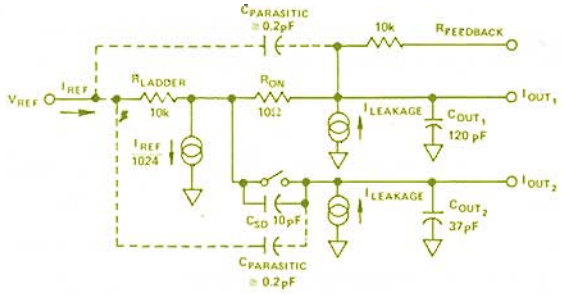
Figure 3 shows the equivalent circuit of the AD7520 at the two extremes of input, all inputs "high" (a) and all inputs "low" (b). V_{REF} (or I_{REF}, if a current reference is used) sees a nominal 10kΩ resistance, regardless of the switch states. The current source $I_{REF}/1024$, represents a 1 LSB current loss through the 20kΩ ladder-termination resistor, shown in Figure 1. R_{ON}, in this case, is the equivalent resistance of all ten switches connected to the I_{OUT_1} bus (a) or the I_{OUT_2} bus (b). Current-source I_{lkg} represents junction- and surface-leakage to the substrate. Capacitors C_{OUT_1} and C_{OUT_2} are the output capacities-to-ground for the *on* and *off* switches. CSD is the open-switch capacitance.

The 1000:1 ratio between R_{ladder} and R_{ON} provides a number of benefits, all related to the small voltage drop across R_{ON}:

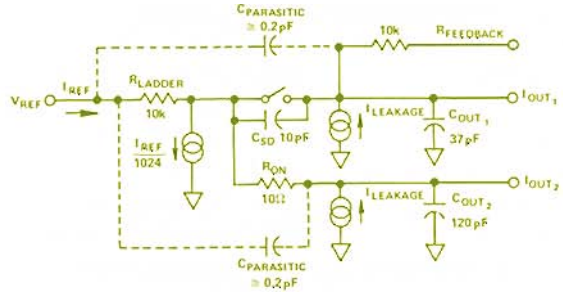
- V_{REF} can assume values exceeding the absolute-maximum CMOS rating, V_{DD}. For example, V_{REF} could be as large as ±25V, even if the AD7520's V_{DD} rating were only +17V.
- The nonlinearity temperature-coefficient depends primarily on how well the ladder resistances track. Since R_{ON} is only a small fraction of R_{ladder}, any R_{ON} tracking errors will be felt only as 2nd- and 3rd-order effects.
- The same argument holds true for power-supply variations. Any change of switch *on* resistance, as the power supply changes, will be swamped by the 1000:1 attenuation factor. Power-supply rejection is better than 1/3 LSB per volt.
- If V_{REF} is a fast ac signal, the feedthrough coupling via CSD, the open-switch capacitance, will be negligible, again be-

[1] The inverted R-2R ladder is one of the structures shown (Figure 18, page II-38) in the *Analog-Digital Conversion Handbook*, edited by D. H. Sheingold, published by Analog Devices, Inc., 1972, 402 pp., $3.95. To order a copy on approval, initial the reply card and request L2.

cause of the 1000:1 voltage stepdown. The parasitic capacitances from V_{REF} to I_{OUT_1} and I_{OUT_2} comprise the major source of ac feedthrough. Careful board layout by the user can result in less than ½ LSB of ac feedthrough at 100kHz.



a. All digital inputs high



b. All digital inputs low

Figure 3. Equivalent circuits of the AD7520 D/A converter

Since the *on* resistance depends only on the value of V_{DD}, not the current through the switch, and the resistance network is unaffected by V_{REF}, the full-scale output current (all bits "high") is nominally $V_{REF}/10.01k\Omega$, less the "constant" current losses shown in Figure 3. This means that I_{OUT} is almost perfectly proportional to V_{REF} over the whole range from -10V to +10V. Equally important, the conversion linearity error (0.05%) is independent of the sign or magnitude of V_{REF}.

The extremely-low analog-linearity error at constant digital input results in excellent fidelity to the input waveform, which suggests some interesting possibilities for the AD7520 in the calibration and control of gain in signal generators, high-fidelity amplifiers, and response-testing systems.

APPLYING THE AD7520

The two most common forms of application are in unipolar D/A conversion (2-quadrant multiplication) and bipolar offset-binary conversion (4-quadrant multiplication), shown in Figures 4 and 5. Where high speed is not desired, the output amplifier may be an AD741. For faster response, the AD518, AD505, or AD509* may be used, with appropriate compensation and a 10–20pF feedback capacitor.

Unipolar conversion. The response equation for Figure 4 is nominally

$$E_o = -\frac{N_{binary}}{1024} V_{REF}$$

Responses to typical codes are tabulated. Since V_{REF} may be positive or negative, two-quadrant multiplication is inherent. Circuit gain is easily trimmed by adjusting V_{REF}, inserting adjustable resistance in series with V_{REF} or $R_{feedback}$, or by tweaking scale factors elsewhere in the system. As noted elsewhere, once set, using low-TC trim resistors, gain stability with temperature is excellent.

*For data on these amplifier types, request **L3**.

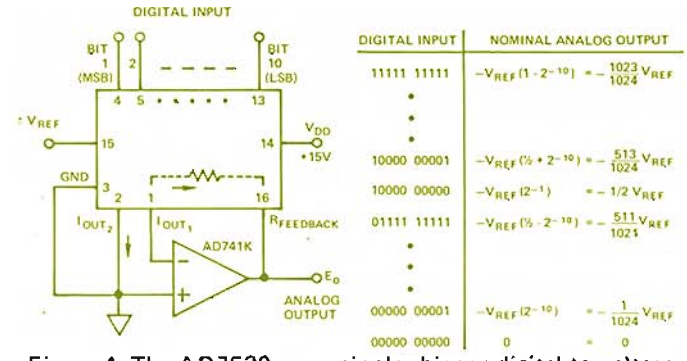


Figure 4. The AD7520 as a unipolar binary digital to voltage converter (2-quadrant multiplier)

Bipolar conversion. The offset binary response equation for Figure 5 is nominally

$$E_o = -\left[\frac{N_{binary}}{512} - 1\right] V_{REF}$$

Responses to typical codes are tabulated. If the MSB is complemented, the conversion relationship will be recognized as appropriate for a 2's-complement input, but with a negative scale factor. The MSB determines the sign, and the last 9 bits determine the magnitude in 2's complement notation. Since V_{REF} may be either positive or negative, 4-quadrant multiplication is inherent.

In this configuration, I_{OUT_2}, which is the complement of I_{OUT_1}, is inverted and added to I_{OUT_1}, halving the resolution (of each polarity) and doubling the gain. The 10MΩ resistor corrects for a 1/1024 difference (inherent in this technique) between I_{OUT_1} and I_{OUT_2} at zero (10000 00000). A2 is shown as a current inverter, but it might also be a voltage inverter, if the AD505 is used.

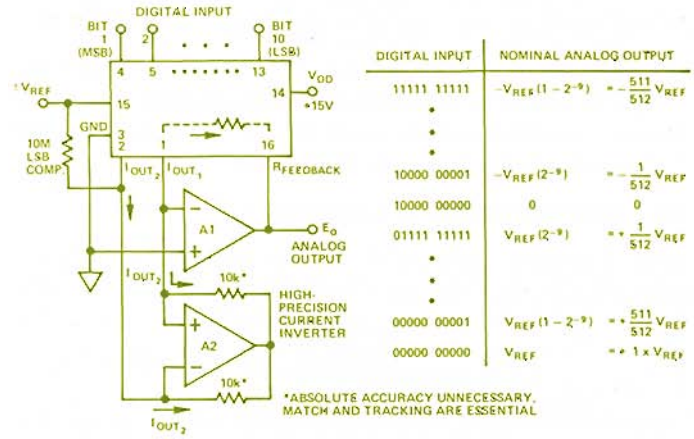


Figure 5. The AD7520 as a bipolar offset-binary digital-to-voltage converter (4-quadrant multiplier)

If sign-magnitude coding is desired, to obtain bipolar conversion with the full 10-bit-plus sign resolution, the output of the *unipolar conversion* circuit may be fed into a sign-magnitude converter, such as Figure 6. An AD7510 quad switch (see page 17) will handle two such circuits.

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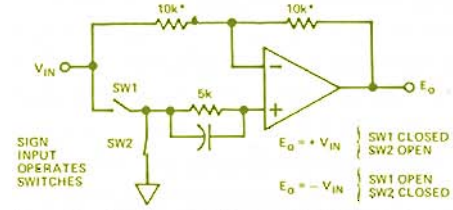

Figure 6. Sign-magnitude to bipolar converter.