LM143 Monolithic High Voltage Operational Amplifier Applications

National Semiconductor
Application Note 127

INTRODUCTION

The LM143 is a general purpose, high voltage operational amplifier featuring ±40V maximum supply voltage operation, output swing to ±37V, ±38V input common-mode range, input overvoltage protection up to ±40V and slew rate greater than 2V/μs*. Offset null capability plus low input bias and offset currents (8 nA and 1 nA respectively) minimize errors in both high and low source impedance applications. Due to isothermal symmetry of the chip layout, gain is constant for loads ≥ 2 kΩ at output levels to ±37V. Because of these features, the LM143 offers advantages not found in other general purpose op amps. The LM143 may, in fact, be used as an improved performance, plug-in replacement for the LM741 in most applications.

This paper describes the operation of the LM143 and presents applications which take advantage of its unique, high voltage capabilities. Obviously, other applications exist where the low input current and high slew rate of the LM143 are useful. (See AN-29 on the LM108.) Application tips are included in the appendix to guide the user toward reliable, trouble-free operation.

CIRCUIT DESCRIPTION

A simplified schematic of the LM143, shown in *Figure 1*, illustrates the basic circuit operation. The super-β input transistors[1], Q1 and Q2, are used as emitter followers to achieve low input bias currents. Although these devices exhibit β = 2000–5000, they inherently have a low collector-base breakdown voltage of about 4V. Therefore, active voltage clamps Q3 and Q4 protect Q1 and Q2 under all input conditions including common-mode and differential overvoltage. Other NPNs in the circuit are representative of those found in standard IC op amps ($\beta \approx 200$, LV_{CEO} = 50–70V).

The input stage differential amplifier Q7 and Q8 with large base width exhibit LV_{CEO} = 90V to 110V and high BV_{EBO} so readily withstand input overvoltages. The total input stage collector current (I_1 = 80 μA) is made higher than in most op amps to improve slew rate. Emitter degeneration resistors, R10 and R11, reduce transconductance[2] to limit small signal bandwidth at 1 MHz for a phase margin of 75°. Q16 and Q17 function as active collector loads for Q7 and Q8 and provide differential to single-ended current conversion with full differential gain.

One of the highest breakdown voltages available in standard planar NPN processing is the collector-base, BV_{CBO} which is typically 90V to 120V. To make use of this high voltage capability in the active region, the second stage consists of a cascode (common emitter-common base pair) connection of Q21 and Q23. The internal voltage bias V_{B1}, shunts avalanche-induced leakage current away from the base of Q21, avoiding β multiplication as found in the LV_{CEO} mode. Q23 and emitter follower Q22 are internally biased at a low voltage so the BV_{CEO} mode is impossible. Frequency compensation is achieved with an internal, high voltage capacitor, C_C.

* An externally compensated version of the LM143, the LM144, offers even higher slew rate in most applications. The LM144 is pin-for-pin compatible with the LM101A.

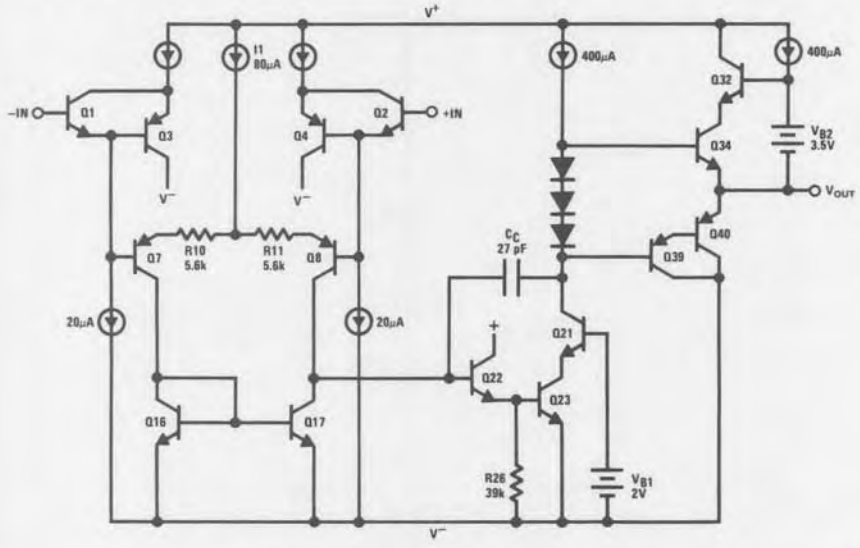

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FIGURE 1. LM143 Simplified Schematic

The second stage drives a complementary class AB output stage. A cascode connection of Q32 and Q34 is again employed for high breakdown voltage. The associated voltage bias, V_{B2}, is internally derived. A Darlington PNP pair, Q39 and Q40 with BV_{CEO} = 100V, provides the active pull-down.

HIGH VOLTAGE APPLICATIONS

The following applications make use of the high voltage capabilities of the LM143. As with most general purpose op amps, the power supplies should be adequately bypassed to ground with 0.1 μF capacitors.

130 Vp-p Drive to a Floating Load

A circuit diagram using two LM143's to drive up to 130V peak-to-peak is given in *Figure 2*.

A non-inverting voltage amplifier, with a gain of $A_V = 1 + (R2/R1)$, is followed by a unity gain inverter. The load is applied across the outputs of A1 and A2. Therefore, $V_{OUT} = V1 - V2 = V1 - (-V1) = 2V1$. If V1 = 65 Vp-p, then 2V1 = 130 Vp-p.

The above circuit was breadboarded and the results are as follows:

i) Maximum output voltage: 138 Vp-p unclipped into 10 kΩ load

ii) Slew rate: 6V/μs

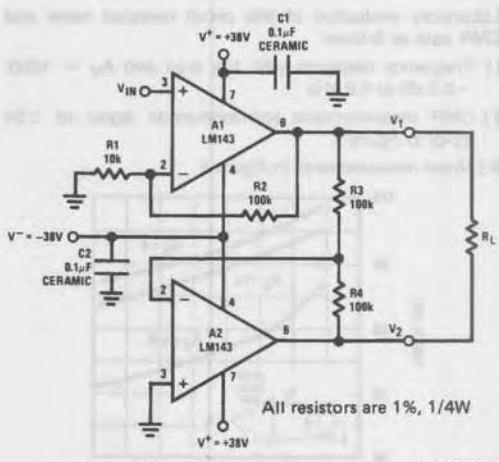

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FIGURE 2. 130V Drive Across a Floating Load

±34V Common-Mode Range Instrumentation Amplifier

An instrumentation amplifier with ±34V common-mode range, high input impedance and a gain of X1000 is shown in *Figure 3*.

For a differential input signal, V_{IN}, A1 and A2 act as non-inverting amplifiers of gain $A_{V1} = 1 + (2R1/R2)$, where R1 = R3. However, the gain is unity for common-mode signals since voltages V1 and V2 are in phase, and no current flow is developed through R1, R2 and R3. The second stage is simply an op amp connected as a simple differential amplifier of gain, $A_{V2} = (R5/R4)$, where R5 = R7 and R4 = R6. The total gain of the instrumentation amplifier is

$$A_V = \left(1 + \frac{2\,R1}{R2}\right)\left(\frac{R5}{R4}\right) = \left(1 + \frac{2 \times 100k}{22.22k}\right)\left(\frac{1.0M}{10k}\right)$$

$$= 1000$$

R7 may be adjusted to take up the resistance tolerances of R4, R5 and R6 for best common-mode rejection (CMR). Also, R2 may be made adjustable to vary the gain of the instrumentation amplifier without degrading the CMR.

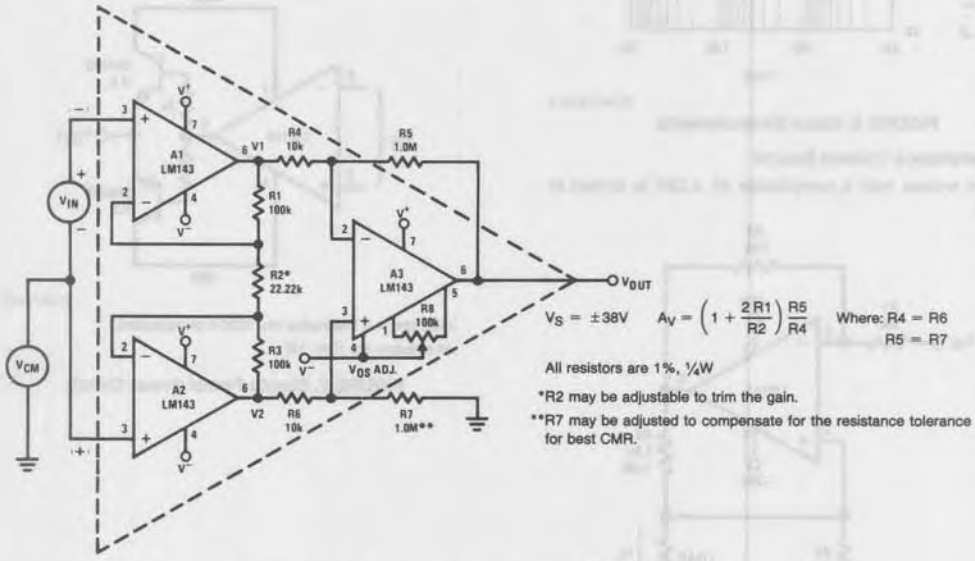

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FIGURE 3. Wide Common-Mode Range Instrumentation Amplifier

Laboratory evaluation of this circuit revealed noise and CMR data as follows:

i) Frequency response with 10k load and A_V = 1000: −3.0 dB at 8.9 kHz

ii) CMR measurements (common-mode signal of ±34 Vp-p) in *Figure 4*

iii) Noise measurements in *Figure 5*

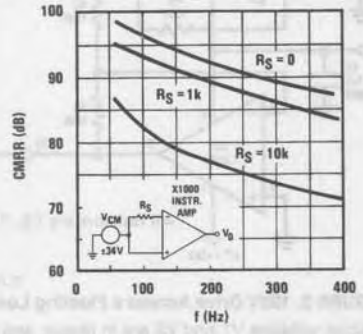

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FIGURE 4. Common-Mode Rejection Measurements

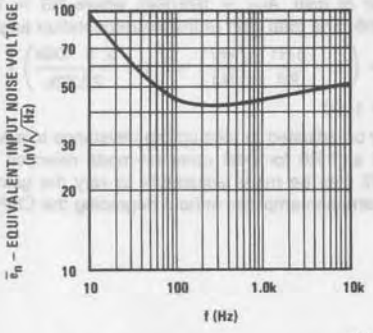

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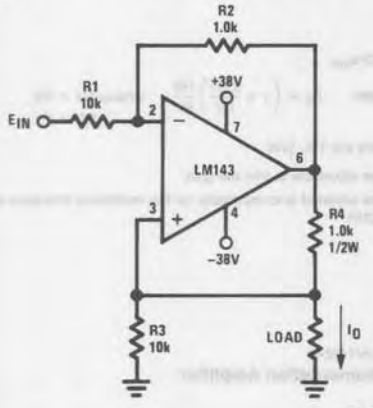
FIGURE 5. Noise Measurements

High Compliance Current Source

A current source with a compliance of ±28V is shown in *Figure 6*.



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All resistors 1% metal film, ¼W unless otherwise specified.

FIGURE 6. High-Compliance Current Source

The non-inverting input of the op amp senses the current through R4 to establish an output current, I_O proportional to the input voltage. The expression for I_O is

$$I_O = -\frac{E_{IN}\,R2}{R1\,R4} = -\frac{0.1\text{ mA}}{V}E_{IN}.$$

R3 keeps the circuit stable under any value of load resistance. Measured circuit performance is as follows:

I_{OMAX} = ±3.5 mA at E_{IN} = ±35V

R_{OUT} = 2 MΩ at I_{OUT} = ±2.0 mA

CURRENT BOOSTED APPLICATIONS

Because of the high voltage capability of the LM143, some thought must be given for the selection of the minimum load resistance. At an ambient temperature of 25°C, the LM143 can dissipate 680 mW. Worst case dissipation arises when the load resistance R_L is connected to one supply and V_O = 0. Then the amplifier sources I_O = (38V/R_L) with 38V internal voltage drop. During this condition,

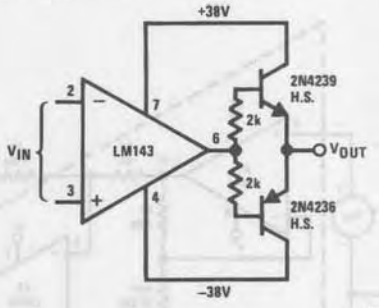
$$P_{MAX} = 680\text{ mW} = \frac{E_L{}^2}{R_L} = \frac{(38V)^2}{R_L}$$

$$\text{or } R_L = \frac{1444V^2}{680\text{ mW}} \approx 2.1\text{ k}\Omega$$

Hence, load resistances less than 2k will cause excessive power dissipation.

Simple Power Boost Circuit

For loads less than 2 kΩ, a power boost circuit should be added. The simple booster shown in *Figure 7* has the advantage of minimal parts count, but crossover distortion is noticeable and there is no short circuit protection; hence, either the LM143 or the boost transistors may fail under short circuit conditions.



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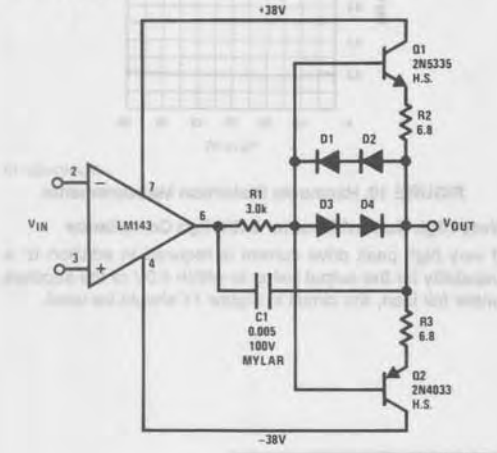
Heat sink is a Thermalloy No. 2230-5 or equivalent.

All resistors are 10%, 1W.

FIGURE 7. Simple Power Boost Circuit

100 mA Current Boost Circuit

With the addition of 4 diodes, a resistor and a capacitor, the booster circuit can be short circuit protected at 100 mA as shown in *Figure 8*.



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Heat sink is a Thermalloy No. 2230-5 or equivalent.

All diodes are 1N914.

All resistors are ½W, 10%.

FIGURE 8. 100 mA Current Boost Circuit

R1 protects the LM143 by limiting the maximum drive current to (38V/3.0k) ≅ 12.5 mA, thereby keeping safely within the device dissipation limit of 680 mW. D1—D4 in conjuction with R2 and R3 protect the output transistors Q1 and Q2 by shunting the output drive current if the voltage drop across R2 or R3 exceeds 0.7V.

Breadboard Data:

i) Frequency Response: Limited by LM143 frequency response and slew rate.

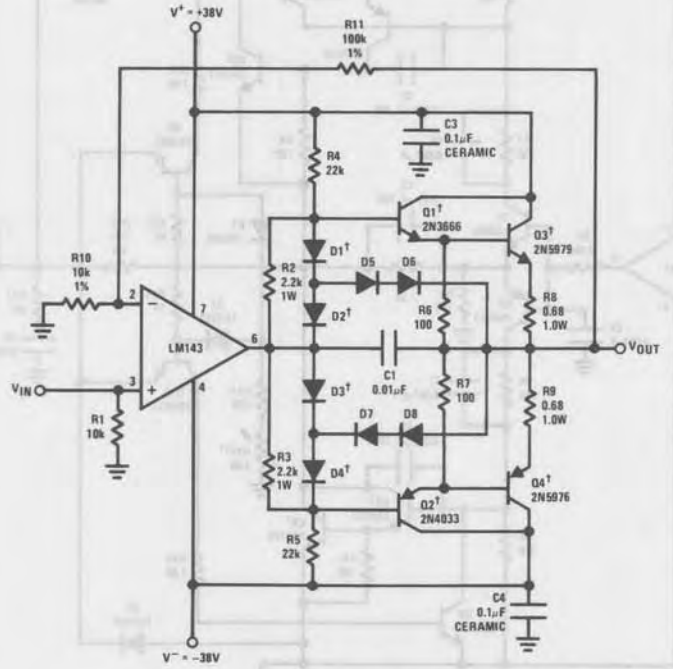
ii) Step response for unity gain, voltage follower configuration: Less than 10% overshoot for 1.0V step with 0.01 μF capacitive load, 50% overshoot with 0.47 μF capacitive load. The circuit is unconditionally stable for capacitive loads.

iii) Output Voltage: ±33 Vp-p into 400Ω load

1.0 Amp Class AB Current Booster

If crossover distortion is objectionable and currents of up to 1.0A are needed, the circuit in *Figure 9* should be used.

The output of the LM143 drives a class AB complementary output stage. The quiescent current for the output stage is set by the current flow through R4, R5 and diodes D1–D4. The diodes D1–D4 are on a common heat sink with the output transistors Q3 and Q4 so that the voltage drops across the diodes and base-emitter junctions of the output



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†Put on common heat sink, Thermalloy 6006B or equivalent.

All diodes are 1N3193.

All resistors are 10%, ¼W except as noted.

FIGURE 9. 1 Amp Class AB Current Booster with Short Circuit Protection

transistors will track with temperature. Normally, R4 and R5 supply the current drive for the output Darlingtons, Q1, Q3 and Q2, Q4, but if additional drive is needed, the LM143 supplies the remainder through R2 and R3. For short circuited load, the drive current is bypassed around the output transistors through D1, D5 and D6 during the positive half cycle and through D4, D7 and D8 during the negative half cycle. Drive current bypassing, or output current limiting, occurs whenever R8 or R9 sees more than one diode drop (≅ 0.7V). An expression for the maximum output current is

$$I_{MAX} \cong \frac{0.7V}{0.68\Omega}$$

$$I_{MAX} \cong 1.0A.$$

Capacitor C1 stabilizes the circuit under most feedback and load conditions and C3 and C4 bypass the power supply. Measured performance is as follows:

i) Maximum output voltage with $R_L = 40\Omega$: +29.6V, −28V with $V_S = \pm 38\ V_{DC}$.

ii) Harmonic distortion measurements of *Figure 10* were measured with a closed loop gain of 10.

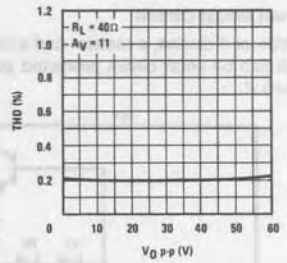

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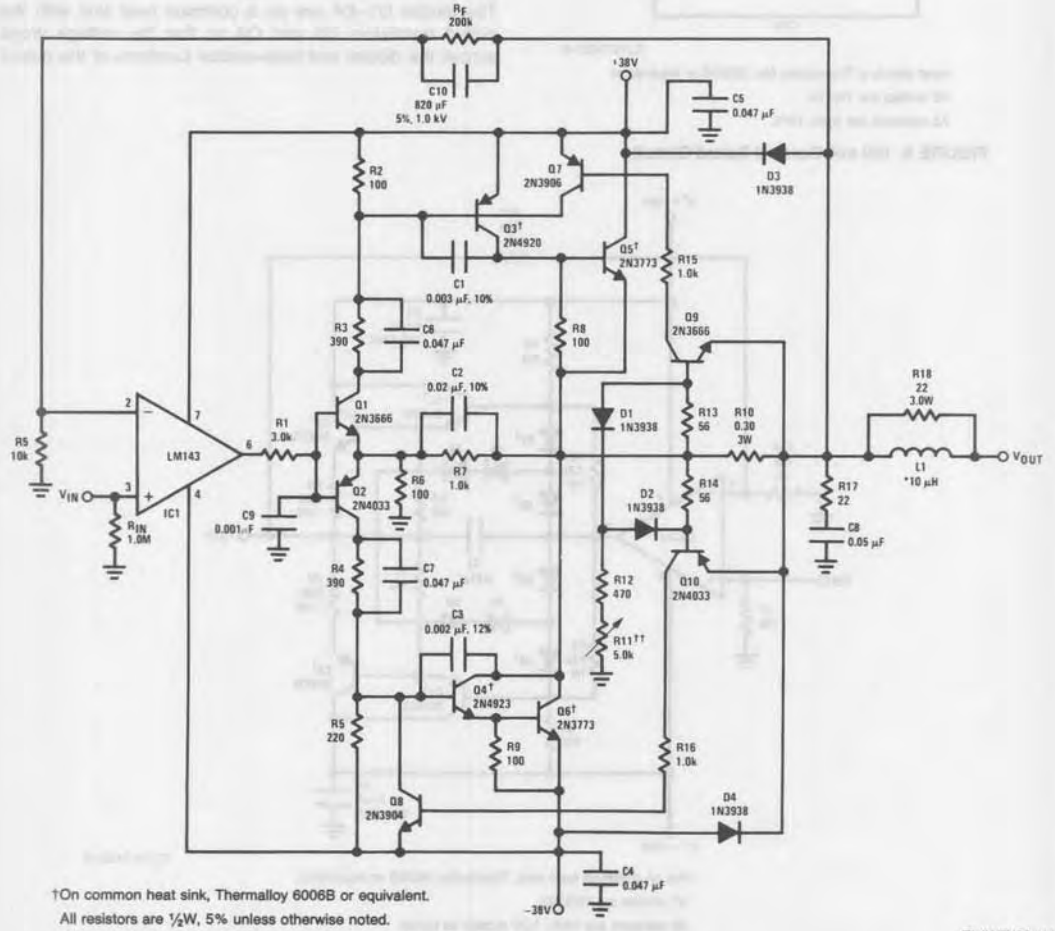
FIGURE 10. Harmonic Distortion Measurements

Very High Current Booster with High Compliance

If very high peak drive current is required in addition to a capability for the output swing to within 4.0V of the supplies under full load, the circuit in *Figure 11* should be used.



†On common heat sink, Thermalloy 6006B or equivalent.

All resistors are ½W, 5% unless otherwise noted.

All capacitors are 20%, 100V, ceramic disc unless otherwise noted.

††Output current limit adjust.

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FIGURE 11. Very High Current Booster with High Compliance

Excluding the LM143, the current booster has three stages. The first stage is made up of Q1 and Q2 which level shifts and boosts the current output of the LM143 to about 100 mA. Q3 and Q4 further boost the output of Q1 and Q2 to about 1.0A. Q5 and Q6 then have adequate drive to source and sink at least 10A. There is no quiescent current path when the output voltage is zero since Q1 and Q2 are biased off.

The short circuit protection circuit is made up of Q7 and Q9 on the positive side and Q8 and Q10 on the negative side. Q9 or Q10 turns on as soon as $V_{BE} \cong 0.7V$ appears across R10 when the output terminal is shorted to ground. Then Q7 or Q8 bypass the drive to the output devices, Q5 and Q6. Since R10 is 0.3Ω, current limiting under short circuited output occurs at 2.3A and is relatively independent of the current limit adjustment resistor, R11. An expression for the maximum output current, $I_{OUT\ MAX}$, with V_{OUT} and R11 as variables is

$$|I_{OUTMAX}| \cong \frac{(|V_{OUT}| - V_{D1})\,R13}{R11 + R12 + R13} + V_{BE9}$$

$$\cong \frac{(|V_{OUT}| - 0.7)\,56\Omega}{R11 + 526\Omega} + 0.7V$$

The equation is valid for both output polarities. The plot in *Figure 12* superimposes the above equation on the maximum operating area curve for the 2N3773 and illustrates the safe area protection feature.

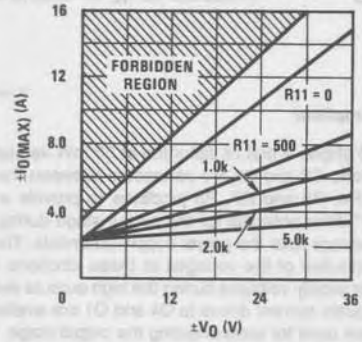

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FIGURE 12. Maximum Output Current as a Function of R11 and V_{OUT}

The diodes, D1 and D2, are in the circuit to keep the base-emitter junctions of Q9 and Q10 from being reversed biased during the opposite polarity output voltage swings. C1, C2, C3, C6, C7 and C9 are judiciously inserted in the circuit to prevent oscillation. R17, R18, C8 and L1 are used in the circuit to maintain stability under all load conditions. Diodes D3 and D4 provide protection for inductive loads.

All measurements taken with a 4Ω load and ±38V supplies unless otherwise stated:

i) Maximum power out: 144 Wrms

ii) Frequency response:
   a) −3.0 dB at 10 kHz at full power
   b) −3.0 dB at 11.5 kHz at 10 Vp-p out

iii) Maximum output voltage: ±34V

iv) Maximum capacitive load: 10 μF with 10% overshoot for a small signal step response

v) DC deadband: 20 μV

vi) Quiescent current: 12.7 mA (positive supply), 2.1 mA (negative supply)

vii) Input impedance: 1 MΩ

viii) Voltage gain: 21

HIGH POWER APPLICATIONS

90 Wrms Audio Power Amplifier

A circuit diagram of an audio power amplifier which is capable of 90 Wrms into a 4Ω speaker or 70 Wrms into an 8Ω speaker is given in *Figure 13*. The circuit features safe area, short circuit and overload protection, harmonic distortion less than 0.1% at 1.0 kHz, and an all NPN output stage.

The output of the LM143 drives a quasi-complementary output stage made up of Q1, Q2, Q3 and Q4. This quasi-complementary circuit, which makes possible an all NPN output, was chosen over the complementary output circuit due to the lack of low cost high voltage power PNP transistors.

Safe area current limiting occurs whenever the output current is

$$|I_{OUTMAX}| = \frac{(|V_{OUT}| - V_{D3})\,R11}{R11 + R13} + V_{BE5}$$

where R11 = R15 = 330Ω,

R13 = R14 = 3.9k,

R12 = R16 = 0.25Ω and

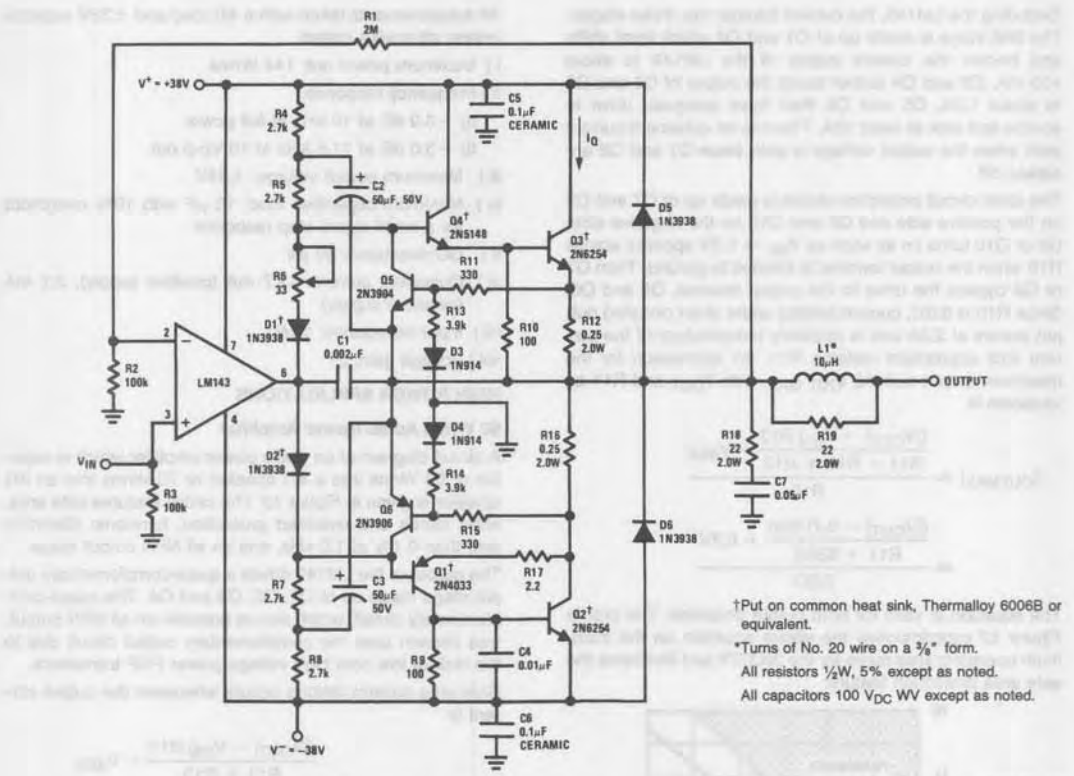
$V_{BE5} \cong V_{BE6} \cong V_{D3} \cong V_{D4} \cong 0.7V$.

If the output is shorted, the above equation simplifies to

$$I_{OUTMAX} = \frac{V_{BE5}}{R12} \cong \frac{0.7V}{0.25\Omega} = 2.8A$$

If the output voltage is 30V,

$$I_{OUTMAX} = \frac{\frac{(30V - 0.7V)\,330}{4.23k} + 0.7V}{0.25\Omega} \cong \frac{2.3 + 0.7V}{0.25} = 12A$$



†Put on common heat sink, Thermalloy 6006B or equivalent.

*Turns of No. 20 wire on a ⅜" form.

All resistors ½W, 5% except as noted.

All capacitors 100 V_{DC} WV except as noted.

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FIGURE 13. 90W Audio Power Amplifier

The maximum output current, $I_{O(MAX)}$, versus V_O is plotted in *Figure 14*. D4 and D3 are in the circuit to keep Q5 off during the negative half of the output voltage cycle and Q6 off during the positive half cycle.

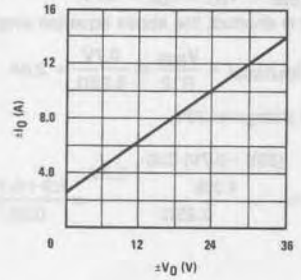

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FIGURE 14. Output Current Limiting as a Function of Output Voltage

The output stage is biased into class AB operation by using the resistor string R4, R5, R7 and R8 to set the voltage drops across R6, D1 and D2, which then determine the quiescent current through the output transistors. These diodes are thermally coupled to the output devices to track their base-emitter junction voltages with temperature. Low distortion at low power levels is achieved by adjusting R6 to set the quiescent current through Q3 and Q2 to about 100 mA.

Figure 15 shows a plot of distortion at 50 mW versus quiescent current. C2 and C3 are connected between the output and the R4, R5 and R7, R8 junctions to provide a "bootstrapped" drive potential for the output stage during output voltage swings near the power supply potentials. The absolute magnitudes of the voltages at these junctions exceed the power supply voltages during the high outputs swings so that adequate current drives to Q4 and Q1 are available. C1 and C4 are used for compensating the output stage. C5 and C6 are used for power supply bypassing. R18, C7, R19 and L1 are included in the circuit to keep the amplifier stable under all load conditions. D5 and D6 provide protection for inductive loads.

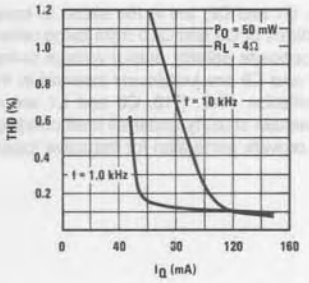

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FIGURE 15. Quiescent Current vs Distortion

The input impedance of the audio amplifier is simply the value of R3. To keep the output offset voltages to a minimum, R3 ≅ R1 ‖ R2. The voltage gain is

$$A_V = 1 + \frac{R1}{R2} = 1 + \frac{2.0M}{100k} = 21$$

The following data was taken with $V_S = \pm 38V$:

i) Maximum power output before visible clipping:
   a) 90 Wrms at 1.0 kHz into 4Ω load
   b) 70 Wrms at 1.0 kHz into 8Ω load

ii) Distortion measurement: distortion versus frequency and power is plotted in *Figures 16* and *17*.

iii) Maximum capacitive load: 20 μF

iv) Output noise, 10 Hz to 20 kHz: 100 μVrms

v) Frequency response:
   a) Small signal (1.0 Vrms into 4.0Ω): −3.0 dB at 40 kHz
   b) Power (90W into 4Ω): −3.0 dB at 29 kHz
   c) Power (70W into 8Ω): −3.0 dB at 30 kHz

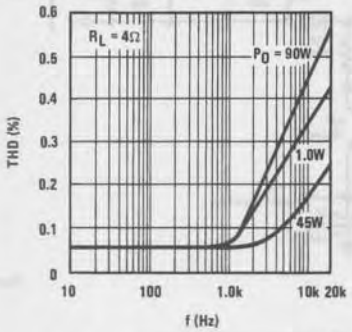

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FIGURE 16. Distortion vs Frequency, $R_L = 4\Omega$

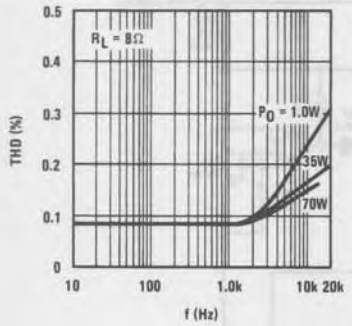

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FIGURE 17. Distortion vs Frequency, $R_L = 8\Omega$

POWER SUPPLY CIRCUITS

The ability of the LM143 to withstand up to 80V can be exploited fully in the design of regulated power supplies. The circuits to be described use a zener reference voltage, an IC voltage amplifier, and a discrete power transistor pass element. If care is taken to keep the voltage drop across the pass element within 40V, standard three terminal voltage regulators such as the LM340, LM120, etc. may be used as pass elements and significantly decrease parts count and circuit complexity. Circuits using this approach are given in the LM340 application note (see AN-103).

A Tracking ±65V Supply with 500 mA Output

A tracking power supply circuit can be made by modifying the circuit for the 130 Vp-p driver circuit. The modified circuit is given in *Figure 18*.

A 2N4275 is used as a stable zener voltage reference of about 6.5V. Its output is amplified from one to about 10 times by the circuitry associated with IC1. The output of IC1 is applied through R10 to the Darlington connected transistors, Q2 and Q3. The feedback resistor, R5, one end of which is connected to the V^+ output node, is made variable so that the V^+ output voltage will vary from 6.5V to about +65V. The V^+ output is applied to a unity gain inverting power amplifier to generate the V^- output voltage. The output circuit of the unity gain inverter uses a composite PNP, Q4 and Q5, to provide the current boost.

Since the input terminals of A2 are at ground potential, the positive supply lead cannot be grounded; instead, it is connected to the output of a 4.7V zener diode, D8, to keep within the input common-mode range.

C1, C3 and C4 are used for decreasing the power supply noise. C2 is used in bypassing most of the noise generated by the reference voltage and C5 and C6 are used to reduce the voltage output noise. Short circuit protection is provided by D1, D2, D3, R10 and R14 on the positive side and by D4, D5, R11 and R15 on the negative side. The short circuit protection circuit is the same as the one used in the 1.0A current booster circuit.

The short circuit current is given by

$$I_{MAX} \cong \frac{V_{BE}}{R14} \cong \frac{V_{BE}}{R15}$$

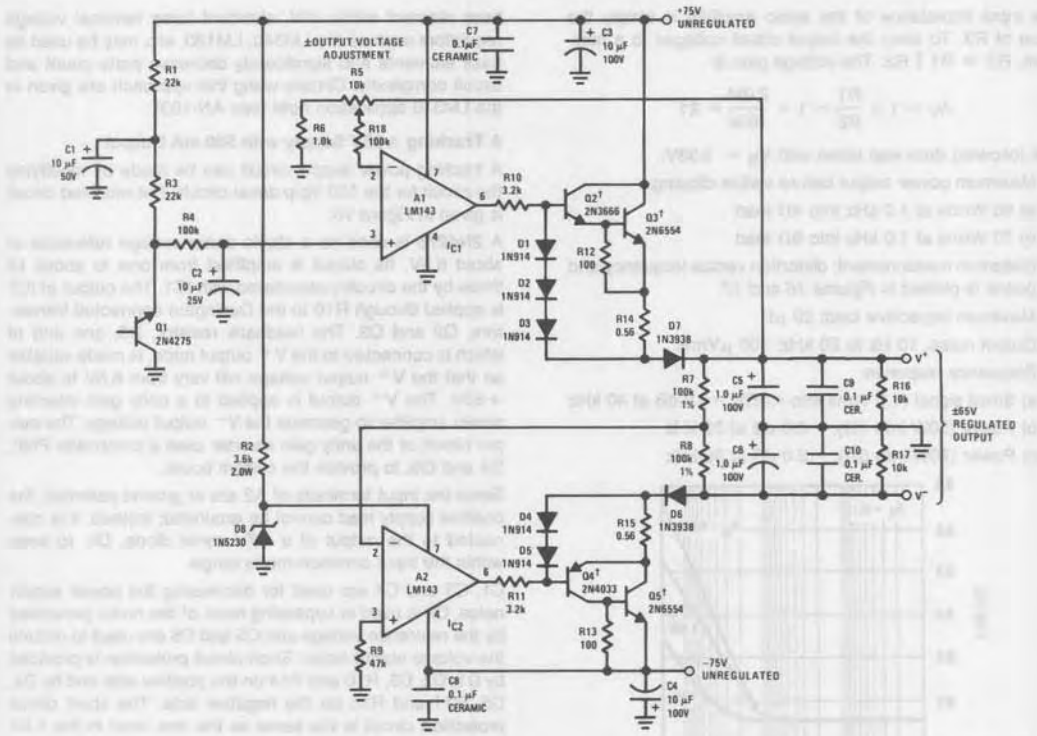
$$\cong \frac{0.7}{0.56} = 1.25A$$

where V_{BE} = voltage drop across a diode.

±65V, 1.0A Power Supply with Continuously Variable Output Current and Voltage

If a continuously variable output current as well as output voltage supply is needed, a power supply circuit given in *Figure 19* will do the job. It has an output range from 7.1V to 65V with an adjustable output current range of 0 to 1.0A.

Basically, the power supply circuit is a non-ideal voltage source in series with a non-ideal current source. A reference voltage of approximately 6.5V is obtained by zenering the base-emitter junction of the 2N4275. The positive temperature coefficient of the zenering voltage is compensated by the negative temperature coefficient of the forward biased base-collector junction. The output of the voltage reference goes to the variable gain power amplifier made up of IC2, Q6, Q7 and their associated components and to a reference current source made up of Q2, D1 and components around them. The variable gain power amplifier multiplies the reference voltage from one to ten times due to the variable feedback resistor, R17. since the maximum current output of IC2 is at most 20 mA, the Darlington connected Q6 and Q7 are used to boost the available output current to 500 mA.



†Put on common heat sink, Thermalloy 6006B or equivalent.
All resistors are ½W, 5%, except as noted.

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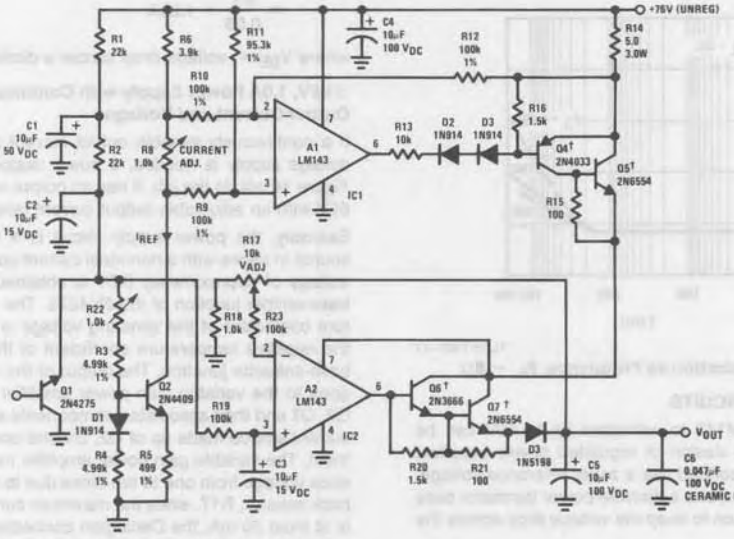
FIGURE 18. Tracking 65V, 1A Power Supply with Short Circuit Protection



†Put on common heat sink, Thermalloy 6006B or equivalent.
All resistors ½W, 10% unless otherwise noted.
All capacitors 20%.

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FIGURE 19. 1A, 65V Power Supply with Variable Current Limit

Breadboard Data for the Tracking 65V Power Supply

$V_{IN} = \pm 75V$, $I_{OUT} = \pm 500$ mA, $T_j = 25°C$, $T_A = 25°C$, $V_{OUT} = \pm 40V$, unless otherwise specified.

Parameter	Conditions	Measured Data	
		$+V_{OUT}$	$-V_{OUT}$
Load Regulation	$0 \le I_{OUT} \le 500$ mA	0.5 mV	1.0 mV
Line Regulation	$\lvert\pm 50V\rvert \le V_{IN} \le \lvert\pm 80V\rvert$ $I_{OUT} = \pm 100$ mA $I_{OUT} = \pm 500$ mA	 175 mV 169 mV	 176 mV 173 mV
Quiescent Current	$I_{OUT} = 0$	Pos. Supply 28.22 mA	Neg. Supply 6.55 mA
Output Noise Voltage*	10 Hz ≤ f ≤ 100 kHz	0.125 mV	0.135 mV
Ripple Rejection	$I_{OUT} = \pm 20$ mA, f = 120 Hz	−72.5 dB	−63.4 dB
Output Voltage Drift*		3.38 mV/°C	3.43 mV/°C

*The output noise and drift are due primarily to the zener reference.

Measured Performance of the 1A, 65V Power Supply

$V_{IN} = +76V$, $I_{OUT} = 500$ mA, $T_j = 25°C$, $V_{OUT} = +40V$ unless otherwise specified

Parameter	Conditions	Measured Data
Load Regulation	$0 \le I_{OUT} \le 500$ mA (Pulsed Load)	5.0 mV
Line Regulation	$46V \le V_{IN} \le 76V$ $I_{OUT} = 100$ mA $I_{OUT} = 500$ mA (dc Loads)	 297 mV 286 mV
Maximum Output Voltage	dc Load	68.6V
Quiescent Current		21.4 mA
Output Noise Voltage*	10 Hz ≤ f ≤ 100 kHz	0.280 mV
Ripple Rejection	$I_{OUT} = 20$ mA f = 120 Hz $\Delta V_S = 3.0$ Vp-p $\Delta V_O = 6.0$ mVp-p	66.6 dB
Loads are Pulsed Loads	200 μs Pulse Every 200 ms	

*The output noise is due primarily to zener reference

The power current source is an op amp used as a differential amplifier which senses the voltage drop across R8 and maintains this same voltage across R14. Hence, the maximum output current is

$$I_{OUT} = \frac{R8}{R14} \times I_{REF} \le \frac{1.0k}{5.0\Omega} \times 5.0\text{ mA} = 1.0A.$$

Since the output load under most conditions will not demand what the power current source can deliver, Q4 and Q5 will remain in saturation during normal operation. When Q4 and Q5 are pulled out of saturation, the output load voltage will drop until the load current just equals what is available from the power current source. Because the positive supply terminal of IC2 is tied to the collectors of Q4 and Q5, IC2 will supply just enough current drive to Q6 and Q7 to keep itself on. Hence, a current limiting resistor is unnecessary for IC2. A 10k current limiting resistor, R13, is present since the total unregulated power supply voltage is available for IC1. R6 is used to stay within the input common-mode voltage range of IC1.

I_{REF} is derived from the 6.5V reference source, Q1, by using Q2 in a current source configuration. R22 is made adjustable so that I_{REF} can be set for 5.0 mA.

CONCLUSION

The LM143 is a high performance operational amplifier suited for applications requiring supply voltages up to ±40V. The LM143 is especially useful in power supply circuits where the unregulated voltages are as high as ±40V and in amplifier circuits where output voltages greater than ±30V peak are needed. The LM143 is internally compensated and is pin-for-pin compatible with the LM741. Compared with the LM741, the LM143 exhibits an order of magnitude lower input bias currents, better than five times the slew rate and twice the output voltage swing.

APPENDIX

Toward the goal of trouble-free applications, this appendix details some of the more subtle features of the LM143 and reviews application hints pertinent both to op amps in general and the LM143 in particular. The complete schematic of the LM143 is shown in *Figure 20*.

The circuit starts drawing supply current, at supply voltages of ±4V, when current is provided to a 7.5V zener diode D5 by the collector FET Q41. The gate-channel junction of Q41 exhibits 100V breakdown as source and drain are lightly doped NPN collector and substrate material. The collector current of Q18 biases current sources Q25 through Q30 and sets the supply current at nearly zero TC.

Q19 furnishes a bias voltage, 5V above the negative supply, for the collectors of Q15, Q20 and Q22. The low impedance 2V reference (V_{B1} in *Figure 1*) for the base of Q21 appears at the emitter of Q20 and has the correct TC to insure that Q23 never saturates. Should this occur, the low resistance of Q23 would cause premature LV_{CEO} breakdown of Q21.

The input transistors, Q1 and Q2, are biased by Q13 and Q14 which have a breakdown voltage essentially equal to BV_{CBO} by virtue of the high emitter impedance, R18 and R19, relative to the low dynamic impedance of D4. In a similar way, Q18 and Q19 stand off essentially the full supply voltage. These devices have a high output impedance caused by series feedback and so hold the supply current nearly constant to prevent excessive power dissipation at high supply voltages.

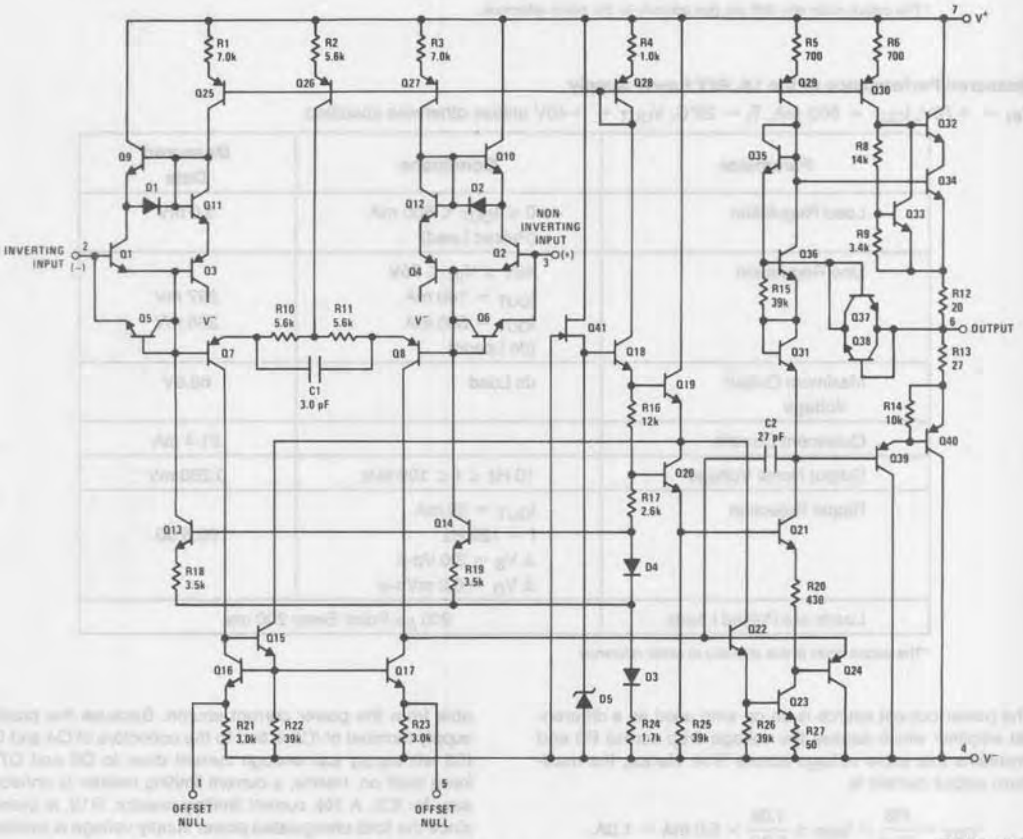

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FIGURE 20. Complete Schematic of the LM143

While the simple voltage clamping scheme, Q3 and Q4 in *Figure 1*, is adequate, it is prone to oscillation when built with high β PNPs. The more elaborate scheme of *Figure 20* prevents instability. This clamping method is similar to that used in the LM108, but allows large differential inputs to exist with complete input overvoltage protection. Q9 and Q10, which withstand the high input common-mode voltage, have a BV_{CBO}-type breakdown due to the low impedance diodes seen from the base leads and the high impedance of Q1 and Q2 (enhanced by 100% series feedback) in the emitter leads. Input overvoltage protection also holds up under high-level transient input voltages.

With a large negative-going step input, as could occur in the unity-gain voltage follower configuration, diode-connected Q6 turns "ON", protecting the emitter-base junction of Q2 from zener breakdown and subsequent long-term β degradation. At the same time, stray capacitance at the collector of Q2 is discharged by D2 through Q4 and Q12. This holds Q10 in a true BV_{CBO} mode (emitter open-circuited) and clamps the voltage across Q2 to 3 V_{BE}.

With a large positive-going step input, stray capacitance at the collectors of Q2 and Q12 is charged by the forward-biased collector junction of Q2. As before, with D2 conducting, Q10 is again in the BV_{CBO} breakdown mode. Since the inverting input can be subject to the same transients, Q1 is afforded the same protection.

Distributed capacitance associated with R10 and R11, together with the collector-base capacitance of Q26, cause a high frequency transmission pole (the "tail" pole[2]) which can degrade phase margin. This is avoided by adding a small lead capacitor, C1, which provides an alternative low-impedance signal path, thus bypassing the tail pole.

The offset null resistors, R21 and R23, are made larger than that strictly necessary to null the offset voltage. This reduces the transconductance of Q17 and, therefore, the noise gain of the active loads into R10 and R11. By this simple expedient, broadband input noise voltage is substantially reduced.

The voltage reference for the output stage (V_{B2} in *Figure 1*) is realized by actively simulating a 4-diode stack. The voltage across Q33, given by (1 + R8/R9) V_{BE}, is about 3.5V. Biased at 400 μA from Q30, the circuit presents a low impedance, less than 50Ω, to the base of Q32. Since the TC of the reference is negative, Q34 is designed to always remain out of saturation under worst-case conditions of high temperature and high output current. This avoids potential destructive breakdown of Q32.

Current limiting for Q32 and Q34 is provided by diode-connected Q37 and resistor R12. When the voltage drop across R12 turns on Q37, it removes base drive from Q34. In a similar fashion, current limiting in the negative direction is initiated when the voltage drop across R13 causes Q38 to conduct. This current is limited in Q21 by R20 to about 1 mA. When this occurs, base drive is removed from Q39.

Although output short circuits to ground or either supply can be sustained indefinitely at supply voltages lower than $\pm$22V, short circuits should be of limited duration when operating at higher supply voltages. Units can be destroyed by any combination of high ambient temperature, high supply voltages, and high power dissipation which results in excessive die temperature. This is also true when driving low impedance or reactive loads or loads that can revert to low impedance; for example, the LM143 can drive most general purpose op amps outside of their maximum input voltage range, causing heavy current to flow and possibly destroying both devices.

Precautions should be taken to insure that the power supplies never become reversed in polarity—even under transient conditions. With reverse voltage, the IC will conduct excessive current, fusing the internal aluminum interconnects. As with all IC op amps, voltage reversal between the power supplies will almost always result in a destroyed unit.

Finally, caution should be exercised in high voltage applications as electrical shock hazards are present. Since the negative supply is connected to the case, users may inadvertently contact voltages equal to those across the power supplies.

REFERENCES

1. R. J. Widlar, "Super Gain Transistors for ICs", National Semiconductor TP-11, March 1969.
2. J. E. Solomon, "The Monolithic Op Amp: A Tutorial Study", IEEE Journal of Solid-State Circuits, Vol. SC-9, No. 6, December 1974.