Two-amplifier integrator extends timing performance

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A simple integrator normally consists of a single operational amplifier and an RC network for setting up the desired time constant. Although uncomplicated, this approach can be troublesome if either a very small or a very large time constant is needed.

The integrator in the figure, however, makes it easy to obtain either short or long timing periods because the values of the timing components are scaled by a straight resistance ratio. The integrator's output voltage is given by:

$$V_{out} = -\frac{R_1}{RCR_2}\int V_{in}\,dt$$

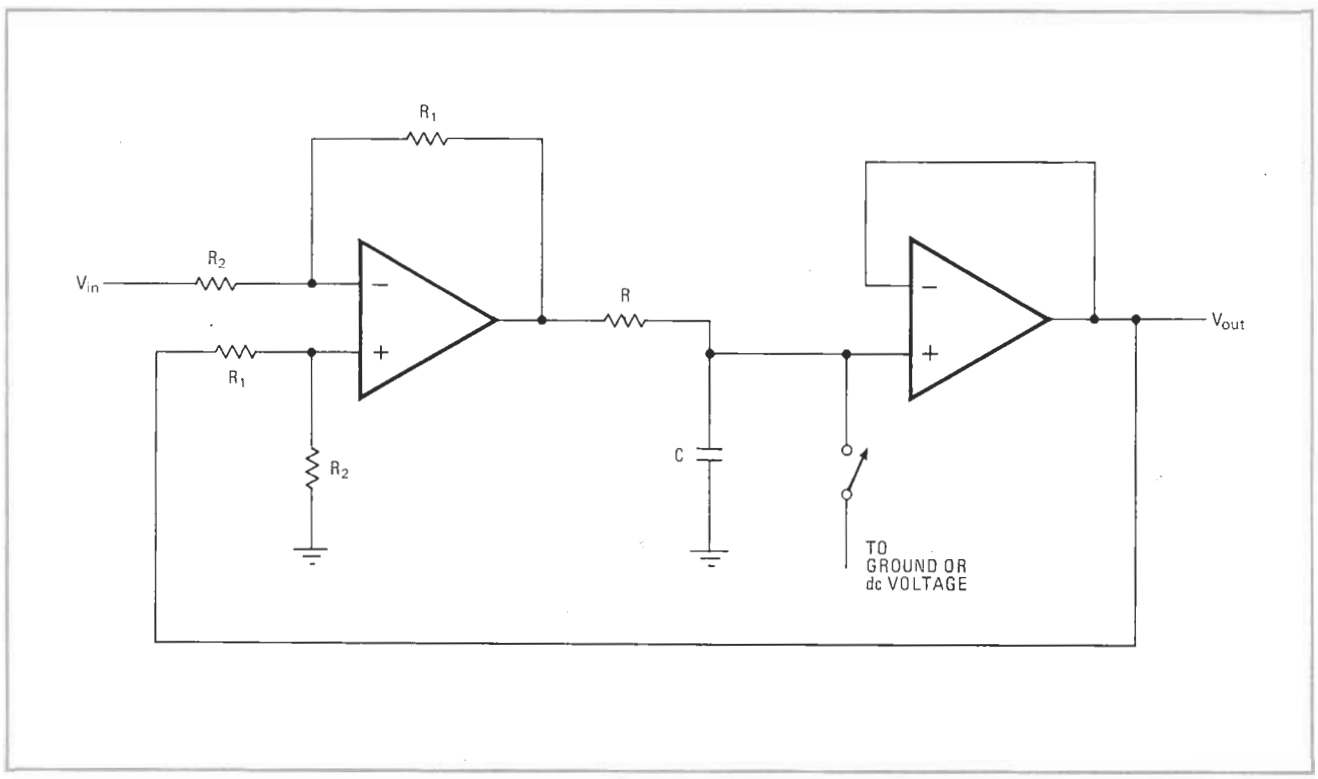
and its time constant becomes $(R_2/R_1)RC$. The circuit provides very good linearity when precision resistors having a tolerance of ±0.1% are used for resistors R_1 and R_2.

Although a second op amp is needed to build the integrator, the circuit offers some additional advantages. For example, it permits initial conditions to be established easily. One of the capacitor's leads goes to ground, and if one end of the switch is connected either to ground or to some dc voltage, the capacitor's initial condition can be set up as either zero or otherwise by simply closing the switch.

Furthermore, when the switch is activated, the integrator's output is not shorted, and the circuit's output op amp operates as a voltage-follower. In a conventional integrator, the initial-condition switch is generally placed across the capacitor, which is in the op amp's feedback loop. With the switch closed, then, the output of a conventional integrator is shorted to the op amp's inverting input.

The integration period of the two-amplifier circuit described here can be as short as 1 nanosecond or as long as 1,000 seconds. The bandwidth of the integrator depends on which op amps are used. For high-frequency operation, National's type LM318 op amp and RCA's type CA3100 op amp are recommended. □

Broad timing range. An extra op amp permits this integrator's time constant to be scaled by resistors R_1 and R_2 so that an exceptionally short or long timing period can be obtained easily. The time constant is $(R_2/R_1)RC$, rather than the usual RC alone. The desired initial condition for the capacitor is established by simply closing the switch, which can go to ground (for zero initial charge) or to some dc voltage.



Inverting transistor boosts integrator's time constant

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Designers of low-frequency analog instrumentation will welcome an integrator that can provide a large time constant with a low-value capacitor. The accompanying circuit does just that. Its integration time constant is the RC product multiplied by the current gain of a superbeta Darlington transistor. Moreover, this circuit has high input impedance, which is an absolute necessity in such applications as an integrator driven by a peak detector. And it offers a third characteristic that is desirable for any integrator—its transient response is critically damped, which prevents integration from being seriously disturbed by noise or transients.

The key feature of this integrator is the inclusion of an inverting transistor in the feedback loop to the input of an operational amplifier. Because the transistor provides inversion, the incoming signal can be applied to the high-impedance noninverting-input terminal of the operational amplifier. The process of inversion, i.e., degenerative feedback through the integrating capacitor, provides critical damping. The value of the capacitor is effectively multiplied by the current-gain factor of the transistor.

The circuit diagram shows that the 741 op amp is connected as an amplifier, with the incoming signal applied through 10-kilohm resistor R to the high-impedance noninverting terminal. To prevent high-frequency oscillations and to limit low-frequency noise, part of the output from the 741 is fed back to the inverting input through a parallel resistor-capacitor combination. The op amp drives a 2N4974 pnp superbeta Darlington transistor. The transistor is biased by the voltage drops across the two zener diodes and across the emitter-to-base junction, which produce a dc base drive of 2 microamperes through the 50-kilohm resistor. The 4.7-kilohm resistor is not critical—it merely limits the current through the 1N573A zener to about 1 milliampere.

Current gain in the transistor, β, is 5,000, so the dc collector current is 10 milliamperes. This current, flowing through the 1-kilohm resistor, centers the voltage level for integrating capacitor C at -7 volts so that the integrator can handle both positive and negative inputs.

When signal e_i is applied at the input to this circuit through resistor R, the output signal of reverse polarity, e_o, is fed back through integrating capacitor C to the noninverting terminal of the op amp. The over-all transfer function of the circuit is

$$A(s) = e_o(s)/e_i(s) = -1/R\beta Cs$$

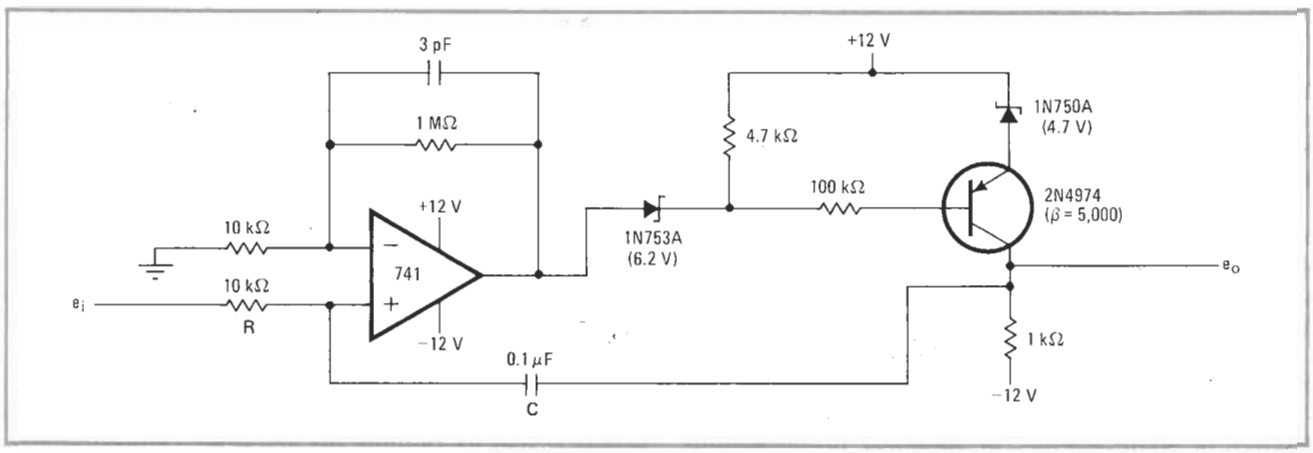
A conventional op-amp integrator using the same R and C would have a transfer function of $-1/RCs$. Thus, to provide the same transfer function, the integrator that includes a transistor can use a capacitor that is smaller by the factor β. Or, if the capacitor value is held fixed, the transistor provides an integrating time constant that is larger by the factor β.

The circuit shown here has an effective time constant

$$\tau = \beta RC$$
$$= 5{,}000 \times 10{,}000 \text{ ohms} \times 0.1 \times 10^{-6} \text{ F}$$
$$= 5 \text{ seconds}$$

To achieve this time constant, a conventional op-amp integrator would require a 500-microfarad capacitor.

This integrator circuit can function effectively at any frequency that the operational amplifier can handle, and at any signal level that does not saturate the transistor. Any of several operational amplifiers can be used; the 741 was chosen here for its good compensation. Likewise, many transistor types can be used. The 2N4974 was chosen for its availability and high β. □



Integrator. Operational amplifier plus transistor makes integrator with large time constant, despite small size of integrating capacitor C. The circuit shown here has an effective time constant βRC of 5 seconds. Feeding the noninverting input terminal of the operational amplifier gives high input impedance, and degenerative feedback through the transistor provides critically damped transient response.

Waveform integrator averages over variable elapsed times

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Finding the long-term average voltage of a waveform is much more difficult when the signal averaging must be done over a variable rather than a fixed time. But the average value of any signal sampled over an interval of 1 minute to 2 hours can be found easily with this circuit, which performs the task with the aid of an integrator-oscillator, an up-down counter, and a digital-to-analog converter. The basic transfer function relating output voltage V_o to input voltage V_{in} at time t:

$$V_o = \frac{1}{t}\int_0^t V_{in}(t)dt \qquad (1)$$

is generated when feedback is implemented and when circuit constants are selected with care.

For the circuit to perform integration, a simple feedback loop is required. A voltage-controlled oscillator is used to drive an up-down counter in this circuit, and the counter, in turn, has an effect on the VCO frequency. The frequency of the VCO is determined by V_{in} and reference voltage V_{ref}. The oscillator is so configured that its output frequency (point A) is:

$$f_o = \frac{K_1 V_{in}}{V_{ref}} = \frac{K_1 (V_{in} - V_{out})}{V_{ref}} \qquad (2)$$

where K_1 is a constant. Thus the up-down counter increments at a rate of f_o when V_{in} is positive and decrements at the same rate when V_{in} is negative.

The contents of the counter at any time t is therefore:

$$B = \int_0^t f_o dt = K_1 \int_0^t \frac{V_{in} - V_o}{V_{ref}} \qquad (3)$$

Now, the ramp- and output-voltage equations are:

$$V_{ref} = K_2 t \qquad (4)$$

$$V_o = K_3 B \qquad (5)$$

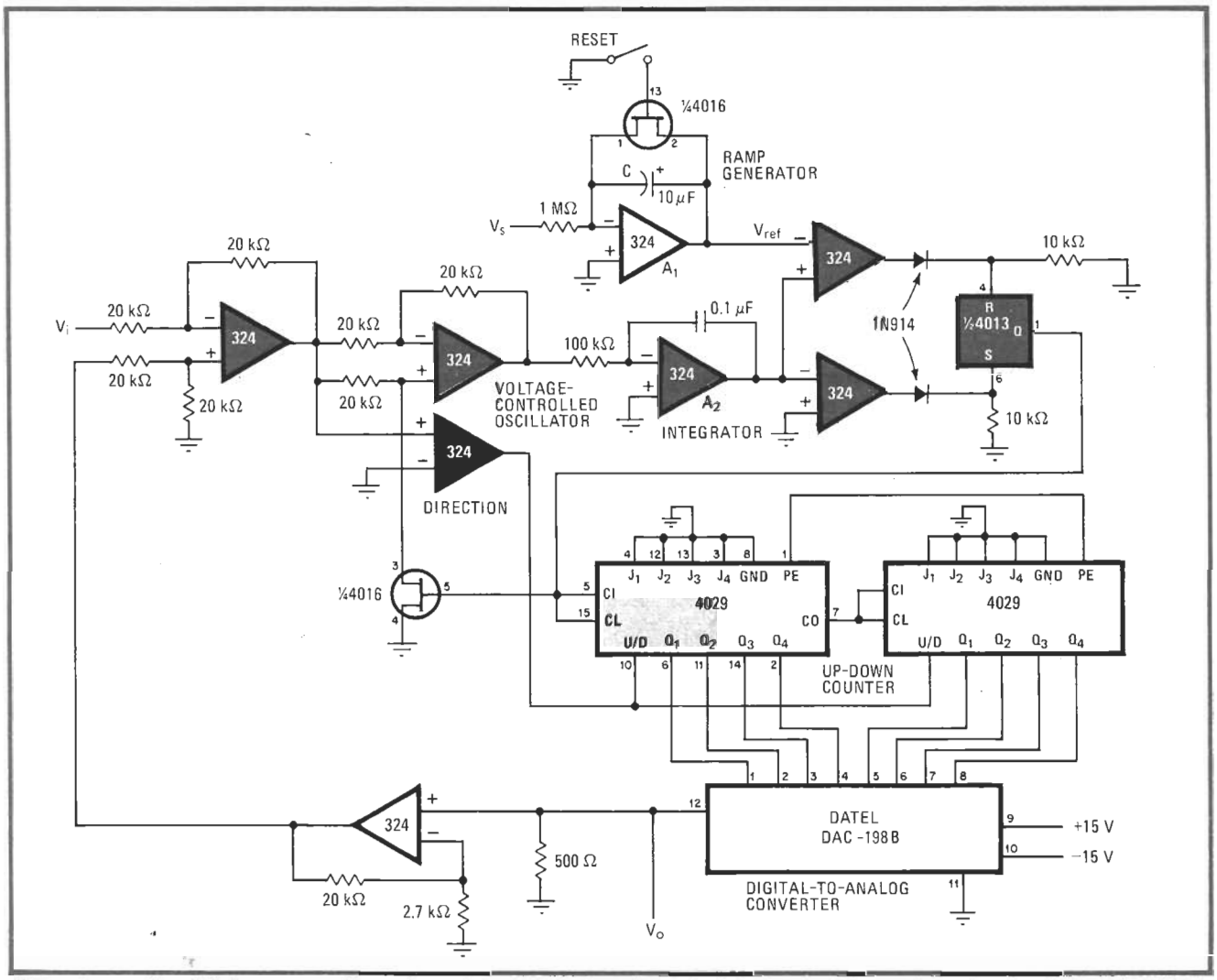
where K_2 and K_3 are, respectively, the initial amplitude of the ramp and the proportionality constant of the d-a converter.

When Eq. 4 is substituted into Eq. 3 and thence into Eq. 5, and when circuit constants are selected so that $K_1 K_3 = K_2$, then:

$$V_o = \int \frac{V_{in} - V_o}{t} dt \qquad (6)$$

Differentiating and rearranging this equation yields:

$$V_o + t\frac{dV_o}{dt} \equiv \frac{d}{dt}(V_o t) = V_{in} \qquad (7)$$



True average. Circuit finds average voltage of waveforms sampled over interval of 1 minute to 2 hours. Averaging time is determined by C. Averaged voltage is in digital form at the output of the up-down counter, in analog form at the output of the d-a converter.

and this equation reduces to Eq. 1 when integrated.

The actual circuit uses all standard components. The ramp generator (A_1) is a standard integrator circuit, which is reset at the start of a timing interval. In this application, however, the integrator requires a low-leakage integrating capacitor. A maximum integration time of 1 hour can be achieved with a 10-microfarad capacitor and an integrator input voltage of 0.03 volt.

The voltage-controlled oscillator is somewhat unusual. Any input voltage, positive or negative, will cause integrator A_2 to ramp in the positive direction starting from the initial V_{in} potential and will also drive the 4013 flip-flop high. The logic 1 generated at the Q output will increment or decrement the counter. When the ramp voltage from A_2 reaches V_{ref}, the flip-flop will be reset, generating a feedback voltage that causes A_2 to ramp in the negative direction at the same rate it rose. When the ramp reaches ground potential, A_2 prepares to integrate V_{in} once more. The instantaneous value of V_{in} is again introduced into the integrator, and the process is repeated until the ramp generated by A_2 fails to reach the signal produced by A_1, which is slowly rising toward the positive supply voltage; this will be recognized as the end of the sampling interval. The contents of the 4029 counter or Datel 198B d-a converter can, of course, be observed at any time. The averaged voltage will be in digital form at the output of the counter or may be obtained in analog form at the output of the d-a converter.

In practice, the minimum value of V_{ref} should always be above ground potential. The lower limit, in general, will be determined by the response time and frequency capability of the particular VCO used. The ramp slope can then be selected so that V_{ref} will be less than the supply voltage for the longest averaging time expected. Of course, since V_{ref} cannot start from zero, an error will be observed at the output when the analog signal is first processed (that is, for small values of t).

The highest frequency at which the VCO can cycle is 10 kilohertz. At this rate, the maximum measurement error will be 1% after 2 minutes if the maximum averaging time is 1 hour. Accuracy will improve with time and will be directly proportional to the VCO frequency. □

Engineer's notebook is a regular feature in *Electronics*. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay $50 for each item published.

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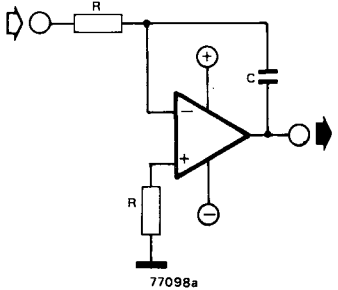
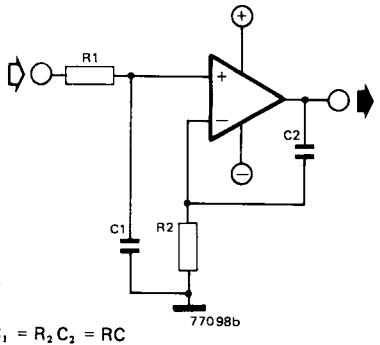
non-inverting integrator

A drawback of conventional integrator circuits (figure a) is that the R-C junction is at virtual earth; this means that C appears as a capacitive load across the op-amp output, a fact that may adversely affect the stability and slew rate of the op-amp. Since the non-inverting character of an integrator is of minor importance in many applications the circuit shown in figure b offers a viable alternative to conventional arrangements.

a



b



$R_1 C_1 = R_2 C_2 = RC$

This integrator, unlike that in figure a, is non-inverting. The time constants $R_1 C_1$ and $R_2 C_2$ should be equal.
If both R_1 and C_1, and R_2 and C_2 are transposed then the result is a non-inverting differentiator.
For correct offset-compensation R_1 and R_2 should have the same value.