Service Scope

USEFUL INFORMATION FOR USERS OF TEKTRONIX INSTRUMENTS

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SOME BASIC SAMPLING CONCEPTS REVIEWED

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Editor's Notes

The basic concepts reviewed in this article apply to all sampling instruments. The information, however, as it is presented here was developed around the calibration of the Tektronix Type 4S1 Dual-Trace Sampling Unit. It is directed principally toward those who, when exposed to sampling techniques, feel the need for a bit more support. By developing a fuller understanding of these important features of fundamental concern, the author hopes to supply this support and to dispel the needless fear of sampling that seems to hover in the minds of some.

This article has been prepared for those involved in the calibration of the Tektronix Sampling Units, with the Type 4S1 Dual-Trace Sampling Unit being used as an example. It is intended to dissolve a few ordinary misgivings about approaching the unit and to outline an orderly and effective method of system diagnosis and treatment. You should make an effort to thoroughly understand what each adjustment accomplishes. Once you attain this objective, you will no longer need to rely on detailed instructions to calibrate the instrument. You should find it possible to perform all the necessary adjustments on a Type 4S1 in a very few minutes. Performing all the checks that insure the instrument meets original specifications may, however, take an hour or more.

	RISETIME	SAMPLING EFFICIENCY	LOOP GAIN	DOT TRANSIENT RESP.	NOISE	SCALING DRIFT	ATTENUATOR BALANCE	BRIDGE DYNAMIC RANGE
SNAP-OFF CURRENT	X	X		X	X			
MEMORY GATE WIDTH			X	X	X			
"A" BRIDGE VOLTS	A	A		A	A	A		A
"B" BRIDGE VOLTS	B	B		B	B	B		B
AC AMP GAIN (A)	A		A	A	A			
AC AMP GAIN (B)	B		B	B	B			
"A" BRIDGE BALANCE							A	A
"B" BRIDGE BALANCE							B	B
"A" SMOOTHING			A	A	A			
"B" SMOOTHING			B	B	B			
"A" SMOOTHING BAL							A	
"B" SMOOTHING BAL							B	
"A" DC OFFSET							A	A
"B" DC OFFSET							B	B

TABLE 1

Excellent performance should not be expected from random adjustments. Rather, an orderly and systematic approach must be taken to restore the Type 4S1 to its proper characteristics. Adjustment is neither a difficult nor an extremely simple thing to do. A few adjustments, because they have an effect on several different characteristics (all of which we wish to hold within specified limits), confound the recalibration. The chart (see Table 1) shows the adjustments that have an effect on several different characteristics. Your principal objective should be to first diagnose the ills by knowing the symptoms, select the most suitable remedy, and *then* perform the operation you have selected.

Let's review some basic sampling concepts with the intent of learning what characteristics are changed by each adjustment within the sampling "head". First of all we should have a good understanding about *sampling efficiency* which is a measure of signal transfer across the bridge diodes sampling gate. Consider the diagram shown in Figure 1. Our purpose in opening the sampling gate is to permit the sampling capacitance (C_s) to "see" the input signal for a small period of time, the duration of the sample being a limiting factor of system risetime. (Instrument risetime can be no faster than the length of time the sampling gate is open.) We know that it invariably takes some time to fully charge a capacitor because the source and current path have impedance. The pre-amplifier input capacitance (frequently called the sampling capacitance) in the Type 4S1 will charge to

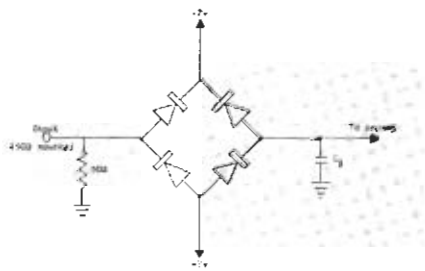

Figure 1. Schematic of a simplified sampling-bridge gate.

only about 25% of the difference in voltage across the sampling gate in 0.35 nanoseconds. This percentage is referred to as the sampling efficiency.

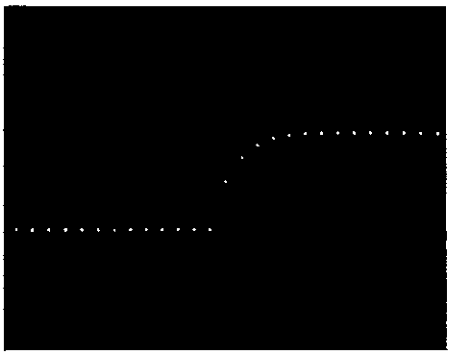

Figure 2. Waveform of the exponential increase in the sampling-capacitance charge with each successive sample, when very few samples/division are taken.

Since this capacitance will not be discharged between samples, we would expect the charge to increase exponentially with each successive sample as shown in Figure 2. Our system would then reconstruct a pulse with severe rolloff even from an infinitely fast step function if very few samples per division were taken. The rolloff would become less obvious, of course, if more samples per division of horizontal deflection were taken. For example, if 10 samples were required to fully charge the sampling capacitance, the rolloff would be evident for 1 division at 10 samples per division. But with 100 samples per division the rolloff would take place in less than one-tenth of a division and would be less apparent.

But let's suppose that the oscilloscope operator should choose to decrease the time required to complete a display of low reprate signals. He may do this by reducing the number of samples taken per trace (fewer samples/div). Since under these circumstances a fast rising step function may go from zero volts to its maximum voltage between samples, we must somehow cause the sampling capacitance to become the gate with only one sample. The method used here is to amplify the change in voltage on the sampling capacitance and add the amplifier voltage to this capacitance between samples in such a way that it has a voltage equal to the input signal voltage at the instant when last sampled. In other words, the amplifiers and attenuators in the entire loop should cause the sampling capacitance to charge to the level it was exponentially headed for during the preceding sample.

Refer to Figure 3 and assume a one-volt step signal applied to the input of this system. The system we may assume has a sampling efficiency of 25%. The sampling capacitance would therefore charge to 0.25 volts on the first sample. Between samples we could amplify the charge with an amplifier having a gain of four and feed back this one-volt signal level to the sampling capacitance for a period of time that permits full transfer of the charge. We then end up with the required one volt across the sampling capacitance. Now we can change the number of samples per division and the transient response of the observed waveform should remain the same. We could say, then, that our "dot transient response" is correct since we have a gain of exactly one through the entire loop when referred to the input signal. (Remember, though, that this required *a gain of four* when referred to the charge on the sampling capacitance.)

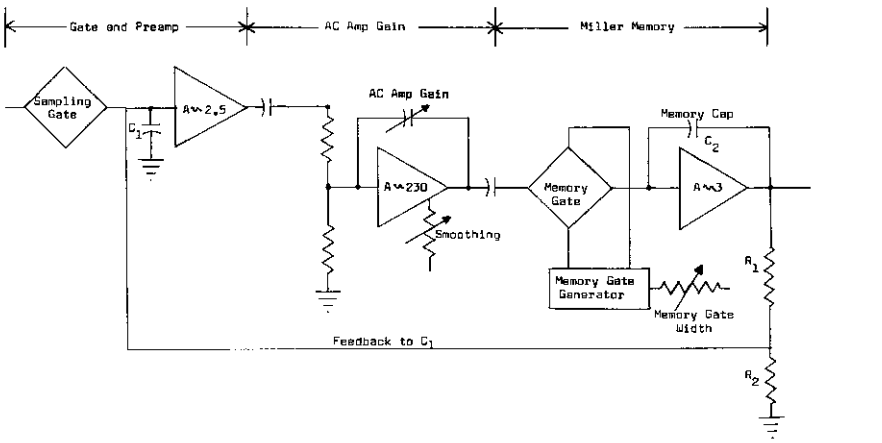

Figure 3. Tektronix slide-back, feed-back sampling system.

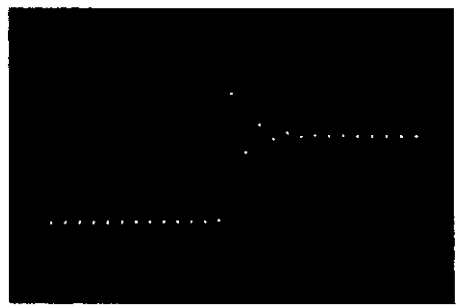

Figure 4. Waveform of overshoot due to the product of sampling efficiency and the amplified feed-back signal being greater than unity.

Obviously then, anything that we do within the sampling loop that changes either sampling efficiency or gain within the loop will also change dot transient response. In other words, *dot transient response is a function of both sampling efficiency and loop gain.*

Suppose that the product of sampling efficiency and the amplified feedback signal were to equal more than unity. Our presentation would then appear to have overshoot and/or ringing as shown in Figure 4. This is just as undesirable as the rolled-off presentation shown in Figure 2.

The four-diode sampling gate performs a few functions which require further explanation. During quiescent conditions the gate is closed so that the signal cannot pass through. To do this, we back-bias the gate with a positive and negative dc voltage of approximately two volts. The dynamic range of the gate is limited by the magnitude of this holdoff bias (BRIDGE VOLTS); a signal greater than two volts might overcome the holdoff bias and improperly charge the sampling capacitance. A trigger pulse from the timing unit initiates the generation of the strobe pulse (to open the sampling gate) and the memory gate pulse (to open the memory gate). The amplitude of the narrow strobe pulse must be sufficient to rise above the holdoff bias for a period of time T, thus forward biasing the bridge diode gate as shown in Figure 5. An increase of strobe amplitude will usually cause an increase in sampling efficiency because the sampling capacitance has longer exposure to the input signal and therefore can charge to a higher voltage. Also, a higher strobe amplitude will cause the diodes to exhibit a lower impedance during the sampling interval. The gain required through the amplifiers and feedback attenuators to yield a loop gain of unity (correct dot transient response) is the reciprocal of sampling efficiency, so we would need to reduce loop gain to compensate for an increase in sampling efficiency if we were to maintain proper dot transient response. Note that a reduction of BRIDGE VOLTS (keeping strobe amplitude constant) could cause a similar change in sampling efficiency.

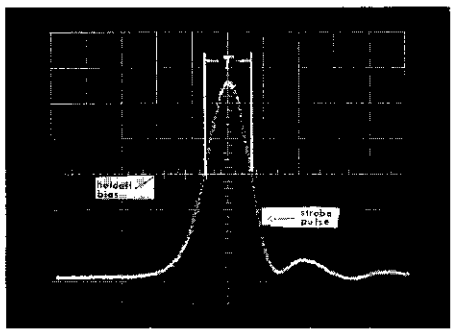

Fig. 5. The narrow strobe pulse rises above holdoff bias for a period of time "T" to forward bias the bridge-diode gate.

A few words are in order concerning the generation of strobe pulses. A trigger pulse from the 5T1A timing unit causes the normally forward-biased snap-off diode to become reverse biased by a reverse current of high and relatively constant amplitude. A peculiar characteristic of the snap-off diode is that this large reverse current ends very abruptly (within a few picoseconds) and the snap-off diode becomes a very high impedance. The reverse current that was flowing down the 50-Ω shorted transmission (clip) line in trying to continue to flow, produces a voltage pulse of short duration that overcomes the back bias on the sampling gate and causes the diodes to conduct. When all the bridge diodes are conducting, they represent a low impedance path for the input signal to get to the input preamplifier. When the voltage pulse is reflected (after about 0.35 nanoseconds) due to current traveling in the shorted clip-line, the sampling gate is returned to its reverse-bias condition thus locking out the input signal once again. The combined snap-off diode and clip-line action produces a very fast rising and falling pulse of a very short controlled duration. Amplitude of reverse current in the clip-line is determined by the stored charge in the diode which is a function of forward SNAP-OFF CURRENT. Reverse current must be sufficient in magnitude so that the voltage created while it travels in the 50-Ω clip line is more than enough to overcome the holdoff bias on the sampling gate.

Let's refer again to Figure 3 and review some of the primary objectives here which are: (1) charge C_1 to the amplitude of the input signal as much as possible during the useable period of the strobe pulse to increase sampling efficiency, (2) feed back an amplified version of this signal between samples to charge C_1 to the full level of the input signal, (3) simultaneously charge C_2 to a value proportional to the input signal level and permit C_2 to retain this charge long enough for us to observe low rep-rate signals.

The voltage on the Memory Capacitor is proportional to the input signal and is used to drive the scope's vertical amplifier. To deflect the dot a given distance with a larger signal at the input requires attenuation of the larger signal before it is applied to the Memory. In other words, the Memory output signal will normally always be proportional to the deflection it causes. Stray capacitance and other factors prohibit using a switched attenuator at the input connector for reducing the deflection sensitivity. It is more feasible to use an attenuator at the pre-amplifier output to limit the signal coupled to the high gain ac amplifier and also prevent overdriving this stage. But we must maintain loop gain close to unity. This requires a second attenuator in the feedback path from the Memory Capacitor to the pre-amplifier input capacitance—one that will track with the ac amplifier attenuator. This will increase the feedback applied to the sampling capacitance as the ac amplifier signal is decreased (as referred to the signal applied to the 4S1 input connector) with less sensitive settings. R_1 and R_2 make up the second attenuator. (Attenuation is reduced here when it is increased between amplifiers with both attenuators operated by the same control knob). The resistor divider ratio of this pair determines the basic calibration of the sampling loop.

Another diode gate precedes the Memory stage. When the fast, narrow strobe pulse is generated, a relatively wide (250-350 nanosecond) pulse is also generated to open the memory gate. The paramount functions of the memory gate circuits are to: (1) control the in-phase feedback to the sampling capacitance and prevent the memory from responding to this regenerative feedback signal, (2) insure maximum coupling of the amplified error signal to C_2, and (3) limit memory capacitor discharge between samples. (Leakage of the charge in this capacitor causes vertical deflection of the dots between samples and is called Memory Slash.) It limits the maximum permissible time between samples for a useful display. This leakage is caused by Memory Amplifier grid current or diode gate leakage.

A cursory analysis of the system as shown in Figure 3 reveals that the following controls all have a direct effect on dot transient response:

1. Those that control *sampling efficiency* are
   a. SNAP-OFF CURRENT—common to both sampling gates
   b. BRIDGE VOLTS—one for each sampling gate
2. Those that control *loop gain* are
   a. AC AMPLIFIER GAIN—one for each sampling gate
   b. MEMORY GATE WIDTH—common to both memories
   c. SMOOTHING—a front panel control for each ac amplifier

The primary purpose of the SMOOTHING control is to reduce random noise by reducing gain of the ac amplifier. Since this is within the feedback loop, it necessarily follows that dot transient response will be effected corresponding to the amount of smoothing used, but may not be apparent when using lots of samples.

Your preparation for recalibration and/or repair should include the following additional presets on the Type 4S1:

MV/CM SWITCH	200
VARIABLE	Calibrated
VERTICAL POSITIONING	Midrange (dot to 12 o'clock)
SMOOTHING	Normal (Maximum loop gain)
DC OFFSET	Adjust for zero volts ±100 mv at the DC OFFSET MONITOR jack

With a free-running sweep, both traces should be well within the central graticule area of a properly adjusted instrument. Severity of imbalance is often indicated in this display and your observations here may help in the diagnosis. If the presentation looks other than normal, first perform steps 3 and 4 of the recalibration guide which follows this article and then start back with step number 1.

Several methods, each having its own merits, may be used to show dot transient response error. A most useful method is to apply a step-function to the input and use a sweep speed that will display no more than two or three samples on the leading edge of the pulse (low vertical dot density) at 100 or more samples per division. Should the pulse shape or transient response change when switching from 100 to 10 or fewer samples, *then dot transient response is not correct.* Quite often in using only 10 samples/div an important part of the trace may be missing and the overshoot or undershoot that appeared with 100 samples/div will not be displayed because it occured between dots in the presentation. Therefore, when operating at few samples/div you may need to relocate the dots along different portions of the trace or "slide" them back and forth to simulate a solid trace by rotating either the TIME POSITION or VARIABLE TIME/CM control. (The slow sweep speed required for low vertical dot density usually places the beginning of the pulse towards the left edge of the crt. Using the VARIABLE TIME/CM control is generally more desirable for this situation since it moves the trace to the right, towards the center of the screen.)

Another method requires a generator of the mercury-pulser variety (Tektronix Type 109 or Type 110) with a small charge line on one side of the switch and no charge line on the other side. Here the sampling gate is opening on the two inputs alternately. The sampling capacitance most of the time must alternately charge from the amplitude extremes between the voltage at the top of the pulse input and the zero volts from the other input. Response with each sample is manifested in the display. Proper DTR (dot transient response) would give a presentation that should look like Figure 6a. Low loop gain would give a presentation that should look like Figure 6b, and exces-

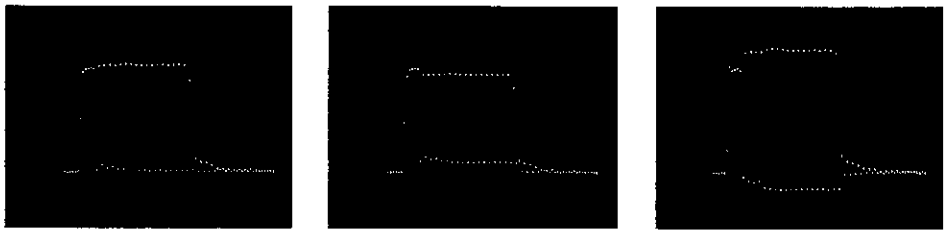

Fig. 6. Waveforms of: (a) correct DTR, (b) low loop gain, (c) excessive loop gain, using a small charge line on one side of the switch and none on the other.

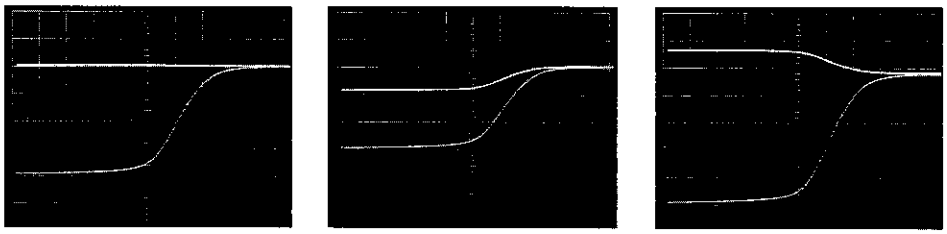

Figure 7. Waveforms of: (a) correct DTR, (b) low loop gain, (c) excessive loop gain, with the 5T1A set up for + INTERNAL triggering at a sweep speed of about 2 NSEC/CM and using a TU-5 Pulser/Adapter operated by a 25-kc square wave from a Type 105 Square-Wave Generator to drive the Type 4S1.

sive loop gain would give a presentation that should look like Figure 6c.

Low repetition rates inherent with mercury-pulsers are sufficiently annoying to warrant investigating other ways of obtaining a similar "twosies" type of display. One such way follows, but requires dc internal triggering: Using a Type 5T1A Timing Plug-In Unit set up for + INTERNAL triggering at a sweep speed of about 2 NSEC/CM, obtain a normal display of the leading edge of a pulse from a Tektronix Type TU-5 Pulser operated by a 25 kc square wave from the Tektronix Type 105 Square Wave Generator. Switching the 4S1 triggering switch from ac to dc trigger coupling should produce a display similar to those shown in Figure 7. Here the trigger circuit is alternately responding to the leading edge and pulse top. Triggering on the pulse top occurs because the pulse top is still more positive than the THRESHOLD setting after trigger recovery takes place making the Type 5T1A ready to trigger again whenever the THRESHOLD level is exceeded. Pulse amplitude after the next recovery cycle will be below the THRESHOLD level which will prevent the trigger circuit from responding until the next positive excursion through the THRESHOLD level setting. The sampling capacitance must therefore charge to the pulse amplitude extremes during the first few centimeters of display with each successive sample.

The chart shown in Table 1 is another useful tool during recalibration. Use it to increase your understanding of the interaction between the various amplifiers and controls.

TYPE 4S1 RECALIBRATION GUIDE

Field recalibration is usually a relatively simple process if previous calibration settings have not since been misadjusted. The following method may be used to perform routine recalibration. This is *not* a complete recalibration procedure, but should serve as a useful reference in conjunction with the regular recalibration procedure in the instruction manuals.

1. Adjust MEMORY GATE WIDTH for maximum loop gain (i.e., maximum overshoot when observing DTR—dot transient response).

NOTE: Before adjusting SNAP-OFF CURRENT or BRIDGE VOLTS, first determine which adjustments need to be made by application of the following concepts:

2. *Check* DTR on both channels.
   a. If the same DTR error exists on both channels, adjust SNAP-OFF CURRENT for correct DTR on both channels.
   b. If Channel A DTR is poor and Channel B DTR is good, adjust Channel A BRIDGE VOLTS for proper DTR on Channel A.
   c. If Channel B is poor and Channel A is good, adjust Channel B BRIDGE VOLTS for proper DTR on Channel B.
   d. If both channels exhibit DTR errors in opposite directions (one showing too much loop gain and the other showing insufficient loop gain), perform the following steps:
      (1) Adjust BRIDGE VOLTS on both channels to maximum clockwise positions.
      (2) Adjust SNAP-OFF CURRENT for proper DTR on the channel that has the highest loop gain as indicated by the most overshoot when samples/cm is changed.
      (3) Adjust BRIDGE VOLTS on the *other* channel for proper DTR.
3. Adjust BRIDGE BALANCE on both channels so that the trace remains on the screen throughout MV/CM settings. (DC OFFSET must be zero volts). Be sure not to brush the DC OFFSET control as you rotate MV/CM.
4. Adjust SMOOTHING BALANCE for no trace shift while rotating SMOOTHING—both channels.
5. Apply a known amplitude to B Channel and adjust B GAIN ADJUST for proper deflection.
6. Apply a known amplitude to A Channel and adjust A-B BALANCE (on the front panel) for proper deflection.
7. Adjust INVERTER ZERO on both channels for less than 2 mm trace shift when switching from NORMAL to INVERTED (DC OFFSET MUST BE ZERO).

This completes the adjustments for the Type 4S1, leaving only a series of checks that should be performed to insure that the instrument is functioning properly. The most important considerations include:

a. RISETIME—less than 0.35 nanoseconds computed.
b. NOISE—less than 1 mv (consider 90% of the dots).
c. BASELINE SHIFT—less than 3 mv base-line shift between 50 cps and 100 kc rep-rates. (This is a shift of the dc reference level or base-line with changes of rep-rate. It may come from several sources including improper adjustments, and is usually greatest between 90 kc to 100 kc. Scaling drift is checked by observing a trace with no signal applied and triggering the sweep from 10 cps to 100 kc using a Type 111 Pulse Generator or equivalent.)
d. MEMORY SLASH—less than ½ cm vertical trace slash at 10 cps.
e. OVERSHOOT or UNDERSHOOT—3% maximum.
f. DOT TRANSIENT RESPONSE—correct for both positive and negative going signals of less than ±½ v in amplitude.

If risetime is adequate but noise and/or scaling drift are excessive, decrease BRIDGE VOLTS and readjust SNAP-OFF CURRENT for proper dot transient response, then repeat steps 2, 3 and 4 above. Make sure that BRIDGE VOLTS is at least 2 volts above and below ground for your final setting.

NOTE—Refer to your instruction manual or recalibration procedure for other checks to be performed.

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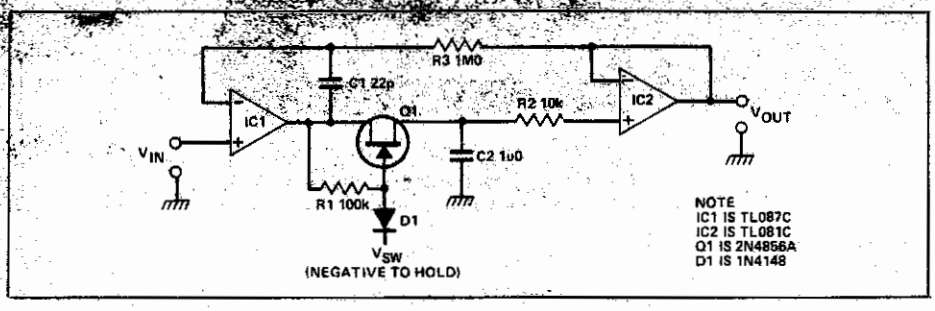

Fig. 12. Low offset sample and hold circuit.

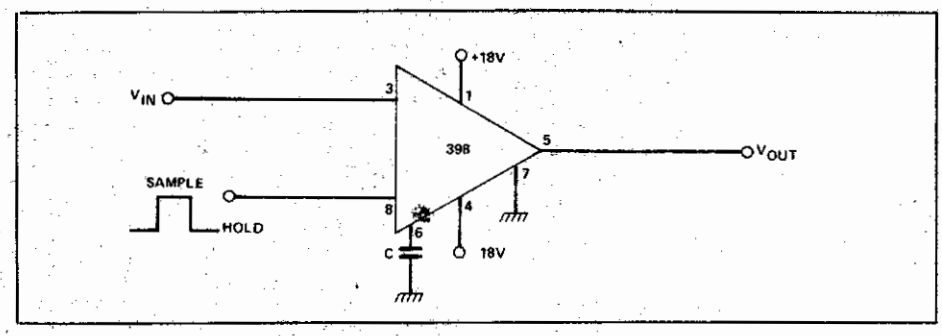

Fig. 13. A ready-made unit, the LM398.

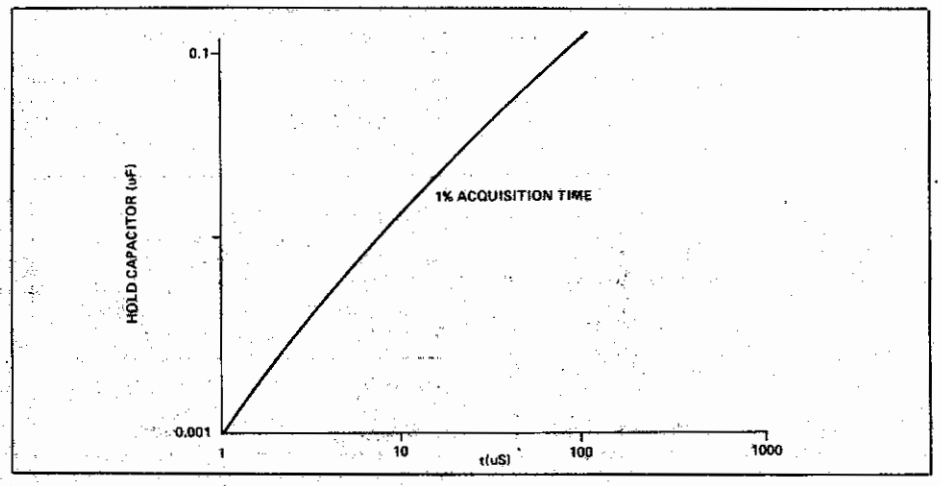

Fig. 14. Choosing the capacitor value for Figure 13.

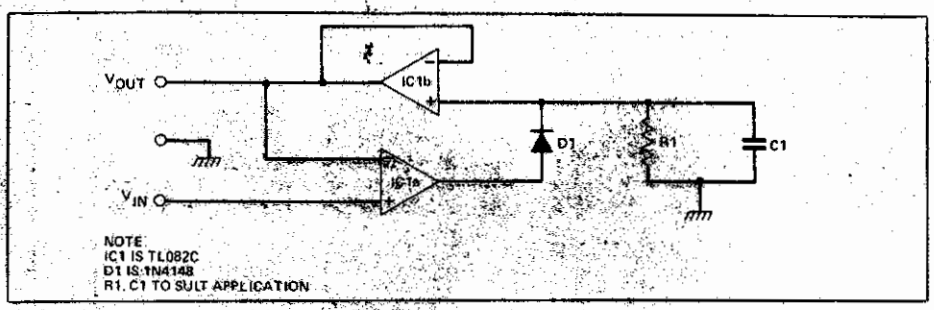

Fig. 15. A simple 'peak picker' circuit.

its internal circuitry is very similar to the configuration that we have looked at in this article, with the difference that the capacitor is an external component to the chip. This device makes the construction of a simple sample and hold circuit much more straightforward. A typical configuration is shown in Fig. 13. The signal that is being sampled is put in to pin 3 of the device, and the output is taken from pin 5. C_h is the capacitor that stores the voltage at hold, and the value of this capacitor is best estimated from the graph in Fig. 14. Taking pin 8 to a logic 1, say 5 volts, will cause sampling to take place, and restoring it to a logic 0 will cause a hold state to ensue.

A capacitor of a value of 1n0 will give a settling time of around 5*u*S, indicating that after this time, after sampling has started, a voltage will be available at the output. Thus after this time you can hold and get an accurate result. This device has found use in analog to digital conversion systems, where it is used to hold a typical value of a rapidly varying analog signal long enough for digitization to occur to the desired degree of accuracy.

Uses

With regard to applications, the field of computer interfacing is the most obvious. In an analog to digital conversion system, the circuit would sample the input and then hold it until conversion had occurred. Obviously, the device used would need to be fast enough to follow the input, but would also require a droop rate which was low enough to allow the conversion to occur before the voltage held on the capacitor had decayed substantially. In this type of application, we would be using the sample and hold circuit to make it possible for a relativley slow analog to digital converter, providing values of a fast moving waveform at regular intervals. Without the sample and hold circuit, the input waveform would have changed before conversion was complete, thus giving an inaccurate reading.

Digital instrumentation is a similar field of application. Electronic synthesizers also utilize them, enabling complex electrical signals to be used to control voltage controlled amplifiers, filters and oscillators.

Slightly modified sample and hold circuits are also used in circuits known as "peak pickers". These circuits continuously sample the input signal, but have as their output, a value representing the highest signal that they've experienced within a given time. The output voltage shows droop, but these circuits find use in estimating rapid transients that have occurred in circuits. Figure 15 shows one peak picker due to TI.

I hope that this article has given you some insight into the sample and hold circuit — a circuit that is finding new applications in the field of data conversion.

ET

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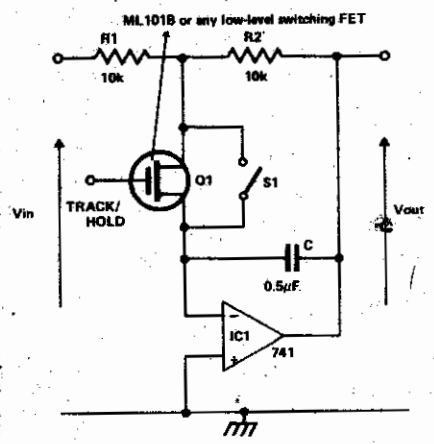
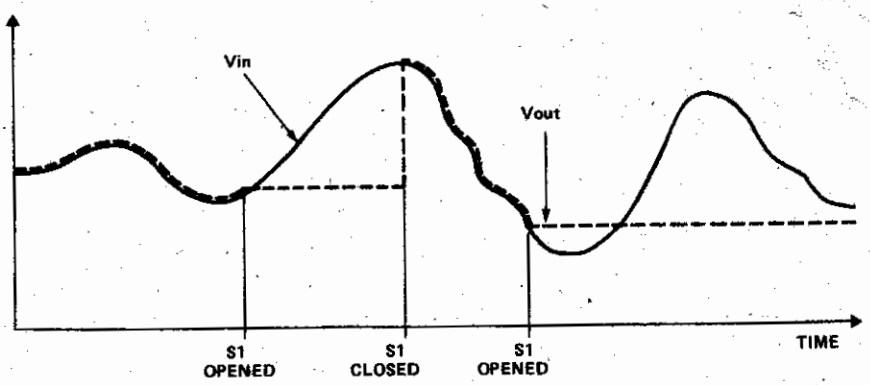
SIGNAL TRACK AND HOLD CIRCUIT





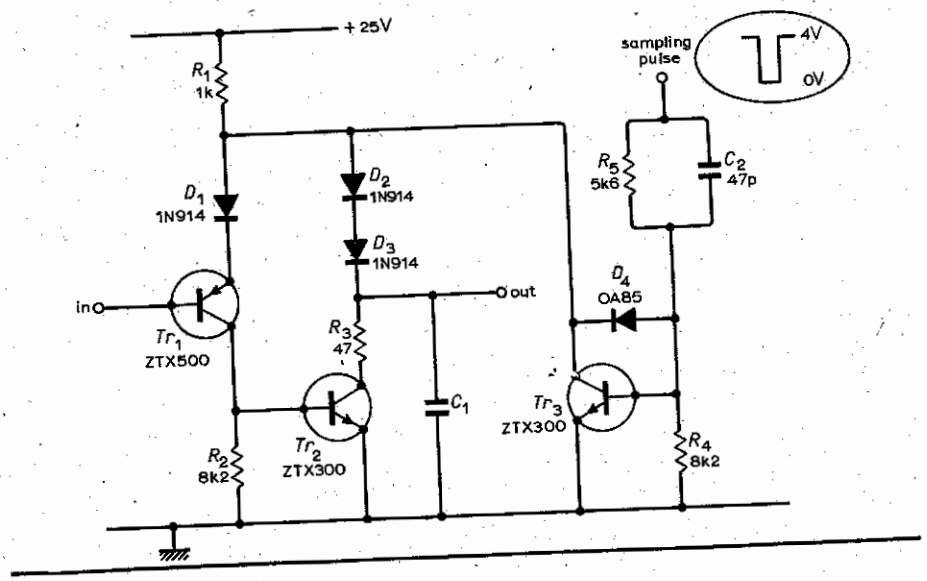
When the switch is closed (or the FET conducting), circuit is behaving as an inverting amplifier with a gain of $\frac{R2}{R1}$. As the inverting terminal of the op amp is a virtual earth, the capacitor is kept charged to the output voltage by the op amp. When the switch is opened (and the FET non-conducting) the voltage at the output is held constant by the capacitor, the current demands of the next stage being met by the op amp. Note that the value of C should be chosen such that its impedance at the operating frequency is large compared to R1 and R2.

Sample-and-hold circuit

The circuit can operate over a wide range of input voltages, with small offset between input and output.

During 'follow' operation Tr_3 is off and Tr_1 and Tr_2 form a simple voltage follower, with low output impedance, driving C_1. Transistor Tr_1 may be easily replaced by an f.e.t. (a p-channel type like 2N3820 for the polarities shown), though the low offset is then lost. To hold the output at any time, Tr_3 is turned on, which turns off D_2, D_3 and Tr_2 via Tr_1 thus isolating C_1. Diode D_1 is required to protect Tr_1 against too much reverse base-emitter voltage, and D_2 to balance the voltage drop across D_1 during 'follow' operation. Both may be removed if a suitably low rail voltage is used and the input and output can approach correspondingly closer to the positive rail. Diode D_4 may be almost any germanium type and stops Tr_3 saturating if the fastest operation is required. Resistors R_4 and R_5 match the input to t.t.l. levels.

J. Kilvington,
Oxford.



Digital sample and hold

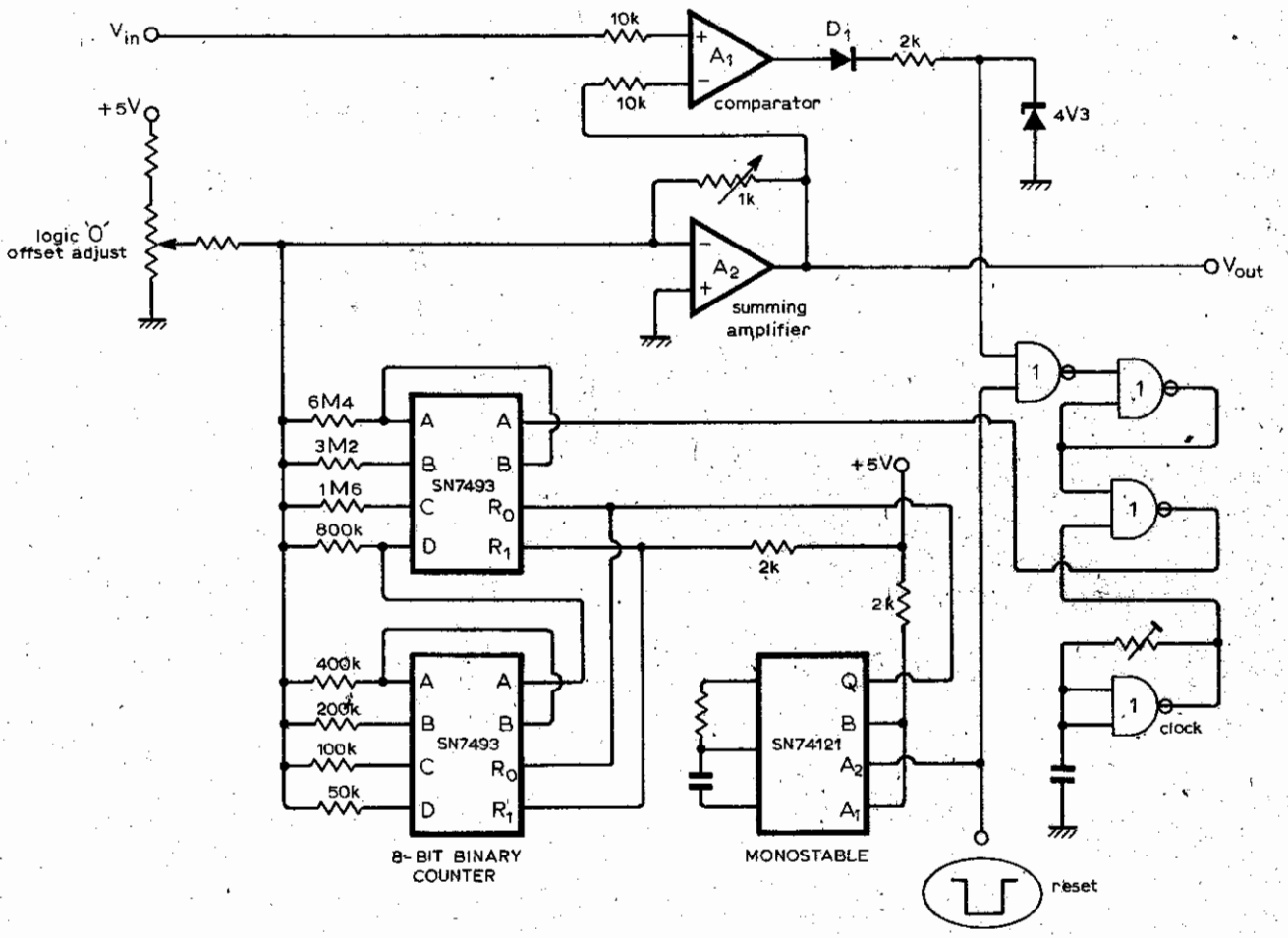
To hold a sampled voltage for long periods, a process of digital approximation provides negligible drift. This circuit is t.t.l.-compatible and provides an analogue-to-digital conversion facility.

The basic element is an 8-bit binary counter using two cascaded 7493s. This provides 256 discrete voltage levels from the op-amp A_2. The input voltage provides a varying reference voltage to comparator A_1.

Applying a 0 at the reset input clears the counter for a period determined by the monostable. The counter now provides a staircase waveform, via A_2, to A_1. When the staircase is equal or greater than V_{in} the comparator goes high and disables the counter clock. The count is held and a sample voltage appears at the output. The reset state has to have a period greater than the sum of the monostable period and 256 clock periods. The speed of the clock is limited by the response of the op amps.

Greater accuracy may be obtained by cascading more counters, but at the risk of increasing the period between voltage transitions at the output. Digital conversion is available directly at the outputs of the counters.

N. Macdonald,
Northampton.



Bias-current network improves sample-and-hold response

by H. F. Nissink
Physics Department, University of Tasmania, Hobart, Australia

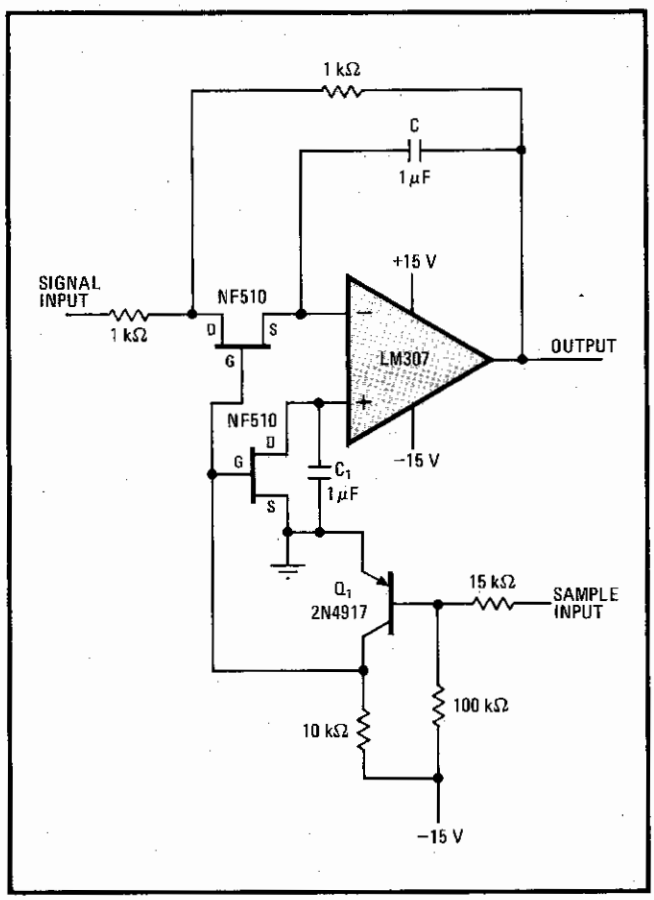
A compensating bias-current network greatly enhances the voltage-holding quality of a sample-and-hold circuit. Connected to the noninverting port of the operational amplifier, the network detects and restores the charge lost by the hold capacitor.

As shown in the figure, an input signal is sampled at the NF510 transmission gate by a pulse from switching transistor Q_1. The sampled voltage appears across C almost instantaneously and should be stored indefinitely. However, there is a small loss of charge with time because of voltage drift at the op-amp output. The drift is due to the op amp's minute bias current, which flows into the inverting input. This current lowers the output voltage and thus the voltage across C.

However, because the bias currents flowing at both inputs of the op amp are approximately equal in magnitude (although opposite in polarity) over a wide range of input voltages, circuitry added to the inputs can compensate for the bias-current flow. Specifically, if C_1 is made equal to C, each port will look out onto an identical circuit. Thus small changes in the bias current at the inverting port, which removes charge from C, will be countered by like changes in the current at the noninverting port, which charges C_1, and the op amp's input offset voltage will be minimized.

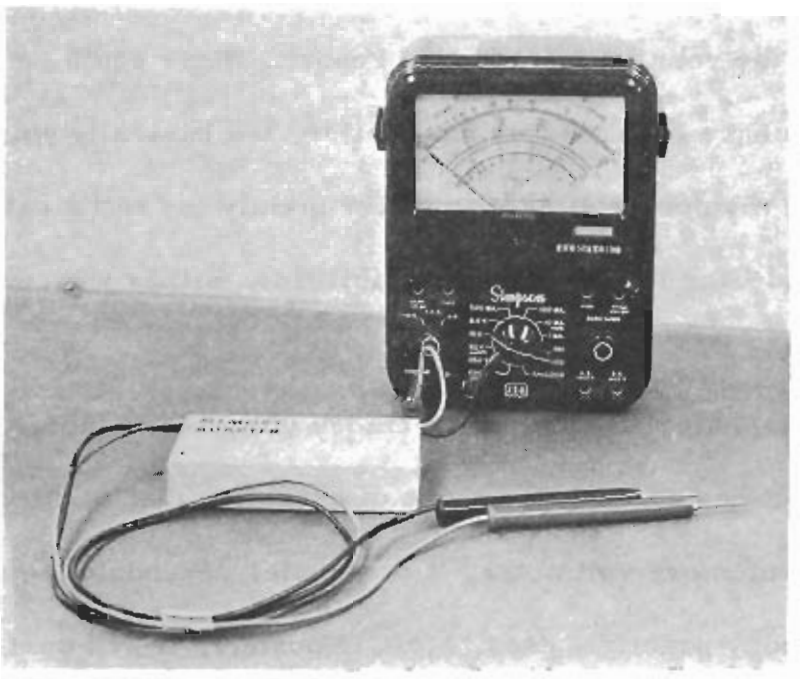
Of course, because of the inherent properties of the op amp, the magnitude of the input currents cannot continue to increase for a constant output voltage. A condition will therefore eventually occur in which the current at the inverting port will exceed the current at the noninverting port, and the output voltage will fall.

The circuit has a hold time—arbitrarily defined as the time in which the output voltage decays by 100 millivolts—of approximately 4 minutes with the values shown and about 10 minutes if both capacitors are doubled in value. The decay is independent of the magnitude or polarity of the input voltage. □



Charge restorer. Sample-and-hold response is improved if charge lost by hold capacitor C is replaced. Voltage change across capacitor due to op amp's inverting-port bias current is cancelled by compensating network. Droop rate, only 100 millivolts per 10-minute period, may be improved if capacitors C and C_1 are matched.

MEMORY VOLTMETER ADAPTER



CONTENT:

BASIC DESCRIPTION.

The Memory Voltmeter Adapter is a device which operates on a principle quite different from that of any memory voltmeter on the present market. Basically, it is a small unit (see Fig. 1 and Fig. 2) used in conjunction with a voltmeter. It has two pairs of leads---one pair is plugged into a voltmeter; the other is used as ordinary test leads. As you see, the whole unit is essentially used as an extension of the test leads. The only difference is that you don't need to hook up the test leads into the circuit to read the voltage. Just a quick touch---and for about a minute the voltage stays displayed on the voltmeter. To make another voltage measurement, make another "touch." The unit will reset itself and display the new voltage. It always remembers the last voltage applied to the test leads. Anyone who has experienced the trouble of holding test leads firmly in the circuit, trying not to cause a short and at the same time reading the voltmeter over his shoulder,will appreciate the convenience of this device. When measuring in highly inaccessible places, you can even disconnect the unit from the voltmeter and put it into your shirt pocket. After making a "touch" connect the device to any voltmeter and conveniently read the voltage!

Besides the utilization of this device as a memory voltmeter, the basic circuit (which is essentially an analog memory cell) can find numerous applications in projects requiring an analog memory.

HOW IT WORKS.

This part is a technical one---skip it if you are not interested in the theory---or read as much as you want.

Regarding Fig. 2, which is a block diagram of the adapter, you see that the set-up is quite simple. Voltmeter V is connected between the output and the non-inverting input of a high gain DC amplifier. The inverting input is tied to the output through capacitor C. Test leads are connected as indicated.

When a DC voltage (Vin) is applied to the test leads, the amplifier will develop a voltage (V_{out}) across the voltmeter. If the gain of the amplifier is G, then:

$$V_{out} = V_{in} \left(1 - \frac{1}{G}\right)$$

In our case the gain G is very high and the term 1/G is so small compared with 1 that we can, for any practical purpose, assume that $V_{out} = V_{in}$. In other words, the voltage across the voltmeter is the same as that applied to the test leads, and the voltmeter reading is correct.

If the test leads are removed from the circuit, the voltage V_{in} will disappear, but the voltmeter will still indicate, since the voltage V_{out} will remain. The reason is that capacitor C provides a strong differentiating negative feedback that resists any change in output voltage. The reading will stay within 1% for about a minute before starting to drift. If you want to reset the voltmeter to zero, just short the test leads. But you don't have to do it before another measurement is taken. The device will set itself automatically to

any new voltage applied to the test leads, regardless of whether the previously displayed voltage was higher or lower. The explanation is simple: The differentiating feedback is not present during the time the test leads are hooked into an auxiliary circuit (the capacitor C is shorted by the circuit being measured). Fig. 3 gives a complete schematic of the circuit. You will find all the necessary data and explanation for the parts in Table 1. The values are given for a 9V battery version, which works on input voltages up to 8V. By using two batteries (18V version), you can measure up to 16V, which is more than adequate for most transistor circuits. If you want to build a unit for higher voltages, please refer to Chapter 6 , How TO MODIFY THE DESIGN. The layout in Fig. 3 is straightforward. Transistors T_1, T_2 and T_3 form a DC current amplifier, Transistors T_4 and T_5 are used as a combined Darlington emitter follower for driving the voltmeter. Potential divider (R_1, R_2) ensures a low collector voltage for T_1 and, consequently, a low leakage collector current. Capacitor C_2 prevents oscillation of the whole system. The divider formed by resistors R_3 and R_4 is used to properly bias the input transistor T_1. When measuring with the device, observe proper polarity as indicated in the diagram. When a voltage of reversed polarity is applied, however, the voltmeter will read slightly below zero. This is an indication that the test leads should be reversed. The device draws such a low current (about one microampere) that a battery switch is not necessary and is omitted. The only considerable battery load is the current drawn by the voltmeter (20uA to 200uA in most cases), so it is a good practice to disconnect the voltmeter

when the device is not used for a prolonged period of time (several days). In this way a longer battery life will be obtained. In our experimental model, two cheap (19¢) batteries were still working after a year of uninterrupted operation.

HOW TO BUILD IT.

The circuit is "tame" and can be built in any way you decide. Printed board, Vectorboard, or even a "crow's nest" wiring will give good results. No shielding is necessary. Figures 4 , 5 and 6 show the actual wiring. An example of a unit built on a vectorboard is depicted in Fig. (7). An 18V version of the Voltmeter Memory Adapter (Fig.1 on the front page) is built into a simple plywood box. It contains two standard 9V transistor radio batteries, one 1.5V penlight battery and the circuit built according to Fig.1. The arrangement is shown in a sketch (Fig 8). The whole unit was permanently attached to a Simpson voltmeter and tested for about a year in an actual operation (troubleshooting of transistor instruments). The results demonstrated the excellent features and handiness of this concept.

HOW TO MODIFY THE DESIGN.

The memory adapter described in the previous chapters is battery operated. The limit of the measurable voltage is about 90% of the battery voltage, which is about 16V for the two-battery version. Where higher voltages are to be measured, the unit can be designed to operate from 115VAC instead of batteries. Please realize,however, that making any changes requires a knowledge of electronic design. If you have this knowledge, here are some hints on how to make changes:

1. The DC power supply must deliver two voltages: 1.5V for the bias and, for the collector, a voltage which is about 10% higher than the highest voltage to be measured. The current drawn from the power supply will be about 2 microamperes plus that drawn by the connected voltmeter. Needless to say, the power supply must be completely floating.

2. The original design will work to about 25V. For higher voltages, transistors T3, T4 and T5 (2N3393) must be replaced by transistors that have V equal to or higher than the power supply voltage. The value of resistors R_2 and R_5 in megohms should be equal to the magnitude of the power supply voltage in volts. Capacitors C_1 and C_2 should have a voltage rating of at least twice the power supply voltage.

By following these directions, it will be easy for the experienced designer to modify the adapter to fit nearly any need. Again, if you don't have sufficient knowledge, use the original design.

MARKETING.

Let's face it: You could be a production wizard, turning out one adapter per second, but unless you sell them---you won't make any profit. Though choosing the right product for your basement "factory" is a very important and difficult first step, marketing is the crucial factor affecting your final target---i.e., financial gain. Please do not underestimate this part of your operation---it definitely will determine how much money you will make in the long run. If you want to sell everything you produce, easily and in quantity, you should follow these rules:

1. Unless you are a born salesman, avoid personal selling. (The only exception is the testing of your product.)
2. Use the services of Uncle Sam: Sell by mail, either directly or in response to classified or display ads.

Unfortunately, most technical-minded people are usually not marketing-oriented, and they very seldom know anything about the easy ways and the vast possibilities that selling by mail offers. If you are one of these, get a copy of Joe Cossman's book: "How I Made $1,000,000 In Mail Order." If you doubt the correctness of the figure of one million---you are right. He made about <u>twenty millions</u> before he retired. In his book, the best on marketing by mail ever written, Joe Cossman gives a step-by-step explanation of the foolproof method that brought him millions just by selling through the mail. (Being retired, he can afford to do this.) This 239-page book, written in an easy-to-understand language, can be obtained in the better bookstores or directly from Prentice Hall, Englewood Cliffs, N.J. The price is under 10 dollars. Everyone who can read and follow the easy steps in this book can solve all his marketing problems forever.

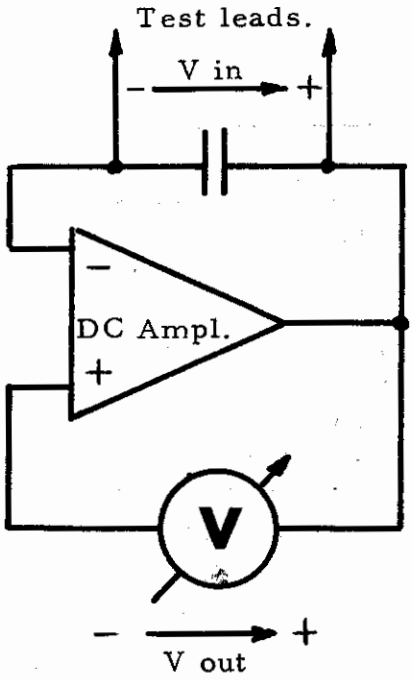


FIG.2

BLOCK DIAGRAM.

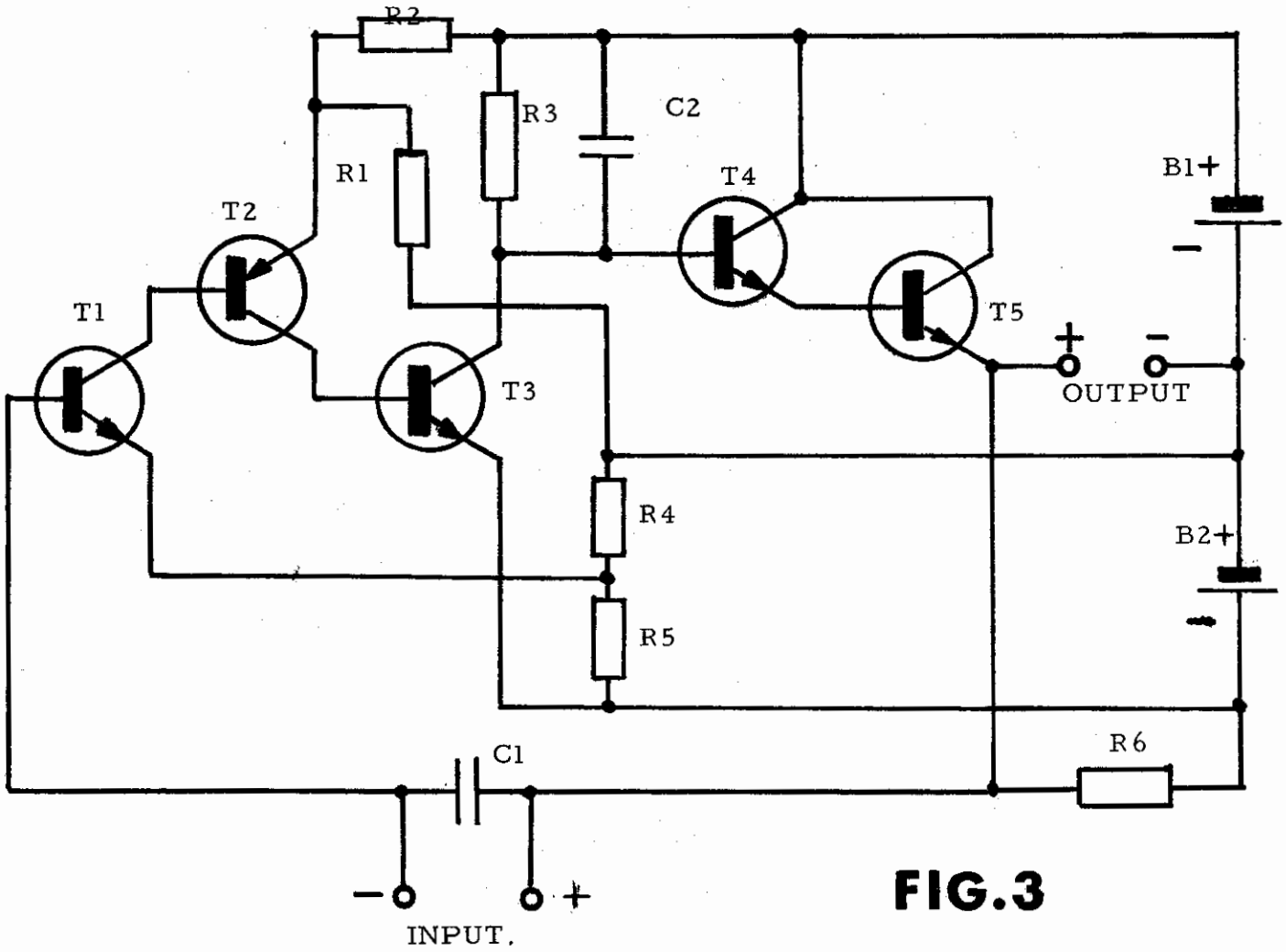


FIG.3

Table 1.

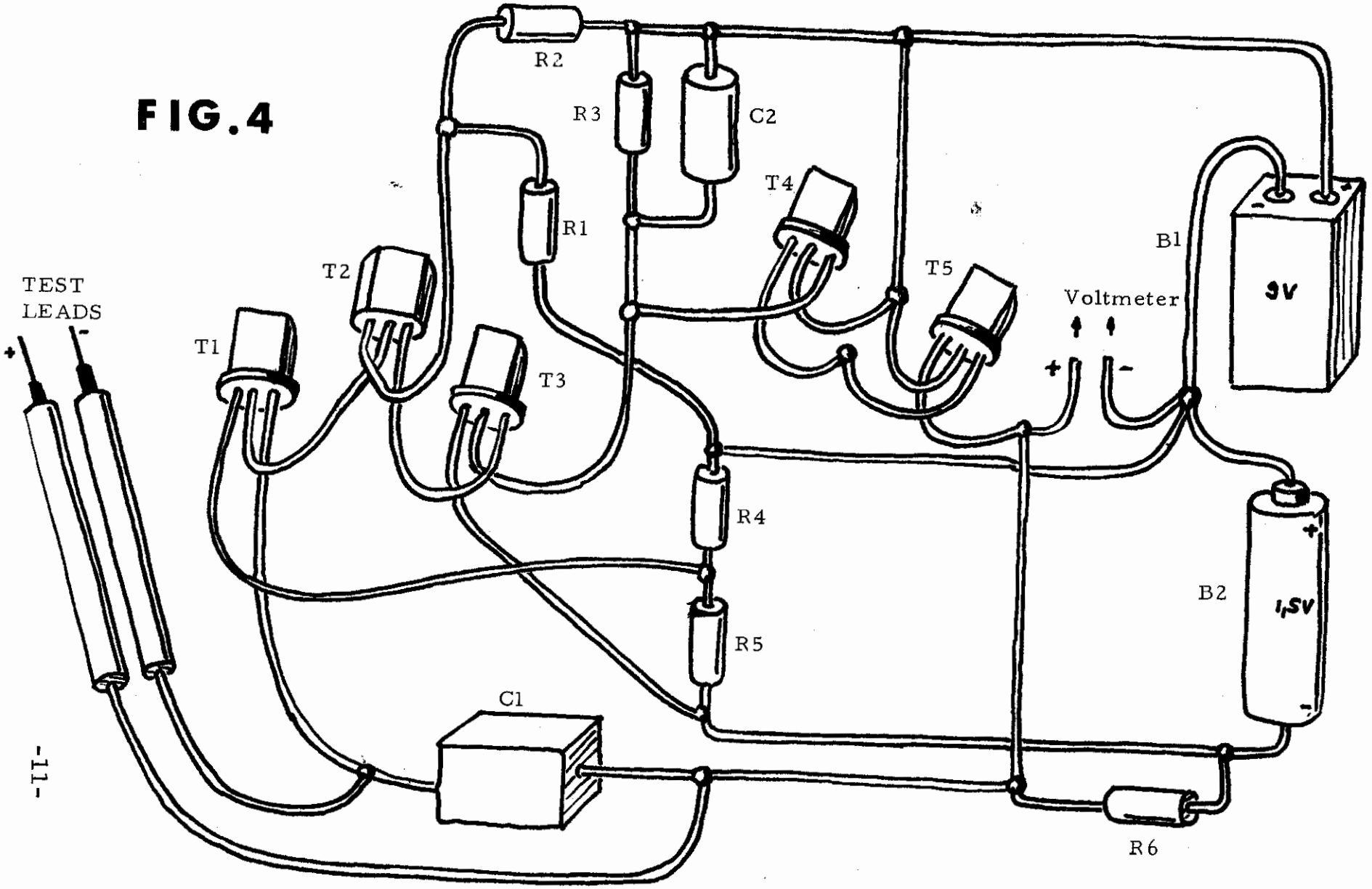
1.	T1, T 3 T4, T5.	NPN silicon transistor 2N3393. Connection--see Fig. 5. Available at you local shop or write for a catalog (free) to addresses listed at bottom.
2.	T2	PNP transistor 2N4126 Connection--see Fig. 6. Availability same as Item 1.
3.	R1	Resistor 1MΩ 0.5W, 10%. Color code: brown, black, green. Availability same as Item 1 or consult chapter 5.
4	R2	Resistor 10MΩ, 0.5W, 10%. Color code: brown, black blue. Availability same as Item 3. For the 18V version: 20M , color code :red, black, blue. For higher voltage version see chapter 6.
5.	R3	Resistor 20MΩ, o, 5W , 10%. Color code: red, black , blue. Availability same as Item 3.
6.	R4	Resistor 300kΩ, 0, 5W, 10%. Color code: orange, black, yellow. Availability same as Item 3. Note: Value should be changed for proper zero setting.
7.	R5	Resistor 1.2MΩ, 0.5W, 10%. Color code: brown, red, green. Availability same as Item 3.
8.	C1	Paper or mylar capacitor .47uF /100V 20% Availability same as Item 3.
9	C2	Capacitor .047uF /100V 20% Availability same as Item3.
10.	R6.	Resistor 1MΩ, 0.5W, 10%. Color code brown, black, green Availability same as Item 3.
11.	B1	9V battery for transistor radios.
12,	B2	1.5V penlite battery.

For a free catalog of electronic components write to:

Allied Radio Shack 2725 W. 7th St., Forth Worth, TX 76107

Lafayette Radio Electronics, Box 10 Syosset, L. I., NY 11791

FIG.4


R2
R3
C2
T4
R1
B1
9V
T2
T5
TEST
LEADS
Voltmeter
T1
T3
R4
B2
1,5V
R5
C1
R6

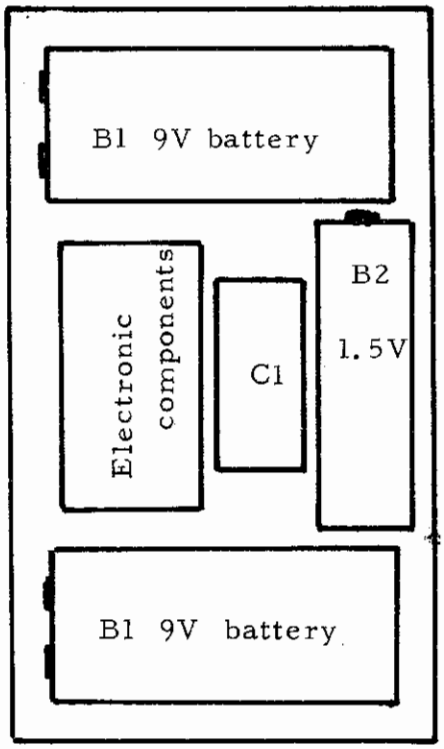


Fig. 8.

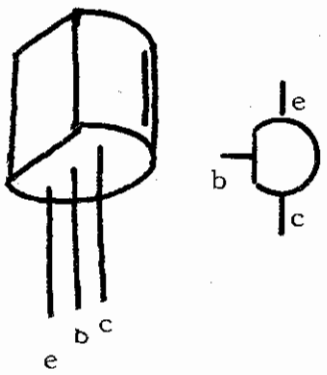


Fig. 5. Transistor 2N4126

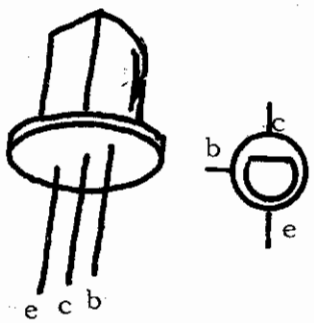


Fig. 6. Transistor 2N3393

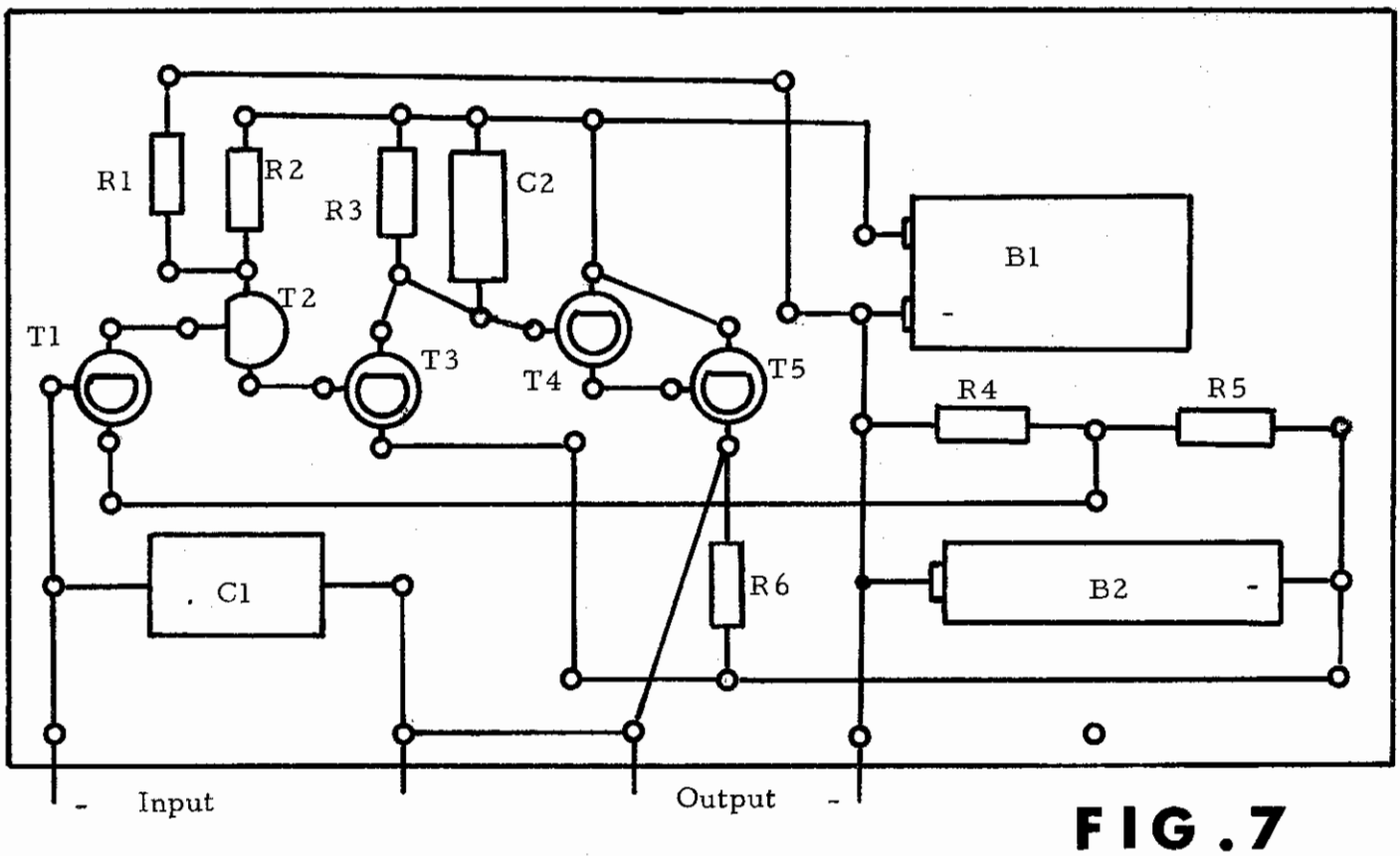


FIG. 7

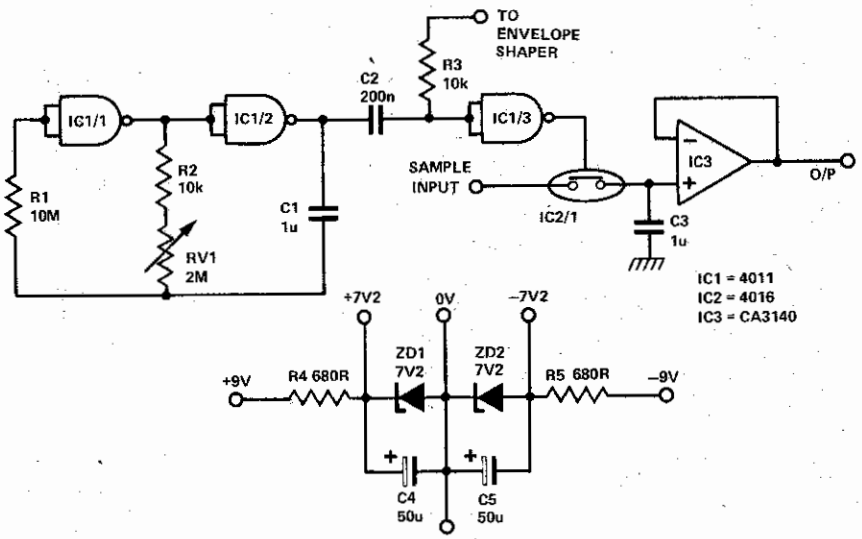
Sample And Hold For Music Synthesizers

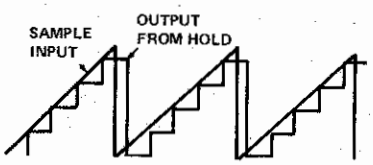
L. Robinson

Sample and hold is a useful effect for use with music synthesizers and consists of 'sampling' an input voltage function such as a waveform for a very short time and then 'holding' it at this selected voltage level for the duration of the clock period. This voltage is then used to control the frequency of a voltage controlled oscillator, filter etc.

It is therefore possible to produce random or repeating sound patterns by varying the input waveform and frequency, pink noise can be used as a sample source to create authentic random voltages.

The circuit shown is much simpler than previously designed sample and hold circuits, this is possible by the use of CMOS technology. The clock oscillator is a standard CMOS square wave oscillator as found in RCA application notes, and this is used to provide a variable frequency rate from 0.2 Hz to 45 Hz. The output then goes to the synthesizer envelope shaper which should be of the ADSR type for maximum effect. The clock output also goes into a monostable which produces an output pulse of approximately 20 mS which opens the 4016 analogue gate for this period. The voltage input is therefore sampled and the value of the amplitude at this point of the waveform is remembered by the high input impedance (10^{12} Ohms) CA3140 voltage follower. This output is then used to control the VCO etc. The oscillator and monostable can be constructed from either a CMOS 4001 or 4069, ensuring that unused pins are connected to the high or low power supply line via a 1k resistor. The input waveform to the analogue switch can have an amplitude of ± 7 V maximum.





If a FET was used as the gate, it would only respond to negative voltages, so the more expensive analogue switch is used for this reason. The total cost of the circuit, including the ± 7 V rail, is less than £3.

Experimenter's Corner

By Forrest M. Mims

THE ANALOG SAMPLE/HOLD CIRCUIT

MICROPROCESSOR enthusiasts are constantly seeking simple ways to interface small controllers and computers with the outside world of analog signals. One well-known analog circuit with many interfacing applications is the op-amp sample/hold (or sample and hold) circuit.

A sample/hold circuit stores in a capacitor the instantaneous voltage present at its input. The stored voltage, which can represent anything from the intensity of light illuminating a photocell to an audio signal, can be converted into digital form by an analog-to-digital converter for processing by a microprocessor. What's more, a sample/hold stage can be used in many different analog applications.

Simple Sample/Hold Circuit. Figure 1 schematically shows a very simple but functioning sample/hold circuit. The key component of the circuit is capacitator *C1*. When switch *S1* is momentarily toggled to its SAMPLE position, the capacitor charges to the voltage present at the input. The charge on the capacitor is monitored by *IC1*, an op amp with a very high input impedance, which should be an NE536 or similar amplifier with a FET input stage. When switch *S1* is released, it returns to its center (off) HOLD position and disconnects *C1* from the input of the circuit. Because the op amp's input impedance is very high, the charge stored in the capacitor is effectively trapped and the voltage across *C1* remains almost constant for an appreciable amount of time.

The op amp is connected as a voltage follower with unity gain. This arrangement permits the charge on the capacitor to be measured by a standard multimeter without significantly altering the amount of stored charge. Connecting a conventional, low-input-impedance voltmeter across the capacitor would, of course, quickly drain the capacitor of its charge. After the magnitude of the voltage sample has been determined, the switch can be momentarily placed in its RESET position to remove the charge from the capacitor and prepare the circuit for a new sample.

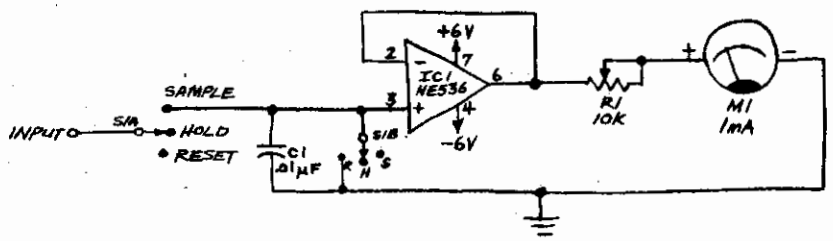


Fig. 1. Schematic of a demonstration sample/hold circuit.

It's easy to operate the circuit in Figure 1. Use a 1.5-volt cell to supply the input voltage. With the sample switch closed, adjust calibration potentiometer *R1* until the meter reads 0.15 mA, which corresponds to a voltage of 1.5 volts.

You can omit the milliammeter and potentiometer if you prefer to connect a voltmeter directly to the output of the op amp. Because the op amp is connected as a unity-gain voltage follower, the voltage at its output will be identical to that at its input. This does not mean that the op amp is superfluous. To the contrary, it provides the very high input impedance that permits the voltage stored across *C1* to be monitored without significant loss.

After you have sampled the input voltage, allow the switch to return to its HOLD position and monitor the meter reading. If *C1* is a high-quality, low-loss polystrene or Mylar unit, the sampled voltage will remain constant for a substantial period of time. Lower-quality capacitors including some ceramic discs will lose their stored charge at a much faster rate, as will be evidenced by a noticeable downward movement of the meter needle.

To increase the circuit's useful storage time, a capacitor larger than the one specified in Figure 1 can be used. But it will require a longer sample interval to charge up to the full input voltage, especially if the sample generator has a significant internal impedance.

Incidentally, if you don't have an NE536 or similar FET-input op amp on hand, you can use a standard 741 for demonstration purposes. You'll have to increase the capacitance of *C1* to 1μF or more, because the stored voltage will

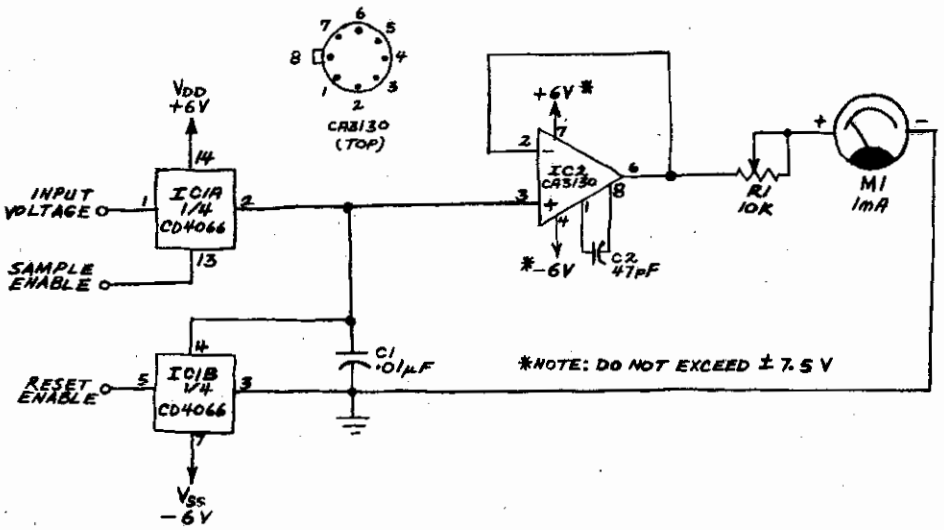


Fig. 2. Digitally controlled sample/hold circuit using CMOS chips. To sample: make sample enable high. To reset: make reset enable high.

be lost much more rapidly than if a FET-input op amp is used, due to the 741's much lower input impedance.

Adding Digital Control. The circuit we have just described is fine for demonstration purposes, but the circuit shown in Fig. 2 is more practical because the sample/hold process is controlled by logic levels instead of mechanical switches. As you can see by comparing the two circuits, the ganged sample/hold/reset switches have been replaced by two of the analog switches in a CD4066 quad analog switch. Furthermore, the NE536 has been replaced by a CA3130 MOSFET-input op amp, but the circuit will work with the 536 as a pin-for-pin replacement without *C2*.

The analog switch is a newcomer to this column. Like the three-state gate described in the March 1978 issue, the analog switch has an ENABLE input and ports that allow a signal to enter and leave. The analog switch, however, can transmit or block both digital logic levels *and* analog (variable) voltages. Like a conventional mechanical switch, an analog switch can pass a signal in either direction. Figure 3 shows the equivalent circuit of the analog switch.

The CA3130 op amp is also a newcomer to this column. I'll have more to say about both it and the CD4066 in future columns. Meanwhile, suffice it to say that the CD4066 is one of a family of CMOS analog switches having many fascinating applications. The switches in the CD4066 are *off* when their ENABLE inputs are *low* and *on* when their ENABLE inputs are *high*. The "off" resistance is around 10^{11} ohms, and the "on" resistance is typically 80 ohms.

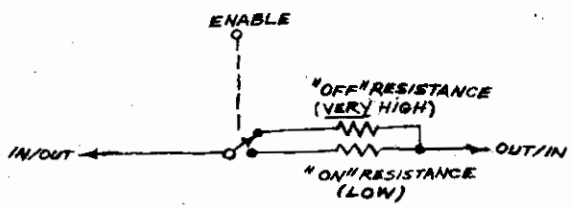


Fig. 3. Equivalent circuit of a basic analog switch.

To sample a voltage with the circuit shown in Fig. 2, the SAMPLE ENABLE input, which is normally kept low, is allowed to go high. The sampled signal level is then stored by *C1* until the RESET ENABLE input, which also is normally kept low, goes high. This allows *C1* to discharge to ground through *IC1B*.

If the RESET ENABLE input is again made low, *C1* will immediately store the voltage present at the input if the SAMPLE ENABLE input is still high. Of course, if the SAMPLE ENABLE input is low, *C1* will not receive the new sample until the SAMPLE ENABLE input is high. (Ordinarily, both ENABLE lines should *not* be allowed to go high simultaneously. Otherwise, the signal source output will be connected to ground via a low-impedance path.)

As you can see, there are several operating possibilities for the circuit, each of which can be readily selected by a two-bit logic signal. The factors governing the calibration of the output meter and the selection of *C1* are identical to those that apply to the previous circuit.

Applications. The most straightforward application for the sample/hold circuit of Fig. 2 is an analog memory circuit capable of storing a transduced temperature, light intensity, or pressure, or any other analog signal for later processing.

The circuit can also be used as a timer. Replace meter *M1* and *R1* with a LED and 330-ohm series resistor. The LED will glow until the voltage across *C1* drops below the LED's turn-on threshold. Increase the capacitance of *C1* for longer time delays. Increasing the magnitude of the sampled voltage up to a maximum of V_{DD} will also give longer delays.

You can create unusual sound effects by connecting the output of the circuit to a voltage-controlled oscillator such as the 566 function generator or unijunction transistor relaxation oscillator. For a siren effect, connect a high resistance (e.g. 1 megohm) between pin 4 of *IC1B* and *C1*. When the RESET ENABLE input is activated, the output voltage will slowly decrease, causing the vco to generate a siren-like sound. The upward wail of the siren is obtained by connecting a second high-value resistor between pin 1 of *IC1A* and the INPUT VOLTAGE source.

No doubt you will find other applications for both circuits with which we've been experimenting this month. I plan to cover some of those that I have found in a future column. ◇