HOW TO SELECT R & C FOR MINIMUM INTEGRATOR DRIFT

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The transfer function for the integrator circuit in Figure 1 is $e_o/e_i = 1/RCS$ where R is the input resistance, C is the feedback capacitance and 1/S is the LaPlace operator denoting integration. This article will show that for a given amplifier, output drift rate due to offset voltage (e_{os}) and bias current (i_b) can be minimized by a proper selection of R and C. For a more complete discussion of integrators, the reader is referred to an article entitled "Operational Integrators" in Volume I, number 1, of Analog Dialogue.

The term (1/RC) can be thought of as the "gain" of the integrator in terms of volts per second output, per volt input. For a desired value of "gain" R and C can be arbitrarily chosen although the lower limit on R is often set by the minimum input impedance required.

Offset referred to the input of an integrator is equal to the sum of e_{os} and i_bR. This corresponds to a drift *rate* at the output equal to

$$\frac{de_o}{dt} = \frac{e_{os}}{RC} + \frac{i_{os}}{C}.$$

If this expression is examined it can be seen that the contribution due to voltage offset is a function of gain (1/RC) while the contribution due to bias current can be minimized by selecting a large C. In fact if C were large enough, this term would be negligible compared to e_{os}/RC.

Figure 2 is a plot of output drift rate vs. capacitance for various gains for several different operational amplifiers given in Figure 3. Here it is assumed that the initial offsets have been balanced and that we are examining the output drift rate only as a function of temperature. The curves are plotted on a log-log scale in a manner analogous to a Bode diagram.

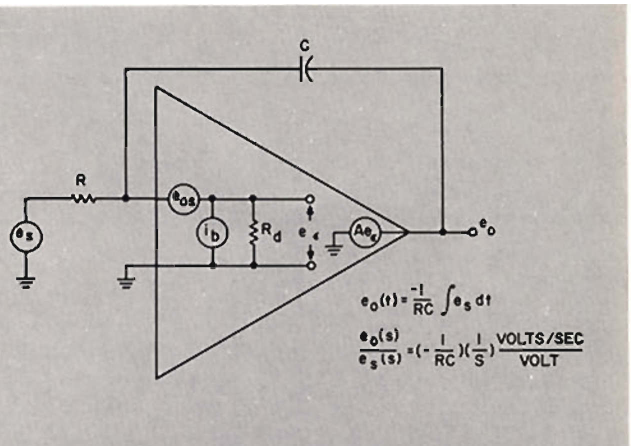

FIGURE 1. Equivalent circuit for Integrator.

For low values of C, drift rate is due almost entirely to bias current i_b/C, and decreases at 6dB/octave as C increases. For high values of C, drift rate reaches a constant value determined by offset voltage, e_{os}/RC. The breakpoint between these two conditions is set by the capacitance for which $e_{os}/RC = i_b/C$.

A number of interesting conclusions can be drawn from the plot. First, to minimize drift rate it can be argued that an optimum value for C occurs at the breakpoint. For larger values of C there is no net reduction in drift rate but only the disadvantages of a smaller input impedance, R, and a more expensive and physically larger size capacitor. (Remember RC is assumed to be constant.) It may not be practical to use the optimum value of C for a given amplifier because of two factors;

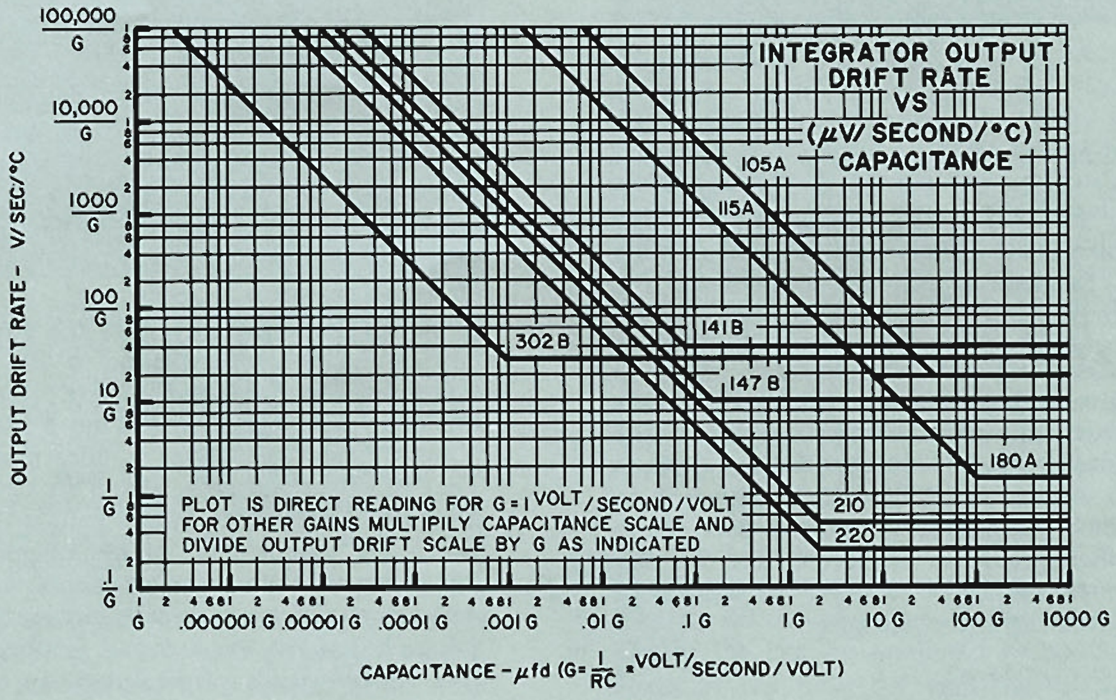

FIGURE 2. Integrator Output Drift Rate vs. (μV/Second/°C) capacitance.

1. The required value for C may be so large and expensvie that it would be wiser to choose an amplifier with lower bias current for a required output drift rate.

2. The resulting input impedance for the optimum value of C would be so low that an amplifier with lower bias current should be selected to keep the input impedance up.

Note that the plots in Figure 2 can be made to apply for any value of gain (that is $G = 1/RC$). Another general point can be made in comparing the plots at different gains. That is at higher gains ($G = 10$), offset voltage tends to be more important in choosing an amplifier for a given drift rate whereas for lower gains ($G = .1$) bias tends to be more important in choosing an amplifier for lowest drift rate.
It is also quite apparent that the best amplifier choice in terms of output drift rate vs. price depends very much on the required gain and the capacitance to be used.

Model and Type		$\frac{\Delta i_b}{\Delta t}$ (pa/°C)	$\frac{\Delta e_{os}}{\Delta t}$ (μV/°C)	\$ (1-9)
105A	Bipolar Transistor	700	20	16.00
115A	Bipolar Transistor	150	20	18.00
180A	Bipolar Transistor	150	1.5	80.00
141B	Field Effect Transistor	3	40	30.00
147B	Field Effect Transistor	1.5	10	115.00
302B	Varactor Bridge	.025	30	135.00
210	Chopper Stabilized	1	0.5	157.00
220	Chopper Stabilized	0.5	0.25	165.00

Figure 3. Comparison of Amplifier Types for Integrator Use.