Ask The Applications Engineer—18

SETTLING TIME

by Peter Checkovich

Q. *Why is settling time important?*

A. Op amp settling time is a key parameter for guaranteeing the performance of data acquisition systems. For accurate data acquisition, the op amp output must settle before the A/D converter can accurately digitize the data. However, settling time is generally not an easy parameter to measure.

Over the years, the techniques and equipment used to measure the settling time of op amps have been barely able to keep up with the performance of the devices themselves. As each new generation of op amps settles to better accuracy in shorter time, greater demands have been placed on test equipment, its designers, and its users. A major dilemma, often causing disagreement among engineers, is whether some combination of techniques and equipment actually measures the device under test (DUT) or just some limiting property of the test setup. So there is continual development of new test equipment and techniques in an effort to specify this ever-demanding parameter.

In a data-acquisition system, the output of an op amp should settle to within 1 LSB [i.e., $2^{-n}FS$] of final value of the A/D that it drives within a time period dictated by the sampling rate of the system. To settle within 1 LSB of full scale implies the settling accuracy of the A/D is ±1/2 LSB. Thus, a 10-bit system will require the op amp to settle to half of one part in 1024, or approximately 0.05%. A 12-bit system will require settling to half of one part in 4096 (0.01%). The requirements for 14-bits and greater are yet more demanding. Settling-time values such as 0.1% and 0.01% are the most widely specified.

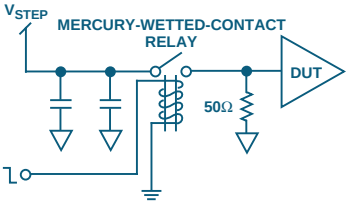
Although a larger full-scale signal range will increase the size of the LSB, easing the problem somewhat, it is not a feasible approach for high-frequency systems. Most high frequency A/Ds have a full-scale span of 1 V or, at most, 2 V. For a 10-bit system with a 1-V full scale signal, an LSB is about 1 mV. For a 12-bit system, an LSB is approximately 250 µV. To resolve the settling characteristics for a full-scale transition, dynamic ranges approaching four orders of magnitude must be handled. With settling times of new op amps [e.g., the AD9631 and AD9632] dropping to the 20 ns to 10 ns range, the measurement of settling time presents quite a challenge.

Q. *How is settling time measured?*

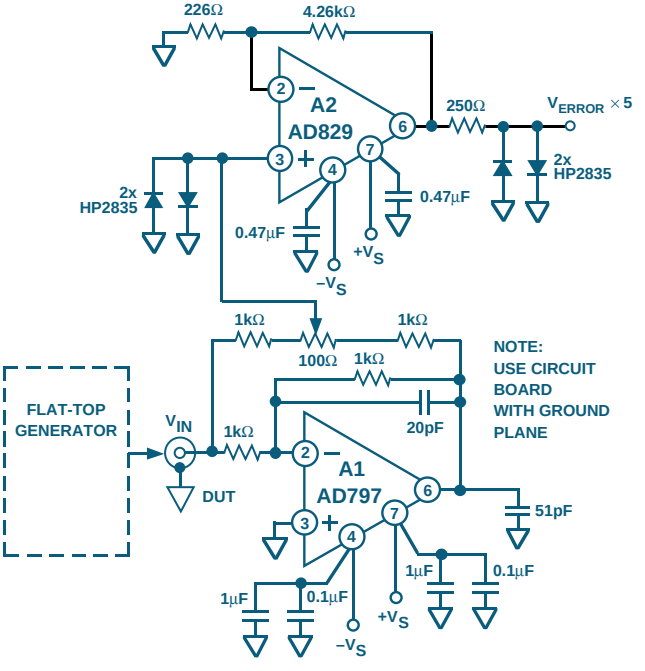
A. A key requirement over the years has been the need to drive the input of the op amp with a fast, precise signal source, often referred to as a flat-top generator. As the name implies, such a generator would have a sharp transition between two levels of known amplitude at time, t_0, should have minimal overshoot (or undershoot) and then remain flat for the remainder of the measurement time. In this case "flat" means significantly flatter than the error to be measured in the amplifier.

The great accuracy is required to be certain that any output signal from the op amp is entirely due to its settling response and not its response to a signal that is present at the input after the step transition. Any active device in the path of this signal would require better settling characteristics than the DUT.

Such generators are in practice very difficult to develop. A rather "low-tech" device has served for quite some time as a means for generating a flat-top transition; the contact opening of a mercury-wetted-contact relay connected to a stable low-impedance voltage source can be used to produce a rather clean (and surprisingly fast) flat-topped pulse. The figure shows a simple circuit that performs this function. For a negative-going transition, with the relay closed, a dc voltage, VSTEP, is applied to the input of the DUT and a 50-Ω resistor to ground. When the relay opens, the input node rapidly discharges to ground, creating the input transition. The open relay contact ensures that all other elements are totally isolated from the amplifier input; the input level is held constant (grounded through 50 Ω) for as long as the relay remains open.



Next problem: directly measuring the output requires handling a large dynamic range. If the DUT is configured as an inverter, a subtractor circuit can be created that only looks at the error signal and does not have to handle the entire dynamic range of the output. This figure shows a circuit used for measuring the 16-bit settling time of the AD797—800 ns typical to 0.0015%.



A1, the DUT in this circuit, is configured for a gain of –1. The voltage divider from input to output forms a second "false" summing node that will replicate the signal at the amplifier's summing node. The 100-Ω potentiometer is used to null the dc voltage. The wiper of the potentiometer is clamped by the diodes at the input of A2 to limit saturation effects in this amplifier. The output is also similarly clamped.

Since the pre- and post-transition voltages at the output of A2 will be the same (i.e., the difference will be zero), the settling

characteristics of this amplifier due to a step change are not important for measuring A1. Thus, the output of A2 can be measured to find the settling time of A1.

This technique requires that the DUT be configured as an inverting amplifier. The circuit can be made to work at other gains, but the resistor values and setting of the dc balance potentiometer will have more influence on the measurement.

Q. *Any other techniques?*

A. Another technique for measuring settling time uses the computing power of a digital oscilloscope. It calculates a waveform that represents the settling error as the instantaneous difference between the acquired input and output signals of the DUT and compares them with the values for an ideally settling device. The resulting waveform is the error of the DUT.

If there is a gain error in this system, it will show up as a dc offset in the error waveform. The calculation can be adapted for a DUT with any gain, either inverting or non inverting. It also can compensate for a signal generator that itself has a low frequency settling tail. The DUT response to a low frequency input will not be influenced by that settling time.

Because such oscilloscopes are designed primarily for speed, in order to determine errors at higher resolutions, averaging must be used. For example, if the A/D used in the oscilloscope has only 8 bit resolution, but accuracy better than 8 bits, a number of cycles can be averaged to increase the effective resolution of the measurement.

Q. *Any more?*

A. Yet a third way to measure settling time is to look at the output directly. A Data Precision Data 6000 can directly digitize signals of up to 5 V with 16-bit accuracy and 10-ps resolution. The only fly in the ointment is that the instrument relies on repetitive sampling with a comparator probe. The waveform is built up one bit at a time for each of the sample points. As a result, obtaining a settling characteristic can be very time consuming. This is especially so when using a relay-type flat top generator with a 1-kHz upper frequency.

Q. *Why do data sheets sometimes define short term and long term settling characteristics?*

A. The traditional definition of settling time is the time from the input transition to the time when the amplifier output enters the specified error zone and does not leave again. This concept is relatively uncomplicated and straightforward. However, there are some cases where the initial settling is fast, followed by an extended period of settling to the final value. Single-supply amplifiers may exhibit this characteristic in the vicinity of the lower rail. Of greater prevalence for large transients, a "thermal tail" is a slow drift that continues for a relatively long time after rapid settling to apparently excellent initial accuracy.

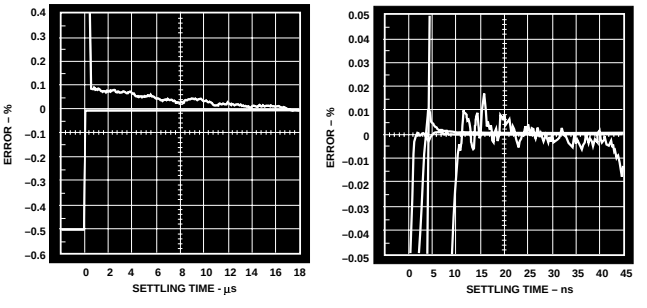
Thermal tails are produced when voltage level changes within the op amp caused by a step transition create temperature gradients among the transistors. Matched transistors will not track well while they are at temporarily different temperatures. The thermal time constant of the chip determines how long it takes for equilibrium to return. Op amps are designed to prevent or reduce these effects by careful placement of devices and strategies to produce thermal symmetry, but this is easier for low-level high-precision devices than those designed for high-speed, because of the large, rapid swings of power that occur.

In particular, the new dielectrically isolated processes (like XFCB) that have worked wonders for improving the raw speed of the op amps can have some difficulty in minimizing the presence of thermal tails. This is because the process provides each transistor a separate dielectric "tub." While this dielectric isolation reduces the parasitic capacitance and greatly speeds up electrical performance, it also provides thermal insulation that slows the dissipation of heat to the substrate.

The seriousness of long tails depends on the application. For example, some systems sample at rates compatible with the initial short-term settling time and are not seriously affected by longer term drifts. Communication systems and others, where the frequency domain properties of the converted signal are most important, are examples of such systems. Although long-term settling errors can produce variations in gain and offset, the long-term thermal tails will have minimal contribution to the distortion products of the digitized signal. For these systems, frequency domain measurements—such as distortion products—are more important than time domain measurements, such as settling time.

On the other hand, systems such as video and scanners might produce a step input, followed by a long-duration plateau of constant value. During this time, repetitive A/D conversions of the op amp output signal will track the long-term settling characteristic. For these systems it is important to understand the long term settling characteristics of the op amp.

The figures below illustrate the long- and short-term settling patterns for the AD8036, a unity-gain-stable high-speed clamp amp that is a good candidate for an A/D driver in high speed systems. The figure at left shows that after the initial large transition, the output is still about 0.09% from its long-term final value. However, the right-hand figure shows, on a 300× faster scale, that after about 16 ns the output has entered a local 0.01% short-term settling region which can be usefully sampled by some systems. The distortion of the AD8036 is extremely low (2nd and 3rd harmonics down by more than 65 dB with 500-Ω load) so it would be a good candidate in systems where this kind of performance is critical.



Reference: Demrow, Robert, "Settling time of operational amplifiers," in *The Best of Analog Dialogue*, 1967 to 1991, pages 32-42.

Analog-Digital Conversion Handbook. Norwood, MA; Analog Devices, 1986, pp. 312-317 and 436-439 (DAC settling time).