Understanding Op Amp Parameters

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11.1 Introduction

This chapter is about op amp data sheet parameters. The designer must have a clear understanding of what op amp parameters mean and their impact on circuit design. The chapter is arranged for speedy access to parameter information. Their definitions, typical abbreviations, and units appear in Section 11.2. Section 11.3 digs deeper into important parameters for the designer needing more in-depth information.

While these parameters are the ones most commonly used at Texas Instruments, the same parameter may go by different names and abbreviations at other manufacturers. Not every parameter listed here may appear in the data sheet for a given op amp. An op amp that is intended only for ac applications may omit dc offset information. The omission of information is not an attempt to "hide" anything. It is merely an attempt to highlight the parameters of most interest to the designer who is using the part the way it was intended. There is no such thing as an ideal op amp — or one that is universally applicable. The selection of any op amp must be based on an understanding of what particular parameters are most important to the application.

If a particular parameter cannot be found in the data sheet, a review of the application may well be in order and another part, whose data sheet contains the pertinent information, might be more suitable. Texas Instruments manufactures a broad line of op amps that can implement almost any application. The inexperienced designer could easily select an op amp that is totally wrong for the application. Trying to use an audio op amp with low total harmonic distortion in a high-speed video circuit, for example, will not work — no matter how superlative the audio performance might be.

Some parameters have a statistically normal distribution. The typical value published in the data sheet is the mean or average value of the distribution. The typical value listed is the 1σ value. This means that in 68% of the devices tested, the parameter is found to be $\pm$ the typical value or better. Texas Instruments currently uses 6σ to define minimum and maximum values. Usually, typical values are set when the part is characterized and never changes.

11.2 Operational Amplifier Parameter Glossary

There are usually three main sections of electrical tables in op amp data sheets. The *absolute maximum ratings* table and the *recommended operating conditions* table list constraints placed upon the circuit in which the part will be installed. *Electrical characteristics* tables detail device performance.

Absolute maximum ratings are those limits beyond which the life of individual devices may be impaired and are never to be exceeded in service or testing. Limits, by definition, are maximum ratings, so if double-ended limits are specified, the term will be defined as a range (e.g., operating temperature range).

Recommended operating conditions have a similarity to maximum ratings in that operation outside the stated limits could cause unsatisfactory performance. Recommended operating conditions, however, do not carry the implication of device damage if they are exceeded.

Electrical characteristics are measurable electrical properties of a device inherent in its design. They are used to predict the performance of the device as an element of an electrical circuit. The measurements that appear in the electrical characteristics tables are based on the device being operated within the recommended operating conditions.

Table 11–1 is a list of parameters and operating conditions that are commonly used in TI op amp data sheets. The glossary is arranged alphabetically by parameter name. An abbreviation cross-reference is provided after the glossary in Table 11–2 to help the designer find information when only an abbreviation is given. More detail is given about important parameters in Section 11.3.

Table 11–1.   Op Amp Parameter GLossary

PARAMETER	ABBV	UNITS	DEFINITION	INFO
Bandwidth for 0.1 dB flatness		MHz	The range of frequencies within which the gain is $\pm$ 0.1 dB of the nominal value.	
Case temperature for 60 seconds		°C	Usually specified as an absolute maximum — It is meant to be used as guide for automated soldering processes.	
Common-mode input capacitance	C_{ic}	pF	Input capacitance a common-mode source would see to ground.	11.3.7.1
Common-mode input impedance	Z_{ic}	Ω	The parallel sum of the small-signal impedance between each input terminal and ground.	
Common-mode input voltage	V_{IC}	V	The average voltage at the input pins.	11.3.3
Common-mode rejection ratio	CMRR or k_{CMR}	dB	The ratio of differential voltage amplification to common-mode voltage amplification. Note: This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.	11.3.9

PARAMETER	ABBV	UNITS	DEFINITION	INFO
Continuous total dissipation		mW	Usually specified as an absolute maximum. It is the power that can be dissipated by the op amp package, including the load power. This parameter may be broken down by ambient temperature and package style in a table.	
Crosstalk	X_T	dBc	The ratio of the change in output voltage of a driven channel to the resulting change in output voltage from another channel that is not driven.	
Differential gain error	A_D	%	The change in ac gain with change in dc level. The ac signal is 40 IRE (0.28 V_{PK}) and the dc level change is $\pm$100 IRE ($\pm$0.7 V). Typically tested at 3.58 MHz (NTSC) or 4.43 MHz (PAL) carrier frequencies.	
Differential input capacitance	C_{ic}	pF	(see common mode input capacitance)	11.3.7.1
Differential input resistance	r_{id}	Ω	The small-signal resistance between two ungrounded input terminals.	
Differential input voltage	V_{ID}	V	The voltage at the noninverting input with respect to the inverting input.	
Differential phase error	Φ_D	°	The change in ac phase with change in dc level. The ac signal is 40 IRE (0.28 V_{PK}) and the dc level change is $\pm$100 IRE ($\pm$0.7 V). Typically tested at 3.58 MHz (NTSC) or 4.43 MHz (PAL) carrier frequencies.	
Differential voltage amplification	A_{VD}	dB	(see open loop voltage gain)	11.3.6
Fall time	t_f	ns	The time required for an output voltage step to change from 90% to 10% of its final value.	
Duration of short-circuit current			Amount of time that the output can be shorted to network ground — usually specified as an absolute maximum.	
Input common-mode voltage range	V_{ICR}	V	The range of common-mode input voltage that, if exceeded, may cause the operational amplifier to cease functioning properly. This is sometimes is taken as the voltage range over which the input offset voltage remains within a set limit.	11.3.3
Input current	I_I	mA	The amount of current that can be sourced or sinked by the op amp input — usually specified as an absolute maximum rating.	
Input noise current	I_n	$\dfrac{pA}{\sqrt{Hz}}$	The internal noise current reflected back to an ideal current source in parallel with the input pins.	11.3.13
Input noise voltage	V_n	$\dfrac{nV}{\sqrt{Hz}}$	The internal noise voltage reflected back to an ideal voltage source in parallel with the input pins.	11.3.13
Gain bandwidth product	GBW	MHz	The product of the open-loop voltage gain and the frequency at which it is measured.	11.3.13
Gain margin	A_m	dB	The reciprocal of the open-loop voltage gain at the frequency where the open-loop phase shift first reaches $-180°$.	
High-level output voltage	V_{OH}	V	The highest positive op amp output voltage for the bias conditions applied to the power pins.	11.3.5
Input bias current	I_{IB}	μA	The average of the currents into the two input terminals with the output at a specified level.	11.3.2

PARAMETER	ABBV	UNITS	DEFINITION	INFO
Input capacitance	c_i	pF	The capacitance between the input terminals with either input grounded.	11.3.7.1
Input offset current	I_{IO}	μA	The difference between the currents into the two input terminals with the output at the specified level.	11.3.2
Input offset voltage	V_{IO}, V_{OS}	mV	The dc voltage that must be applied between the input terminals to cancel dc offsets within the op amp.	11.3.1
Input offset voltage long-term drift		$\frac{\mu V}{month}$	The ratio of the change in input offset voltage to the change time. It is the average value for the month.	11.3.1
Input resistance	r_i	MΩ	The dc resistance between the input terminals with either input grounded.	11.3.7.1
Input voltage range	V_I	V	The range of input voltages that may be applied to either the IN+ or IN– inputs	11.3.15
Large-signal voltage amplification	A_V	dB	(see open loop voltage gain)	
Lead temperature for 10 or 60 seconds		°C	Usually specified as an absolute maximum. It is meant to be used as guide for automated and hand soldering processes.	
Low-level output current	I_{OL}	mA	The current into an output with input conditions applied that according to the product parameter will establish a low level at the output.	
Low-level output voltage	V_{OL}	V	The smallest positive op amp output voltage for the bias conditions applied to the power pins.	11.3.5
Maximum peak output voltage swing	$V_{OM\pm}$	V	The maximum peak-to-peak output voltage that can be obtained without clipping when the op amp is operated from a bipolar supply.	11.3.5
Maximum peak-to-peak output voltage swing	$V_{O(PP)}$	V	The maximum peak-to-peak voltage that can be obtained without waveform clipping when the dc output voltage is zero.	
Maximum-output-swing bandwidth	B_{OM}	MHz	The range of frequencies within which the maximum output voltage swing is above a specified value or the maximum frequency of an amplifier in which the output amplitude is at the extents of it's linear range. Also called full power bandwidth.	11.3.15
Noise figure	NF	dB	The ratio of the total noise power at the output of an amplifier, referred to the input, to the noise power of the signal source.	
Open-loop transimpedance	Z_t	MΩ	In a transimpedance or current feedback amplifier, it is the frequency dependent ratio of change in output voltage to the frequency dependent change in current at the inverting input.	
Open-loop transresistance	R_t	MΩ	In a transimpedance or current feedback amplifier, it is the ratio of change in dc output voltage to the change in dc current at the inverting input.	
Open -loop voltage gain	A_{OL}	dB	The ratio of change in output voltage to the change in voltage across the input terminals. Usually the dc value and a graph showing the frequency dependence are shown in the data sheet.	
Operating temperature	T_A	°C	Temperature over which the op amp may be operated. Some of the other parameters may change with temperature, leading to degraded operation at temperature extremes.	

PARAMETER	ABBV	UNITS	DEFINITION	INFO
Output current	I_O	mA	The amount of current that is drawn from the op amp output. Usually specified as an absolute maximum rating — not for long term operation at the specified level.	
Output impedance	Z_o	Ω	The frequency dependent small-signal impedance that is placed in series with an ideal amplifier and the output terminal.	11.3.8
Output resistance	r_o	Ω	The dc resistance that is placed in series with an ideal amplifier and the output terminal.	
Overshoot factor	–	–	The ratio of the largest deviation of the output voltage from its final steady-state value to the absolute value of the step after a step change at the output.	
Phase margin	Φ_m	°	The absolute value of the open-loop phase shift at the frequency where the open-loop amplification first equals one.	11.3.15
Power supply rejection ratio	PSRR	dB	The absolute value of the ratio of the change in supply voltages to the change in input offset voltage. Typically both supply voltages are varied symmetrically. Unless otherwise noted, both supply voltages are varied symmetrically.	11.3.10
Rise time	t_r	nS	The time required for an output voltage step to change from 10% to 90% of its final value.	
Settling time	t_s	nS	With a step change at the input, the time required for the output voltage to settle within the specified error band of the final value. Also known as total response time, t_{tot}.	
Short-circuit output current	I_{OS}	mA	The maximum continuous output current available from the amplifier with the output shorted to ground, to either supply, or to a specified point. Sometimes a low value series resistor is specified.	
Slew rate	SR	V/µs	The rate of change in the output voltage with respect to time for a step change at the input.	11.3.12
Storage temperature	T_S	°C	Temperature over which the op amp may be stored for long periods of time without damage.	
Supply current	I_{CC}/I_{DD}	mA	The current into the V_{CC+}/V_{DD+} or V_{CC-}/V_{DD-} terminal of the op amp while it is operating.	
Supply current (shutdown)	I_{CC-}/I_{DD-} SHDN	mA	The current into the V_{CC+}/V_{DD+} or V_{CC-}/V_{DD-} terminal of the amplifier while it is turned off.	
Supply rejection ratio	k_{SVR}	dB	(see power supply rejection ratio)	11.3.10
Supply voltage sensitivity	k_{SVS}, $\Delta V_{CC\pm}$, $\Delta V_{DD\pm}$, or ΔV_{IO}	dB	The absolute value of the ratio of the change in input offset voltage to the change in supply voltages.	11.3.10
Supply voltage	V_{CC}/V_{DD}	V	Bias voltage applied to the op amp power supply pin(s). Usually specified as a ± value, referenced to network ground.	
Temperature coefficient of input offset current	αI_{IO}	µA/°C	The ratio of the change in input offset current to the change in free-air temperature. This is an average value for the specified temperature range.	11.3.2

PARAMETER	ABBV	UNITS	DEFINITION	INFO
Temperature coefficient of input offset voltage	αV_{IO}	μV/°C	The ratio of the change in input offset voltage to the change in free-air temperature. This is an average value for the specified temperature range.	11.3.1
Total current into $V_{CC}+$/ V_{DD+}		mA	Maximum current that can be supplied to the positive power terminal of the op amp — usually specified as an absolute maximum.	
Total current out of V_{DD-}		mA	Maximum current that can be drawn from the negative power terminal of the op amp — usually specified as an absolute maximum.	
Total harmonic distortion	THD	dB	The ratio of the RMS voltage of the first nine harmonics of the fundamental signal to the total RMS voltage at the output.	
Total harmonic distortion plus noise	THD+N	dB	The ratio of the RMS noise voltage and RMS harmonic voltage of the fundamental signal to the total RMS voltage at the output.	11.3.14
Total power dissipation	P_D	mW	The total dc power supplied to the device less any power delivered from the device to a load. Note: At no load: $P_D = V_{CC+} \times I$ or $P_D = V_{DD+} \times I$	
Turn-on voltage (shutdown)	$V_{IH-SHDN}$	V	The voltage required on the shutdown pin to turn the device on.	
Turn-off voltage (shutdown)	$V_{IL-SHDN}$	V	The voltage required on the shutdown pin to turn the device off.	
Turn-on time (shutdown)	t_{EN}	μs	The time from when the turn-on voltage is applied to the shutdown pin to when the supply current has reached half of its final value.	
Turn-off time (shutdown)	t_{DIS}	μs	The time from when the turn-off voltage is applied to the shutdown pin to when the supply current has reached half of its final value.	
Unity gain bandwidth	B_1	MHz	The range of frequencies within which the open-loop voltage amplification is greater that unity.	11.3.15

Table 11–2. Cross-Reference of Op Amp Parameters

ABBV	PARAMETER
αI_{IO}	Temperature coefficient of input offset current
$\Delta V_{CC\pm}$/ $\Delta V_{DD\pm}$	Supply voltage sensitivity
αV_{IO}	Temperature coefficient of input offset voltage
ΔV_{IO}	Supply voltage sensitivity
A_D	Differential gain error
A_m	Gain margin
A_{OL}	Open loop voltage gain
A_V	Large-signal voltage amplification
A_{VD}	Differential voltage amplification

ABBV	PARAMETER
B_1	Unity gain bandwidth
B_{OM}	Maximum-output-swing bandwidth
c_i	Input capacitance
C_{ic}	Common-mode input capacitance
CMRR	Common-mode rejection ratio
GBW	Gain bandwidth product
$I_{CC-SHDN}/I_{DD-SHDN}$	Supply current (shutdown)
I_{CC}/I_{DD}	Supply current
I_I	Input current
I_{IB}	Input bias current
I_{IO}	Input offset current
I_n	Input noise current
I_O	Output current
I_{OL}	Low-level output current
I_{OS}	Short-circuit output current
k_{CMR}	Common-mode rejection ratio
k_{SVR}	Supply rejection ratio
k_{SVS}	Supply voltage sensitivity
NF	Noise figure
P_D	Total power dissipation
PSRR	Power supply rejection ratio
r_i	Input resistance
R_{id}	Differential input resistance
R_o	Output resistance
R_t	Open-loop transresistance
SR	Slew rate
T_A	Operating temperature
t_{DIS}	Turn-off time (shutdown)
t_{EN}	Turn-on time (shutdown)
THD	Total harmonic distortion
t_f	Fall time
THD+N	Total harmonic distortion plus noise
t_r	Rise time
t_s	Settling time
T_S	Storage temperature
V_{CC}/V_{DD}	Supply voltage
V_I	Input voltage range
V_{IC}	Common-mode input voltage
V_{ICR}	Input common-mode voltage range

ABBV	PARAMETER
V_{ID}	Differential input voltage
V_{IHSHDN}	Turn-on voltage (shutdown)
$V_{IL-SHDN}$	Turn-off voltage (shutdown)
V_{IO}, V_{OS}	Input offset voltage
V_n	Input noise voltage
$V_{O(PP)}$	Maximum peak-to-peak output voltage swing
V_{OH}	High-level output voltage
V_{OL}	Low-level output voltage
$V_{OM\pm}$	Maximum peak output voltage swing
X_T	Crosstalk
Z_{ic}	Common-mode input impedance
Z_o	Output impedance
Z_t	Open-loop transimpedance
Φ_D	Differential phase error
Φ_m	Phase margin

11.3 Additional Parameter Information

Depending on the application, some op amp parameters are more important than others. This section contains additional information for parameters that impact a broad range of designs.

11.3.1 Input Offset Voltage

All op amps require a small voltage between their inverting and noninverting inputs to balance mismatches due to unavoidable process variations. The required voltage is known as the input offset voltage and is abbreviated V_{IO}. V_{IO} is normally modeled as a voltage source driving the noninverting input.

Figure 11–1 shows two typical methods for measuring input offset voltage — *DUT* stands for device under test. Test circuit (a) is simple, but since Vout is not at zero volts, it does not really meet the definition of the parameter. Test circuit (b) is referred to as a *servo loop*. The action of the loop is to maintain the output of the DUT at zero volts.

Bipolar input op amps typically offer better offset parameters than JFET or CMOS input op amps.
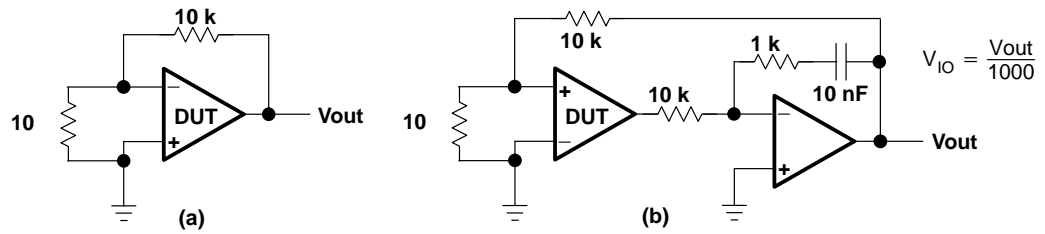
Figure 11–1. Test Circuits for Input Offset Voltage

TI data sheets show two other parameters related to V_{IO}; the average temperature coefficient of input offset voltage, and the input offset voltage long-term drift.

The average temperature coefficient of input offset voltage, αV_{IO}, specifies the expected input offset drift over temperature. Its units are $\mu V/^\circ C$. V_{IO} is measured at the temperature extremes of the part, and αV_{IO} is computed as $\Delta V_{IO}/\Delta^\circ C$.

Normal aging in semiconductors causes changes in the characteristics of devices. The input offset voltage long-term drift specifies how V_{IO} is expected to change with time. Its units are $\mu V/month$.

V_{IO} is normally attributed to the input differential pair in a voltage feedback amplifier. Different processes provide certain advantages. Bipolar input stages tend to have lower offset voltages than CMOS or JFET input stages.

Input offset voltage is of concern anytime that DC accuracy is required of the circuit. One way to null the offset is to use external null inputs on a single op amp package (Figure 11–2). A potentiometer is connected between the null inputs with the adjustable terminal connected to the negative supply through a series resistor. The input offset voltage is nulled by shorting the inputs and adjusting the potentiometer until the output is zero.
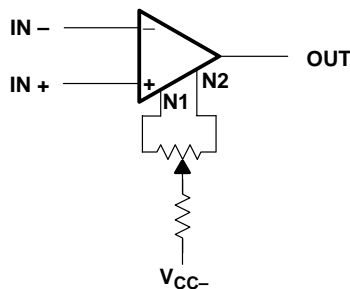
Figure 11–2. Offset Voltage Adjust

11.3.2 Input Current

The input circuitry of all op amps requires a certain amount of bias current for proper operation. The input bias current, I_{IB}, is computed as the average of the two inputs:

$$I_{IB} = \frac{\left(I_N + I_P\right)}{2} \tag{11–1}$$

CMOS and JFET inputs offer much lower input current than standard bipolar inputs. Figure 11–3 shows a typical test circuit for measuring input bias currents.

The difference between the bias currents at the inverting and noninverting inputs is called the input offset current, $I_{IO} = I_N - I_P$. Offset current is typically an order of magnitude less than bias current.

S1 Closed

$$I_P = \frac{Vout - Vref}{10^7}$$

S2 Closed

$$I_N = \frac{Vout - Vref}{10^7}$$
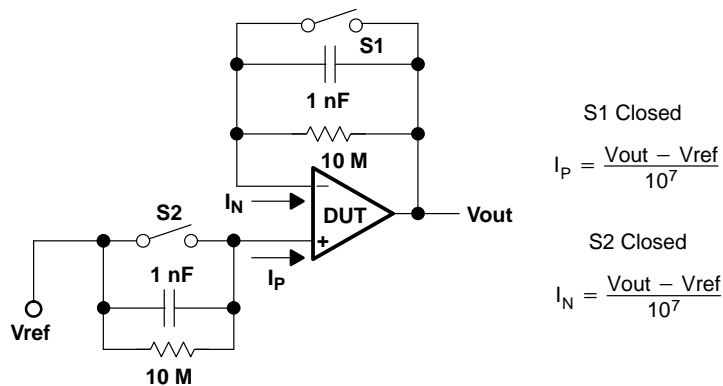
Figure 11–3. Test Circuit – I_{IB}

Input bias current is of concern when the source impedance is high. If the op amp has high input bias current, it will load the source and a lower than expected voltage is seen. The best solution is to use an op amp with either CMOS or JFET input. The source impedance can also be lowered by using a buffer stage to drive the op amp that has high input bias current.

In the case of bipolar inputs, offset current can be nullified by matching the impedance seen at the inputs. In the case of CMOS or JFET inputs, the offset current is usually not an issue and matching the impedance is not necessary.

The average temperature coefficient of input offset current, αI_{IO}, specifies the expected input offset drift over temperature. Its units are $\mu A/^\circ C$. I_{IO} is measured at the temperature extremes of the part, and αI_{IO} is computed as $\Delta I_{IO}/\Delta^\circ C$.

11.3.3 Input Common Mode Voltage Range

The input common voltage is defined as the average voltage at the inverting and noninverting input pins. If the common mode voltage gets too high or too low, the inputs will shut down and proper operation ceases. The common mode input voltage range, V_{ICR}, specifies the range over which normal operation is guaranteed.

Different input structures allow for different input common-mode voltage ranges:

The LM324 and LM358 use bipolar PNP inputs that have their collectors connected to the negative power rail. This allows the common-mode input voltage range to include the negative power rail.

The TL07X and TLE207X type BiFET op amps use P-channel JFET inputs with the sources tied to the positive power rail via a bipolar current source. This allows the common-mode input voltage range to include the positive power rail.

TI LinCMOS op amps use P-channel CMOS inputs with the substrate tied to the positive power rail. This allows the common-mode input voltage range to include the negative power rail.

Rail-to-rail input op amps use complementary N- and P-type devices in the differential inputs. When the common-mode input voltage nears either rail, at least one of the differential inputs is still active, and the common-mode input voltage range includes both power rails.

The trends toward lower, and single supply voltages make V_{ICR} of increasing concern.

Rail-to-rail input is required when a noninverting unity gain amplifier is used and the input signal ranges between both power rails. An example of this is the input of an analog-to digital-converter in a low-voltage, single-supply system.

High-side sensing circuits require operation at the positive input rail.

11.3.4 Differential Input Voltage Range

Differential input voltage range is normally specified as an absolute maximum. Exceeding the differential input voltage range can lead to breakdown and part failure.

Some devices have protection built into them, and the current into the input needs to be limited. Normally, differential input mode voltage limit is not a design issue.

11.3.5 Maximum Output Voltage Swing

The maximum output voltage, $V_{OM\pm}$, is defined as *the maximum positive or negative peak output voltage that can be obtained without wave form clipping, when quiescent DC output voltage is zero*. $V_{OM\pm}$ is limited by the output impedance of the amplifier, the saturation voltage of the output transistors, and the power supply voltages. This is shown pictorially in Figure 11–4.
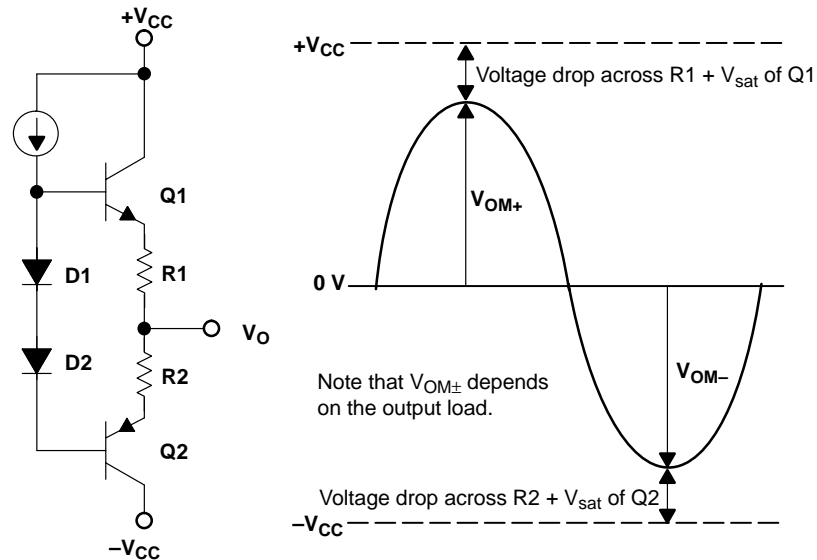

Figure 11–4. V_{OM}

This emitter follower structure cannot drive the output voltage to either rail. Rail-to-rail output op amps use a common emitter (bipolar) or common source (CMOS) output stage. With these structures, the output voltage swing is only limited by the saturation voltage (bipolar) or the on resistance (CMOS) of the output transistors, and the load being driven.

Because newer products are focused on single supply operation, more recent data sheets from Texas Instruments use the terminology V_{OH} and V_{OL} to specify the maximum and minimum output voltage.

Maximum and minimum output voltage is usually a design issue when dynamic range is lost if the op amp cannot drive to the rails. This is the case in single supply systems where the op amp is used to drive the input of an A to D converter, which is configured for full scale input voltage between ground and the positive rail.

11.3.6 Large Signal Differential Voltage Amplification

Large signal differential voltage amplification, A_{VD}, is similar to the open loop gain of the amplifier except open loop is usually measured without any load. This parameter is usually measured with an output load. Figure 11–11 shows a typical graph of A_{VD} vs. frequency.

A_{VD} is a design issue when precise gain is required. The gain equation of a noninverting amplifier:

$$\text{Gain} = \frac{1}{\beta} \times \frac{1}{1 + \dfrac{1}{A_{VD}\,\beta}} \tag{11–2}$$

β is a feedback factor, determined by the feedback resistors. The term $\dfrac{1}{A_{VD}\,\beta}$ in the equation is an error term. As long as A_{VD} is large in comparison with $\dfrac{1}{\beta}$, it will not greatly affect the gain of the circuit.

11.3.7 Input Parasitic Elements

Both inputs have parasitic impedance associated with them. Figure 11–5 shows a model of the resistance and capacitance between each input terminal and ground and between the two terminals. There is also parasitic inductance, but the effects are negligible at low frequency.

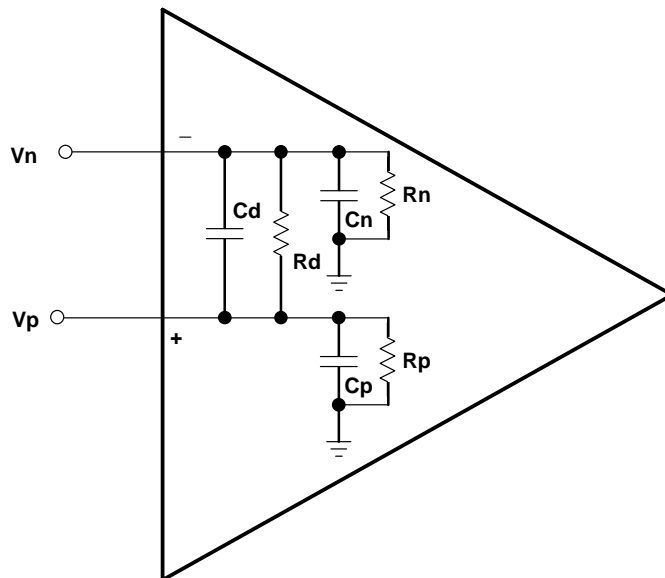Input impedance is a design issue when the source impedance is high. The input loads the source.

Figure 11–5. Input Parasitic Elements

11.3.7.1 Input Capacitance

Input capacitance, C_i, is measured between the input terminals with either input grounded. C_i is usually a few pF. In Figure 11–5, if V_p is grounded, then $C_i = C_d \| C_n$.

Sometimes common-mode input capacitance, C_{ic} is specified. In Figure 11–5, if V_p is shorted to V_n, then $C_{ic} = C_p \| C_n$. C_{ic} is the input capacitance a common mode source would see referenced to ground.

11.3.7.2 Input Resistance

Input resistance, r_i is the resistance between the input terminals with either input grounded. In Figure 11–5, if V_p is grounded, then $r_i = R_d \| R_n$. r_i ranges from $10^7\,\Omega$ to $10^{12}\,\Omega$, depending on the type of input.

Sometimes common-mode input resistance, r_{ic}, is specified. In Figure 11–5, if V_p is shorted to V_n, then $r_{ic} = R_p \| R_n$. r_{ic} is the input resistance a common mode source would see referenced to ground.

11.3.8 Output Impedance

Different data sheets list the output impedance under two different conditions. Some data sheets list *closed-loop* output impedance while others list *open-loop* output impedance, both designated by Z_o.

Z_o is defined as the small signal impedance between the output terminal and ground. Data sheet values run from 50 Ω to 200 Ω.

Common emitter (bipolar) and common source (CMOS) output stages used in rail-to-rail output op amps have higher output impedance than emitter follower output stages.

Output impedance is a design issue when using rail-to-rail output op amps to drive heavy loads. If the load is mainly resistive, the output impedance will limit how close to the rails the output can go. If the load is capacitive, the extra phase shift will erode phase margin.

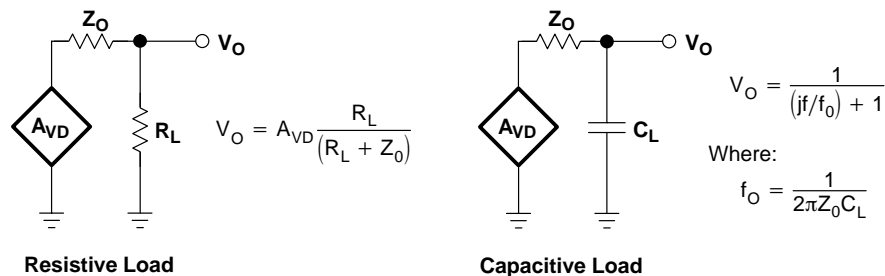Figure 11–6 shows how output impedance affects the output signal assuming Z_o is mostly resistive.

For the resistive load:
$$V_O = A_{VD}\frac{R_L}{(R_L + Z_0)}$$

For the capacitive load:
$$V_O = \frac{1}{(jf/f_0) + 1}$$

Where:
$$f_O = \frac{1}{2\pi Z_0 C_L}$$

Figure 11–6. Effect of Output Impedance

Some new audio op amps are designed to drive the load of a speaker or headphone directly. They can be an economical method of obtaining very low output impedance.

11.3.9 Common-Mode Rejection Ratio

Common-mode rejection ratio, CMRR, is defined as the ratio of the differential voltage amplification to the common-mode voltage amplification, A_{DIF}/A_{COM}. Ideally this ratio would be infinite with common mode voltages being totally rejected.

The common-mode input voltage affects the bias point of the input differential pair. Because of the inherent mismatches in the input circuitry, changing the bias point changes the offset voltage, which, in turn, changes the output voltage. The real mechanism at work is $\Delta V_{OS}/\Delta V_{COM}$.

In a Texas Instruments data sheet, CMRR = $\Delta V_{COM}/\Delta V_{OS}$, which gives a positive number in dB. CMRR, as published in the data sheet, is a dc parameter. CMRR, when graphed vs. frequency, falls off as the frequency increases.

A common source of common-mode interference voltage is 50-Hz or 60-Hz ac noise. Care must be used to ensure that the CMRR of the op amp is not degraded by other circuit components. High values of resistance make the circuit vulnerable to common mode (and other) noise pick up. It is usually possible to scale resistors down and capacitors up to preserve circuit response.

11.3.10 Supply Voltage Rejection Ratio

Supply voltage rejection ratio, k_{SVR} (AKA power supply rejection ratio, PSRR), is the ratio of power supply voltage change to output voltage change.

The power voltage affects the bias point of the input differential pair. Because of the inherent mismatches in the input circuitry, changing the bias point changes the offset voltage, which, in turn, changes the output voltage.

For a dual supply op amp, $K_{SVR} = \dfrac{\Delta V_{CC\pm}}{\Delta V_{OS}}$ or $K_{SVR} = \dfrac{\Delta V_{DD\pm}}{\Delta V_{OS}}$. The term $\Delta V_{CC\pm}$ means that the plus and minus power supplies are changed symmetrically. For a single supply op amp, $K_{SVR} = \dfrac{\Delta V_{CC}}{\Delta V_{OS}}$ or $K_{SVR} = \dfrac{\Delta V_{DD}}{\Delta V_{OS}}$.

Also note that the mechanism that produces k_{SVR} is the same as for CMRR. Therefore k_{SVR} as published in the data sheet is a dc parameter like CMRR. When k_{SVR} is graphed vs. frequency, it falls off as the frequency increases.

Switching power supplies produce noise frequencies from 50 kHz to 500 kHz and higher. k_{SVR} is almost zero at these frequencies so that noise on the power supply results in noise on the output of the op amp. Proper bypassing techniques must be used (see Chapter 17) to control high-frequency noise on the power lines.

11.3.11 Supply Current

Supply current, I_{DD}, is the quiescent current draw of the op amp(s) with no load. In a Texas Instruments data sheet, this parameter is usually the total quiescent current draw for the whole package. There are exceptions, however, such as data sheets that cover single and multiple packaged op amps of the same type. In these cases, I_{DD} is the quiescent current draw for each amplifier.

In op amps, power consumption is traded for noise and speed.

11.3.12 Slew Rate at Unity Gain

Slew rate, SR, is the rate of change in the output voltage caused by a step input. Its units are V/μs or V/ms. Figure 11–7 shows slew rate graphically. The primary factor controlling slew rate in most amps is an internal compensation capacitor C_C, which is added to make the op amp unity gain stable. Referring to Figure 11–8, voltage change in the second stage is limited by the charging and discharging of the compensation capacitor C_C. The maximum rate of change is when either side of the differential pair is conducting $2I_E$. Essentially $SR = 2I_E/C_C$. Remember, however, that not all op amps have compensation capacitors. In op amps without internal compensation capacitors, the slew rate is determined by internal op amp parasitic capacitances. Noncompensated op amps have greater bandwidth and slew rate, but the designer must ensure the stability of the circuit by other means.

In op amps, power consumption is traded for noise and speed. In order to increase slew rate, the bias currents within the op amp are increased.
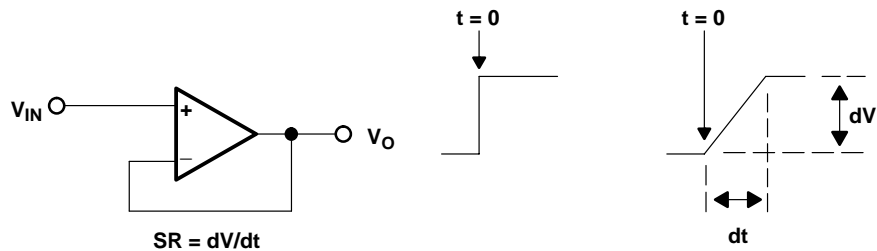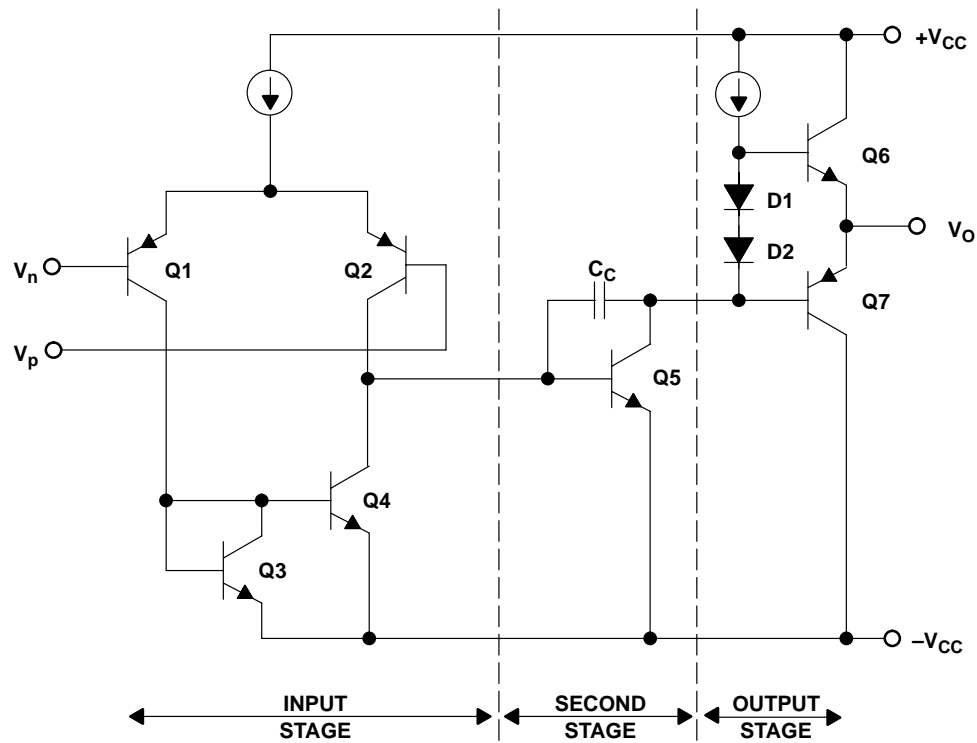

Figure 11–7. Figure 6. Slew Rate

Figure 11–8. Figure 7. Simplified Op Amp Schematic

11.3.13   Equivalent Input Noise

Noise is covered in more detail in Chapter 10.

All op amps have parasitic internal noise sources. Noise is measured at the output of an op amp, and referenced back to the input. Therefore, it is called equivalent input noise.

Equivalent input noise parameters are usually specified as voltage, V_n, (or current, I_n) per root Hertz. For audio frequency op amps, a graph is usually included to show the noise over the audio band.

11.3.13.1   *Spot Noise*

The spectral density of noise in op amps has a pink and a white noise component. Pink noise is inversely proportional to frequency and is usually only significant at low frequencies. White noise is spectrally flat. Figure 11–9 shows a typical graph of op amp equivalent input noise.

Usually spot noise is specified at two frequencies. The first frequency is usually 10 Hz where the noise exhibits a 1/f spectral density. The second frequency is typically 1 kHz

where the noise is spectrally flat. The units used are normally $\frac{nV_{rms}}{\sqrt{Hz}}$ (or $\frac{pA_{rms}}{\sqrt{Hz}}$ for current noise). In Figure 11–9 the transition between 1/f and white is denoted as the corner frequency, f_{nc}.

11.3.13.2 *Broadband Noise*

A noise parameter like $V_{N(PP)}$, is the a peak to peak voltage over a specific frequency band, typically 0.1 Hz to 1 Hz, or 0.1 Hz to 10 Hz. The units of measurement are typically nV P–P.

Given the same structure within an op amp, increasing bias currents lowers noise (and increases SR, GBW, and power dissipation).

Also the resistance seen at the input to an op amp adds noise. Balancing the input resistance on the noninverting input to that seen at the inverting input, while helping with offsets due to input bias current, adds noise to the circuit.
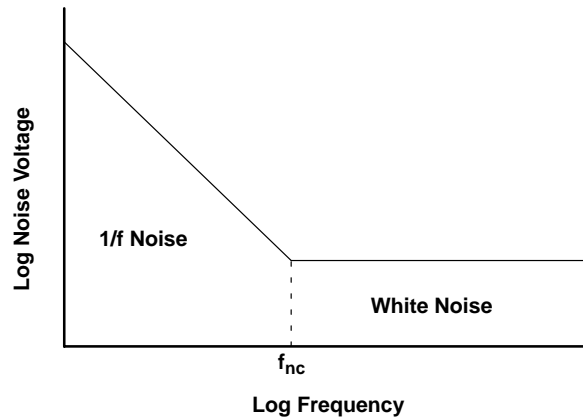

Figure 11–9. Typical Op amp Input Noise Spectrum

11.3.14 Total Harmonic Distortion Plus Noise

Total harmonic distortion plus noise, THD + N, compares the frequency content of the output signal to the frequency content of the input. Ideally, if the input signal is a pure sine wave, the output signal is a pure sine wave. Due to nonlinearity and noise sources within the op amp, the output is never pure.

THD + N is the ratio of all other frequency components to the fundamental and is usually specified as a percentage:

$$THD + N = \left[\frac{(\Sigma\ Harmonic\ voltages + Noise\ Voltages)}{Fundamental} \right] \times 100\% \qquad (11–3)$$

Figure 11–10 shows a hypothetical graph where THD + N = 1%. The fundamental is the same frequency as the input signal. Nonlinear behavior of the op amp results in harmonics

of the fundamental being produced in the output. The noise in the output is mainly due to the input noise of the op amp. All the harmonics and noise added together make up 1% of the fundamental.

Two major reasons for distortion in an op amp are the limit on output voltage swing and slew rate. Typically an op amp must be operated at or below its recommended operating conditions to realize low THD.
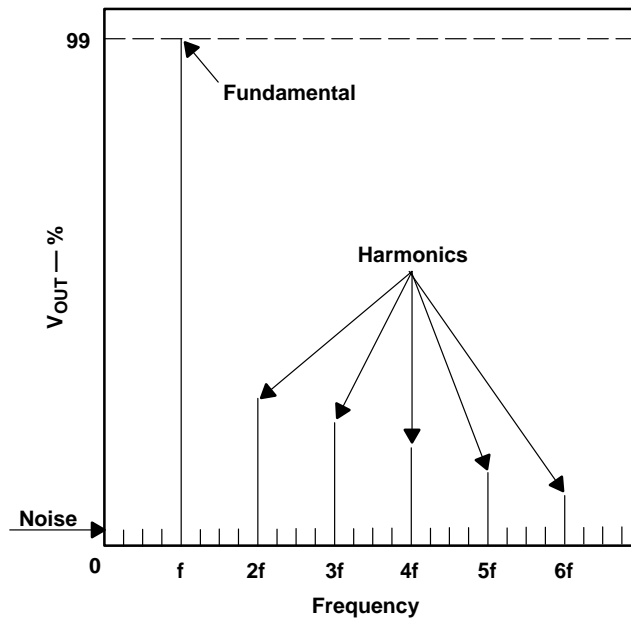

Figure 11–10.   Output Spectrum with THD + N = 1%

11.3.15   Unity Gain Bandwidth and Phase Margin

There are five parameters relating to the frequency characteristics of the op amp that are likely to be encountered in Texas Instruments data sheets. These are unity-gain bandwidth (B_1), gain bandwidth product (GBW), phase margin at unity gain (ϕ_m), gain margin (A_m), and maximum output-swing bandwidth (B_{OM}).

Unity-gain bandwidth (B_1) and gain bandwidth product (GBW) are very similar. B_1 specifies the frequency at which A_{VD} of the op amp is 1:

$$B_1 = (f)A_{VD} = 1 \tag{11–4}$$

GBW specifies the gain-bandwidth product of the op amp in an open loop configuration and the output loaded:

$$GBW = A_{VD} \times f \tag{11-5}$$

GBW is constant for voltage-feedback amplifiers. It does not have much meaning for current-feedback amplifiers because there is not a linear relationship between gain and bandwidth.

Phase margin at unity gain (ϕ_m) is the difference between the amount of phase shift a signal experiences through the op amp at unity gain and $180°$:

$$\phi_m = 180° - \phi@B1 \tag{11-6}$$

Gain margin is the difference between unity gain and the gain at $180°$ phase shift:

$$Gain\ margin = 1 - Gain\ @180° phase\ shift \tag{11-7}$$

Maximum output-swing bandwidth (B_{OM}) specifies the bandwidth over which the output is above a specified value:

$$B_{OM} = f_{MAX,}\ while\ V_O > V_{MIN} \tag{11-8}$$

The limiting factor for B_{OM} is slew rate. As the frequency gets higher and higher the output becomes slew rate limited and can not respond quickly enough to maintain the specified output voltage swing.

In order to make the op amp stable, capacitor, C_C, is purposely fabricated on chip in the second stage (Figure 11–8). This type of frequency compensation is termed dominant pole compensation. The idea is to cause the open-loop gain of the op amp to roll off to unity before the output phase shifts by $180°$. Remember that Figure 11–8 is very simplified, and there are other frequency shaping elements within a real op amp.

Figure 11–11 shows a typical gain vs. frequency plot for an internally compensated op amp as normally presented in a Texas Instruments data sheet.

As noted earlier, A_{VD} falls off with frequency. A_{VD} (and thus B_1 or GBW) is a design issue when precise gain is required of a specific frequency band.

Phase margin (ϕ_m) and gain margin (A_m) are different ways of specifying the stability of the circuit. Since rail-to-rail output op amps have higher output impedance, a significant phase shift is seen when driving capacitive loads. This extra phase shift erodes the phase margin, and for this reason most CMOS op amps with rail-to-rail outputs have limited ability to drive capacitive loads.
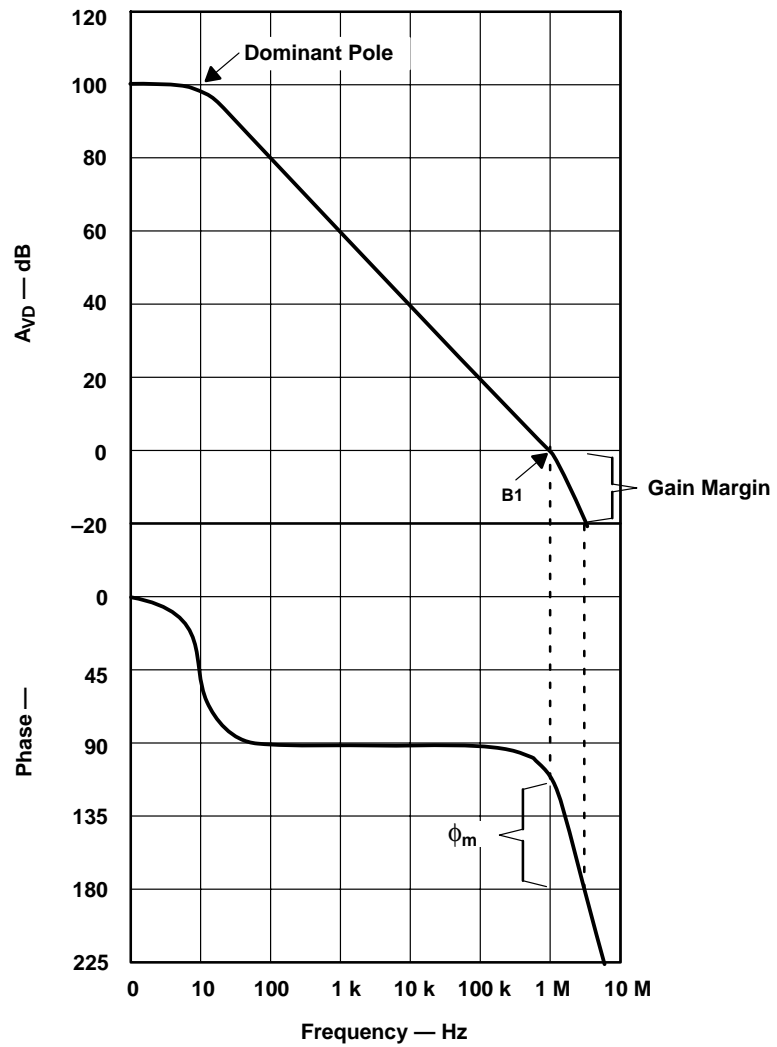
Figure 11–11. Voltage Amplification and Phase Shift vs. Frequency

11.3.16 Settling Time

It takes a finite time for a signal to propagate through the internal circuitry of an op amp. Therefore, it takes a period of time for the output to react to a step change in the input. In addition, the output normally overshoots the target value, experiences damped oscillation, and settles to a final value. Settling time, t_s, is the time required for the output voltage to settle to within a specified percentage of the final value given a step input.
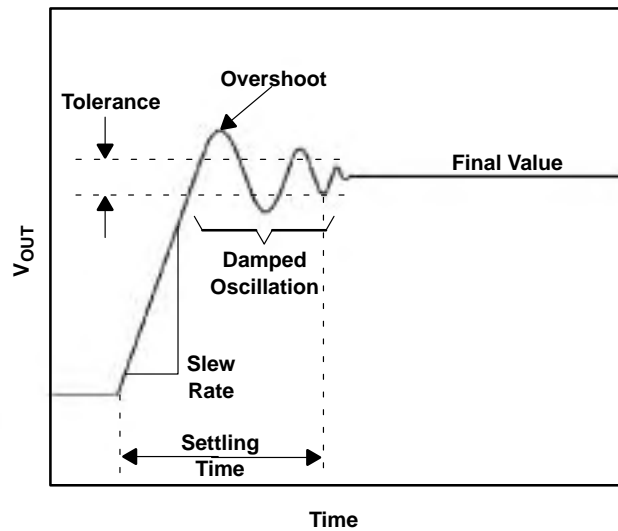
Figure 11–12 shows this graphically:

Figure 11–12.   Settling Time

Settling time is a design issue in data acquisition circuits when signals are changing rapidly. An example is when using an op amp following a multiplexer to buffer the input to an A to D converter. Step changes can occur at the input to the op amp when the multiplexer changes channels. The output of the op amp must settle to within a certain tolerance before the A to D converter samples the signal.