Working with High Impedance Op Amps

National Semiconductor
Application Note 241

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Abstract. *New developments have dramatically reduced the error currents of IC op amps, especially at high temperatures. The basic techniques used to obtain this peformance are briefly described. Some of the problems associated with working at the high impedance levels that take advantage of these low error currents are discussed along with their solutions. The areas involved are printed-circuit board leakage, cable leakage and noise generation, semiconductor-switch leakages, large-value resistors and capacitor limitations.*

introduction

A new, low cost op amp reduces dc error terms to where the amplifier may no longer be the limiting factor in many practical circuits. FET bias currents are equalled at room temperature; but unlike FETs, the bias current is relatively stable even over a −55°C to 125°C temperature range. Offset voltage and drift are low because bipolar inputs and on-wafer trimming are used. The 100 μV offset voltage and 25 pA bias current are expected to advance the state of the art for high impedance sensors and signal conditioners.

bias currents

There has been a continual effort to reduce the bias current of IC op amps ever since the μA709 was introduced in 1965. The LM101A, announced in 1968, dropped this current by an order of magnitude through improved processing that gave better transistor current gain at low operating currents. In 1969, super-gain transistors (see appendix) were applied in the LM108 to beat FET performance when temperatures above 85°C were involved.

In 1974 FETs were integrated with bipolar devices to give the first FET op amp produced in volume, the LF155. These devices were faster than general purpose bipolar op amps and had lower bias current below 70°C. But FETs exhibit higher offset voltage and drift than bipolars. Long-term stability is also about an order of magnitude worse. Typically, this drift is 100 μV/year, but a small percentage could be as bad as 1 mV. Laser trimming and other process improvements have lowered initial offset but have not eliminated the drift problem.

The new IC is an extension of super-gain bipolar techniques. As can be seen from *Figure 1*, it provides low bias currents over a −55°C to 125°C temperature range. The offset current is so low as to be lost in the noise. This level of performance has previously been unavailable for either low-cost industrial designs or high reliability military/space applications.

This low bias current has not been obtained at the expense of offset voltage or drift. Typical offset voltage is under a millivolt and provision is made for on-water trimming to get it below 100 μV. The low drift exhibited in *Figure 2* indicates that the circuit is inherently balanced for exceptionally low drift, typically 1 μV/°C below 100°C.

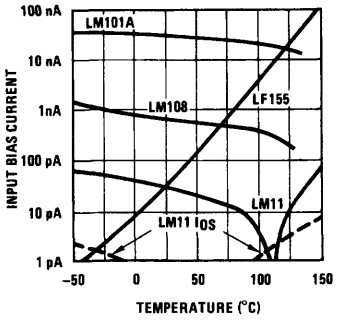

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Figure 1. Comparison of typical bias currents for various types of IC op amps. New bipolar device not only has lower bias current over practical temperature ranges but also lower drift. Offset current is unusually low with the new design.

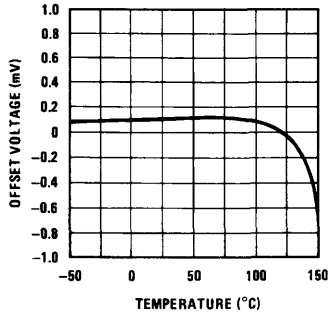

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Figure 2. Bipolar transistors have inherently low offset voltage and drift. The low drift of the LM11 over a wide temperature range shows that there are no design problems degrading performance.

the new op amp

The LM11 is, in essence, a refinement of the LM108. A modified Darlington input stage has been added to reduce bias currents. With a standard Darlington, one transistor is biased with the base current of the other. This degrades dc amplifier performance because base current is noisy, subject to wide variation and generally unpredictable.

Supplying a bleed current greater than the base current, as shown in *Figure 3*, removes this objection. The 60 nA provided is considerably in excess of the 1 nA base current. The bleed current is made to vary as absolute temperature to maintain constant impedance at the emitters of Q1 and Q2. This stabilizes frequency response and also reduces the thermal variation of bias current. Parasitic capacitances of the current generator have been bootstrapped so that the 0.3 V/μs slew rate of the basic amplifier is unaffected.

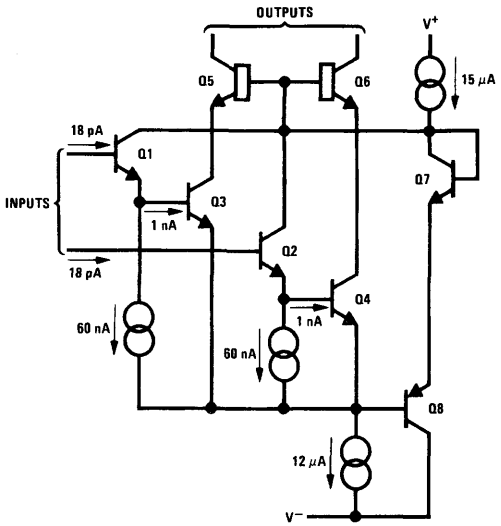

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Figure 3. Modifying Darlington with bleed current reduces offset voltage, drift and noise. Unique circuitry provides well-controlled current with minimal stray capacitance so that speed of the basic amplifier is unaffected.

Results to date suggest that the base currents of this modified Darlington input are better matched than the simple differential amplifier. In fact, offset current is so low as to be unmeasurable on production test systems. Therefore, guaranteed limits are determined by the test equipment rather than the IC.

noise

Operating transistors at very low currents does increase noise. Thus, the LM11 is about a factor of four noisier than the LM108. But the low frequency noise, plotted in *Figure 4*, is still slightly less than that of FET amplifiers. Long-term measurements indicate that the offset voltage shift is under 10 μV.

In contrast to the noise voltage, low frequency noise current is subject to greater unit-to-unit variation. Generally, it is below 1 pA, peak-to-peak, about the same magnitude as the offset current.

With the LM11, both voltage and current related dc errors have been reduced to the point where overall circuit performance could well be noise limited, particularly in limited temperature range applications.

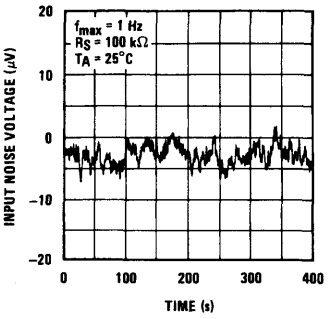

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Figure 4. Lower operating currents increase noise, but low frequency noise is still slightly lower than IC FET amplifiers. Long-term stability is much improved.

reliability

The reliability of the LM11 is not expected to be substantially different than the LM108, which has been used extensively in military and space applications. The only significant difference is the input stage. The low current nodes introduced here might possibly be a problem were they not bootstrapped, biased and guarded to be virtually unaffected by both bulk and surface leakages. This opinion is substantiated by preliminary life-test data.

This IC could, in fact, be expected to improve reliability when used to replace discrete or hybrid amplifiers that use selected components and have been trimmed and tweaked to give the required performance.

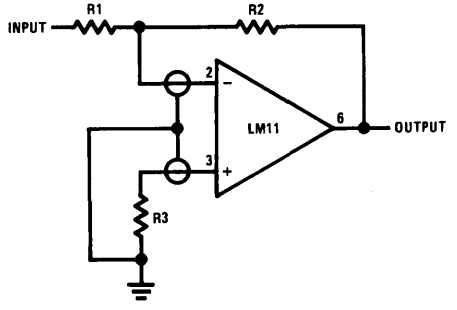
From an equipment standpoint, reliability analysis of insulating materials, surface contamination, cleaning procedures, surface coating and potting are at least as important as the IC and other components. These factors become more important as impedance levels are raised. But this should not discourage designers. If poor insulation and contamination cause a problem when impedance levels are raised by an order of magnitude, it is best found out and fixed.

Even so, it may not be advisable to take advantage of the full potential of the LM11 in all cases, especially when hostile environments are involved. For example, there should be no great difficulty in finding an LM11 with offset current less than 5 pA over a −55°C to 125°C temperature range. But anyone designing high-reliability equipment that is going to be in trouble if combined leakages are greater than 10 pA at 125°C had best know what he is about.

electrical guarding

The effects of board leakage can be minimized using an old trick known as guarding. Here the input circuitry is surrounded by a conductive trace that is connected to a low impedance point at the same potential as the inputs. The electrical connection of the guard for the basic op amp configurations is shown in *Figure 5*. The guard absorbs the leakage from other points on the board, drastically reducing that reaching the input circuitry.

To be completely effective, there should be a guard ring on both sides of the printed-circuit board. It is still recommended for single-sided boards, but what happens on the unguarded side is difficult to analyze unless Teflon inserts are used on the input leads. Further, although surface leakage can be virtually eliminated, the reduction in bulk leakage is much less. The reduction in bulk leakage for double-sided guarding is about an order of magnitude, but this depends on board thickness and the width of the guard ring. If there are bulk leakage problems, Teflon inserts on the through holes and Teflon or kel-F standoffs for terminations can be used. These two materials have excellent surface properties without surface treatment even in high-humidity environments.



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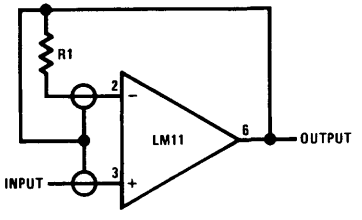
a. inverting amplifier



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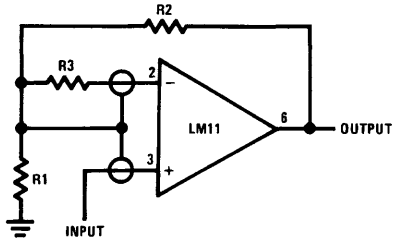
b. follower



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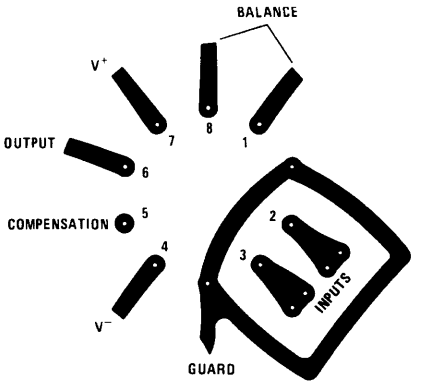
c. non-inverting amplifier

Figure 5. Input guarding for various op amp connections. The guard should be connected to a point at the same potential as the inputs with a low enough impedance to absorb board leakage without introducing excessive offset.

An example of a guarded layout for the metal-can package is shown in *Figure 6*. Ceramic and plastic dual-in-line packages are available for critical applications with guard pins adjacent to the inputs both to facilitate board layout and to reduce package leakage. These guard pins are not internally connected.



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Bottom View

Figure 6. Input guarding can drastically reduce surface leakage. Layout for metal can is shown here. Guarding both sides of board is required. Bulk leakage reduction is less and depends on guard ring width.

signal cables

It is advisable to locate high impedance amplifiers as close as possible to the signal source. But sometimes connecting lines cannot be avoided. Coaxially shielded cables with good insulation are recommended. Polyethelene or virgin (not reconstituted) Teflon is best for critical applications.

In addition to potential insulation problems, even short cable runs can reduce bandwidth unacceptably with high source resistances. These problems can be largely avoided by bootstrapping the cable shield. This is shown for the follower connection in *Figure 7*. In a way, bootstrapping is positive feedback; but instability can be avoided with a small capacitor on the input.

Cable Bootstrapping

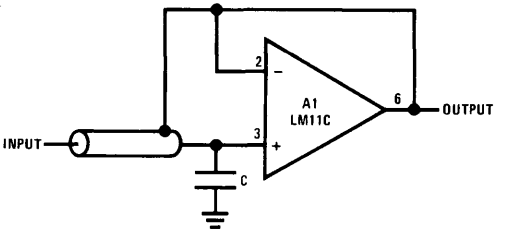

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Figure 7. Bootstrapping input shield for a follower reduces cable capacitance, leakage and spurious voltages from cable flexing. Instability can be avoided with small capacitor on input.

With the summing amplifier, the cable shield is simply grounded, with the summing node at virtual ground. A small feedback capacitor may be required to insure stability with the added cable capacitance. This is shown in *Figure 8*.

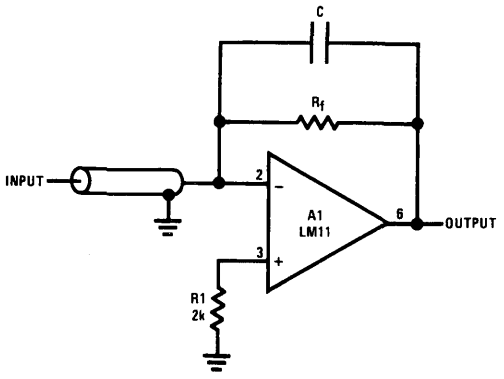

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Figure 8. With summing amplifier, summing node is at virtual ground so input shield is best grounded. Small feedback capacitor insures stability.

An inverting amplifier with gain may require a separate follower to drive the cable shield if the influence of the capacitance, between shield and ground, on the feedback network cannot be accounted for.

High impedance circuits are also prone to mechanical noise (microphonics) generated by variable stray capacitances. A capacitance variation will generate a noise voltage given by

$$e_n = \frac{\Delta C}{C} V,$$

where V is the dc bias on the capacitor. Therefore, the wiring and components connected to sensitive nodes should be mechanically rigid.

This is also a problem with flexible cables, in that bending the cable can cause a capacitance change. Bootstrapping the shield nearly eliminates dc bias on the cable, minimizing the voltage generated. Another problem is electrostatic charge created by friction. Graphite lubricated Teflon cable will reduce this.

switch leakage

Semiconductor switches with leakage currents as low as the bias current of the LM11 are not generally available when operation much above 50°C is involved. The sample-and-hold circuit in *Figure 9* shows a way around this problem. It is arranged so that switch leakage does not reach the storage capacitor.

Isolating leakage current requires that two switches be connected in series. The leakage of the first, Q1, is absorbed by R1 so that the second, Q2, only has the offset voltage of the op amp across its junctions. This can be expected to reduce leakage by at least two orders of magnitude. Adjusting the op amp offset to zero at the maximum operating temperature will give the ultimate leakage reduction, but this is not usually required with the LM11.

MOS switches with gate-protection diodes are preferred in production situations as they are less sensitive to damage from static charges in handling. If used, D1 and R2 should be included to remove bias from the protection diode during hold. This may not be required in all cases but is advised since leakage from the protection diode depends on the internal geometry of the switch, something the designer does not normally control.

A junction FET could be used for Q1 but not Q2 because there is no equivalent to the enhancement mode MOSFET. The gate of a JFET must be reverse biased to turn it off, and leakage on its output cannot be avoided.

high-value resistors

Using op amps at very high impedance levels can require unusually large resistor values. Standard precision resistors are available up to 10 MΩ. Resistors up to 1 GΩ can be obtained at a significant cost premium. Larger values are quite expensive, physically large and require careful handling to avoid contamination. Accuracy is also a problem. There are techniques for raising effective resistor values in op amp circuits. In theory, performance is degraded; in practice, this may not be the case.

With a buffer amplifier, it is sometimes desirable to put a resistor to ground on the input to keep the output under control when the signal source is disconnected. Otherwise it will saturate. Since this resistor should not load the source, very large values can be required in high-impedance circuits.

Figure 10 shows a voltage follower with a 1 GΩ input resistance built using standard resistor values. With the input disconnected, the input offset voltage is multiplied by the same factor as R2; but the added error is small because the offset voltage of the LM11 is so low. When the input is connected to a source less than 1 GΩ, this error is reduced. For an ac-coupled input, a second 10 MΩ resistor could be connected in series with the inverting input to virtually eliminate bias current error; bypassing it would give minimal noise.

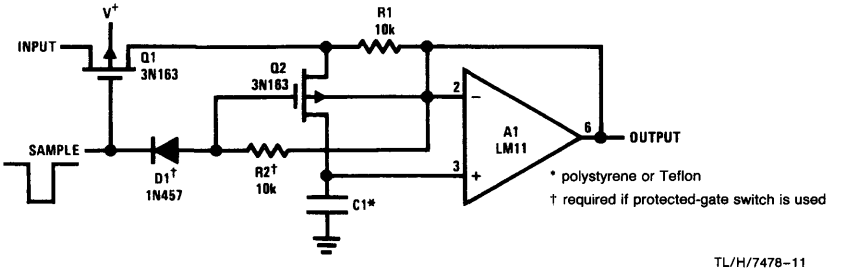

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Figure 9. Switch leakage in this sample and hold does not reach storage capacitor. If Q2 has an internal gate-protection diode, D1 and R2 must be included to remove bias from its junction during hold.

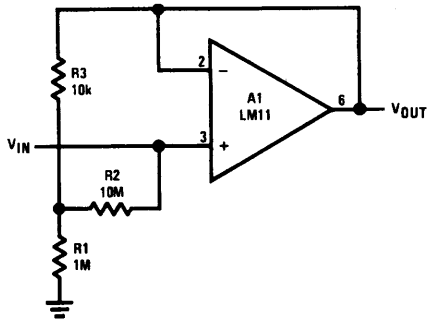

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Figure 10. Follower input resistance is 1 GΩ. With the input open, offset voltage is multiplied by 100, but the added error is not great because the op amp offset is low.

The voltage-to-current converter in *Figure 11* uses a similar method to obtain the equivalent of a 10 GΩ feedback resistor. Output offset is reduced because the error can be made dependent on offset current rather than bias current. This would not be practical with large value resistors because of cost, particularly for matched resistors, and because the summing node would be offset several hundred millivolts from ground. In *Figure 11*, this offset is limited to several millivolts. In addition, the output can be nulled with the usual balance potentiometer. Further, gain trimming is easily done.

Resistance Multiplication

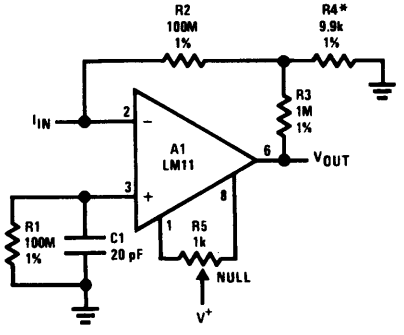

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Figure 11. Equivalent feedback resistance is 10 GΩ, but only standard resistors are used. Even though the offset voltage is multiplied by 100, output offset is actually reduced because error is dependent on offset current rather than bias current. Voltage on summing junction is less than 5 mV.

This circuit would benefit from lower offset current than can be tested and guaranteed with automatic test equipment. But there should be no problem in selecting a device for critical applications.

capacitors

Op amp circuits impose added requirements on capacitors, and this is compounded with high-impedance circuitry. Frequency shaping and charge measuring circuits require control of the capacitor tolerance, temperature drift and stability with temperature cycling. For smaller values, NPO ceramic is best while a polystyrene-polycarbonate combination gives good results for larger values over a −10°C to 85°C range.

Dielectric absorption can also be a problem. It causes a capacitor that has been quick-charged to drift back toward its previous state over many milliseconds. The effect is most noticeable in sample-and-hold circuits. Polystyrene, Teflon and NPO ceramic capacitors are most satisfactory in this regard. Choice depends mainly on capacitance and temperature range.

Insulation resistance can clearly become a problem with high-impedance circuitry. Best performer is Teflon, with polystyrene being a good substitute below 85°C. Mylar capacitors should be avoided, especially where higher temperatures are involved.

Temperature changes can also alter the terminal voltage of a capacitor. Because thermal time constants are long, this is only a problem when holding intervals are several minutes or so. The effect is reported to be as high as 10 mV/°C, but Teflon capacitors that hold it to 0.5 mV/°C are available*.

An op amp with lower bias current can ease capacitor problems, primarily by reducing size. This is obvious with a sample-and-hold because the capacitor value is determined by the hold interval and the amplifier bias current. The circuit in *Figure 12* is another example. An RC time constant of more than a quarter hour is obtained with standard component values. Even when such long time constants are not required, reducing capacitor size to where NPO ceramics can be used is a great aid in precision work.

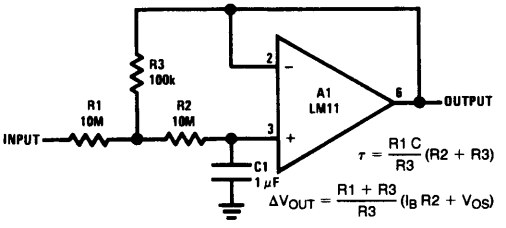

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Figure 12. This circuit multiplies RC time constant to 1000 seconds and provides low output impedance. Cost is lowered because of reduced resistor and capacitor values.

conclusions

A low cost IC op amp has been described that not only has low offset voltage but also advances the state of the art in reducing input current error, particularly at elevated temperatures. Designers of industrial as well as military/space equipment can now work more freely at high impedance levels.

Although high-impedance circuitry is more sensitive to board leakages, wiring capacitances, stray pick-up and leakage in other components, it has been shown how input guarding, bootstrapping, shielding and leakage isolation can largely eliminate these problems.

*Component Research Co., Inc., Santa Monica, California.

acknowledgment

The author would like to acknowledge the assistance of the staff at National Semiconductor in implementing this design and sorting out the application problems. Discussions with Bob Dobkin, Bob Pease, Carl Nelson and Mineo Yamatake have been most helpful.

appendix

super-gain techniques

Super-gain transistors are not new, having been developed for the LM102/LM110 voltage followers in 1967 and later used on the LM108 general-purpose op amp. They are similar to regular transistors, except that they are diffused for high current gains (2,000–10,000) at the expense of breakdown voltage. A curve-tracer display of a typical device is shown in *Figure A1*. In an IC, super-gain transistors can be made simultaneously with standard transistors by including a second, light base predeposition that is diffused less deeply.

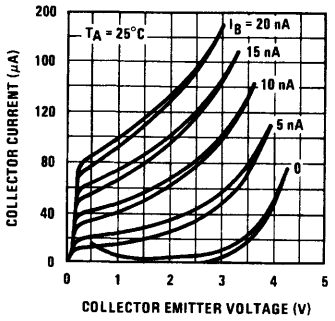

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Figure A1. curve tracer display of a super-gain transistor

Super-gain transistors can be connected in cascode with regular transistors to form a composite device with both high gain and high breakdown. The simplified schematic of the LM108 input stage in *Figure A2* shows how it is done. A common base pair, Q3 and Q4, is bootstrapped to the input transistors, Q1 and Q2, so that the latter are operated at nearly zero collector-base voltage, no matter what the input common-mode. The regular NPN transistors are distinguished by drawing them with wider base regions.

Operating the input transistors at very low collector-base voltage has the added advantage of drastically reducing collector-base leakage. In this configuration bipolar transistors are affected little by the leakage currents that limit performance of FET amplifiers.

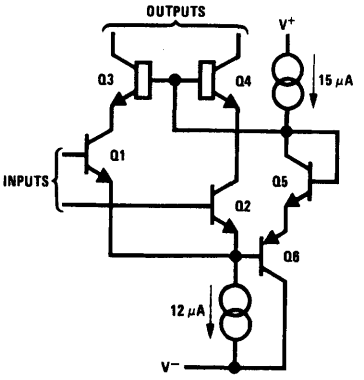

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Figure A2. A bootstrapped input stage

***See Addendum at the End of Application Note 242.**

Reducing DC Errors in Op Amps

National Semiconductor
Technical Paper 15

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Abstract. *An IC op amp design that reduces bias currents below 100 pA over a −55°C to +125°C temperature range is discussed. Super-gain bipolar transistors with on-wafer trimming are used, providing low offset voltage and drift. The key to low bias current is the control of high temperature leakage currents along with the development of reasonably accurate nanoampere current sources with low parasitic capacitance.*

introduction

A bipolar replacement for the LM108 [1] drastically reduces offset voltage, bias current and temperature drift. This design, the LM11, does not depend on new technology. Instead, the improvements result from a better understanding of transistor behavior, new circuit techniques and the application of proven offset trimming methods. Table I summarizes the results obtained. The combination of low offset voltage and low bias current is unique to IC op amps, while the performance at elevated temperatures represents an advance in the state of the art.

TABLE I. Input error terms of the LM11 show an improvement over FET op amps even at room temperature. There is little degradation in performance from −55°C to 125°C. Other important specifications are somewhat better than LM108A.

Parameter	T_J = 25°C		−55°C ≤ T_J ≤ +125°C	Units
	Typ	Max	Max	
Input Offset Voltage	0.1	0.3	0.6	mV
Input Offset Current	0.5	10	30	pA
Input Bias Current	25	50	150	pA
Offset Voltage Drift	1		3	μV/°C
Offset Current Drift	20			fA/°C
Bias Current Drift	0.5		0.5	pA/°C

junction FETs

At first glance, field effect transistors seem to be the ideal input stage for an op amp, mainly because they have a low gate current, independent of their operating current. Practically, they do provide an attractive combination of performance characteristics in a relatively simple design. But there are serious shortcomings.

For one, FETs do not match as well as bipolar devices: the offset voltage is at least an order of magnitude worse. Laser trimming can compensate for this to some extent. But with FETs, low offset voltage does not guarantee low drift, as it does with bipolars. FETs are also sensitive to mechanical strains and subject to offset shifts during assembly or with temperature cycling.

Typically, long term stability is about 100 μV/year, although this can go to 1 mV/year with no prior warning in early life. This contrasts to a 10 μV/year long term stability for bipolar pairs.

Lastly, although the input current of FETs is low at room temperature, it doubles for every 10°C increase. This, coupled with high offset voltage drift, makes FETs much less attractive as operating temperature is increased.

MOS FETs

Field effect transistors, with a metal gate and oxide insulation, give the ultimate in low input current. Practically, this advantage disappears when diodes are included to protect the gate from static charges encountered in normal handling. Further, the offset voltage problems of JFETs go double for MOS FETs. They are also subject to offset shifts due to contamination.

Interesting designs are on the horizon for various chopper-stabilized complementary MOS ICs. These solve most offset voltage problems, but not that of input leakage current. Even at moderate temperatures, this input current will seriously degrade the low offset voltage and drift even with relatively low source resistances. Chopper-stabilized amplifiers have added problems with overload recovery and noise, especially with high source impedances. These problems have limited solutions, but chopper stabilization is not usually suitable for general purpose applications.

bipolar op amps

Offset voltage, its drift or long term stability has not been a serious problem with bipolar-input op amps. Such techniques as cross-coupling or zener-zap trimming have reduced offset voltage to 25 μV in production. The real problem has been bias current. The LM108, introduced in 1968, has represented the state of the art in low bias currents for standard bipolar devices. At 3 nA, maximum over temperature, the bias current is lower than FETs above 85°C.

A Darlington version of the LM108, the LM216, provided bias currents in the 50 pA range; but this design was seriously marred by high offset voltage, drift, excessive low frequency noise and anomalous leakage currents at higher temperatures.

Improvements in this design were thwarted by the inability to provide nanoampere bleed currents to stabilize the Darlington input and the erroneous belief that uncontrollable surface states created the anomalous leakage.

a new design

With bipolar transistors, there is a tradeoff between current gain and breakdown voltage. Super-gain transistors are devices that have been diffused for maximum current gain at the expense of breakdown voltage (which is typically a couple volts for a current gain of 5000). These low voltage transistors can be operated in a cascode connection with standard transistors to give a composite device with both high gain and breakdown voltage.

Figure 1 shows a modified Darlington input stage for a super-gain op amp. Common base standard transistors (Q5 and Q6, drawn with a wider base) are bootstrapped to the super-gain input transistors so that the latter are operated at near zero collector base voltage. In addition to permitting the use of super-gain inputs, this connection also isolates the input transistors from common-mode variations, increasing common-mode rejection.

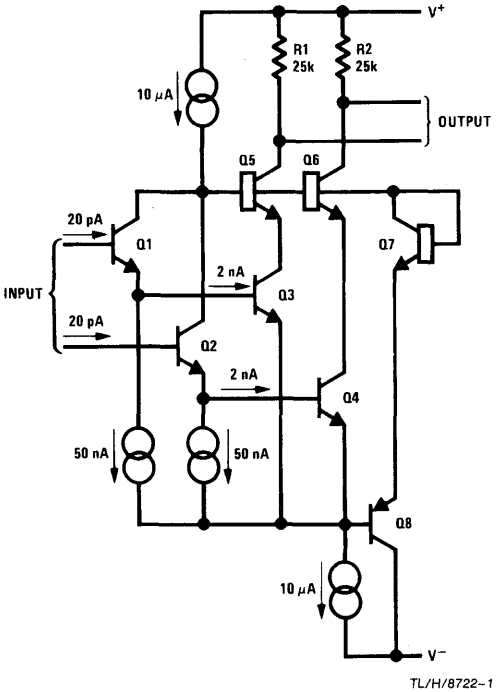

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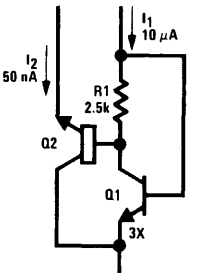
Figure 1. Bootstrapped input stage using super-gain transistors in modified-Darlington connection. The objectionable characteristics of the Darlington are virtually eliminated by operating the input transistors at a much larger current than the base current of the transistors they are driving.

The usual problems with the Darlington connection are avoided by providing a bleed current that operates the input transistors, Q1 and Q2, at a current much higher than the base current of the transistors they are driving, Q3 and Q4. This is necessary because the base currents are not that well matched, especially over temperature, and have excess low frequency noise.

a nanoampere current source

A circuit that generates the 50 nA bleed current is shown in *Figure 2*. A super-gain transistor operated in the forward mode is used to bias a standard transistor in the reverse mode. The reverse connection is used because the capacitance of an ordinary collector tub would reduce the common-mode slew rate from 2 V/μs to 0.02 V/μs.



$$I_2 = \frac{h_{fe2}A_2 I_1}{h_{fe1}A_1} \exp \frac{qI_1R_1}{kT}$$

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Figure 2. Forming a nanoampere current source with low parasitic capacitance. Design takes advantage of predictable V_{BE} difference between standard and super-gain transistors and fact that V_{BE} of a transistor is the same when operated in forward or reverse mode.

At first look, this biasing scheme would seem to be subject to a number of process variations. This is not so. For one, the V_{BE} of a transistor depends on the base Gummel number ($Q_B/\bar{\mu}_B$), the number of majority carriers per unit area divided by their effective mobility. Since the Gummel number and the effective area are unchanged when the collector and emitter are interchanged, the V_{BE} will be the same in either connection, provided that base recombination is not excessive. In standard IC transistors, reverse h_{fe} is about 30, indicating that recombination is not a significant factor. Measured reverse h_{fe} is much lower, but this is the result of a parasitic PNP that does not affect V_{BE} or α_E, the common base current gain.

The bleed current depends also on the ratio of super-gain to standard transistor h_{fe}, as indicated by the equation in *Figure 2*. Intuition suggests that super-gain h_{fe} will increase much faster than standard transistor h_{fe} with increasing emitter diffusion time, giving lower bleed current with higher super-gain h_{fe}. However, measurements with variances of standard LM108 processing indicate that the bleed current remains within 25% of design center.

As shown in *Figure 2*, higher current ratios can be obtained by increasing the area of Q1 relative to Q2 or by including R1. The equation in *Figure 2* assumes that I_1 varies as absolute temperature. If the voltage drop across R1 is equal to kT/q, changes in the V_{BE} of Q1 with small changes in I_1 will be cancelled by changes in the voltage drop across R1. This makes input bias current essentially unaffected by variations in supply or common-mode voltage as long as I_1 is reasonably well controlled.

leakage currents

The input leakage currents of bipolar op amps can be kept under control because small geometry devices are satisfactory and because the collector-base junction can be operated at an arbitrarily low voltage if bootstrapping is used.

Simple theory predicts that bulk leakage saturates for reverse biases above 2kT/q. But generation in the depletion zone dominates below 125°C. Because the depletion width varies with reverse bias, so does leakage. The characteristics of a high quality junction plotted in *Figure 3* show that leakage current can be reduced with lower bias.

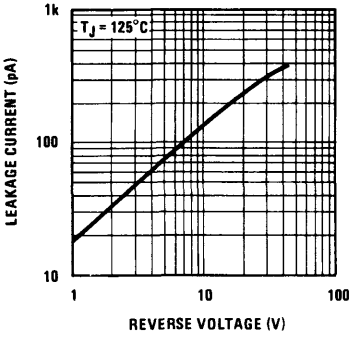

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Figure 3. Voltage sensitivity of collector base leakage indicates that generation in the depletion zone dominates even at 125°C.

When more than one junction is involved, minimum leakage is not necessarily obtained for zero bias. This is illustrated in *Figure 4*, a plot of I_{CBO} for a junction isolated NPN transistor. A parasitic PNP is formed between the base and the isolation as diagrammed in the inset. Zero leakage is obtained when V_{CB} is set so that the PNP diffusion current equals I_{CBO} of the NPN.

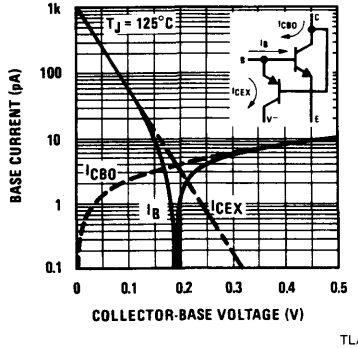

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Figure 4. Plot above explains "anomalous" leakage of NPN transistors in ICs. As collector base bias is reduced, base current reverses then increases exponentially. This excess current is the forward diffusion current of parasitic PNP to substrate (see inset).

input protection

The input clamps perform a dual function. Most important, they protect the emitter base junction of the input transistors from damage by in-circuit overloads or static charges in handling. Secondly, they limit the voltage change across junction capacitances on low current nodes under transient conditions. This minimizes recovery delays.

The clamp circuitry is shown in *Figure 5*. Emitters are added on the input transistors and cross-coupled to limit the differential input voltage. Another transistor, Q5, has been added to limit voltage on the input transistors if the inputs are driven below V^-.

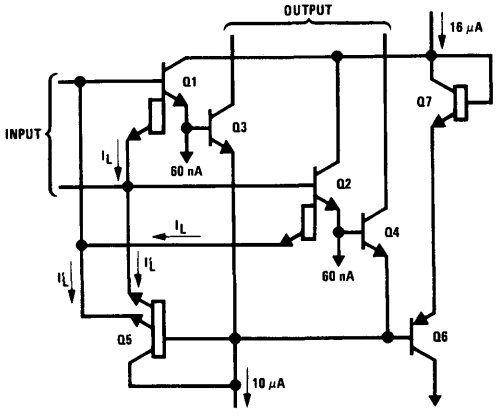

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Figure 5. Separate clamps are used for differential and common-mode overloads. Leakage currents, I_{CES} of forward and reverse connected transistors, cancel.

The differential clamp transitors do contribute to input current because $V_{CB} > 0$, so collector current is not zero for $V_{BE} \cong 0$ ($I_{CES} \cong 100$ pA at 125°C). The common-mode input clamp, Q5, is also operated at $V_{BE} = 0$ and $V_{CB} > 0$, although in the inverted mode. The resulting error is diffusion current, dependent only on the characteristic V_{BE} of the transistors. Thus, the current contributed by the differential clamp transistors is cancelled, within a couple percent, by that from the common-mode clamp.

bias current

Figure 6 shows some results of the design approach described here. A room temperature bias current of 25 pA is obtained, and this his held to 60 pA over a −55°C to 125°C temperature range. The figure also shows the results of

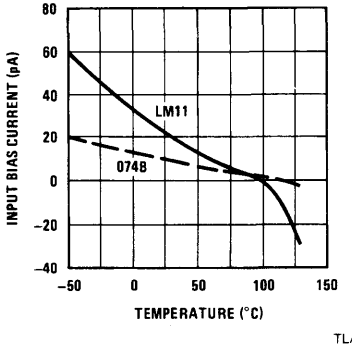

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Figure 6. Input bias current of the LM11 remains low over military temperature range. Improvements in development give even better results (074B). Offset current is usually below 1 pA.

some improvements in development that have reduced bias current to 20 pA over the full operating temperature range.

Figure 6 shows that bias current is very nearly a linear function of temperature, at least from −55°C to +100°C. This, coupled with the fact that bias current is virtually unaffected by changes in common-mode or supply voltage, suggests that bias current compensation can be provided for critical applications. An appropriate circuit is shown in *Figure 7*. Details are given in reference [2], but properly set up it should be possible to hold bias currents to less than 20 pA over a −55°C to +100°C temperature range or 5 pA over a 15°C to 55°C range with a simple room temperature adjustment.

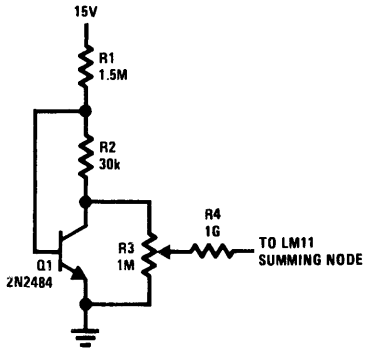

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Figure 7. Bias current of LM11 varies linearly with temperature so it can be effectively compensated with this circuit. Bias currents less than 5 pA over 15°C to 55°C range or 20 pA over −55°C to +100°C are practical.

noise

The broadband noise of a bipolar transistor is given by

$$e_n = kT\sqrt{2\Delta f/qI_C}. \quad (1)$$

Therefore, operating the input transistors at low collector current does increase noise. Because the noise of most op amps is greater than the theoretical noise voltage of the input transistors, the noise increase from low current input buffers is not as great as might be expected. In addition,

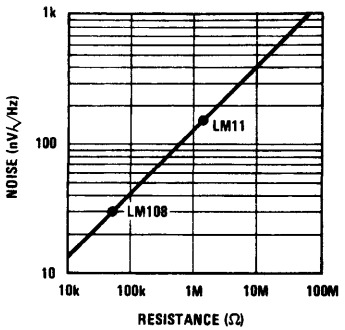

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Figure 8. Increased noise of LM11 is consequence of low collector current in input transistors. But in high impedance applications, op amp noise is masked by the thermal noise of source resistance given above.

when operating from higher source resistances, op amp noise is obscured by resistor noise, as shown in *Figure 8*.

Low frequency noise is not as easily accounted for as broadband noise, but lower operating currents increase noise in much the same fashion. The low frequency noise of the LM11, shown in *Figure 9*, is a bit less than FETs but greater than that of the LM108 when it is operated from source resistances less than 500 kΩ.

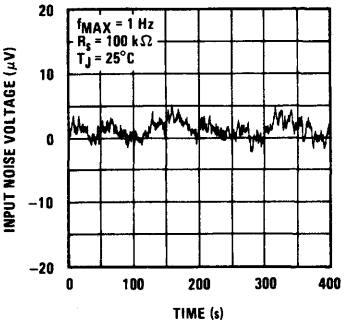

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Figure 9. Low frequency noise of LM11 is high compared to other bipolar devices but somewhat less than FETs. It is equal to LM108 operating from 500 kΩ source resistances.

complete circuit

A schematic diagram of an IC op amp using the techniques described is shown in *Figure 10*. Other than the input stage, the circuitry is much like the LM112, a compensated version of the LM108 that includes offset balancing.

One significant change has been the inclusion of wafer level trimming for offset voltage. This is done using zener-zap trimming across portions of the input stage collector load resistors, R4 and R5. This kind of zener is simply the emitter base junction of an NPN transistor. When pulsed with a large reverse current at wafer sort, the junction is destroyed by the formation of a low resistance filament between the emitter and base contact beneath the protective oxide. This shorts out a portion of the collector load resistor. The process is repeated on binary weighted segments until the offset voltage has been minimized.

Offset voltage of the LM11 is conservatively specified at 300 μV. Although low enough for most applications, offset voltage trimming is provided for fine adjustment. Balance range is determined by the resistance of the balance potentiometer, varying from ±5 mV at 100 kΩ to ±400 μV at 1 kΩ. Incidentally, when nulling offset voltages of 300 μV, the thermal matching of balance-pot resistance to the internal resistors is not a significant factor.

The actual balancing is done on the emitters of lateral PNP transistors, Q9 and Q10, that imbalance the collector loads of the input stage. This particular arrangement was used so that no damage would result from accidental connection of the balance pins to voltages outside either supply. Not obvious is that a balance pin voltage 15V more negative than V^+ can effectively short these PNP transistors with a parallel P-channel MOS transistor, forcing the output to one limit or another.

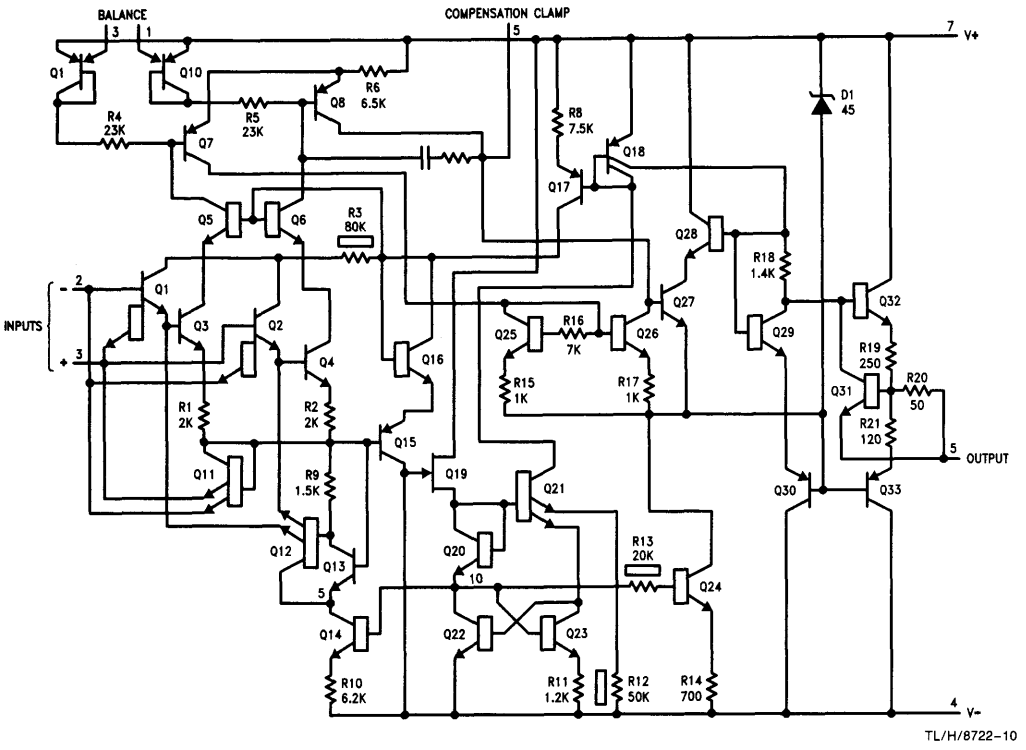

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Figure 10. Complete schematic of the LM11. Except for the input stage, circuit is much like the LM112, a compensated version of the LM108 that includes offset balancing.

Although the LM11 is specified to a lower voltage than the LM108, the minimum common-mode voltage is a diode drop further from V^- because the bleed current generator, Q12 and Q13, has been added.

Proceeding from the input stage, the second stage amplifier is a differential pair of lateral PNPs, Q7 and Q8. These feed a current mirror, Q25 and Q26, which drive a super-gain follower, Q27. The collector base voltage of Q26 is kept near zero by including Q28. The current mirror is bootstrapped to the output so that second stage gain error depends only on how well Q7 and Q8 match with changes in output voltage. This gives a gain of 120 dB in a two stage amplifier. Frequency compensation is provided by MOS capacitor C1.

The output stage is a complementary class-B design with current limiting. Biasing has been altered so that the guaranteed output current is twice the LM108. A zener diode, D1, limits output voltage swing to prevent stressing the MOS capacitor to the point of catastrophic failure in the event of gross supply transients.

The main bias current generator design (Q20–Q23) is due to Dobkin [3]. It is powered by Q19, a collector FET. The circuit is auto-compensated so that output current of Q14 and Q21 varies as absolute temperature and changes by less than 1% for a 100:1 shift in Q19 current.

speed

With a unity gain bandwidth of 500 kHz and a 0.3 V/μs slew rate the LM11 is not fast. But it is no slower than might be expected for a supply current of only 300 μA.

If the precision of the LM11 is required along with greater speed, the circuit in *Figure 11* might be used. Here, the LM11 senses input voltage and makes appropriate adjustments to the balance terminals of a fast FET amplifier. The main signal path is through the fast amplifier.

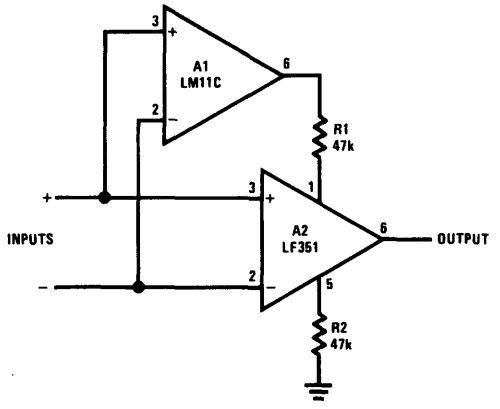

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Figure 11. The LM11 can zero offset of fast FET op amp in either inverting or non-inverting configurations. Speed is that of fast amplifier. FET amplifier can be capacitively coupled to critical input to eliminate its leakage current.

Surprisingly, this connection will work even as a voltage follower. The common-mode slew recovery of the LM11 is about 10 μs to 1 mV, even for 30V excursions. This was accomplished by minimizing or bootstrapping stray capacitances and providing clamping to limit the voltage excursion across the strays.

When bias current is an important consideration, it will be advisable to ac couple the FET op amp to the critical input. Reference [2] discusses this and other practical aspects of fast operation with the LM11.

conclusions

A new IC op amp has been described that can not only increase the performance of existing equipment but also creates new design possibilities. Op amp error has been reduced to the point where other problems can dominate. Many of the practical difficulties encountered in high impedance circuitry are discussed in reference [4] along with solutions. A number of tested designs using these techniques are given in reference [2].

The LM11 is not the result of any breakthrough in processing technology. It is simply a modification of ICs that have been in volume production for over 10 years. The improvements have resulted primarily from an understanding of strange behavior observed on the earlier ICs and taking advantage of certain inherent characteristics of bipolar transistors that were not fully appreciated.

As users of the LM11 may have discovered, the offset voltage and bias current specifications are quite conservative. It seems possible to offer 50 μV offset voltage and perhaps 1 μV/°C drift even on low cost parts. Taking full advantage of 5 pA bias current would require guarded 10-pin TO-5 packages or 14-pin DIP packages. Further, the feasibility of reducing low frequency noise to 2 μV and 0.1 pA, peak to peak, has been demonstrated on prototype parts.

acknowledgement

The author would like to acknowledge the contributions of Dennis Foltz for solving the rather formidable production test problems of the LM11.

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[2] R.J. Widlar, R. Pease and M. Yamatake, "Applying a new precision op amp", National Semiconductor AN-242, April 1980.

[3] R. Dobkin, U.S. patent no. 3930172.

[4] R.J. Widlar, "Working with high impedance op amps", National Semiconductor AN-241, February 1980.