Attenuating transients in analog FET switches

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Analog field-effect-transistor switches may be high-speed devices, but the faster they are toggled, the greater is the risk of unwanted output switching transients. The amplitude of these glitches or spikes can be greatly attentuated by synchronizing the toggling of one FET switch with a second FET switch through logic pulses that have variable rise times and fixed fall times.

Undesirable spiking can occur at the output of an analog switch during toggling because, inside the device, charge can be coupled through either its gate-source or gate-drain capacitance. Previous attempts to cancel these glitches by applying out-of-phase spikes from a second switch failed because turn-on and turn-off times generally vary too much between devices.

In the circuit shown here, TTL inverters having open-collector outputs are used to develop the synchronizing logic pulses. Since these inverters have a pull-down current that is an order of magnitude greater than their pull-up current, the rise time of their output pulses can be increased without appreciably affecting the fall time of their output pulses. Fixed resistors (R_L) establish the pull-up currents for the inverters.

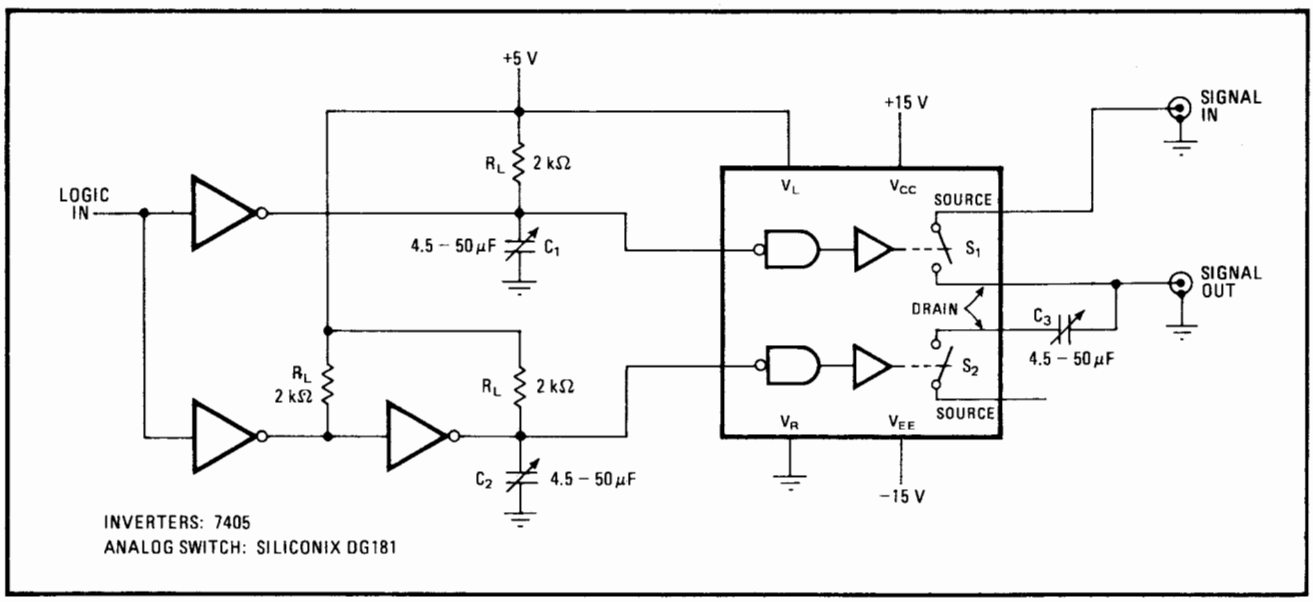
The output rise times of the inverters determine the times required to reach the toggling thresholds of analog switches S_1 and S_2. For the FET devices used here, this threshold is approximately 1.4 volts. Variable capacitors (C_1 and C_2) at the outputs of the inverters permit the rise times of these units to be set at the values needed to synchronize switches S_1 and S_2.

Now the turn-on of switch S_1 can be made to coincide with the turn-off of switch S_2, and the turn-off of S_1 can be synchronized with the turn-on of S_2. When the switches are properly matched in this way, the transients appearing at the output of S_1 can be reduced by a factor of 5 or more if R_L is greater than or equal to 10 kilohms and C_1 and C_2 are about 12 picofarads. For R_L = 75 ohms, the magnitude of the unwanted transients will at least be halved.

Transient attenuation can be improved still further by connecting a zener diode (a 6.8-v device, in this example) shunted with a bypass capacitor in series with the negative power supply. The glitches will then be reduced by an additional factor of 2 for both R_L = 75 ohms and R_L = 10 kilohms. However, the analog output voltage swing, which is normally +15 v to -7.5 v, will now be limited to +15 v and -½ v.

To adjust the circuit properly, first set capacitor C_3 at its minimum value and adjust capacitor C_1 for a minimum turn-off transient. The value of capacitor C_3 is then increased until maximum transient cancellation is obtained. Next, capacitor C_2 is adjusted for a minimum turn-on transient. Capacitors C_1 and C_2 will interact slightly with each other, and some compromise may be necessary in the adjustment of C_3 for minimum turn-on and turn-off transients.

In the circuit drawn in the figure, only one signal source is used, and switches S_1 and S_2 provide single-pole, single-throw switching action. To accommodate a second signal source and obtain single-pole, double-throw action, the drain of S_1 is connected directly (without capacitor C_3) to the drain of S_2. The second signal source is then applied to the source terminal of switch S_2. When the switches are wired in this manner, the make-before-break interval is about 30 nanoseconds. □



Squelching spikes. Switching transients at the output of an analog FET switch can be greatly attenuated by synchronizing the turn-on and turn-off of one switch with those of a second switch. Open-collector TTL inverters produce logic pulses whose output rise times can be varied while their output fall times remain fixed. The turn-on of switch S_1 is made to coincide with the turn-off of switch S_2, and vice versa.