A 100 Watt 13.8 Volt Amplifier for LF

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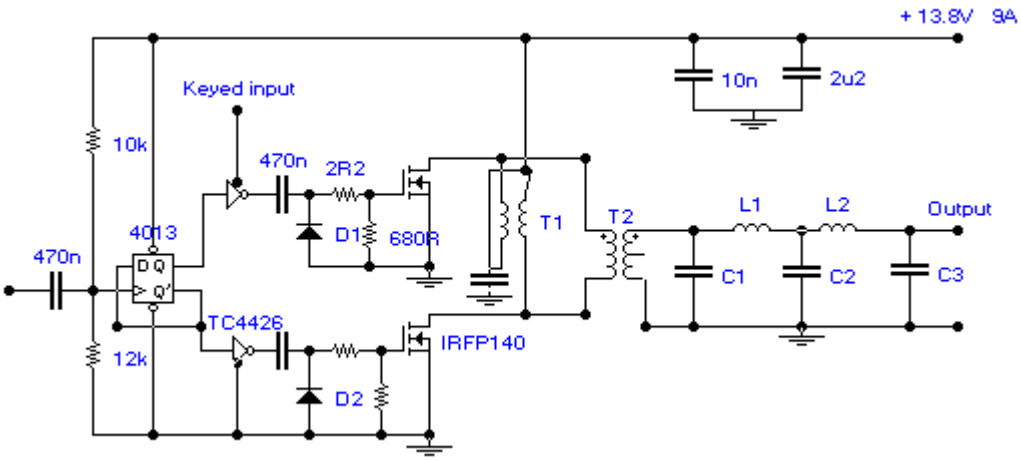
This Class D switching amplifer was designed to enable anyone with an interest in LF to get onto the band quickly and without the need to invest in a separate higher voltage power supply.

The circuit is very simple and can be built in a couple of hours "dead bug style" on a small piece of copper clad board. The circuit operates in class D and has an onboard divide by two stage. Therefore the input to the circuit from a VFO or other signal source should be at twice the required output frequency. Suitable drives could be a LC based VFO, A single crystal for fixed frequency operation, a VXO mixed to give 272kHz out, or a source based on a synthesiser or DDS.

As the input stage is a CMOS 4013 dual D-type flip flop, the input signal can be at logic levels or at a minimum of 4 Volts peak to peak

CIRCUIT DIAGRAM



Notes:

The TC4426 is a dual inverting MOSFET gate driver. Only half of the 4013 is used.
D1 and D2 are MBR150, or equivalent, Schottky diodes
T1 = 8 bifilar turns 1mm dia on 25mm 3C85 ferrite core
T2 = Primary 6 t 1mm. Secondary 21 t 0.8mm on 40mm dia 3C85 ferrite (Philips)
C1 / C3 - 10n and 2.2n polypropylene in parallel
C2 22n and 4n7 polypropylene in parallel
L1 64t 0.8mm on T-157-2. L2. As L1, or same inductance on T-130-2 core

Misc. The decoupling capacitor shown nr T1 is 470nF. Not shown for clarity are a 10uF which decouples the supply pin of the 4013 and a 220nF at the supply pin of the 4426.

CIRCUIT DESCRIPTION

The input signal is applied to a 4013 dual D-Type flip flop. For logic level inputs, DC coupling can be used. For lower signal levels the input is biased to within a volt of mid-supply to ensure reliable switching. The 4013 divides the input frequency by two and produces two anti phase square waves at the Q and /Q outputs. The two square waves are buffered by an inverting MOSFET driver chip. The outputs from the 4426 are AC coupled to the gates of the Power MOSFETs. This simple coupling technique prevents disaster in the absence of drive and ensures that both FETs remain off in the event of a fault condition. The high speed Schottky diodes are necessary to restore the DC levels at the gates which are switched between 0V and 13.8V.
The choice of FETs is important with a low supply Voltage. A pair of IRFP450s tried in the circuit only produced 50 Watts due to their higher Rds-On characteristics.

The output from the push - pull FETs is DC coupled to the output transformer T2. The turns ratio is chosen to match to 50 Ohms. To a limited extent, different numbers of turns on the output of T2 will set the output power of the amplifier. The DC supply is fed to the circuit via balanced feed choke T1. The bifilar winding on T1 helps supress the even order harmonics.

Probably the most difficult part of a class D switching amplifier is designing a suitable keying circuit.
Atempts to turn the 4013 on and off with the set direct pin caused high level key clicks. However, if the supply to the 4426 is increased slowly, the amplifier increases from zero to full power from about 4V to 6V supply. A normal PNP keying transistor cct in the 4426 supply produces a reasonable keying waveform that will please the neighbours and the local ops.

This amplifer can produce 100 W output with a supply current of just over 9 Amps. Measured efficiency (after the low pass filter) was 76%.

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