International
IOR Rectifier

IRS2093_P19

4CH Digital Audio Amplifier

Features

- 4 channel integrated analog input Class D audio amplifier drivers in a 48 pin MLQP package
- Programmable over current protection
- Programmable dead-time generation
- Versatile protection control enabling latched, non-latched, or host controlled shutdown function
- Versatile input structure for self-oscillating PWM, external clock synchronization, or natural carrier based PWM modulations
- Start and stop click noise reduction
- Under voltage protection
- High noise immunity

Product Summary

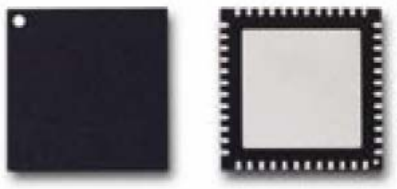
V_{OFFSET} (max)		± 100 V
Gate driver	Io+	0.5A (typ)
Gate driver	Io -	0.6A (typ)
Selectable Dead-time		45/65/85/105ns
OC protection delay		1 µsec (max)
DC offset		<20mV
PWM frequency		~800kHz
Error amplifier open loop gain		>60dB
THD+N* (1kHz, 50W, 4Ω)		0.01% (typ)
Residual Noise* (BW=20kHz)		200µVrms (typ)

* measured with recommended circuit

Description

The IRS2093 integrates four channels of high voltage, high performance Class D audio amplifier drivers with PWM modulators and protections. In conjunction with external MOSFET and external components, a complete 4 channel Class D audio amplifier can be realized. The IRS2093 is designed with floating analog inputs and protection control interface pin especially for half bridge topology. High and low side MOSFET are protected from over current conditions by a programmable bi-directional current sensing. Essential elements of PWM modulator section allow flexible system design. A small MLQP48 package enhances the benefit of smaller size of Class D topology.

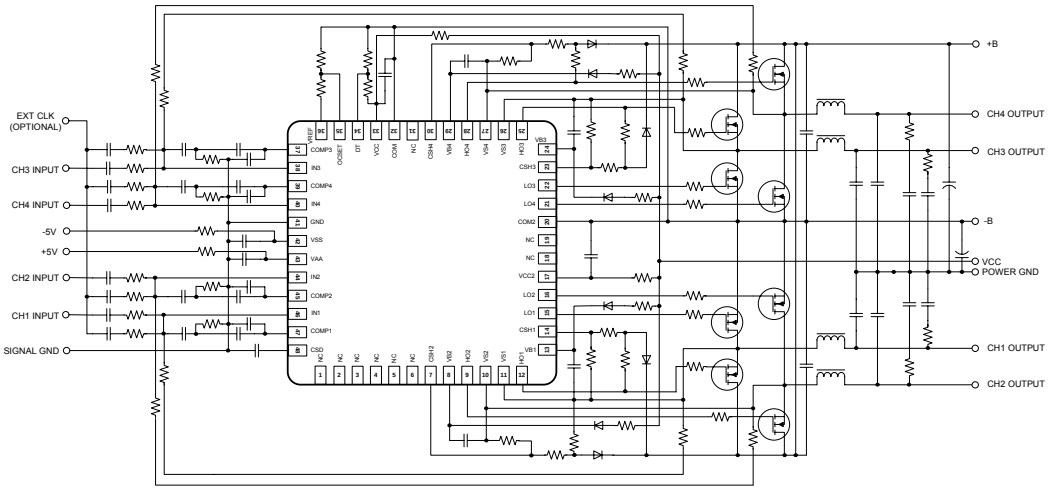
Package



MLPQ48 (7x7mm, 0.50mm pitch)

Typical Connection

(Please refer to Lead Assignments for correct pin configuration. This diagram shows electrical connections only)



Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to V_{SS}; all currents are defined positive into any lead. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply voltage	-0.3	215	V
V_S	High side floating supply voltage (Note2)	(See I_{BSZ})	V_B +0.3	V
V_{HO}	High side floating output voltage	V_S -0.3	V_B +0.3	V
V_{CSH}	CSH pin input voltage	V_S -0.3	V_B +0.3	V
V_{CC}	Low side supply voltage (Note2)	-0.3	20	V
V_{CC2}	Low side output supply voltage (Note2)	-0.3	20	V
COM2	Low side output supply return	-0.3	+0.3	V
V_{LO}	Low side output voltage	-0.3	Vcc+0.3	V
V_{AA}	Floating input positive supply voltage	(See I_{AAZ})	213	V
V_{SS}	Floating input negative supply voltage (Note1)	(See I_{SSZ})	GND +0.3	V
V_{GND}	Floating input supply ground voltage	V_{SS} -0.3	V_{AA} +0.3	V
I_{IN-}	Inverting input current	-	±3	mA
V_{CSD}	SD pin input voltage	V_{SS} -0.3	V_{AA} +0.3	V
V_{COMP}	COMP pin input voltage	V_{SS} -0.3	V_{AA} +0.3	V
V_{DT}	DT pin input voltage	-0.3	V_{CC} +0.3	V
V_{OCSET}	OCSET pin input voltage	-0.3	V_{CC} +0.3	V
I_{AAZ}	Floating input positive supply zener clamp current	-	20	mA
I_{SSZ}	Floating input negative supply zener clamp current	-	20	mA
I_{CCZ}	Low side supply V_{CC} zener clamp current (Note3)	-	5	mA
I_{CCZ2}	Low side supply V_{CC2} zener clamp current (Note3)	-	5	mA
I_{BSZ}	Floating supply zener clamp current (Note3)	-	5	mA
I_{OREF}	Reference output current	-	2	mA
dV_S/dt	Allowable Vs voltage slew rate	-	50	V/ns
dVss/dt	Allowable Vss voltage slew rate (Note3)	-	50	V/ns
dVss/dt	Allowable Vss voltage slew rate upon power-up (Note4)	-	50	V/ms
Pd	Maximum power dissipation @ $T_A \leq +25°C$	-	TBD	W
Rth_{JA}	Thermal resistance, Junction to ambient	-	TBD	°C/W
T_J	Junction Temperature	-	150	°C
T_S	Storage Temperature	-55	150	°C
T_L	Lead temperature (Soldering, 10 seconds)	-	300	°C

Note1: IN+ pin and IN- pin have two clamping diode crossing each other.
Note2: V_{DD} – IN+, IN+ -V_{SS}, Vcc-COM and VB-VS contain internal shunt zener diodes. Please note that the voltage ratings of V_S and Vcc can be limited by the clamping current.
Note3: For the rising and falling edges of step signal of 10V. Vss=15V to 200V.
Note4: Vss ramps up from 0V to 200V.

Recommended Operating Conditions

For Proper operation, the device should be used within the recommended conditions below. The Vs and COM offset ratings are tested with supplies biased at V_{AA}-V_{SS}=10V and V_B-V_S=12V.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply absolute voltage	V_S +10	V_S +17	V
V_S	High side floating supply offset voltage	Note 1	200	V
I_{AAZ}	Floating input positive supply zener clamp current	0	10	mA
I_{SSZ}	Floating input negative supply zener clamp current	0	10	mA
I_{BSZ}	Floating high side supply zener clamp current	0	10	mA
V_{AA}	Floating input supply positive supply voltage	V_{SS} +10	V_{SS} +15	V
V_{SS}	Floating input supply absolute voltage	0	100	V
V_{HO}	High side floating output voltage	Vs	V_B	V
V_{CC}	Low side fixed supply voltage	10	17	V
V_{CC2}	Low side output supply voltage	10	17	V
COM2	Low side output supply return voltage	0	-	V
V_{LO}	Low side output voltage	0	V_{CC}	V
V_{GND}	GND input voltage	V_{SS} (Note 3)	V_{AA} (Note 3)	V
V_{IN-}	Inverting input voltage	V_{GND} -0.5	V_{GND} +0.5	V
I_{IN-}	Inverting input current	-	2	mA
V_{CSD}	SD pin input voltage	V_{SS}	V_{AA}	V
V_{COMP}	COMP pin input voltage	V_{SS}	V_{AA}	V
V_{DT}	DT pin input voltage	0	V_{CC}	V
I_{OREF}	Reference output current to COM (Note 2)	0.3	0.8	mA
V_{OCSET}	OCSET pin input voltage	0.5	5	V
V_{CSH}	CSH pin input voltage	Vs	V_B	V
f_{SW}	Switching Frequency	-	800	kHz
T_A	Ambient Temperature	-40	125	°C

Note 1: Logic operational for Vs equal to –5V to +200V. Logic state held for Vs equal to –5V to –V_{BS}.
Note 2: Nominal voltage for V_{REF} is 5.1V. I_{OREF} of 0.3 – 0.8mA dictates total external resistor value on VREF to be 6.3k to 16.7k ohm.
Note 3: GND input voltage is limited by I_{AAZ} and I_{SSZ}.

Electrical Characteristics

V_{CC} ,V_{BS}= 12 V, V_{AA}=25V, V_{SS}=15V, V_{GND}=20V, C_L=1nF and T_A=25°C unless otherwise specified.

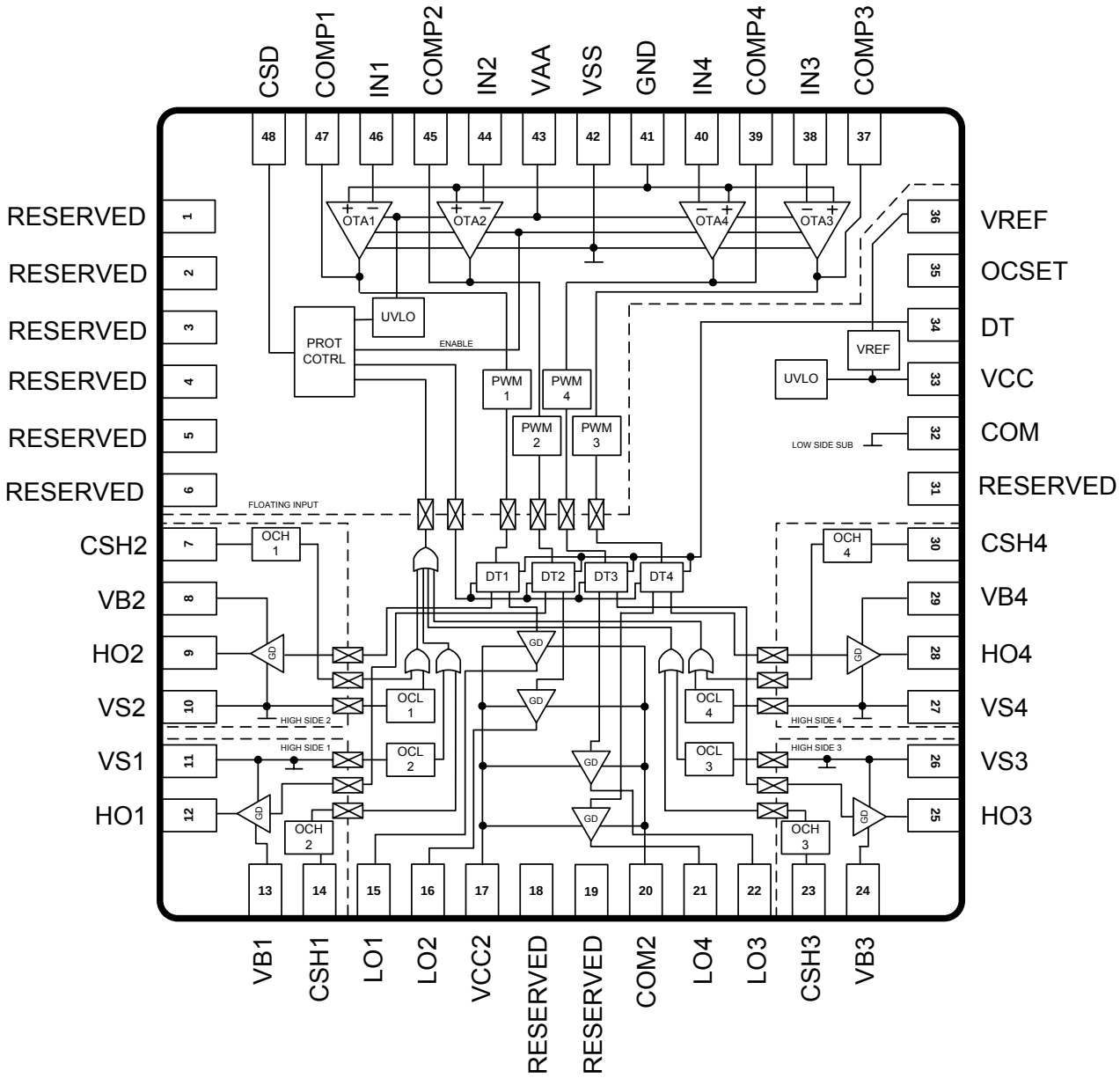
Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Low Side Supply						
UV_{CC+}	Vcc supply UVLO positive threshold	8.4	8.9	9.4	V	
UV_{CC-}	Vcc supply UVLO negative threshold	8.2	8.7	9.2	V	
UV_{CCHYS}	UV_{CC} hysteresis	-	0.2	-	V	
I_{QCC}	Low side quiescent current	-	-	tbd	mA	
V_{CLAMPL}	Low side zener diode clamp voltage	19.8	20.8	21.8	V	I_{CC}=5mA
High Side Floating Supply						
UV_{BS+}	High side well UVLO positive threshold	8.0	8.5	9.0	V	
UV_{BS-}	High side well UVLO negative threshold	7.8	8.3	8.8	V	
UV_{BSHYS}	UV_{BS} hysteresis	-	0.2	-	V	
I_{QBS}	High side quiescent current	-	-	tbd	mA	
I_{LKH}	High to Low side leakage current	-	-	50	µA	V_B=V_S =200V
V_{CLAMPH}	High side zener diode clamp voltage	14.9	15.6	16.4	V	I_{BS}=5mA
Floating Input Supply						
UV_{AA+}	VA+, VA- floating supply UVLO positive threshold	8.2	8.7	9.2	V	V_{SS} =0V
UV_{AA-}	VA+, VA- floating supply UVLO negative threshold	7.7	8.2	8.7	V	V_{SS} =0V
UV_{AAHYS}	UV_{AA} hysteresis	-	0.5	-	V	V_{SS} =0V
I_{QAA0}	Floating Input positive quiescent supply current	-	2	8	mA	V_{AA} =GND + 4.5V V_{CSD} =VSS
I_{QSS0}	Floating Input negative quiescent supply current	-	2	8	mA	V_{SS} = GND -4.5V V_{CSD} =VSS
I_{QAA1}	Floating Input positive quiescent supply current	-	24	40	mA	V_{AA} =GND + 4.5V V_{CSD} =VAA
I_{QSS1}	Floating Input negative quiescent supply current	-	24	40	mA	V_{SS} = GND -4.5V V_{CSD} =VAA
I_{QAA2}	Floating Input positive quiescent supply current	-	24	40	mA	V_{AA} =GND + 4.5V V_{CSD} =GND
I_{QSS2}	Floating Input negative quiescent supply current	-	24	40	mA	V_{SS} = GND -4.5V V_{CSD} =GND
I_{LKM}	Floating input side to Low side leakage current	-	-	50	µA	V_{A+}=V_{A-} =100V
$V_{CLAMPM+}$	Floating supply zener diode clamp voltage, positive		10.4	-	V	
$V_{CLAMPM-}$	Floating supply zener diode clamp voltage, negative	-	-10.4		V	
Audio Input						
V_{OS}	Input offset voltage	-20	0	20	mV	
I_{BIN}	Input bias current	-	-	40	nA	
BW	Small signal bandwidth	-	5	-	MHz	Ccomp=2nF, Rf=3.3k

V_{COMP}	OTA Output voltage	VAA-1		VSS+1	V	
g_m	OTA transconductance	tbd	100	-	mS	V_{IN-}=40mVpp
G_V	OTA gain	60	-	-	dB	
V_{OCM}	Common-mode output voltage range	V_{SS}+2.5	-	V_{AA}-2.5	V	
V_{OPn}	Noise voltage	-	tbd	tbd	uVrms	BW=20kHz
SR	Slew rate	-	5	-	V/us	Cload=1nF
CMRR	Common-mode rejection ratio	-	tbd	-	dB	
PSRR	Supply voltage rejection ratio	-	70	-	dB	V_{AA} =5V, V_{SS} =-5V
PWM comparator						
Vthpwm	PWM comparator threshold	-	(V_{AA} - V_{SS})/2	-	V	
f_{OTA}	Star-up local oscillation frequency	tbd	800	tbd	kHz	V_{CSD} =GND
Δfosc	Self-oscillation frequency temperature drift with respect to 25 degC	-20	-	+20	%	Tj = -40 to +125 degC, 400kHz @Tj=25 degC
Protection						
V_{REF}	Reference output voltage	4.6	5.1	5.6	V	I_{OREF} =0.5mA
Vth_{OCL}	Low side OC threshold in Vs	1.0	(1.2)	1.4	V	OCSET=1.2V, Fig.6
Vth_{OCH}	High side OC threshold in V_{CSH}	1.0+ Vs	1.2+ Vs	1.4+ Vs	V	Vs=200V,
Vth1	CSD pin shutdown release threshold	0.62xV_{AA}	0.70xV_{AA}	0.78xV_{AA}	V	V_{SS} =0V
Vth2	CSD pin self reset threshold	0.26xV_{AA}	0.30xV_{AA}	0.34xV_{AA}	V	V_{SS} =0V
I_{CSD+}	CSD pin discharge current	50	100	150	µA	V_{SD} = V_{SS} +5V
I_{CSD-}	CSD pin charge current	50	100	150	µA	V_{SD} = V_{SS} +5V
t_{SD}	Shutdown propagation delay from V_{CSD} > V_{SS} + Vth_{OCH} to Shutdown	-	0.15	0.5	µs	
t_{OCH}	Propagation delay time from V_{CSH} > Vth_{OCH} to Shutdown	-	0.4	1	µs	Fig.3
t_{OCL}	Propagation delay time from Vs> Vth_{OCL} to Shutdown	-	0.4	1	µs	Fig.4

Gate Driver (Note1)						
Io+	Output high short circuit current (Source)	0.4	0.5	-	A	Vo=0V, PW≤10µS
Io-	Output low short circuit current (Sink)	0.5	0.6	-	A	Vo=12V, PW≤10µS
V_{OL}	Low level out put voltage LO – COM, HO - VS	-	-	0.1	V	
V_{OH}	High level out put voltage VCC – LO, VB - HO	-	-	1.2	V	Io=0A
ton	High and low side turn-on propagation delay (Note2)	-	115	-	ns	V_{DT} = V_{CC} V_S = COM V_{SS} = 10V
toff	High and low side turn-off propagation delay (Note2)	-	100	-	ns	V_{DT} = V_{CC} V_S = COM V_{SS} = 10V
tr	Turn-on rise time (Note2)	-	25	-	ns	
tf	Turn-off fall time (Note2)	-	20	-	ns	
DT1	Deadtime: LO turn-off to HO	30	45	60	ns	V_{DT}>V_{DT1},

	turn-on (DT_{LO-HO}) & HO turn-off to LO turn-on (DT_{HO-LO})					V_{SS} = COM
DT2	Deadtime: LO turn-off to HO turn-on (DT_{LO-HO}) & HO turn-off to LO turn-on (DT_{HO-LO})		65		ns	V_{DT1}>V_{DT}> V_{DT2}, V_{SS} = COM
DT3	Deadtime: LO turn-off to HO turn-on (DT_{LO-HO}) & HO turn-off to LO turn-on (DT_{HO-LO})		85		ns	V_{DT2}>V_{DT}> V_{DT3}, V_{SS} = COM
DT4	Deadtime: LO turn-off to HO turn-on (DT_{LO-HO}) & HO turn-off to LO turn-on (DT_{HO-LO})V_{DT}= V_{DT4}		105		ns	V_{DT3}>V_{DT}> V_{DT4}, V_{SS} = COM
ΔDT	Dead-time temperature drift with respect to DT at 25 degC	-20	-	+20	%	Tj = -40 to +125 degC,
V_{DT1}	DT mode select threshold 2	0.51xVcc	0.57xVcc	0.63xVcc	V	
V_{DT2}	DT mode select threshold 3	0.32xVcc	0.36xVcc	0.40xVcc	V	
V_{DT3}	DT mode select threshold 4	0.21xVcc	0.23xVcc	0.25xVcc	V	

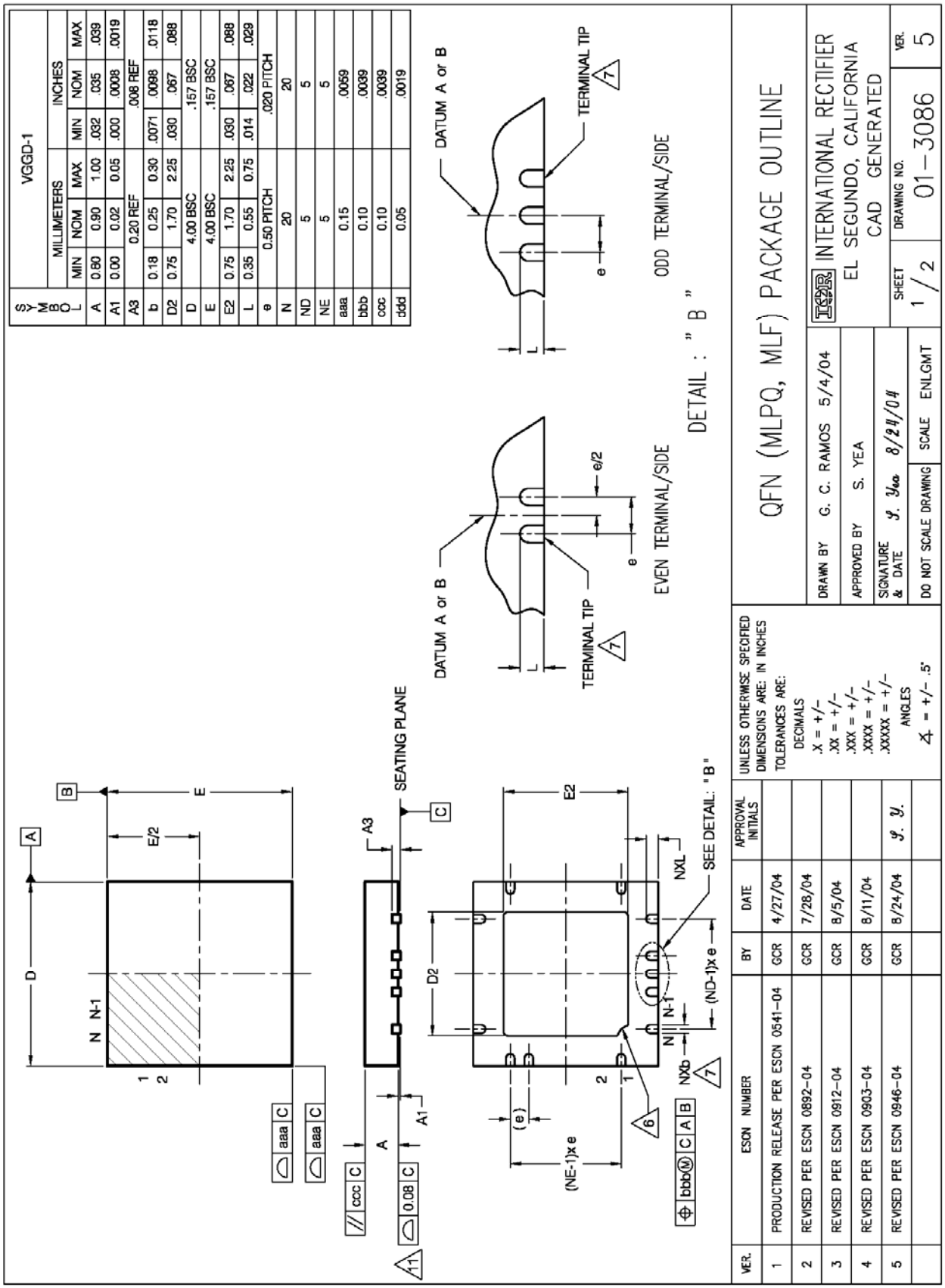
Block Diagram



Lead Definitions

Pin #	Symbol	Description
1 - 6	NC	
7	CSH2	
8	VB2	
9	HO2	
10	VS2	
11	VS1	
12	HO1	
13	VB1	
14	CSH1	
15	LO1	
16	LO2	
17	VCC2	
18, 19	NC	
20	COM2	
21	LO4	
22	LO3	
23	CSH3	
24	VB3	
25	HO3	
26	VS3	
27	VS4	
28	HO4	
29	VB4	
30	CSH4	
31	NC	
32	COM	
33	VCC	
34	DT	
35	OCSET	
36	VREF	
37	COMP3	
38	IN3	
39	COMP4	
40	IN4	
41	GND	
42	VSS	
43	VAA	
44	IN2	
45	COMP2	
46	IN1	
47	COMP1	
48	CSD	

Package Dimensions



MLPQ PACKAGES

SYMBOL	VHHC						VHHD-1						VHHD-5.1						VKKD-2					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES			MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	.032	.035	.039	0.80	0.90	1.00	.032	.035	.039	0.80	0.90	1.00	.032	.035	.039	0.80	0.90	1.00	.032	.035	.039
A1	0.00	0.02	0.05	.000	.0008	.0019	0.00	0.02	0.05	.000	.0008	.0019	0.00	0.02	0.05	.000	.0008	.0019	0.00	0.02	0.05	.000	.0008	.0019
A3	0.20 REF			.008 REF			0.20 REF			.008 REF			0.20 REF			.008 REF			0.20 REF			.008 REF		
b	0.25	0.30	0.35	.010	.012	.013	0.18	0.25	0.30	.0071	.0096	.0118	0.18	0.25	0.30	.0071	.0098	.0118	0.18	0.25	0.30	.0071	.0098	.0118
D2	1.25	2.70	3.25	.050	.106	.127	1.25	2.70	3.25	.050	.106	.127	3.30	3.45	3.55	.130	.136	.139	2.25	4.70	5.25	.089	.185	.206
D	5.00 BSC			.197 BSC			5.00 BSC			.197 BSC			5.00 BSC			.197 BSC			7.00 BSC			.276 BSC		
E	5.00 BSC			.197 BSC			5.00 BSC			.197 BSC			5.00 BSC			.197 BSC			7.00 BSC			.276 BSC		
E2	1.25	2.70	3.25	.050	.106	.127	1.25	2.70	3.25	.050	.106	.127	3.30	3.45	3.55	.130	.136	.139	2.25	4.70	5.25	.089	.185	.206
L	0.30	0.55	0.75	.012	.022	.029	0.35	0.55	0.75	.014	.022	.029	0.30	0.40	0.50	.012	.016	.019	0.30	0.40	0.50	.012	.016	.019
e	0.65 PITCH			.026 PITCH			0.50 PITCH			.020 PITCH			0.50 PITCH			.020 PITCH			0.50 PITCH			.020 PITCH		
N	20			20			28			28			32			32			48			48		
ND	5			5			7			7			8			8			12			12		
NE	5			5			7			7			8			8			12			12		
aaa	0.15			.0059			0.15			.0059			0.15			.0059			0.15			.0059		
bbb	0.10			.0039			0.10			.0039			0.10			.0039			0.10			.0039		
ccc	0.10			.0039			0.10			.0039			0.10			.0039			0.10			.0039		
ddd	0.05			.0019			0.05			.0019			0.05			.0019			0.05			.0019		

SYMBOL	VMMD					
	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	.032	.035	.039
A1	0.00	0.02	0.05	.000	.0008	.0019
A3	0.20 REF			.008 REF		
b	0.18	0.25	0.30	.007	.010	.012
D2	5.00	6.00	7.00	.197	.236	.275
D	9.00 BSC			.354 BSC		
E	9.00 BSC			.354 BSC		
E2	5.00	6.00	7.00	.197	.236	.275
L	0.35	0.40	0.45	.014	.016	.017
e	0.50 PITCH			.020 PITCH		
N	64			64		
ND	16			16		
NE	16			16		
aaa	0.15			.0059		
bbb	0.10			.0039		
ccc	0.10			.0039		
ddd	0.05			.0019		

NOTES

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. DIMENSIONS ARE SHOWN IN MILLIMETERS AND INCHES.
3. CONTROLLING DIMENSION: MILLIMETER.
4. SOURCE: JEDEC MO-220
5. N IS THE TOTAL NUMBER OF TERMINALS.

△6 TERMINAL # 1 IDENTIFIER.

△7 DIMENSION b APPLIES TO METELLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 mm AND 0.30 mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.

△8 ND AND NE TO THE NUMBER OF TERMINAL ON EACH D AND E SIDE.

9. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.

△10 FOR A COMPLETE SET OF DIMENSIONS FOR EACH VARIATION, SEE THE INDIVIDUAL VARIATION.

△11 BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

SHEET	DRAWING NO.	VER.
2 / 2	01-3086	5