AD1896 7.75:1 to 1:8, 192 kHz Stereo ASRC Evaluation Board

EVAL-AD1896EB

OVERVIEW

The AD1896 is a 24-bit, high-performance, single-chip, second generation Asynchronous Sample Rate Converter (ASRC). The AD1896 supports sample rates up to 192 kHz with 7.75:1 downsampling and 1:8 upsampling ranges while maintaining the highest performance. In normal operation, input serial data (@ input sample rate f_{S_IN}) in 3-wire serial format is sourced to the serial input port pins SCLK_I, LRCLK_I, and SDATA_I. The output serial data (@ output sample rate f_S_out) is accessed via the output serial port pins SCLK_O, LRCLK_O, and SDATA_O. The LRCLK_I and LRCLK_O signals define the input and output sample frequency, respectively. The input and output signals are typically asynchronous with respect to each other and to the master clock, MCLK_I.

The AD1896 has very flexible serial input and output data ports for glueless interconnection to audio DACs, DSPs, Digital Interface Receivers (DIR), and Digital Interface Transmitters (DIT). The AD1896 input and output serial data ports can be configured in left-justified, right-justified (16, 18, 20, and 24 bits), I^2S, or TDM mode. Top-level pins are provided for controlling the data formats and other functional modes of the AD1896 without any serial programming. Other features include bypass mode, matched phase mode, group delay selection of the digital filter, mute control, and mute flag pin for an internal error flagging. Please refer to the AD1896 data sheet for the detailed product description.

The overall setup of the evaluation board is described briefly including jumper settings. The AD1896 evaluation board uses a ±9 V to ±15 V dc source. Clean regulated 5 V and 3.3 V are generated to power the AD1896 and other on-board components. Separate 5 V supplies are used for analog and digital sections. Op amps used for the analog filtering are powered from ±15 V. Please refer to Appendix A for the block diagram, schematics, layout plots, Bill of Materials, and PLD code.

INTEGRATED CIRCUIT FUNCTIONS

AD1896 ASRC (U13)
Asynchronous Sample Rate Converter

CS8414 SPDIF Receiver (U1)
Receives the digital signal from an external source in SPDIF/AES format and recovers the data and clocks. The 3-wire signals are then sourced to the AD1896 input serial port. SPDIF receiver supports sample rates up to 96 kHz.

CS8404 SPDIF Transmitter (U6)
Encodes the AD1896 output (3-wire format) in SPDIF format. SPDIF transmitter supports sample rates up to 96 kHz.

AD1852 Stereo DAC (U12)
Stereo DAC for converting the AD1896 output into stereo analog outputs. Supports up to 192 kHz sample rates unlike SPDIF transmitter.

Input CPLD (U2)
This PLD is used to control the input serial port signals of the AD1896. In addition, it controls SPDIF receiver and other control signals of the AD1896.

Output CPLD (U3)
This PLD controls the output serial port signals of the AD1896 as well as the SPDIF transmitter and stereo DAC AD1852.

In addition to these components, there is a circuit that divides the master clock of the AD1896 by two or three, based on the master/slave clock mode and generates the on-board signals 256 f_S, EXT256 f_S, and 128 f_S (Figure 9 of the AD1896EB schematic). If the AD1896 output port is operating in $768 \times f_S$ master mode, then the master clock is divided by three; and if the AD1896 output port is operating in $512 \times f_S$ master mode, then the master clock is divided by two. The 256 f_S clock (for DAC) is divided by two to generate the 128 f_S master clock for SPDIF transmitter.

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The following section highlights key jumpers and switches on the evaluation board. Please refer to the AD1896 evaluation board schematic for more details. These switches and jumpers configure the AD1896 and other components, such as, SPDIF receiver, transmitter, and stereo DAC.

SWITCH AND JUMPER FUNCTIONS

- S1 is used to switch the mux inside the PLD (U2) between the Digital Interface Receiver (DIR), the CS8414 (U1), and the Direct Digital Input (DDI HDR3) signals. The selected signal is sourced to the input serial port of the AD1896. DIR selection works in conjunction with the Switch S2 as described below.
- S2 selects between the RCA SPDIF input (J1) and the TOSLINK optical input (U4). The selected signal is sourced to SPDIF receiver and recovered SCLK_I, LRCLK_I, and SDATA_I signals drive the input serial port of the AD1896.
- S3 is used to select the different input interface format of the AD1896 input serial data. Total of six input serial modes are possible: LJ, I^2S, RJ-24, RJ-20, RJ-18, and RJ-16. Refer to the Digital Audio Input Signals section for the configuration Table IV. Note that the input logic PLD (U2) reads the S3 selection and controls the AD1896 and SPDIF receiver CS8414 accordingly.
- S4 selects the master/slave mode of the input and output serial ports of the AD1896. Refer to Table II for the mode selection settings. In the slave operation, the corresponding SCLK and LRCLK signals are externally provided by the target system. In the master mode, these two signals are internally generated from the MCLK_I signal at $768 \times f_S$, $512 \times f_S$, or $256 \times f_S$ rate. *In MASTER MODE operation, maximum sample rate for MASTER PORT is limited to 96 kHz.*
- S5 resets the AD1896 and other components.
- S6 activates the BYPASS function of the AD1896 where the input serial data is bypassed to the output serial port without any signal processing.
- S7 is used to MUTE the AD1896 output serial data as well as the AD1852 stereo DAC.
- S8 selects between SHORT or LONG group delay for the AD1896.
- JP1 jumper is used to select output interface format and word width of the AD1896 output serial data. Refer to the Digital Audio Output Signals section for configuration Tables V and VI. Again, the output logic PLD (U3) decodes the JP1 signals and configures the AD1852 DAC and CS8404 SPDIF transmitter to match the output data format of the AD1896.
- JP2 selects the internal interpolation ratio of the AD1852 stereo DAC (U12). Based on the sample rate, 8×, 4×, or 2× interpolation could be selected. DAC should be configured in 8×, 4×, or 2×… mode for 48 kHz, 96 kHz, or 192 kHz sample rates, respectively.
- JP3 enables the *autoMUTE* feature where the AD1896 MUTE_IN will be asserted if the MUTE_OUT output from AD1896 is set high. The MUTE_OUT is set high when sample rate of LRCLK_I and LRCLK_O changes.
- JP4 jumper selects between an on-board clock oscillator (12.288 MHz) and on-board third order overtone crystal oscillator (33.8688 MHz) for master clock (MCLK_I) of the AD1896. Please refer to Table IX for the maximum allowable sample rates for $76 \times f_S$, $512 \times f_S$, and $256 \times f_S$ master mode with 33.8688 MHz master clock. *The on-board clock oscillator (12.288 MHz) is enabled only for the SLAVE mode operation of the AD1896 (Switch S4 position 7).*
- 10-pin header HDR1(TDM_IN) is used to input the TDM_IN data from the SHARC® DSP board.
- 10-pin header HDR2 (TDM_OUT) is used to receive the TDM_OUT data from the AD1896 to SHARC DSP board.
- 10-pin header HDR3 (DDI) is used to drive the input serial port signals SCLK_I, LRCLK_I, and SDATA_I in 3-wire format from an external source.
- 10-pin header HDR5 (DDO) is used to drive the output serial port signals SCLK_O, LRCLK_O and SDATA_O in 3-wire format from an external source.

LEDS

- DS1 (VERF) is illuminated when Validity+Error flag output on SPDIF receiver CS8414 goes high, indicating problems with SPDIF receiver or missing audio signal to the SPDIF receiver.
- DS2 (PREEMP) indicates the pre-emphasized data to the SPDIF receiver.
- DS3 (3.3 V) is illuminated when 3.3 V dc supply is present to power up the VDD_CORE of the AD1896.
- DS4 (AVDD = 5 V) is illuminated when analog supply to the stereo DAC AD1852 is present.
- DS5 (RIGHT channel) and DS6 (LEFT channel) DAC ZERO STATUS LEDs are illuminated when no input signal is present to the stereo DAC AD1852 (U12).
- DS7 (AUDIO) is illuminated when the SPDIF receiver CS8414 is receiving audio data.

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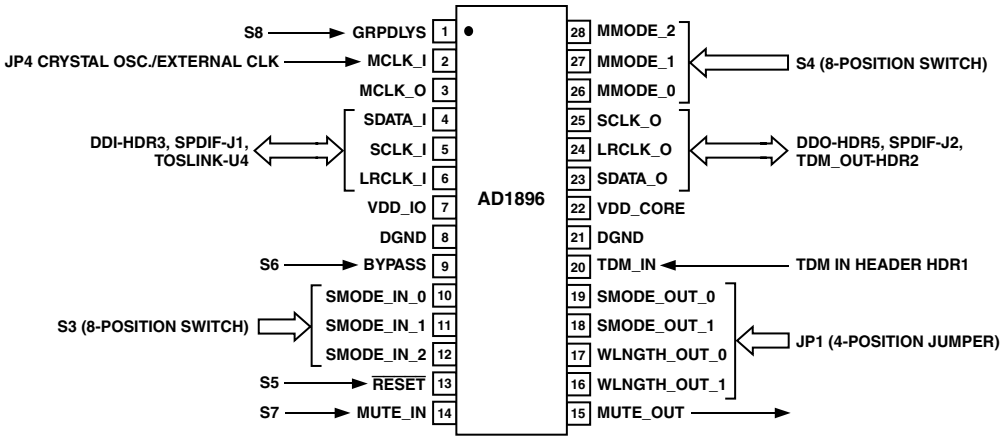


Figure 1. Key Jumpers and Switches on the Evaluation Board

Table I. Pinout Table for 10-Pin Header Connectors

Pin	HDR1 (TDM_IN)	HDR2 (TDM_OUT)	HDR3 (DDI)	HDR5 (DDO)
1	5 V (O)	5 V (O)	5 V (O)	5 V (O)
3	TDM_I (I)	SDATA_O (O)	SDATA_I (I)	SDATA_O (O)
5	SCLK_O (I/O)	SCLK_O (I/O)	LRCLK_I (I/O)	SCLK_O (I/O)
7	LRCLK_O (I/O)	LRCLK_O (I/O)	SCLK_I (I/O)	LRCLK_O (I/O)
2, 4, 6, 8, 10	GND	GND	GND	GND

DIGITAL AUDIO INPUT SIGNALS

Input serial port of the AD1896 can be driven in various ways using this evaluation board.

1. RCA phone jack (J1) or TOSLINK (U4) optical connector can be used to input the AES/EBU or SPDIF signal to the SPDIF receiver CS8414 (U1). SPDIF receiver generated SCLK_I, LRCLK_I, and SDATA_I signals drive the input serial port of the AD1896. *SPDIF input is supported only when the AD1896 serial input port is in SLAVE mode (Switch S4 position 3 to 7) and supports all input serial data formats except RJ-24 bit and RJ-20 bit (Switch S3 positions 2,* 3). The SPDIF receiver limits input sample rates to 96 kHz.
2. Alternatively, an external data header (HDR3) can be used to directly source all three signals SCLK_I, LRCLK_I, and SDATA_I from an external source. Unlike SPDIF receiver, input sample rate up to 192 kHz is possible (input port in slave mode) and set by an external source. All input serial data formats and master/slave clock modes are supported.

SCLK_I and LRCLK_I signals of the input serial port are bidirectional signals. Logic levels on pins MMODE_ [2:0] control the direction of these signals. When the input serial port is in master mode, these signals are generated by the AD1896; whereas, in the slave mode these signals are provided by an external source. MMODE_[2:0] pins are set by the 8-position Switch S4. Tables II and III show the master/slave clock mode corresponding to each switch position.

Input data format, such as, I^2S, LJ, or RJ is set by the logic levels on SMODE_IN_[2:0] pins as shown in Table IV. Set the 8-position Switch S3 on the evaluation board for the proper input data format.

Table II. Input and Output Serial Port Modes

S4 Switch Position	MMODE_[2:0] 2	1	0	Master/Slave Modes
7	0	0	0	Both Serial Ports are in Slave Mode
6	0	0	1	*Output Serial Port is Master with 768 × f_{S_OUT}
5	0	1	0	*Output Serial Port is Master with 512 × f_{S_OUT}
4	0	1	1	*Output Serial Port is Master with 256 × f_{S_OUT}
3	1	0	0	Matched Phase Mode
2	1	0	1	*Input Serial Port is Master with 768 × f_{S_IN}
1	1	1	0	*Input Serial Port is Master with 512 × f_{S_IN}
0	1	1	1	*Input Serial Port is Master with 256 × f_{S_IN}

*In MASTER MODE operation, maximum sample rate for Master Port is limited to 96 kHz.

Table III. Master/Slave Mode Configuration

Switch SW4	f_{S_IN}	f_{S_OUT}	Input Header (HDR3) SCLK_I	LRCLK_I	Output Header (HDR5) SCLK_O	LRCLK_O	MCLK_I [MHz]	Jumper JP4 Short
0	132.3 kHz	Set Externally	Output	Output	Input	Input	33.8688	2-3
1	66.15 kHz	Set Externally	Output	Output	Input	Input	33.8688	2-3
2	44.1 kHz	Set Externally	Output	Output	Input	Input	33.8688	2-3
3	Not Used	Not Used	Input	Input	Input	Input	33.8688	2-3
4	Set Externally	132.3 kHz	Input	Input	Output	Output	33.8688	2-3
5	Set Externally	66.15 kHz	Input	Input	Output	Output	33.8688	2-3
6	Set Externally	44.1 kHz	Input	Input	Output	Output	33.8688	2-3
7	Set Externally	Set Externally	Input	Input	Input	Input	33.8688	2-3

Table IV. Input Interface Formats

S3 Switch Position	SMODE_IN_[2:0] 2	1	0	Input Interface Format
0	0	0	0	Left Justified
1	0	0	1	I^2S
2	1	1	1	Right Justified, 24 Bits
3	1	1	0	Right Justified, 20 Bits
4	1	0	1	Right Justified, 18 Bits
5	1	0	0	Right Justified, 16 Bits
6	0	1	0	Not Used
7	0	1	1	Not Used

DIGITAL AUDIO OUTPUT SIGNALS

Similar to the input serial port, output serial data (SDATA_O, SCLK_O, and LRCLK_O signals) can be accessed in three different ways using this evaluation board.

1. Refer to Figure 8. Direct digital output header (HDR5) or, alternatively, TDM_OUT header (HDR2) can be used to monitor the output serial data of the AD1896 (SDATA_O signal) in the digital form. HDR5 provides LRCLK_O, SCLK_O, and SDATA_O in 3-wire interface format; whereas, HDR2 should be used in TDM mode to interface the TDM output data to the SHARC DSP board.
2. SPDIF output through connector J2, which is generated by the SPDIF transmitter CS8404. In this case, SCLK_O, LRCLK_O, and SDATA_O from AD1896 are encoded in the SPDIF signal. Similar to the SPDIF receiver, the output sample rates above 96 kHz are not possible due to the transmitter functionality. *Note that SPDIF output is supported only for the output port in 768 × f_{S_OUT}, 512 × f_{S_OUT}, and 256 × f_{S_OUT} master mode (Switch S4 positions 4, 5, 6).*
3. RCA jack J6 and J7 provide stereo LEFT and RIGHT analog output signals from AD1852 DAC. Refer to Figure 10. Interpolation ratio of the DAC needs to be set based on the sample rate and set by jumper JP2. *DAC analog output is supported only when the AD1896 output port is configured in 768 × f_{S_OUT}, 512 × f_{S_OUT}, and 256 × f_{S_OUT} master mode (Switch S4 positions 4, 5, 6).*

SCLK_O and LRCLK_O signals of output serial port are bidirectional signals. Logic levels on pins MMODE_ [2:0] control the direction of these signals. Please refer to Table II for the switch position S4 setting to control the Master/Slave mode of the output serial port. The output interface mode, such as I^2S, LJ, RJ, and TDM mode, is set by the pins SMODE_OUT_[2:0]. Also, the output port has two more pins WLNGTH_OUT_[1:0] to set the output word width to 24, 20, 18, or 16 bits. The logic levels on SMODE_OUT_ [1:0] and WLNGTH_OUT_ [1:0] pins allow different serial output data formats. As shown in Tables V and VI, set the jumpers one and two of JP1 for the word width and three and four of JP1 for the output data format.

Table V. Output Interface Formats

JP1[4:3]	SMODE_OUT_[1:0] 1	0	Interface Format
00	0	0	Left-Justified (LJ)
01	0	1	I^2S
10	1	0	TDM Mode
11	1	1	Right-Justified (RJ)

Table VI. Output Signal Word Width

JP1[2:1]	WLNGTH_OUT_[1:0] 1	0	Word
00	0	0	24 Bits
01	0	1	20 Bits
10	1	0	18 Bits
11	1	1	16 Bits

DEFAULT CONFIGURATION

The default configuration of this evaluation board is highlighted in Tables VII and VIII. The AD1896 is configured in 24-bit input and output data format, with input serial ports in slave mode and output serial port in (768 × f_S) master mode. In this configuration, input serial port needs to be driven by an external system, such as, Audio Precision, for the slave mode operation. An on-board third overtone crystal oscillator at 33.8688 MHz clocks the AD1896. Since the output serial port is configured in 768 × f_S master mode and the AD1896 is clocked by 33.8688 MHz clock, the output sample rate will be 44.1 kHz for this configuration. The maximum input sample rate for this case can be up to 192 kHz based on the requirement that the AD1896 master clock must be higher than 138 times the maximum input or output sample rate. The AD1896 can be clocked by secondary on-board clock oscillator (U15) by first inserting the desired clock oscillator in socket U15 and then switching the clock source selection from on-board crystal to clock oscillator (U15) by jumper JP4; *however, clock oscillator is enabled for SLAVE mode only (Switch S3 position 7)*. The evaluation board contains 12.288 MHz (U15) clock oscillator. The operating and quiescent currents for the ±12 V dc supplies are listed below.

+12 V Quiescent Current	~250 mA
–12 V Quiescent Current	~5 mA
+12 V Normal Operation Current	~300 mA–360 mA
–12 V Normal Operation Current	~5 mA

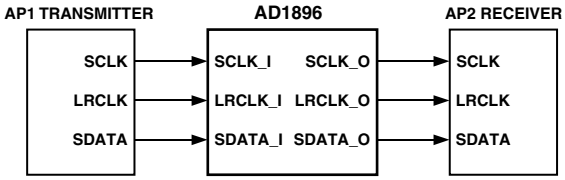


Figure 2. Input and Output Serial Port Direction in Default Configuration

Table VII. Default Jumper/Switch Settings

Input Mode (S3)	Output Mode (JP1)	Master/Slave Mode (S4)	DAC Interpolation Ratio Select (JP2)	Clock Source (JP4)	Group Delay (S8)	Bypass Mode (S6)	Mute (S7)
Position 0	Position 1, 2, 3, 4 Shorted	Position 6	Position 1, 2 Shorted	Position 2, 3 Shorted	Pushed Up	Pushed Down	Pushed Down
LJ-24 Bits	LJ-24 Bits	Output Port Master, 768 f_{S_OUT}	48 kHz Sample Rate	33.8688 MHz Crystal Oscillator	Short	Off	Off

Table VIII. Default Evaluation Board Configuration

Input Mode (S3)		Output Mode (JP1)		Master/Slave Mode (S4)		Input Source (HDR3, HDR1, J1, U4)		Output Source (HDR2, HDR5, J2)		DAC Interpolation Ratio Select (JP2)		Clock Source (JP4)	
LJ	X	LJ-24	X	Both Ports in SLAVE Mode		DIRECT INPUT	X	SPDIF		96/$\overline{48}$	X	On-Board 33.8688 MHz Crystal	X
I^2S		I^2S-24		O_MAS_768	X	TDM_IN		DIRECT OUTPUT	X	192/$\overline{48}$	X	External 256 × f_S Clock	
RJ-24		RJ-24		O_MAS_512		SPDIF		TDM_OUT					
RJ-20		RJ-20		O_MAS_256		TOSLINK							
RJ-18		RJ-18		MATCHED PHASE		**Group Delay (S8)**		**Bypass Mode (S6)**		**Automute Enable (JP3)**		**Mute (S7)**	
RJ-16		RJ-16		I_MAS_768		Short	X	Enable		Enable	X	Enable	
		TDM		I_MAS_512		Long		Disable	X	Disable		Disable	X
				I_MAS_256									

DEFAULT SETUP

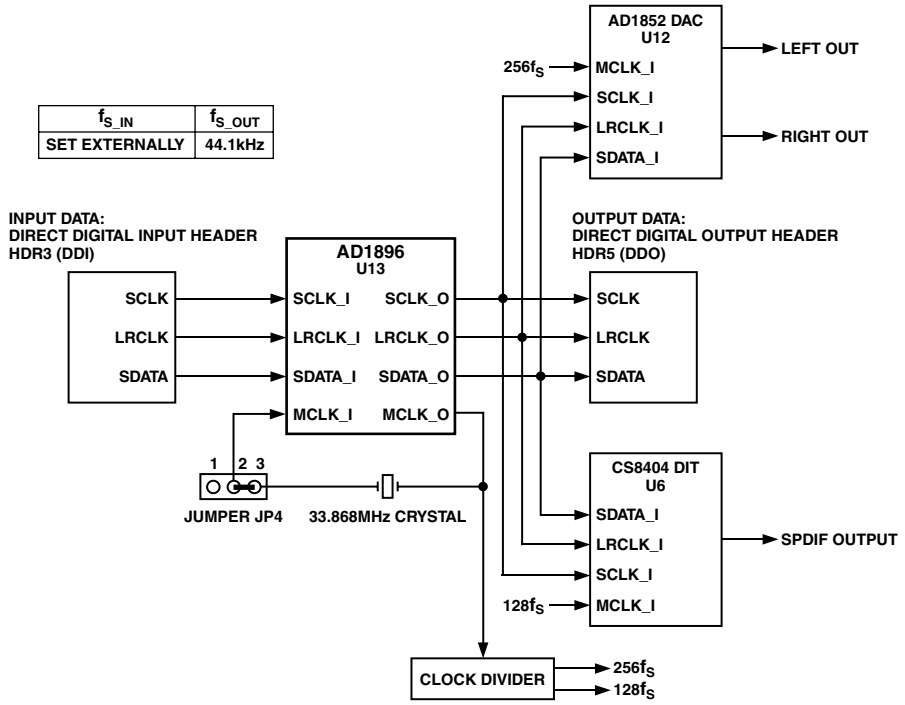


Figure 3. Default Setup (Refer to Figure 5 for Detailed Setup)

TYPICAL PERFORMANCE

Typical performance of the AD1896 for 44.1 kHz:48 kHz (asynchronous) sample rate is listed below.

1. DNR, No Filter –139 dBFS, 20 Hz to 20 kHz (–60 dBFS)
2. DNR, A-Weighted –142 dBFS, 20 Hz to 20 kHz (–60 dBFS)
3. THD+N, No Filter –120 dBFS, 20 Hz to 20 kHz (0 dBFS)
4. Frequency Response ±0.015 dB, 20 Hz to 20 kHz (0 dBFS)

Table IX. MCLK_I Frequencies for Common Sample Rates in Master Mode

	MCLK_I Frequency (MHz)		
Sample Rate (kHz)	**256 × f_S**	**512 × f_S**	**768 × f_S**
44.100	11.289600	22.579200	33.868800
48.000	12.288000	24.576000	
96.000	24.576000		

EXTERNAL 192 kHz CLOCK GENERATOR CIRCUIT

An external circuit can be used to generate the 192 kHz clock signals (SCLK, LRCLK) using on-board 128 × f_S clock oscillator (U15) running at 24.576 MHz. Please refer to Figure 4 for the schematic and instructions on how to connect the external circuit to the AD1896EB. In general, external SCLK and LRCLK can be used for converting the audio input data to 192 kHz rate by connecting SCLK to SCLK_O (DDO_SCLK_O, HDR5 on the AD1896EB) and LRCLK to LRCLK_O (DDO_LRCLK_O, HDR5 on the AD1896EB). On-board SPDIF transmitter CS8404 (U6) does not support sample rates above 96 kHz.

ATTACHMENTS

Appendix A

1. External 192 kHz Clock Generator Circuit
2. AD1896 Evaluation Board Block Diagram, Schematics, and Layout Plots
3. Bill of Materials
4. PLD Code

FURTHER INFORMATION

Ordering Information

Order number is EVAL-AD1896EB

For Application Questions or Technical Support

Contact Analog Devices' Central Applications Department at 1-781-937-1428 for assistance.

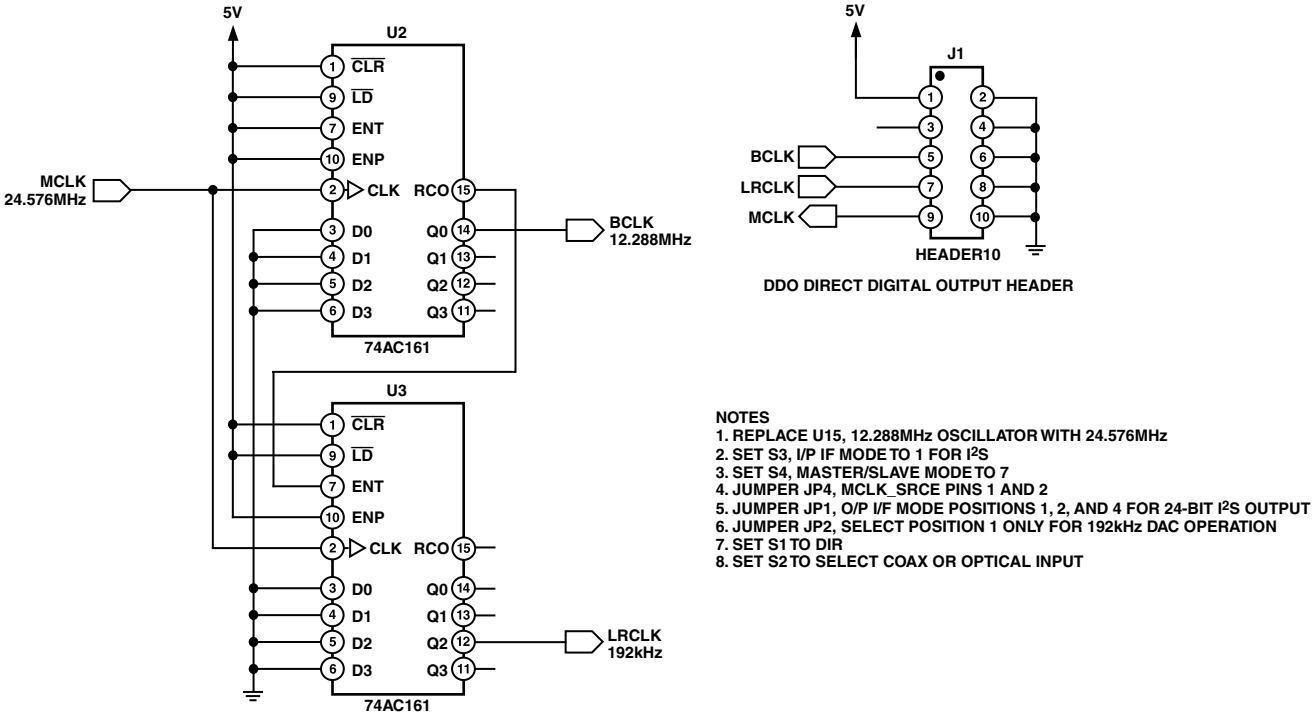


Figure 4. 192 kHz Clock Generator for AD1896EB

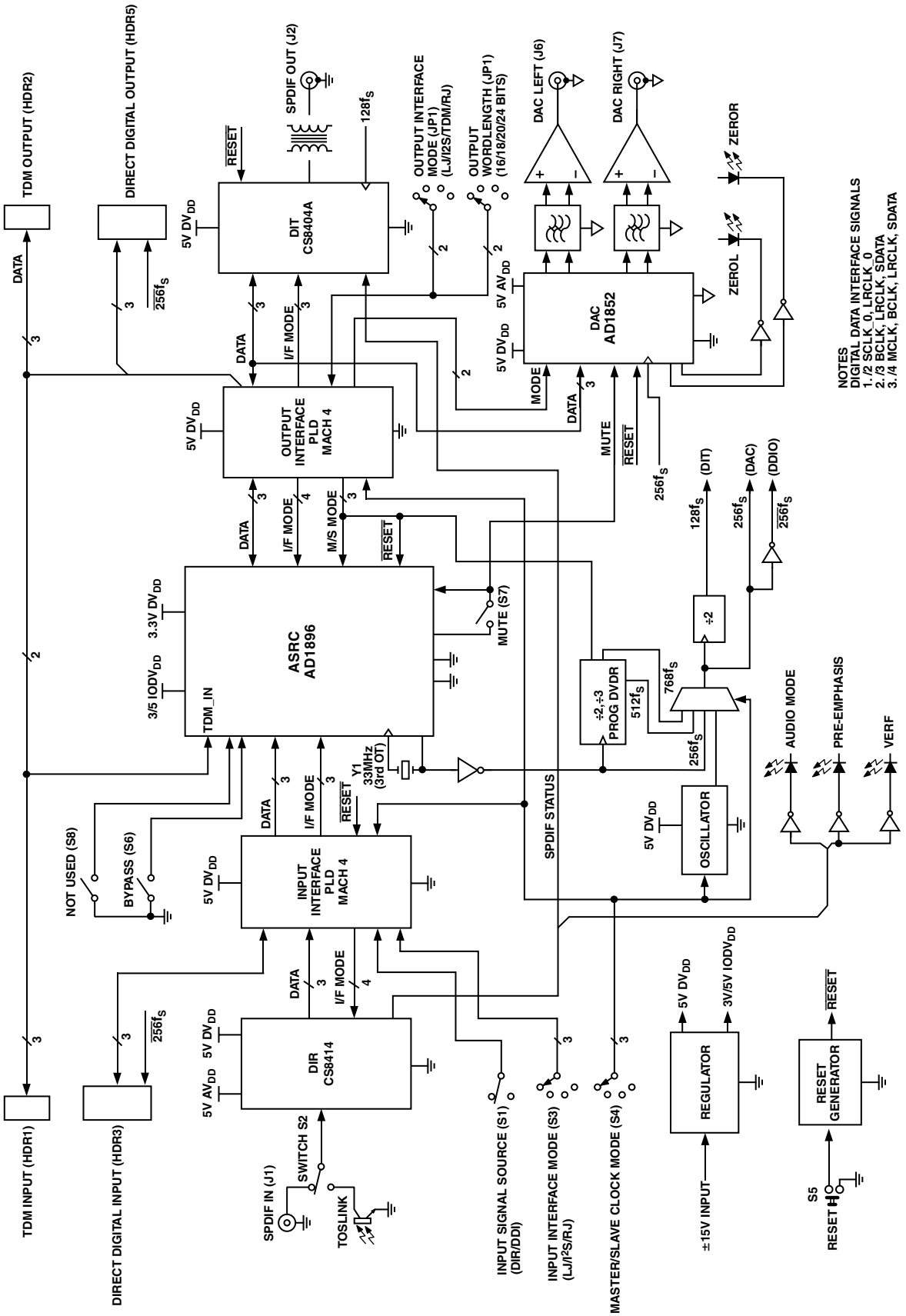
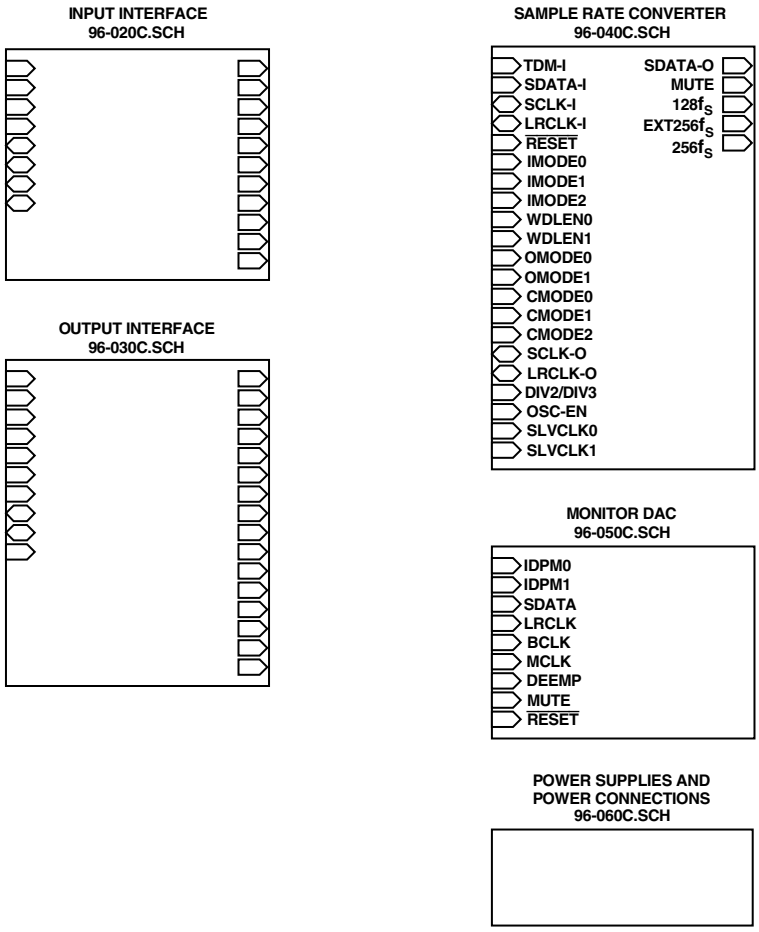


Figure 5. Evaluation Board Block Diagram



UNLESS OTHERWISE NOTED

1.0 ALL RESISTOR VALUES ARE EXPRESSED IN OHMS.
1.1 ALL RESISTORS ARE 1%, 1/10 W, THICK FILM TYPES.
1.2 ALL MF RESISTORS ARE 0.1%, 1/10 W, METAL FILM TYPES.
1.3 R, K, AND M ARE USED INSTEAD OF A DECIMAL POINT IN RESISTOR VALUES.

2. ALL RESISTOR NETWORKS ARE 5%, 1/16 W TYPES WITH THEIR VALUES EXPRESSED IN OHMS.

3.0 ALL CAPACITOR VALUES ARE EXPRESSED IN FARADS.
3.1 U, N, AND P ARE USED INSTEAD OF A DECIMAL POINT IN CAPACITOR VALUES.
3.2 ALL 100N BYPASS CAPACITORS ARE 20%, 50 V, Z5U, CERAMIC MONOLITHIC TYPES.
3.3 ALL NON-ELECTROLYTIC CAPACITORS ARE 10%, 50 V, X7R, CERAMIC MONOLITHIC TYPES.
3.4 ALL NP0 CAPACITORS ARE 5%, 50 V, CERAMIC MONOLITHIC TYPES.
3.5 ALL MY CAPACITORS ARE 5%, 50 V, METALLIZED POLYESTER TYPES.
3.6 ALL PPS CAPACITORS ARE 5%, 50 V, METALLIZED PPS FILM TYPES.
3.7 ALL PC CAPACITORS ARE 5%, 50 V, METALLIZED POLYCARBONATE TYPES.
3.8 ALL ELECTROLYTIC CAPACITORS ARE 20%, 10 V (OR HIGHER), ALUMINUM ELECTROLYTE TYPES.
3.9 ALL T_A CAPACITORS ARE 20%, 10 V (OR HIGHER), TANTALUM ELECTROLYTE TYPES.

4. FOR COMPLETE INFORMATION ON ANY COMPONENT, PLEASE SEE THE ASSOCIATED BILL OF MATERIALS.

5. ALL NET NAMES PRECEDED BY/ARE ACTIVE LOW SIGNALS.

Figure 6. Evaluation Board

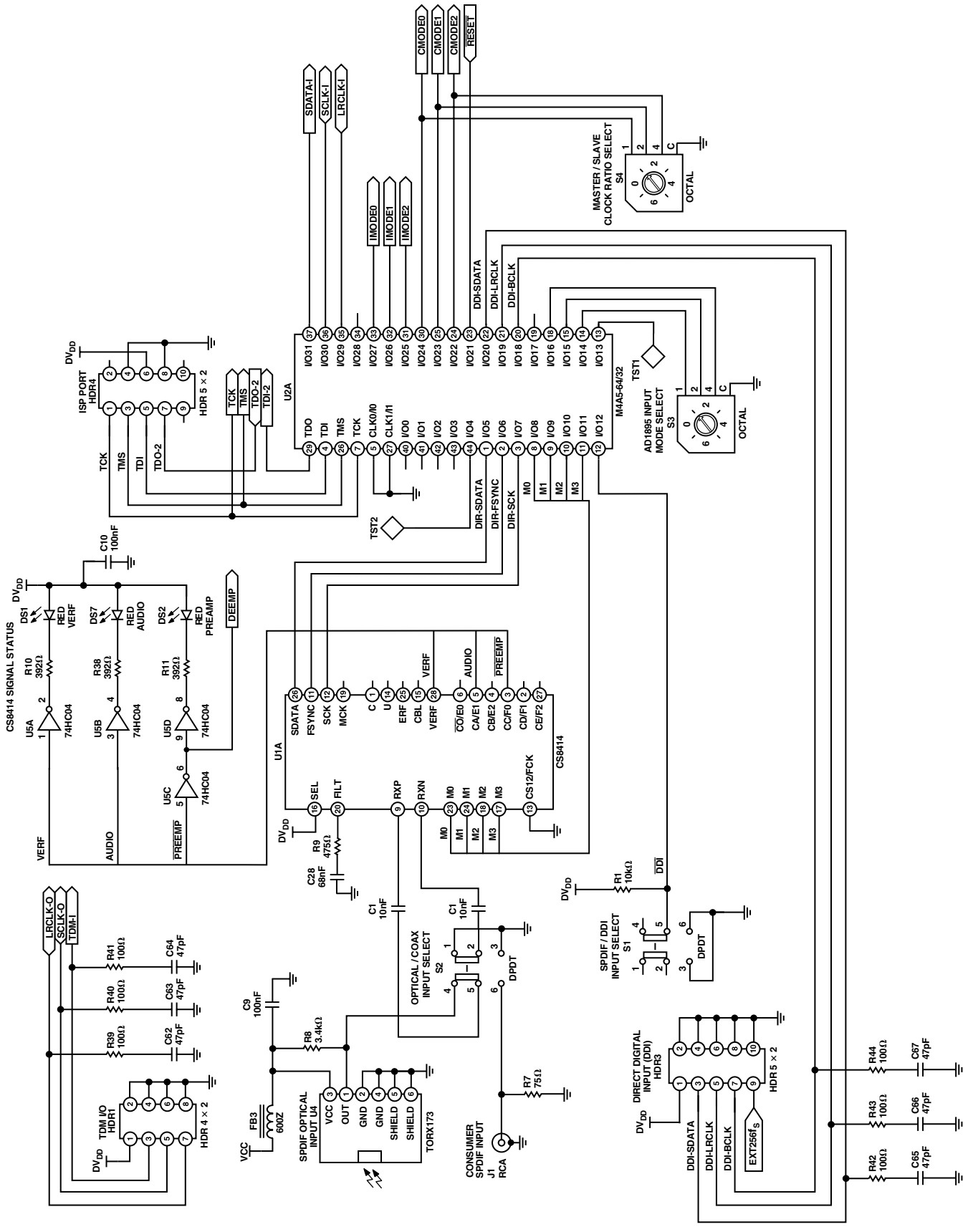


Figure 7. Evaluation Board

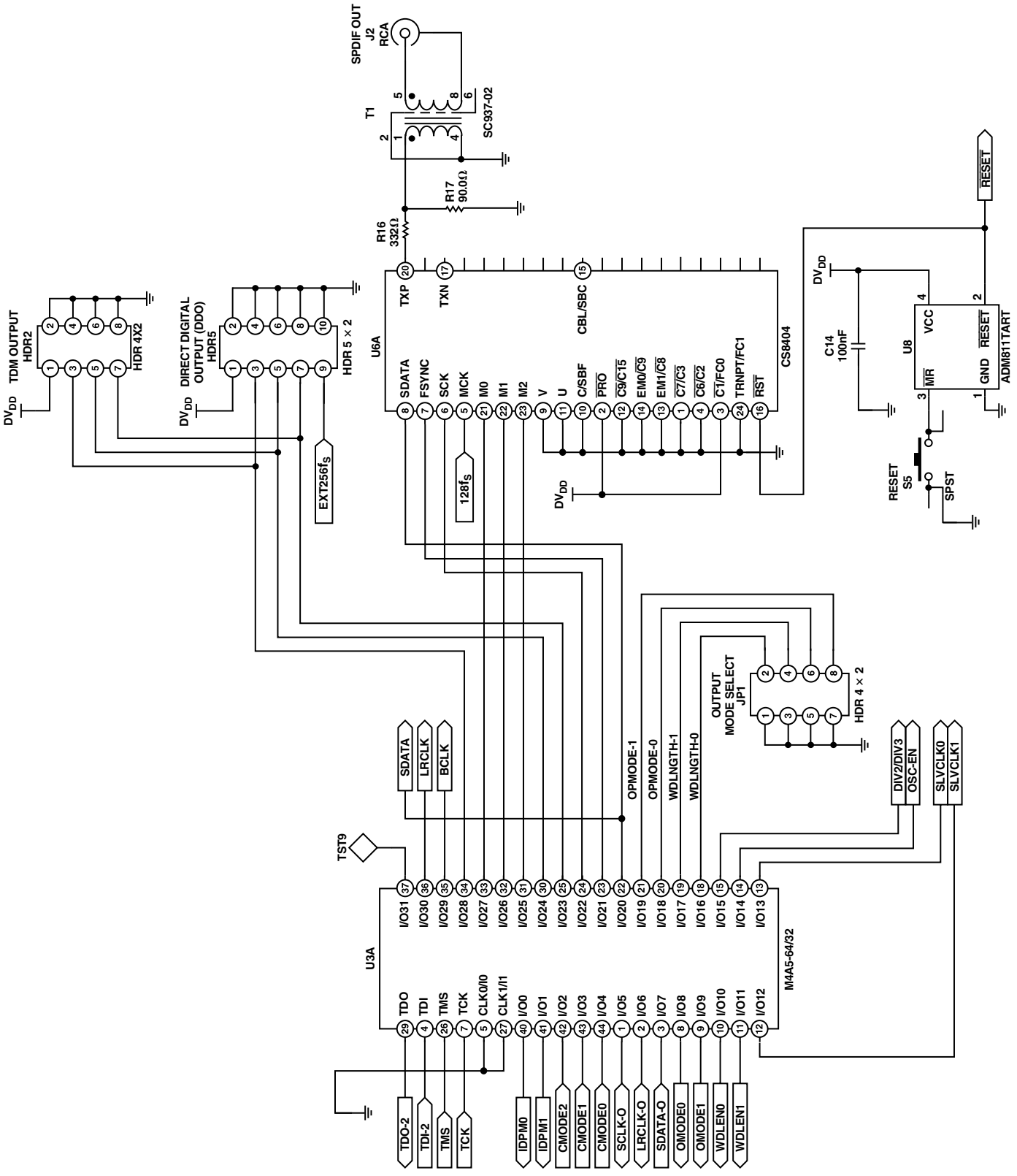


Figure 8. Evaluation Board

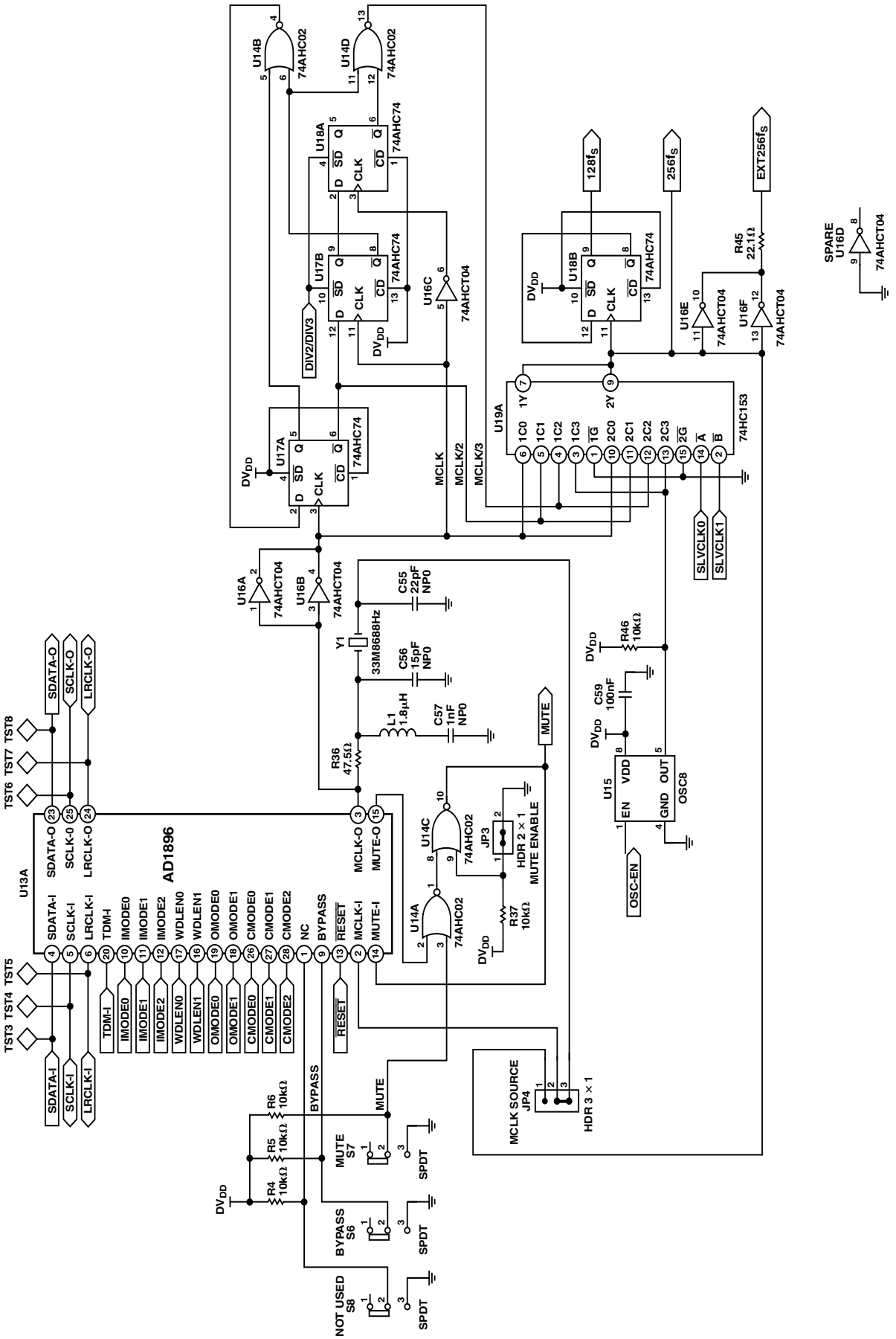


Figure 9. Evaluation Board

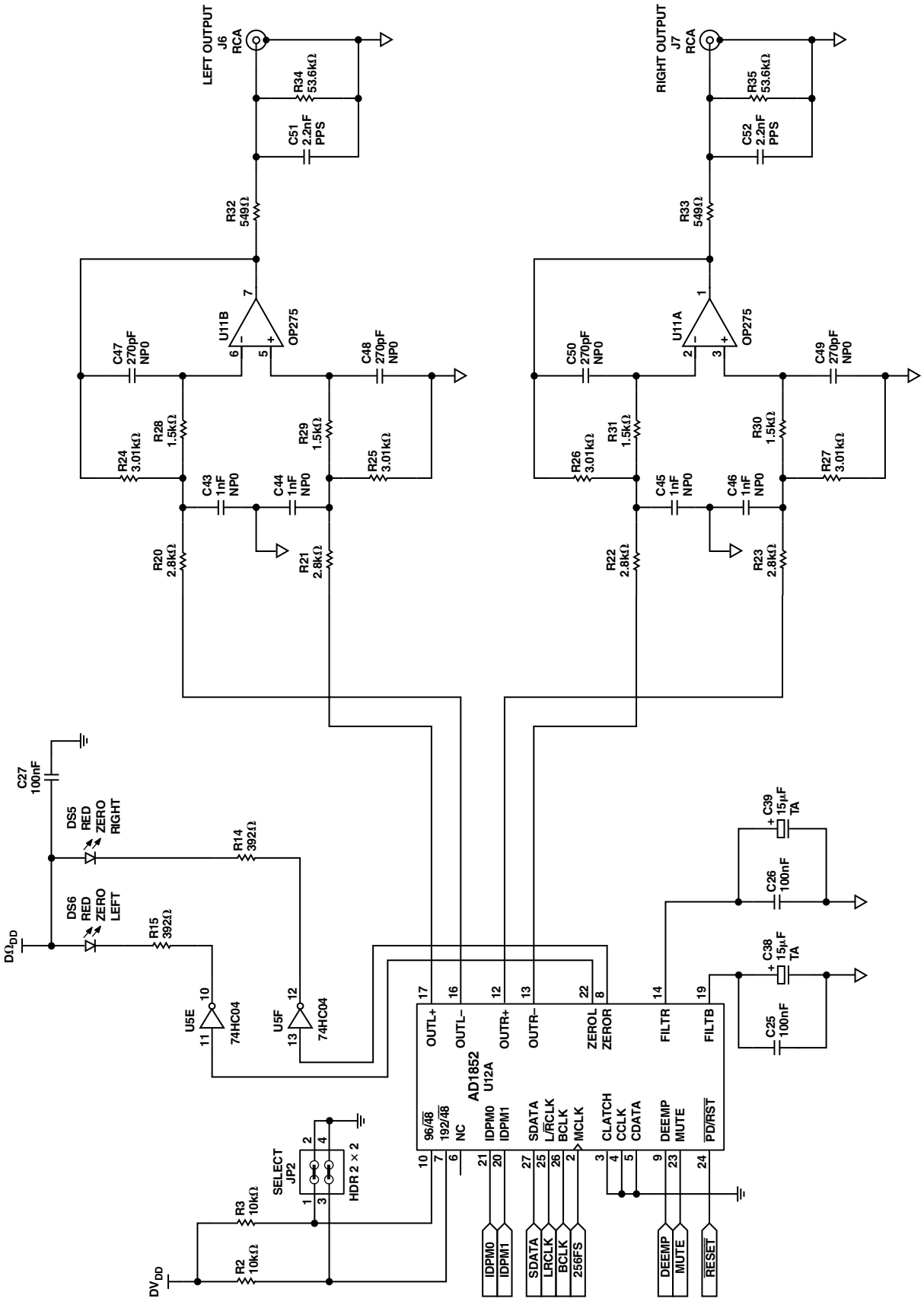


FIgure 10. Evaluation Board

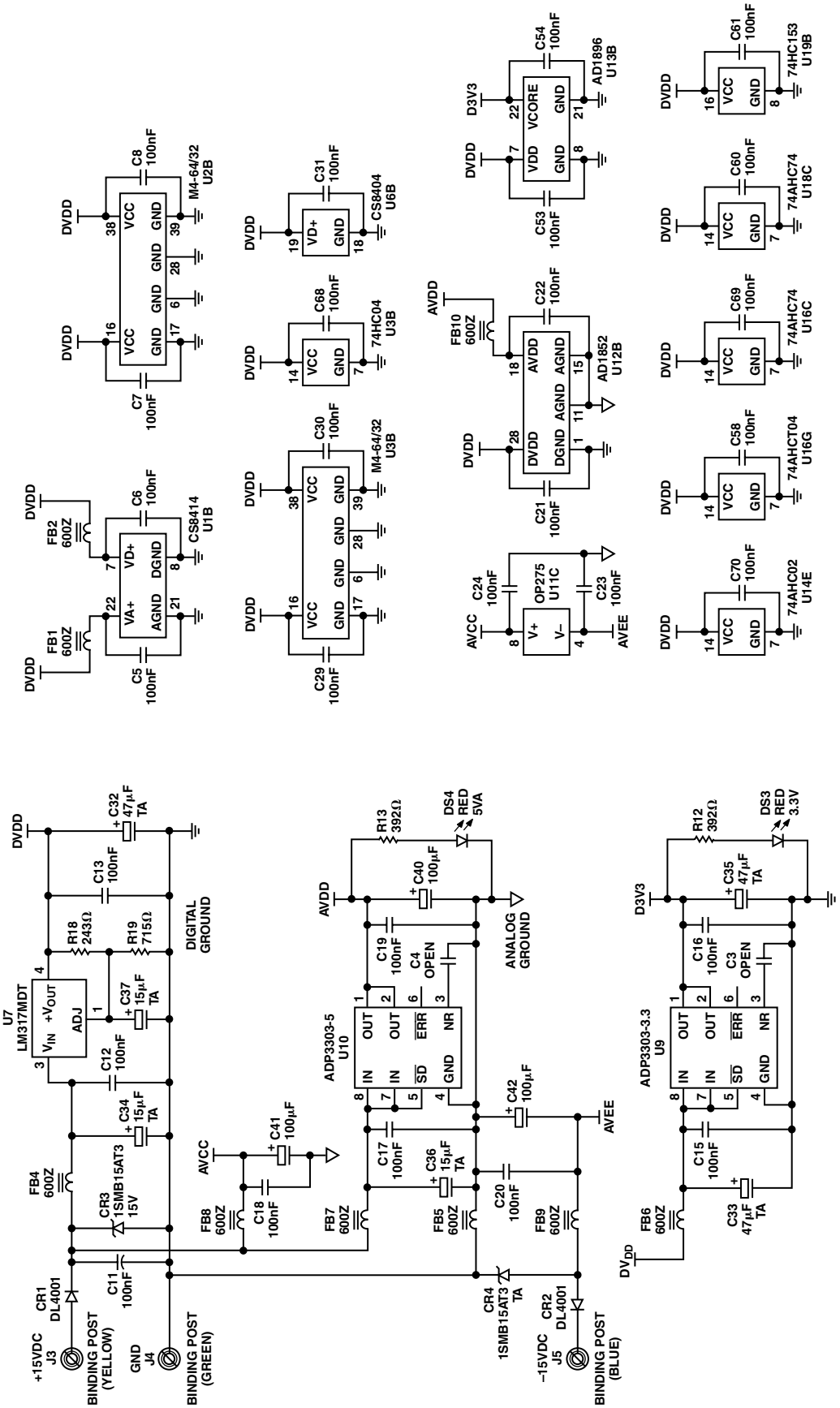


Figure 11. Evaluation Board

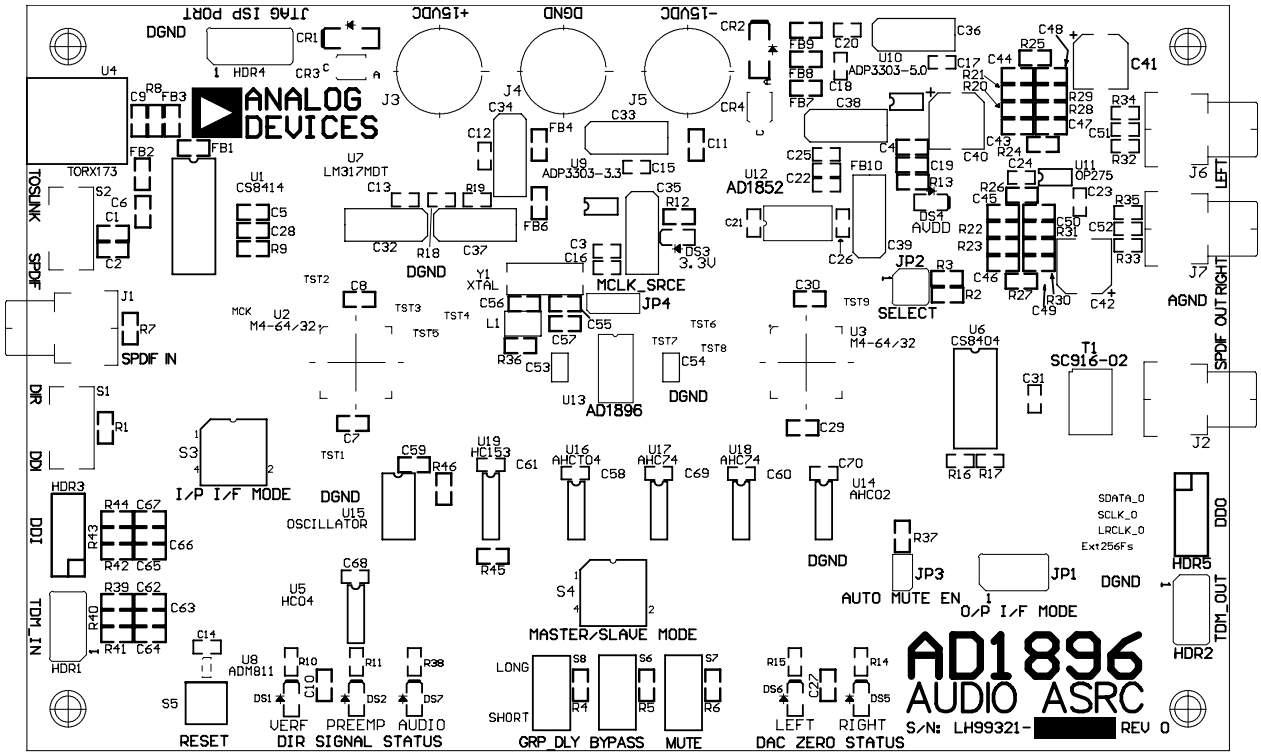


Figure 12. Audio ASRC

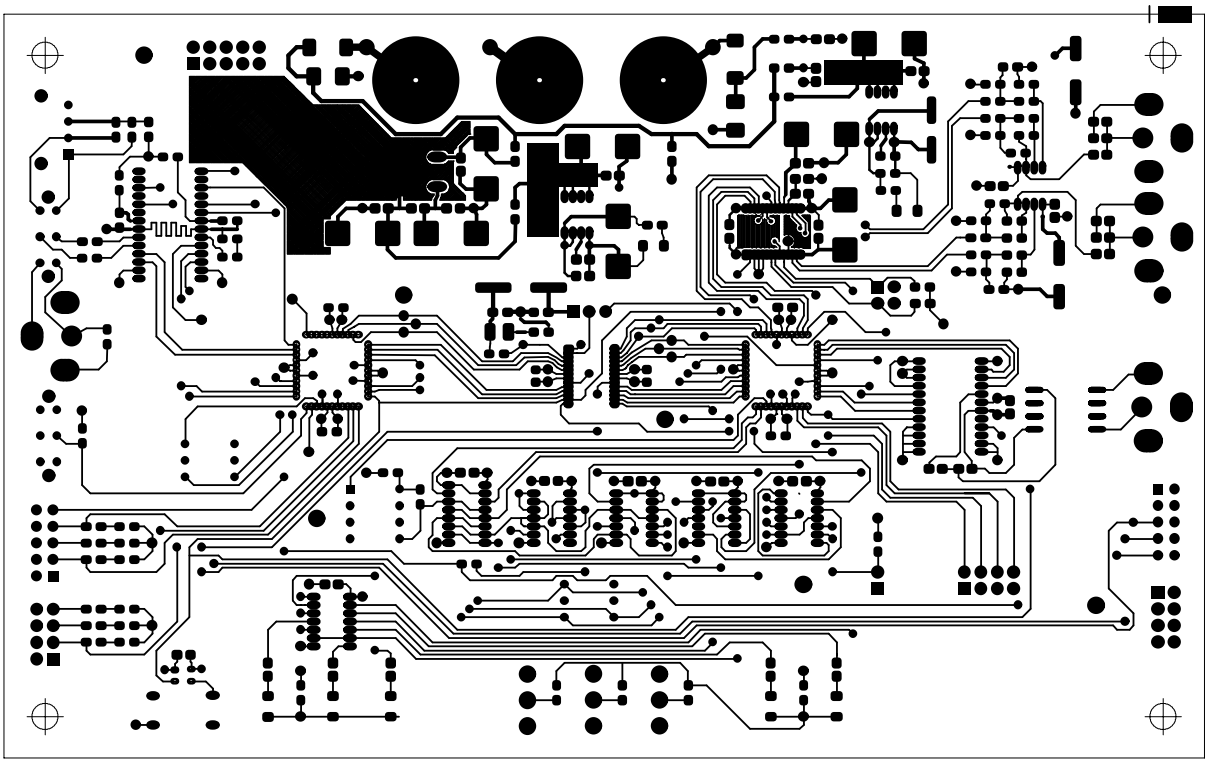


Figure 13. Component Side

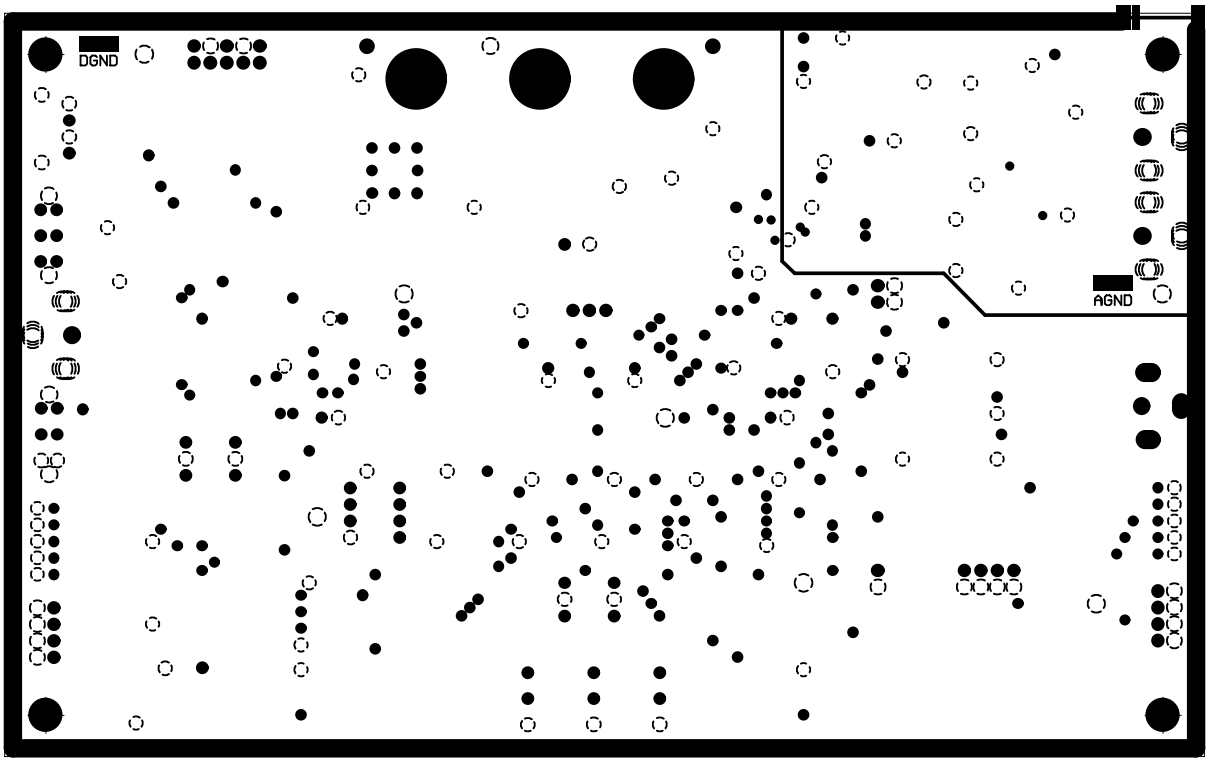


Figure 14. Ground Planes

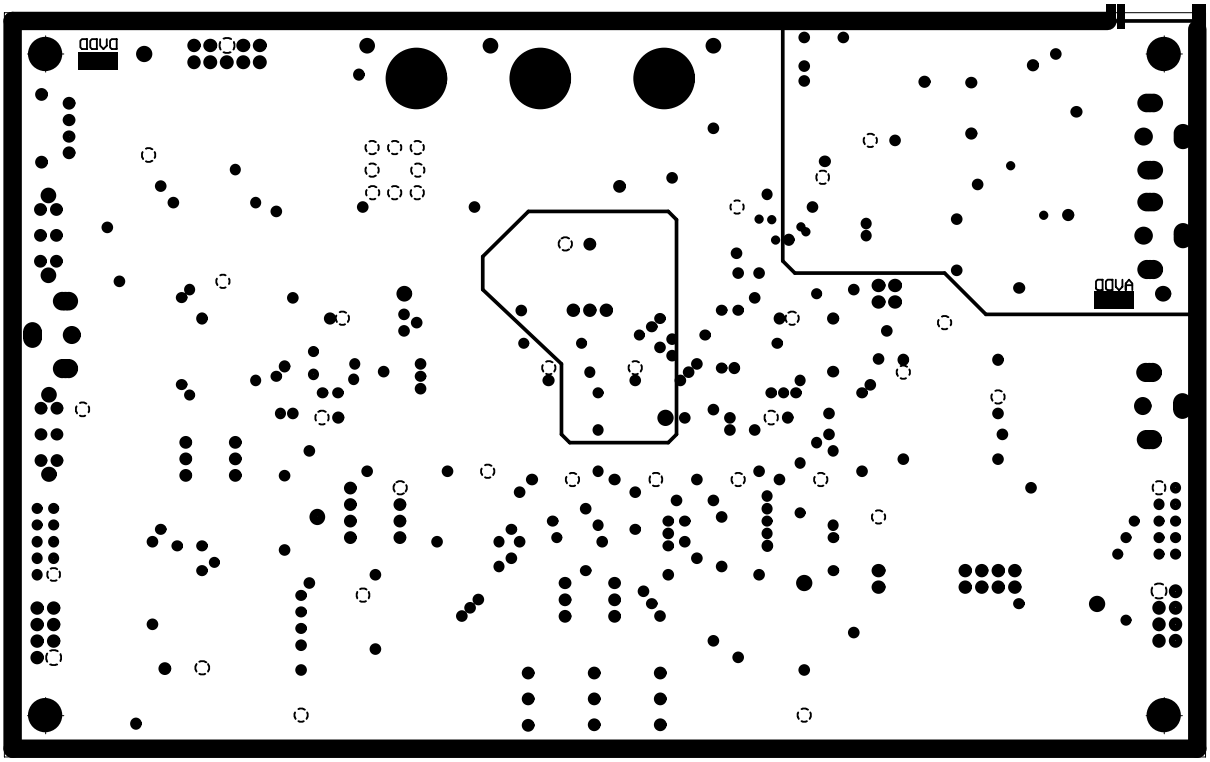


Figure 15. Power Planes

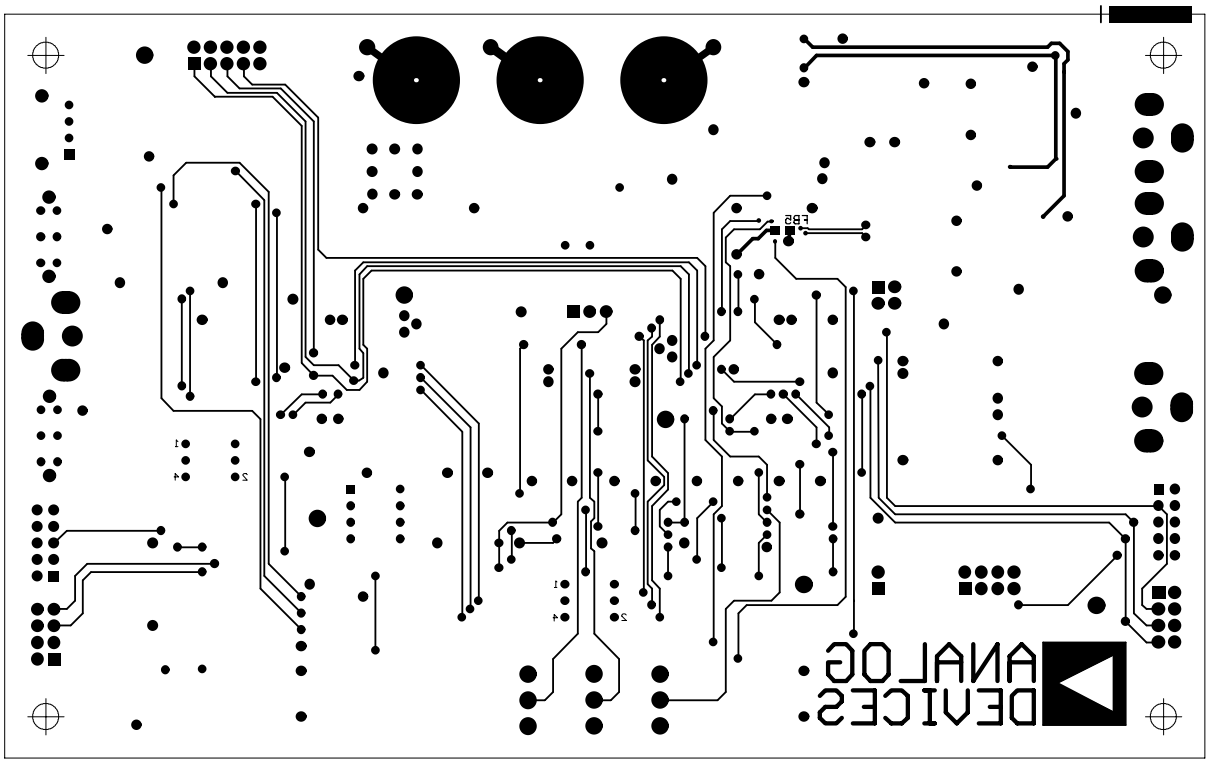


Figure 16. Bottom Layer

BILL OF MATERIALS

Item	Qty	Ref	Detail	Title	Mfr P/N	Mfr Name
1	1		LH99321 Rev 0	PCB FAB AD1895 Evaluation	LH99321 Rev 0	Prototype Circuits, Inc.
2	1	U12	AD1852JRS	IC DAC Stereo 24-Bit 192kS/s SSOP-28	AD1852JRS	Analog Devices, Inc.
3	1	U13	AD1895YRS	IC Async Sample Rate Converter SSOP-28	AD1895YRS	Analog Devices, Inc.
4	1	U8	ADM811TART	IC Reset Generator SOT-143	ADM811TART	Analog Devices, Inc.
5	1	U9	ADP3303AR-3.3	Voltage Regulator 3 V 3 SO-8	ADP3303AR-3.3	Analog Devices, Inc.
6	1	U10	ADP3303AR-5	Voltage Regulator 5 V SO-8	ADP3303AR-5	Analog Devices, Inc.
7	1	U6	CS8404A-CS	IC Digital Audio Transmitter 96 kHz SOIC-24L	CS8404A-CS	Crystal Semiconductor
8	1	U1	CS8414-CS	IC Digital Audio Receiver 96 kHz SOIC-28L	CS8414-CS	Crystal Semiconductor
9	1	U7	LM317MDT	Voltage Regulator Pos Adj DPAK	LM317MDT	Motorola
10	2	U2, U3	M4A5-64/32-10VC	IC PLD CMOS ISP TQFP44	M4A5-64/32-10VC	Lattice
11	1	U11	OP275GS	IC OPAMP Dual Bipolar/JFET SO-8	OP275GS	Analog Devices, Inc.
12	1	U14	74AHC02	IC Quad 2-Input NOR SO-14	74AHC02D	Philips
13	2	U17, U18	74AHC74	IC Dual D Flip-Flop SO-14	SN74AHC74D	Texas Instruments
14	1	U16	74AHCT04	IC Hex Inverter SO-14	SN74AHCT04D	Texas Instruments
15	1	U5	74HC14	IC Hex Schmitt Trigger Inverter SO-14	MM74HC14M	Fairchild
16	1	U19	74HC153	IC Dual 4-Input MUX SO-14	M74HC153M	ST Microelectronics
17	1	T1	SC937-02	Transformer Signal AES/EBU	SC937-02	Scientific Conversion, Inc.
18	1	R45	22R1 Ω	Chip Resistor 1% 100 mW Thick Film 0805	ERJ-6ENF22.1	Panasonic
19	1	R36	47R5 Ω	Chip Resistor 1% 100 mW Thick Film 0805	ERJ-6ENF47.5	Panasonic
20	1	R7	75R0 Ω	Chip Resistor 1% 100 mW Thick Film 0805	ERJ-6ENF75.0	Panasonic
21	1	R17	90R9 Ω	Chip Resistor 1% 100 mW Thick Film 0805	ERJ-6ENF90R9	Panasonic
22	6	R39–R44	100 Ω	Chip Resistor 1% 100 mW Thick Film 0805	ERJ-6ENF1000	Panasonic
23	1	R18	243 Ω	Chip Resistor 1% 100 mW Thick Film 0805	ERJ-6ENF2430	Panasonic
24	1	R16	332 Ω	Chip Resistor 1% 100 mW Thick Film 0805	ERJ-6ENF3320	Panasonic
25	7	R10–R15, R38	392 Ω	Chip Resistor 1% 100 mW Thick Film 0805	ERJ-6ENF3920	Panasonic
26	1	R9	475 Ω	Chip Resistor 1% 100 mW Thick Film 0805	ERJ-6ENF4750	Panasonic
27	2	R32, R33	549 Ω	Chip Resistor 1% 100 mW Thick Film 0805	ERJ-6ENF5490	Panasonic
28	1	R19	715 Ω	Chip Resistor 1% 100 mW Thick Film 0805	ERJ-6ENF7150	Panasonic
29	4	R28–R31	1.5 kΩ	Chip Resistor 1% 100 mW Thick Film 0805	ERJ-6ENF1501	Panasonic
30	4	R20–R23	2.8 kΩ	Chip Resistor 1% 100 mW Thick Film 0805	ERJ-6ENF2801	Panasonic
31	4	R24–R27	3.01 kΩ	Chip Resistor 1% 100 mW Thick Film 0805	ERJ-6ENF3011	Panasonic
32	1	R8	3.4 kΩ	Chip Resistor 1% 100 mW Thick Film 0805	ERJ-6ENF3401	Panasonic
33	8	R1–R6, R37, R46	10 kΩ	Chip Resistor 1% 100 mW Thick Film 0805	ERJ-6ENF1002	Panasonic
34	2	R34, R35	53.6 kΩ	Chip Resistor 1% 100 mW Thick Film 0805	ERJ-6ENF5362	Panasonic
35	1	C56	15 pF	Chip Capacitor 5% 50 V NP0 Ceramic 0805	ECU-V1H150JCN	Panasonic
36	1	C55	22 pF	Chip Capacitor 5% 50 V NP0 Ceramic 0805	ECU-V1H220JCN	Panasonic
37	6	C62–C67	47 pF	Chip Capacitor 5% 50 V NP0 Ceramic 0805	ECU-V1H470JCG	Panasonic
38	4	C47–C50	270 pF	Chip Capacitor 5% 50 V NP0 Ceramic 0805	ECU-V1H271JCG	Panasonic
39	5	C43–C46, C57	1 nF	Chip Capacitor 5% 50 V NP0 Ceramic 0805	ECU-V1H102JCX	Panasonic
40	2	C51, C52	2.2 nF	Chip Capacitor 5% 50 V PPS Film 0805	ECH-U1H222JB5	Panasonic
41	2	C1, C2	10 nF	Chip Capacitor 10% 50 V X7R Ceramic 0805	ECU-V1H103KBG	Panasonic
42	1	C28	68 nF	Chip Capacitor 10% 50 V X7R Ceramic 0805	ECJ-2YB1H683K	Panasonic
43	35	C5–C27, C29–C31, C53, C54, C58–C61, C68–C70	100 nF	Chip Capacitor 10% 50 V X7R Ceramic 0805	ECJ-2YB1H104K	Panasonic
44	5	C34, C36–C39	15 µF	Chip Capacitor 20% 20 V Tantalum 7343	ECS-T1DD156R	Panasonic
45	3	C32, C33, C35	47 µF	Chip Capacitor 20% 10 V Tantalum 7343	ECS-T1AD476R	Panasonic
46	3	C40–C42	100 µF	SMD Capacitor 20% 25 V Aluminum CASE-F	EEV-FC1E101P	Panasonic
47	1	Y1	33M8688 Hz	SMD Crystal HCM49	HCM49-33.8688 MABJT	Citizen
48	10	FB1–FB10	600Z	Chip Ferrite Bead 600 Ω @100 MHz 0805	HZ0805E601R	Steward
49	1	L1	1.8 µs	Chip Inductor 20% 0R82 Ω RLP167	ELJ-FA1R8KF	Panasonic
50	7	DS1–DS7	Red	Chip LED 1206LED	CMD15-21VRD/TR8	Chicago Miniature Lamp, Inc.
51	2	CR1, CR2	DL4001	Chip Diode 50 V 1A SOD-87	DL4001	Microsemi
52	2	CR3, CR4	1SMB15AT3	Chip Transient Suppressor 15 V 600 W SMB	1SMB15AT3	ON Semiconductor
53	2	J1, J2	Black Insert	Connector RCA Female Right Angle CTP-021	CTP-021-A-S-BLK	Connect-Tech Products, Products, Inc.
54	1	J6	White Insert	Connector RCA Female Right Angle CTP-021	CTP-021-A-S-WHT	Connect-Tech Products, Products, Inc.
55	1	J7	Red Insert	Connector RCA Female Right Angle CTP-021	CTP-021-A-S-RED	Connect-Tech Products, Products, Inc.
56	1	JP3	Header 2 × 1	Connector 2P 2 × 1 Male 100ctr SIP2	2340-6111TN	3M
57	1	JP2	Header 2 × 2	Connector 4P 2 × 2 Male 100ctr HDR2X2	2380-6121TN	3M
58	1	JP4	Header 3 × 1	Connector 3P 3 × 1 Male 100ctr HDR3X1	2340-6111TN	3M

BILL OF MATERIALS (continued)

Item	Qty	Ref	Detail	Title	Mfr P/N	Mfr Name
59	3	HDR1, HDR2, JP1	Header 4 × 2	Connector 8P 4 × 2 Male 100ctr HDR4X2	2380-6121TN	3M
60	2	HDR3, HDR5	Header 5 × 2	Connector 10P 5 × 2 Male 100ctr HDR5X2	2380-6121TN	3M
61	1	HDR4	Header 5 × 2	Connector 10P 5 × 2 Male 100ctr Shrouded HDR5X2SHR	51138-44624 30310-6002HB	3M
62	1	U15	Socket 4/8	Socket Oscillator Half Size OSC8	1108800	Aries
63	1	U15	12M288 Hz	IC CMOS Oscillator 12.288 MHz OSC8	SG-531P-12.288MC	Epson Electronics
64	2	S1, S2	EG-2215	Switch Slide DPDT Side Act PCB	EG-2215	E-Switch
65	2	S3, S4	PT65526	Switch Rotary 8 Pos Octal	PT65526	APEM
66	1	S5	FSM6JSMA	Switch PB NO Momentary Tactile	FSM6JSMA	Augat
67	3	S6–S8	10SP001	Switch Slide SPDT Vert Act PCB	10SP001	Mouser
68	1	U4	TORX173	IC Fiber Optic Receiver	TORX173	Toshiba
69	1	J3	Yellow	Connector Binding Post	111-0107-001	Johnson Components, Inc.
70	1	J4	Green	Connector Binding Post	111-0104-001	Johnson Components, Inc.
71	1	J5	Blue	Connector Binding Post	111-0110-001	Johnson Components, Inc.
72	4		Spacer Snap-in	Spacer Nylon 3/4" Snap-In	SPCS-12	SPC Technology

```
                                        in_pld.abl
MODULE IF_Logic
TITLE   'AD1896 EVB Input Interface Logic'
//=============================================================================
//  FILE:               input_pld.abl
//  REVISION DATE:   03-20-01
//  REVISION BY:        Chirag Patel
//  REVISION:    1.0
//
//  DESCRIPTION:
//
// This input interface PLD (U2) selects between the External Data Interface header
// (HDR3) and the on-board CS8414 DIR (U1) for the AD1896 ASRC input signals, depending
// upon the SPDIF/DDI switch position (S1).  When the SPDIF Receiver DIR is the selected
// signal source the digital audio signals, SDATA_I, SCLK_I and LRCLK_I are derived from
// the DIR output.  SPDIF receiver needs the digital data in the SPDIF format in order to
// generate these signals.  When the external data is the selected source the digital
// signals from (HDR3) are applied to the AD1896.

// Signals SCLK_I, LRCLK_I, DDI_SCLK, DDI_LRCLK, DIR_SCLK, DIR_FSYNC on the PLD are
// bi-directional signals.  The direction of these signals are controlled by the
// MASTER_SLAVE MODE switch position (S4).  When the AD1896 input serial port is set in the
// master mode, the SCLK_I and LRCLK_I are generated from the AD1896 input serial port.
// On the other hand, these signals are provided from the external source in the slave mode
// operation.

// PLD also decodes the Input Interface Format Switch (S3) and sets the Interface mode pins
// for both the CS8414 DIR and the AD1896 ASRC.
//=============================================================================

LIBRARY 'MACH';
DECLARATIONS
//   IF_Logic DEVICE 'M4-64/32-15VC';

"INPUTS ================================================================
//  TDI, TCK, TMS                          pin 4,7,26 istype 'com';       //JTAG I/P's
    DIR_SDATA                    pin 1 istype 'com';              //CS8414 DIR SDATA OUT
    SPDIF_DDI                    pin 12 istype 'com';            //SPDIF_DDI SWITCH S1
    DDI_SDATA                    pin 22 istype 'com';       //EXTERNAL DATA INPUT DDI
    RESET                           Pin 23 istype 'com';        //Active hi reset output
to AD1896
    RESET_LO                     Pin 44 istype 'com';           //Active low reset input
    MS_MODE2, MS_MODE1, MS_MODE0    pin 24,25,30 istype 'com';  //MASTER/SLAVE MODE SWITCH S4
    IN_MODE2,IN_MODE1,IN_MODE0          pin 18,15,14 istype 'com';  //INPUT SERIAL MODE
SWITCH S3
"OUTPUTS ===============================================================
//  TDO                             pin 29 istype 'com';           //JTAG O/P
    M0, M1, M2, M3                     pin 8,9,10,11 istype 'com'; //SPDIF_RVR MODE SELECT
    SMODE_I_0, SMODE_I_1, SMODE_I_2    pin 33,32,31 istype 'com';  //INPUT SERIAL MODE FORMAT
FOR AD1896
   SDATA_I                       pin 37 istype 'com';           //SERIAL DATA INPUT TO
AD1896 ASRC

//IO SIGNALS
    DIR_FSYNC, DIR_SCLK                pin 2,3;                      //DIR_FYSNC AND DIR_SCLK
IO'S
    DDI_LRCLK, DDI_SCLK                pin 21,20;                    //EXTERNAL LRCLK AND
SCLK IO'S FOR HDR3
    LRCLK_I, SCLK_I               pin 35,36;                   //LRCLK_I AND SCLK_I IO'S TO
AD1896 ASRC

"NODES
```

```
    I_SDATA, ISCLK, ILRCLK              node istype 'com';

//=============================================================================
                                          in_pld.abl
"MACROS

//INPUT SERIAL DATA FORMATS

// S3 position 0, LEFT-JUSTIFIED
    LJ        =   ( IN_MODE2 &  IN_MODE1 &  IN_MODE0);
// S3 position 1, I2S
    I2S       =   ( IN_MODE2 &  IN_MODE1 &  !IN_MODE0);
// S3 position 2, RIGHT-JUSTIFIED 24-BITS
    RJ24      =   ( IN_MODE2 &  !IN_MODE1 &  IN_MODE0);
// S3 position 3, RIGHT-JUSTIFIED 20-BITS
    RJ20      =   ( IN_MODE2 &  !IN_MODE1 &  !IN_MODE0);
// S3 position 4, RIGHT-JUSTIFIED 18-BITS
    RJ18      =   ( !IN_MODE2 &  IN_MODE1 &  IN_MODE0);
// S3 position 5, RIGHT-JUSTIFIED 16-BITS
    RJ16      =   ( !IN_MODE2 &  IN_MODE1 &  !IN_MODE0);
// S3 positons 6,7 are not used

//MASTER_SLAVE MODE MAPPING

// S4 position 7, INPUT/OUTPUT SERIAL PORTS IN SLAVE MODE
   BOTH_SLAVE  =   (!MS_MODE2 & !MS_MODE1 & !MS_MODE0);
// S4 position 6, OUTPUT SERIAL PORT IN MASTER MODE FSX768
   O_MAS_768   =  (!MS_MODE2 & !MS_MODE1 & MS_MODE0);
// S4 position 5, OUTPUT SERIAL PORT IN MASTER MODE FSX512
   O_MAS_512   =  (!MS_MODE2 & MS_MODE1 & !MS_MODE0);
// S4 position 4, OUTPUT SERIAL PORT IN MASTER MODE FSX256
   O_MAS_256   =  (!MS_MODE2 & MS_MODE1 & MS_MODE0);
// S4 position 3, INPUT SERIAL PORT IN MATCHED_PHASE MODE
   MATCH_PHASE =  (MS_MODE2 & !MS_MODE1 & !MS_MODE0);
// S4 position 2, INPUT SERIAL PORT IN MASTER MODE FSX768
   IN_MAS_768  =  (MS_MODE2 & !MS_MODE1 & MS_MODE0);
// S4 position 1, INPUT SERIAL PORT IN MASTER MODE FSX512
   IN_MAS_512  =  (MS_MODE2 & MS_MODE1 & !MS_MODE0);
// S4 position 0, INPUT SERIAL PORT IN MASTER MODE FSX256
   IN_MAS_256  =  (MS_MODE2 & MS_MODE1 & MS_MODE0);

 "=============================================================================

EQUATIONS

// AD1896 ASRC Input Serial Port Interface Mode Select
    SMODE_I_2 = RJ24 # RJ20 # RJ18 # RJ16;
    SMODE_I_1 = RJ24 # RJ20;
    SMODE_I_0 = RJ24 # RJ18 # I2S;

// CS8414 DIR Interface Mode Select, DIR_FSYNC and DIR_SCLK are bi-directional signals.
// If AD1896 input serial port is in slave mode, the CS8414 DIR RJ-24 and RJ-20 modes
// are not supported.

    M0 =   (RJ16 & (BOTH_SLAVE # MATCH_PHASE # O_MAS_768 # O_MAS_512 # O_MAS_256))
         # ((LJ # RJ24 # RJ20 # I2S) & (IN_MAS_768 # IN_MAS_512 # IN_MAS_256));

    M1 =   ((I2S # RJ18) & (BOTH_SLAVE # MATCH_PHASE # O_MAS_768 # O_MAS_512 # O_MAS_256))
        # (I2S & (IN_MAS_768 # IN_MAS_512 # IN_MAS_256));

    M2 = RJ18 # RJ16;
    M3 = 0;
```

```
                                        in_pld.abl
// IO control logic
    DDI_SCLK.oe   = (IN_MAS_768 # IN_MAS_512 # IN_MAS_256);
    DDI_LRCLK.oe  = (IN_MAS_768 # IN_MAS_512 # IN_MAS_256);
    DIR_FSYNC.oe  = (IN_MAS_768 # IN_MAS_512 # IN_MAS_256);
    DIR_SCLK.oe   = (IN_MAS_768 # IN_MAS_512 # IN_MAS_256);
    SCLK_I.oe     = (BOTH_SLAVE # MATCH_PHASE # O_MAS_768 # O_MAS_512 # O_MAS_256);
    LRCLK_I.oe    = (BOTH_SLAVE # MATCH_PHASE # O_MAS_768 # O_MAS_512 # O_MAS_256);

    DDI_SCLK      = ISCLK;
    DDI_LRCLK     = ILRCLK;
    DIR_SCLK      = ((!ISCLK) & (LJ # RJ24 # RJ20 # RJ18 # RJ16)) # (ISCLK & I2S);
    DIR_FSYNC     = ILRCLK;

// AD1896 ASRC Input Serial port signals

   SCLK_I        = ((LJ # RJ24 # RJ20 # RJ18 # RJ16 # I2S) & (ISCLK) & (!SPDIF_DDI))
                    # ((((LJ # RJ24 # RJ20) & (!ISCLK)) # ((I2S # RJ18 # RJ16) & (ISCLK))) &
(SPDIF_DDI));

   LRCLK_I       = (SPDIF_DDI & DIR_FSYNC) # (((I2S & !DDI_LRCLK) # (!I2S & DDI_LRCLK)) &
(!SPDIF_DDI));
   SDATA_I       = (DDI_SDATA & !SPDIF_DDI) # (((LJ#RJ24#RJ20#RJ18#RJ16#I2S)&(DIR_SDATA)) &
(SPDIF_DDI));


// Internal node signals
   ISCLK   = ((DDI_SCLK) & (BOTH_SLAVE#MATCH_PHASE#O_MAS_768#O_MAS_512#O_MAS_256) &
(!SPDIF_DDI))
             # ((LJ#RJ24#RJ20) & ((DIR_SCLK) &
(BOTH_SLAVE#MATCH_PHASE#O_MAS_768#O_MAS_512#O_MAS_256) & (SPDIF_DDI)))
             # ((SCLK_I) & (IN_MAS_768 # IN_MAS_512 # IN_MAS_256))
             # ((I2S # RJ18 # RJ16) & (DIR_SCLK) &
(BOTH_SLAVE#MATCH_PHASE#O_MAS_768#O_MAS_512#O_MAS_256) & (SPDIF_DDI));

   ILRCLK  = ((DDI_LRCLK) & (BOTH_SLAVE # MATCH_PHASE#O_MAS_768#O_MAS_512#O_MAS_256) &
(!SPDIF_DDI))
             # ((DIR_FSYNC) & (BOTH_SLAVE # MATCH_PHASE#O_MAS_768#O_MAS_512#O_MAS_256) &
(SPDIF_DDI))
             # ((LRCLK_I) & (IN_MAS_768 # IN_MAS_512 # IN_MAS_256));

   I_SDATA  = (DDI_SDATA & !SPDIF_DDI) # (DIR_SDATA & SPDIF_DDI);

"================================================================================
END IF_Logic
```

```
                                        out_pld.abl
//=============================================================================
MODULE      IF_Logic

TITLE          'AD1896 EVB Output Interface Logic'
//=============================================================================
//  FILE:                 output_pld.abl
//  REVISION DATE:  03-20-01
//  REVISION BY:    Chirag Patel
//  REVISION:       1.0

//  DESCRIPTION:
// This output interface PLD (U3) decodes output interface signals of AD1896 and sources
// these signals to the DAC, DIT and external header (HDR2, HDR5).
// Signals SCLK_O, LRCLK_O, DDO_SCLK and DDO_LRCLK on the PLD are bi-directional signals.
// The direction of these signals are controlled by the MASTER_SLAVE MODE switch position
(S4).
// When the AD1896 output serial port is set in the master mode, the SCLK_O and LRCLK_O are
// generated from the AD1896 output serial port.  On the other hand, these signals are pro-
vided
// from the external source in the slave mode operation.
//
// PLD also decodes the Output Interface Format and data width Jumper header (JP1) and sets
// the Interface mode pins for the AD1896 ASRC, AD1852 DAC and CS8404 DIT to meet the inter-
face
// requirements of all three devices in any given mode.
//=============================================================================
LIBRARY 'MACH';
DECLARATIONS
//   IF_Logic DEVICE 'M4-64/32-15VC';

"INPUTS  ====================================================================
//  TDI, TCK, TMS         pin 4, 7, 26 istype 'com';      //JTAG I/P's
    SDATA_O        pin 3 istype 'com, buffer';
    MS_MODE2, MS_MODE1, MS_MODE0 pin 42, 43, 44 istype 'com';
    WDLNGTH1, WDLNGTH0    pin 19, 18 istype 'com';
    OPMODE1, OPMODE0             pin 21, 20 istype 'com';

 "OUTPUTS ===================================================================
//  TDO                   pin 29 istype 'com';            //JTAG O/P
    SMODE_O_1, SMODE_O_0  pin 9, 8 istype 'com';
    WDLNGTH_O_1, WDLNGTH_O_0     pin 11, 10 istype 'com';
    OSC_EN, SLVCLK1, SLVCLK0, DIV2_3   pin 14,12, 13, 15 istype 'com';
    IDPM1, IDPM0          pin 41, 40 istype 'com';
    DDO_SDATA      pin 34 istype 'com, buffer';
    SDATA_DAC_DIT         pin 22 istype 'com, buffer';
    LRCLK_DAC, SCLK_DAC          pin 36, 35 istype 'com, buffer';
    FSYNC_DIT, SCLK_DIT          pin 23, 24 istype 'com, buffer';
    M2,M1,M0       pin 31,32,33 ISTYPE 'com';
    TST9                  pin 37 istype 'com, buffer';

//IO SIGNALS
    SCLK_O, LRCLK_O       pin 1, 2 istype 'com, buffer';
    DDO_SCLK, DDO_LRCLK   pin 30, 25 istype 'com, buffer';

"NODES
    I_SDATA, ISCLK, ILRCLK             node istype 'com, buffer';
//=============================================================================
                                        out_pld.abl

"MACROS
```

```
//OUTPUT SERIAL DATA FORMATS

// JP1[4:3] 0, LEFT-JUSTIFIED
    LJ        =   (!OPMODE1 & !OPMODE0);
// JP1[4:3] 1, I2S
  I2S       =   (!OPMODE1 & OPMODE0);
// JP1[4:3] 2, TDM MODE
    TDM       =   (OPMODE1 & !OPMODE0);
// JP1[4:3] 3, RIGHT-JUSTIFIED
    RJ        =   (OPMODE1 & OPMODE0);

 // OUTPUT DATA BIT WIDTH SETTINGS

// JP1[2:1] 0, 24-BITS
    BITS_24   =   ( !WDLNGTH1 & !WDLNGTH0);
// JP1[2:1] 0, 20-BITS
    BITS_20   =   ( !WDLNGTH1 &  WDLNGTH0);
// JP1[2:1] 0, 18-BITS
    BITS_18   =   (  WDLNGTH1 & !WDLNGTH0);
// JP1[2:1] 0, 16-BITS
    BITS_16   =   (  WDLNGTH1 &  WDLNGTH0);

// OUTPUT SERIAL DATA FORMAT MAPPING

// LJ-24 BITS
   LJ24 = (LJ & BITS_24);
// I2S-24 BITS
   I2S24 = (I2S & BITS_24);
// TDM-24 BITS
   TDM24 = (TDM & BITS_24);
// RJ-24 BITS
   RJ24 = (RJ & BITS_24);
// RJ-20 BITS
   RJ20 = (RJ & BITS_20);
 // LJ-18 BITS
   RJ18 = (RJ & BITS_18);
// LJ-16 BITS
   RJ16 = (RJ & BITS_16);

//MASTER_SLAVE MODE MAPPING

// S4 position 7, BOTH SERIAL PORT IN SLAVE MODE
    BOTH_SLAVE  =   (!MS_MODE2 & !MS_MODE1 & !MS_MODE0);
// S4 position 6, OUTPUT SERIAL PORT IN MASTER MODE FSX768
   O_MAS_768   =  (!MS_MODE2 & !MS_MODE1 & MS_MODE0);
// S4 position 5, OUTPUT SERIAL PORT IN MASTER MODE FSX512
   O_MAS_512   =  (!MS_MODE2 & MS_MODE1 & !MS_MODE0);
// S4 position 4, OUTPUT SERIAL PORT IN MASTER MODE FSX256
   O_MAS_256   =  (!MS_MODE2 & MS_MODE1 & MS_MODE0);
// S4 position 3, INPUT SERIAL PORT IN MATCHED_PHASE MODE
   MATCH_PHASE =  (MS_MODE2 & !MS_MODE1 & !MS_MODE0);
// S4 position 2, INPUT SERIAL PORT IN MASTER MODE FSX768
   IN_MAS_768  =  (MS_MODE2 & !MS_MODE1 & MS_MODE0);
// S4 position 1, INPUT SERIAL PORT IN MASTER MODE FSX512
   IN_MAS_512  =  (MS_MODE2 & MS_MODE1 & !MS_MODE0);
// S4 position 0, INPUT SERIAL PORT IN MASTER MODE FSX256

   IN_MAS_256  =  (MS_MODE2 & MS_MODE1 & MS_MODE0);
"================================================================================
                                        out_pld.abl
```

```
EQUATIONS
// AD1896 ASRC Output Serial Port Interface Mode and word length Select
   WDLNGTH_O_1 = WDLNGTH1;
   WDLNGTH_O_0 = WDLNGTH0;
   SMODE_O_1   = OPMODE1;
   SMODE_O_0   = OPMODE0;

// CS8414 DIT Interface Mode Select.  The chip is configured in the LJ mode when AD1896 output
format are
// set either RJ24, RJ20, RJ18 or RJ16.  Also need to invert the incoming SCLK signal in the
LJ24, RJ24, RJ20,
// RJ18 and RJ16 mode to match the DIT interface requirment for DIT_SCLK.
    M0 = LJ;
    M1 = 0;
    M2 = I2S;

// AD1852 Stereo DAC input serial Interface mode select.  NOTE that the DAC requires serial
programing for
// RJ20, RJ18, RJ16 mode.  Since AD1896 EVB does not allow serial programming of the AD1852
registers,
// AD1852 will be configured in RJ24 mode when AD1896 output port is configured in RJ20, RJ18

and RJ16 mode.


    IDPM1 = LJ;
    IDPM0 = I2S;

// AD1896, DIR, DIT, AD1852 MCLK control logic.  Based on the Master/Slave operation of the
AD1896 in/out ports,
// 33.8688MHz crystal frequency will be divided by either 1, 2 or 3 and the ouput of the di-
vider is feed into the DAC and DIT.
// On-board 12.288MHz clock oscillator is enabled only when input and ouput serial ports are
configured in SLAVE mode.

   OSC_EN  = (BOTH_SLAVE);
   SLVCLK1 = (O_MAS_768) # (BOTH_SLAVE);
   SLVCLK0 = (O_MAS_512) # (BOTH_SLAVE);
   DIV2_3  = (!O_MAS_512) & (O_MAS_768);

// IO control logic for bi-directional signals

   DDO_SCLK.OE  = (O_MAS_768 # O_MAS_512 # O_MAS_256);
   DDO_LRCLK.OE = (O_MAS_768 # O_MAS_512 # O_MAS_256);
   SCLK_O.OE    = (BOTH_SLAVE # MATCH_PHASE # IN_MAS_768 # IN_MAS_512 # IN_MAS_256);
   LRCLK_O.OE   = (BOTH_SLAVE # MATCH_PHASE # IN_MAS_768 # IN_MAS_512 # IN_MAS_256);

// AD1896 ASRC Output Serial port signals

   DDO_SDATA =  SDATA_O;
   DDO_SCLK  = ISCLK;
   DDO_LRCLK = ILRCLK;

   SCLK_O    = ISCLK;
   LRCLK_O   = ILRCLK;

// DAC AND DIT SIGNALS

   SDATA_DAC_DIT = SDATA_O;
   LRCLK_DAC     = ILRCLK;
```

```
   SCLK_DAC      = ISCLK;

   FSYNC_DIT     = ILRCLK;
   SCLK_DIT      = ((!ISCLK) & (LJ # RJ24 # RJ20 # RJ18 # RJ16))  # (ISCLK & I2S);

// Internal node signals

                                        out_pld.abl

 ISCLK   =  ((SCLK_O) & (O_MAS_768 # O_MAS_512 # O_MAS_256))
             # ((DDO_SCLK) & (BOTH_SLAVE # MATCH_PHASE # IN_MAS_768 # IN_MAS_512 #
IN_MAS_256));
    ILRCLK  =  ((LRCLK_O) & (O_MAS_768 # O_MAS_512 # O_MAS_256))
             # ((DDO_LRCLK) & (BOTH_SLAVE#MATCH_PHASE#IN_MAS_768#IN_MAS_512#IN_MAS_256) & (LJ
# TDM # RJ24 # RJ20 # RJ18 # RJ16))
             # ((!DDO_LRCLK) & (BOTH_SLAVE#MATCH_PHASE#IN_MAS_768#IN_MAS_512#IN_MAS_256) &
(I2S));

"=============================================================================
END IF_Logic
```

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