TEXAS INSTRUMENTS

TAS3103

Digital Audio Processor With 3D Effects

Data Manual (Preliminary)

August 2002

Digital Audio Solutions

SLES038

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1 Introduction

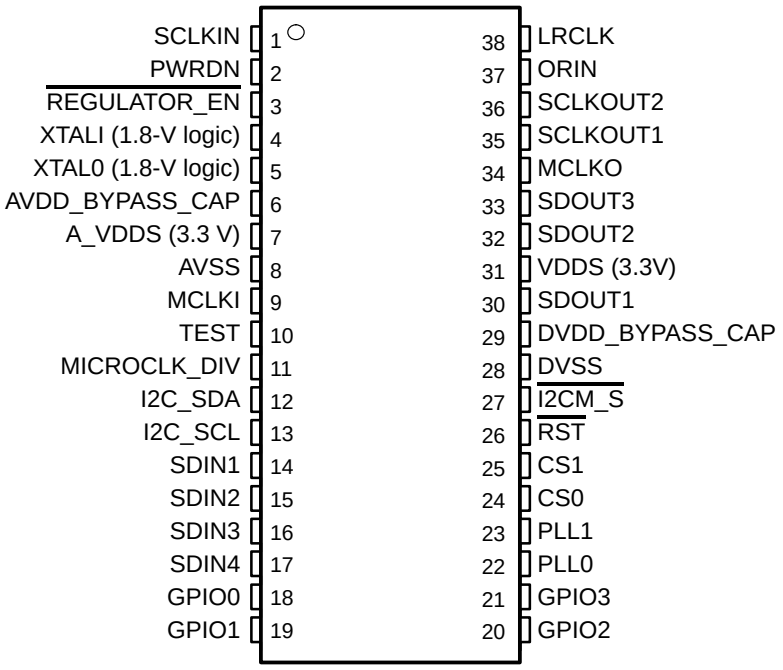
The TAS3103 is a fully configurable digital audio processor that preserves high-quality audio by using a 48-bit data path, 28-bit filter coefficients, and a single cycle 28 x 48-bit multiplier and 76-bit accumulator. Because of the coefficient-configurable fixed-program architecture of the TAS3103, a complete set of user-specific audio processing functions can be realized, with short development times, in a small, low power, low-cost device. A personal computer (PC) GUI-based software development package and a comprehensive evaluation board provide additional facilities to further reduce development times. The TAS3103 uses 1.8-V core logic with 3.3-V I/O buffers, and requires only 3.3-V power. The TAS3103 is available in a 38-pin TSSOP package.

1.1 Features

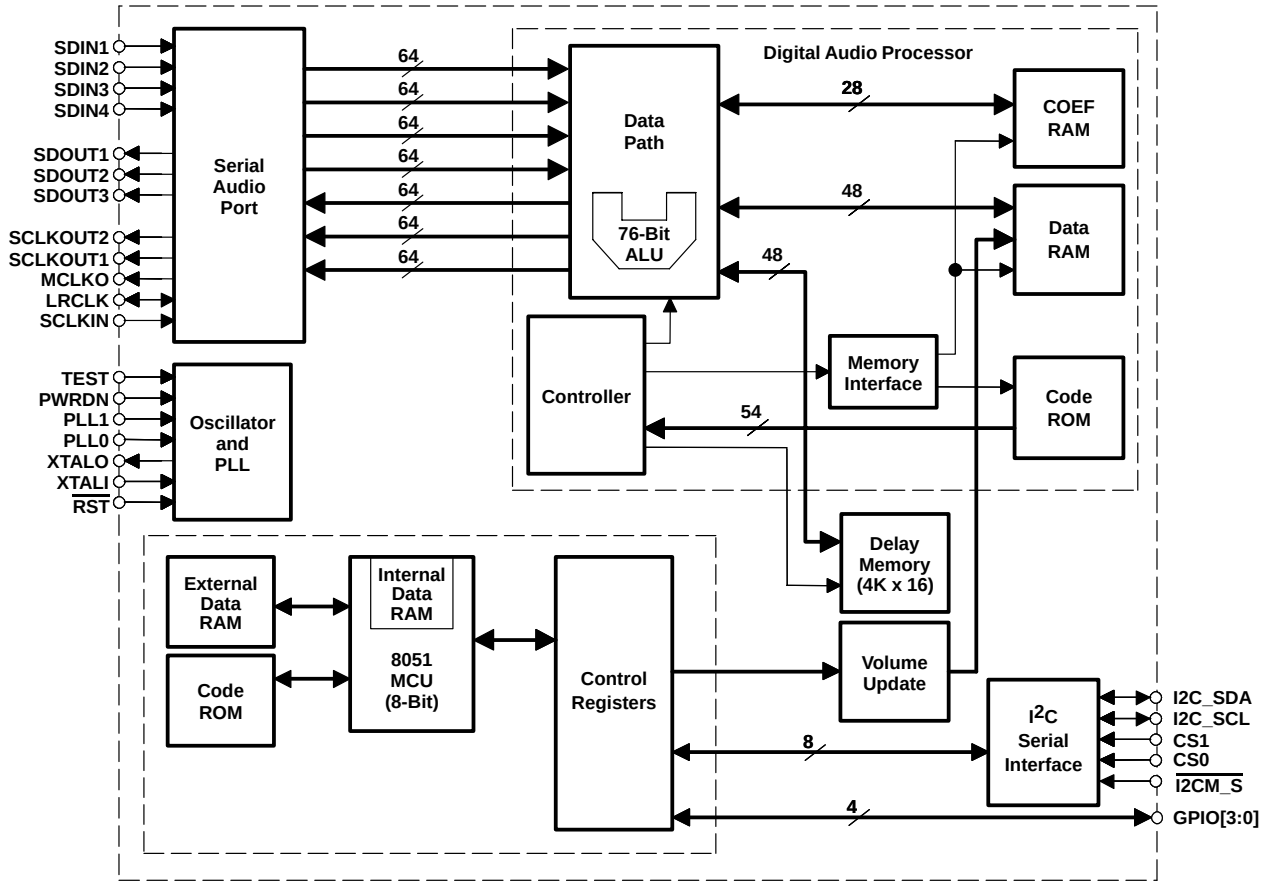
- Audio Input/Output
  - Four Serial Audio Input Channels
  - Three Serial Audio Output Channels
  - 8-kHz to 96-kHz Sample Rates Supported
  - 15 Stereo/TDM Data Formats Supported
  - Input/Output Data Format Selections Independent
  - 16-, 18-, 20-, 24-, and 32-Bit Word Sizes Supported
- Serial Master/Slave I^2C Control Channel
- Three Independent Monaural Processing Channels
  - Programmable Six Input Digital Mixer
  - 3D Effect and Reverb Structure and Filters
  - Programmable 12 Band Digital Parametric EQ
  - Programmable Digital Bass and Treble Controls
  - Programmable Digital Soft Volume Control (24 dB to –-∞ dB)
  - Soft Mute/Unmute
  - Programmable Dither
  - Programmable Loudness Compensation
  - VU Meter and Spectral Analysis I^2C Output
  - Programmable Channel Delay (Up to 42 ms at 48 kHz)
  - 192-dB Dynamic Range (Supports Up to 32-Bit Audio Data)
  - Dual Threshold Dynamic Range Compression/Expansion
- Electrical and Physical
  - Single 3.3-V Power Supply
  - 38-Pin TSSOP Package
  - Low Power Standby

1.2 Terminal Assignments

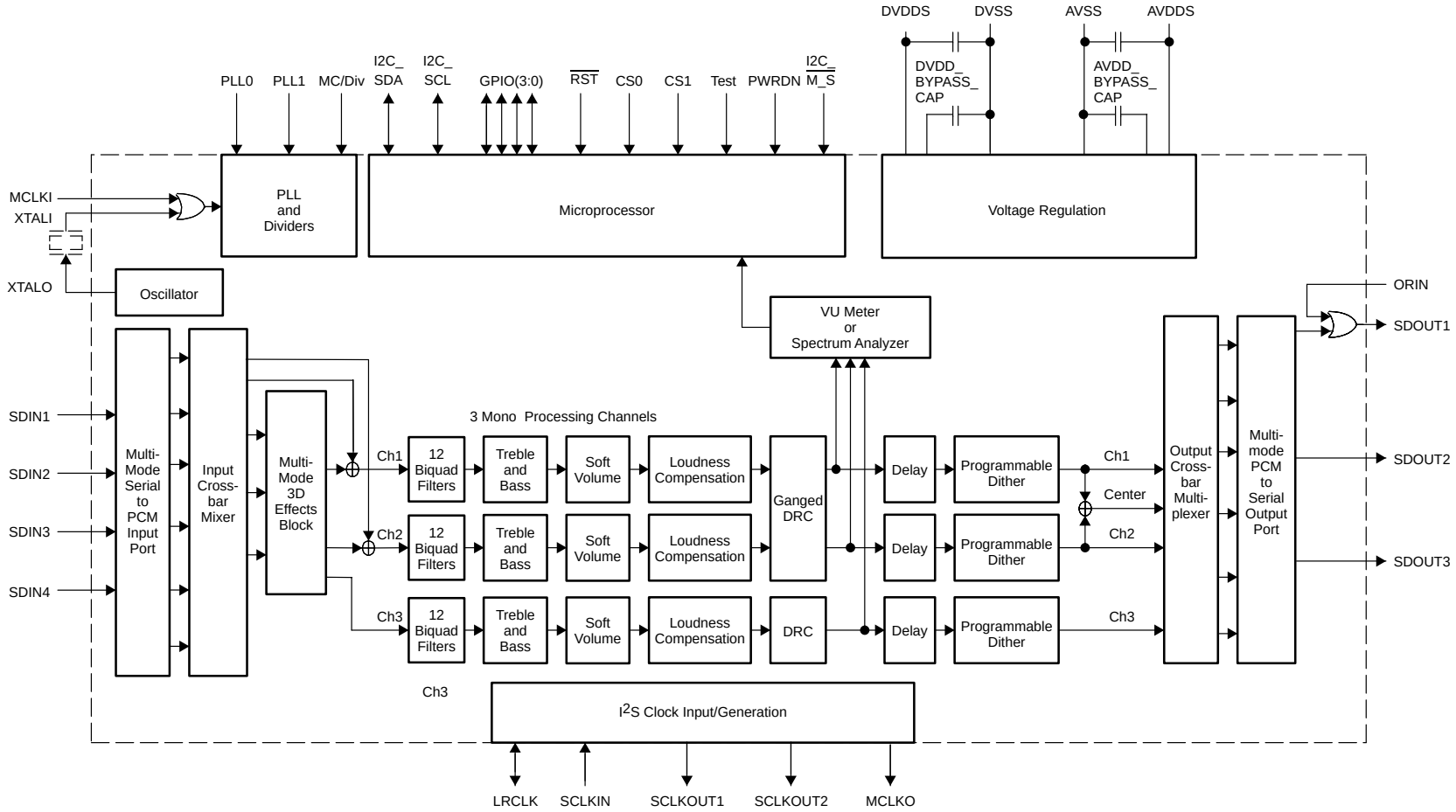
DBT PACKAGE
(TOP VIEW)



1.3 Hardware Block Diagram



1.4 Functional Block Diagram



1.5 Ordering Information

T_A	PLASTIC 38-PIN TSSOP (DBT)
0°C to 70°C	TAS3103DBT

1.6 Terminal Functions

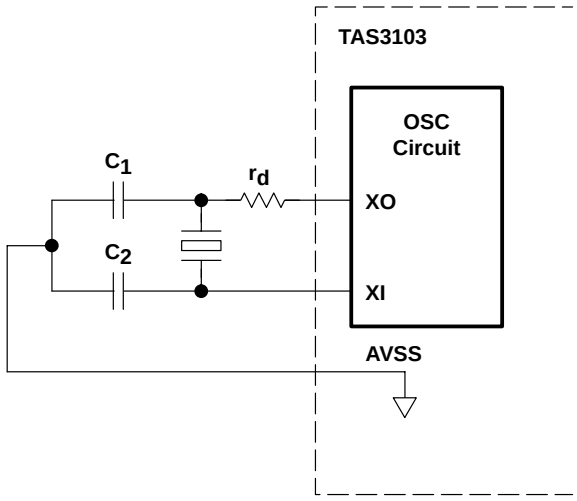
TERMINAL				DESCRIPTION	PULLUP/ DOWN(2)
NAME	NO.	I/O	TYPE(1)		
A_VDSS (3.3V)	7		PWR	The PWR pin is used to input 3.3-V power to the DPLL and clock isolator. This pin can be connected to the same power source used to drive the DVSS power pin. To achieve low DPLL jitter, this pin should be bypassed to AVSS with a 0.01-μF capacitor (low ESR preferable).	None
AVDD_BYPASS_CAP	6		PWR	AVDD_BYPASS_CAP is a pinout of the internally regulated 1.8-VDC power used by the DPLL and crystal oscillator. This pin should be connected to pin 8 with a 0.01-μF capacitor (low ESR preferable). This pin must not be used to power external devices.	None
AVSS	8		PWR	AVSS is the ground reference for the internal DPLL and oscillator circuitry. This pin needs to reference the same ground as DVSS power pin. To achieve low DPLL jitter, ground noise at this pin must be minimized. The availability of the AVSS pin allows a designer to use optimizing techniques such as star ground connections, separate ground planes, or other quiet ground distribution techniques to achieve a quiet ground reference at this pin.	None
CS0	24	I	D	CS0 is the LSB of a 2-bit code used to generate part of an I^2C device address that makes it possible to address four TAS3103 ICs on the same bus without additional chip select logic. The pulldowns on the inputs select 00 as a default when neither pin is connected.	Pulldown
CS1	25	I	D	CS1 is the MSB of a 2-bit code used to generate part of an I^2C device address that makes it possible to address four TAS3103 ICs on the same bus without additional chip select logic.	Pulldown
DVDD_BYPASS_CAP	29		PWR	DVDD_BYPASS_CAP is a pin-out of the internally regulated 1.8-V power used by all internal digital logic. A low ESR capacitor in the range of 0.01 μF should be connected between this pin and pin 28. This pin must not be used to power external devices	None
DVSS	28		PWR	DVSS is the digital ground pin.	None
GPIO0	18	I/O	D	GPIO0 is a general-purpose I/O, controlled by the internal microprocessor through I^2C commands. When in the I^2C master mode, GPIO0 serves as a volume up command for CH1/CH2	Pullup
GPIO1	19	I/O	D	GPIO1 is a general-purpose I/O, controlled by the internal microprocessor through I^2C commands. When in the I^2C master mode, GPIO1 serves as a volume down command for CH1/CH2	Pullup
GPIO2	20	I/O	D	GPIO2 is a general-purpose I/O, controlled by the internal microprocessor through I^2C commands. When in the I^2C master mode, GPIO2 serves as a volume up command for CH3	Pullup
GPIO3	21	I/O	D	GPIO3 is a general-purpose I/O, controlled by the internal microprocessor through I^2C commands. When in the I^2C master mode, GPIO3 serves as a volume down command for CH3	Pullup
$\overline{\text{I2CM\_S}}$	27	I	D	$\overline{\text{I2CM\_S}}$ is a non-latched input that determines whether the TAS3103 acts as an I^2C master or slave. Logic high, or no connection, sets the TAS3103 as an I^2C master device. A logic low sets the TAS3103 as an I^2C slave device. As a master I^2C device, the TAS3103 I^2C port must have access to an external EEPROM for input.	Pullup

TERMINAL				DESCRIPTION	PULLUP/ DOWN(2)
NAME	NO.	I/O	TYPE(1)		
I2C_SCL	13	I/O	D	I2C_SCL is the I^2C clock pin. When the TAS3103 I^2C port is a master, I2C_SCL is $(1/2^N)$ x (1/(M+1)) times the microprocessor clock, where N and M are parameters retrieved from the EEPROM at initialization. When the TAS3103 I^2C port is a slave, input clock rates up to 400 kHz can be supported. This pin must be provided by an external pullup (10 kΩ is recommended for most applications).	External pullup required
I2C_SDA	12	I/O	D	I2C_SDA is the I^2C bidirectional data pin. The TAS3103 I^2C port can support data rates up to 400K bits/sec. This pin must be provided an external pullup (10 kΩ is recommended for most applications).	External pullup required
LRCLK	38	I/O	D	LRCLK is either an input or an output, depending on whether the TAS3103 is in a master or slave serial audio port mode.	Pulldown
MCLKI	9	I	D	MCLKI is a master clock input that provides an alternative to using a fixed crystal frequency. In DPLL modes, the input frequency of this clock can range from 2.8 MHz to 24.576 MHz. In PLL bypass mode, frequencies up to 147 MHz can be used. Whenever MCLKI is not used and XTALI/XTALO provide the master clock input, MCLKI must be grounded.	None
MCLKO	34	O	D	MCLKO is the master output clock pin. It is produced by dividing MCLKI/XTALI by 1, 2, or 4 (depending on the setting of a subaddress control field). MCLKO is provided to interconnect, without the need for additional glue logic, the TAS3103 interfaces chips that require different multiples of the audio sample rate (F_S) as a master clock.	None
MICROCLK_DIV	11	I	D	MICROCLK_DIV sets the division ratio between the digital audio processing clock and the internal microprocessor clock. The audio-processing clock is the DPLL output clock if PLL_bypass is not enabled. The audio-processing clock is MCLKI/XTALI master clock if PLL_bypass is enabled. Logic high on this pin sets the microprocessor clock equal to the audio-processing clock. A logic low sets the microprocessor clock to 1/4 the digital audio-processing clock. MICROCLK_DIV must be set low if the audio processing clock is > 36 MHz. MICROCLK_DIV must be set high if the audio processing clock is ≤ 36 MHz.	Pulldown
ORIN	37	I	D	ORIN allows the processing of a multichannel signal set through two TAS3103s without any additional components. One use of ORIN would be to fully emulate a 6-channel audio processor at speeds up to a 96-kHz sample rate with only two TAS3103s and no glue logic. The two-chip configuration is accomplished by wiring the SDOUT1 port of one of the two TAS3103 chips to the ORIN port of the second TAS3103. Internal to the chip, the ORIN input is OR'ed with internal SDOUT1 data to generate the resulting output data on channel SDOUT1. For TDM output formats, the SDOUT1 outputs of the two chips differ in phasing in both the left and right channels to arrive at the proper composite output. For discrete outputs, one chip contributes the left channel of the composite SDOUT1, and the other chip contributes the right channel of the composite SDOUT1. If not used, ORIN must be connected to ground.	Pulldown
PLL0	22	I	D	PLL0 is the LSB of a 2-bit code used to select four different modes of DPLL multiplexer/input divider operation. PLL[1:0] values of 00, 01, and 10 select the DPLL input clock to be MCLKI/XTALI divided by 1, 2, and 4 respectively. A value of 11 results in MCLKI/XTALI being substituted for the DPLL output. The pullup/pulldown combination provides a default of 01 when neither pin is connected.	Pullup
PLL1	23	I	D	PLL1 is the MSB of a 2-bit code used to select four different modes of DPLL multiplexer/input divider operation. PLL[1:0] values of 00, 01, and 10 select the DPLL input clock to be MCLKI/XTALI divided by 1, 2, and 4 respectively. A value of 11 results in MCLKI/XTALI being substituted for the DPLL output. The pullup/pulldown combination provides a default of 01 when neither pin is connected.	Pulldown

TERMINAL				DESCRIPTION	PULLUP/ DOWN(2)
NAME	NO.	I/O	TYPE(1)		
PWRDN	2	I	D	PWRDN powers down all logic and stops all clocks whenever logic high is applied. However, the coefficient memory remains stable through a power down cycle, as long as a reset is not sent after a power down cycle.	Pulldown
$\overline{\text{REGULATOR\_EN}}$	3	I	D	$\overline{\text{REGULATOR\_EN}}$ is only used in factory tests. This pin should always be tied to ground.	None
$\overline{\text{RST}}$	26	I	D	$\overline{\text{RST}}$ is the master reset input. Applying a logic low to this pin generates a master reset. The master reset results in all coefficients being set to their power-up default state, all data memories being cleared, and all logic signals being returned to their default values.	Pullup
SCLKIN	1	I	D	SCLKIN is the serial audio port (SAP) input data clock. This clock is only used when the SAP is a slave. In master mode, SCLKOUT1 internally provides the serial input clock (SCLKOUT1 from a given TAS3103 must not be connected to SCLKIN on the same TAS3103 chip).	Pulldown
SCLKOUT1	35	O	D	SCLKOUT1 is one of two serial output bit clocks. It is divided from MCLKI/XTALI in master mode, and SCLKIN in slave mode. Subaddress control fields determine the divide ratio in both cases. When the serial audio port is in a master mode, SCLKOUT1 is used to receive incoming serial data and should be wired to the data source(s) providing data to the SDIN inputs.	None
SCLKOUT2	36	O	D	SCLKOUT2 is one of two serial output bit clocks. It is divided from MCLKI/XTALI in master mode, and SCLKIN in slave mode. Subaddress control fields determine the divide ratio in both cases. SCLKOUT2 is always used to clock out serial data from the three serial SDOUT output data channels. SCLKOUT2 is provided separately from SCLKOUT1 to allow discrete in to TDM out and TDM in to discrete out data format conversions without the use of external glue logic.	Output
SDIN1	14	I	D	SDIN1, SDIN2, SDIN3, and SDIN4 are the four TAS3103 serial data input ports. All four input ports support four discrete (stereo) data formats. SDIN1 is the only data input port that also supports eleven time division multiplexed data formats. All four ports are capable of receiving data with bit rates up to 24.576 MHz.	Pulldown
SDIN2	15	I	D	SDIN2 is one of the four TAS3103 serial data input ports. SDIN2 supports four discrete (stereo) data formats, and is capable of receiving data with bit rates up to 24.576 MHz.	Pulldown
SDIN3	16	I	D	SDIN3 is one of the four TAS3103 serial data input ports. SDIN4 supports four discrete (stereo) data formats, and is capable of receiving data with bit rates up to 24.576 MHz.	Pulldown
SDIN4	17	I	D	SDIN4 is one of the four TAS3103 serial data input ports. SDIN4 supports four discrete (stereo) data formats, and is capable of receiving data with bit rates up to 24.576 MHz.	Pulldown
SDOUT1	30	O	D	SDOUT1, SDOUT2, and SDOUT3 are the three TAS3103 serial data output ports. All three output ports support four discrete (stereo) data formats. SDOUT1 is the only data output port that also supports eleven time division multiplexed data formats. All three ports are capable of outputting data at bit rates up to 24.576 MHz.	None
SDOUT2	32	O	D	SDOUT2 is one of the three serial data output ports. SDOUT2 supports four discrete (stereo) data formats, and is capable of outputting data at bit rates up to 24.576 MHz.	None
SDOUT3	33	O	D	SDOUT3 is one of the three serial data output ports. SDOUT3 supports four discrete (stereo) data formats, and is capable of outputting data at bit rates up to 24.576 MHz.	None
TEST	10	I	D	TEST is only used in factory tests. This pin must be left unconnected or grounded.	Pulldown

TERMINAL				DESCRIPTION	PULLUP/ DOWN(2)
NAME	NO.	I/O	TYPE(1)		
VDDS (3.3 V)	31	-	PWR	VDDS is the 3.3-V pin that powers (1) the 1.8 V internal power regulator used to supply logic power to the chip and (2) the I/O ring. It is recommended that this pin be bypassed to DVSS (pin 28) with a low ESR capacitor in the range of 0.01 μF.	None
XTALI	4	I	A	XTALO and XTALI provide a master clock for the TAS3103 via use of an external fundamental mode crystal. XTALI is the 1.8-V input port for the oscillator circuit. See Note 3 for recommended crystal type and accompanying circuitry. This pin should be grounded when the MCLKI pin is used as the source for the master clock.	None
XTALO	5	O	A	XTALO and XTALI provide a master clock for the TAS3103 via use of an external fundamental mode crystal. XTALO is the 1.8-V output drive to the crystal. XTALO can support crystal frequencies between 2.8 MHz and 20 MHz. See Note 3 for recommended crystal type and accompanying circuitry. This pin should be left unconnected in applications using an external clock input to MCLKI	None

NOTES: 1. TYPE: A = analog; D = 3.3-V digital; PWR = power/ground/decoupling
2. All pullups are 20-μA weak pullups, and all pulldowns are 20-μA weak pulldowns. The pullups and pulldowns are included to assure proper input logic levels if the pins are left unconnected (pullups => logic 1 input; pulldowns => logic 0 input). Devices that drive inputs with pullups must be able to sink 20 μA while maintaining a logic 0 drive level. Devices that drive inputs with pulldowns must be able to source 20 μA while maintaining a logic 1 drive level.
3. Crystal type and recommended circuit:



- Crystal type = parallel-mode, fundamental-mode crystal
- r_d = drive level control resistor—vendor specified
- C_L = Crystal load capacitance (capacitance of circuitry between the two terminals of the crystal)
- $C_L = (C_1 \times C_2) / (C_1 + C_2) + C_S$ (where C_S = board stray capacitance ~2 pF)
  - Example: Vendor recommended C_L = 18 pF, C_S = 3 pF $\Rightarrow C_1 = C_2 = 2 \times (18 - 3) = 30$ pF

1.7 Operational Modes

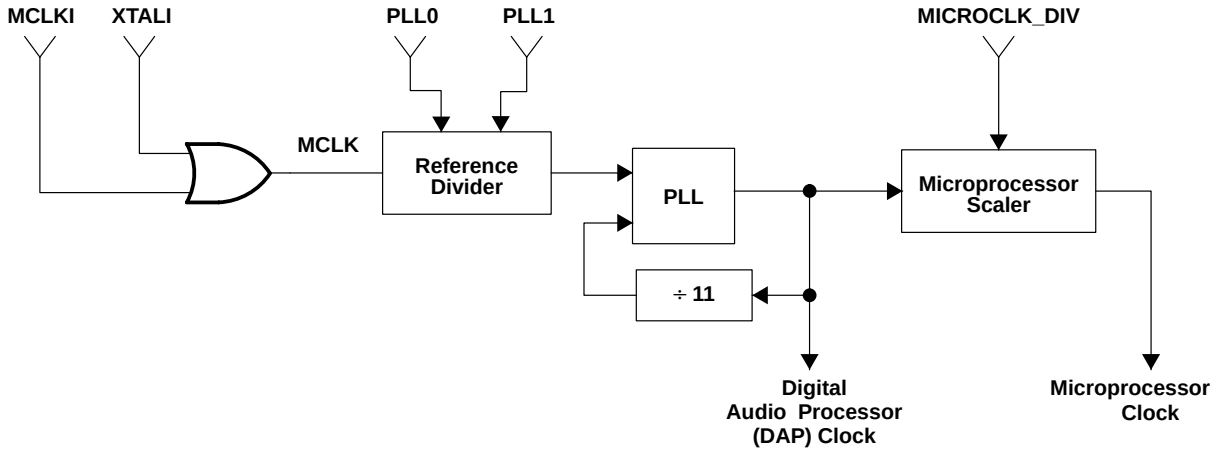
The TAS3103 operation is governed by I/O terminal voltage level settings and register / coefficient settings within the TAS3103. The terminal settings are wholly sufficient to address all external environments - allowing the remaining configuration settings to be determined by either I^2C commands or by the content of an I^2C serial EEPROM (when the I^2C master mode is selected).

1.7.1 Terminal-Controlled Modes

1.7.1.1 Clock Control

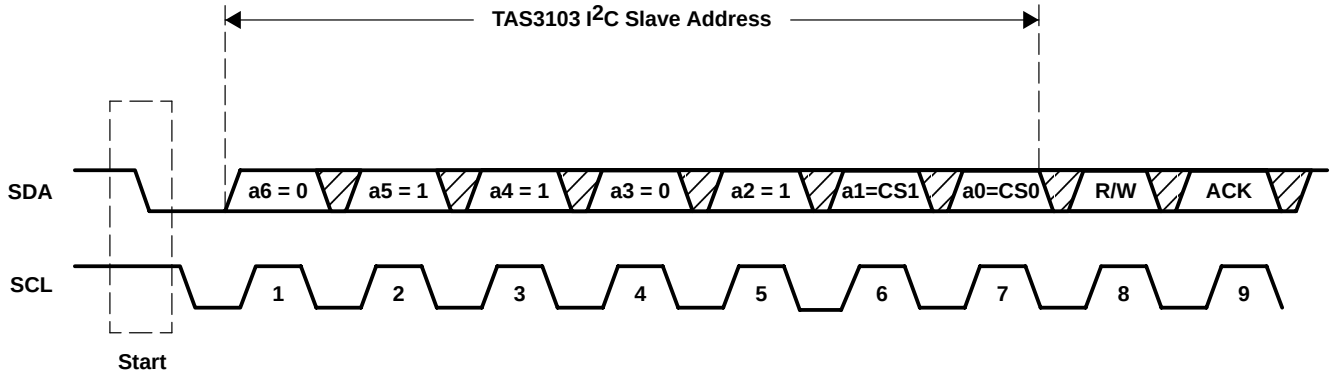
PLL1	PLL0	DAP Clock
0	0	11 MCLK
0	1	(11 MCLK)/2
1	0	(11 MCLK)/4
1	1	MCLK (PLL bypass)

MICROCLK_DIV	MICROPROCESSOR CLOCK
0	DAP clock/4
1	DAP clock



1.7.1.2 I²C Bus Setup

$\overline{\text{I2CM\_S}}$	I²C BUS MODE
0	Slave
1	Master

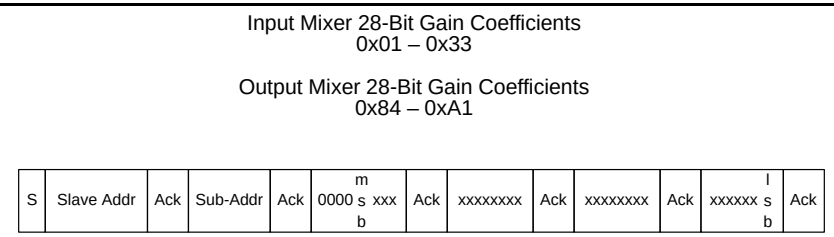


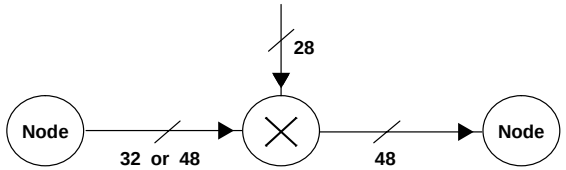
1.7.1.3 Power-Down/Sleep Selection

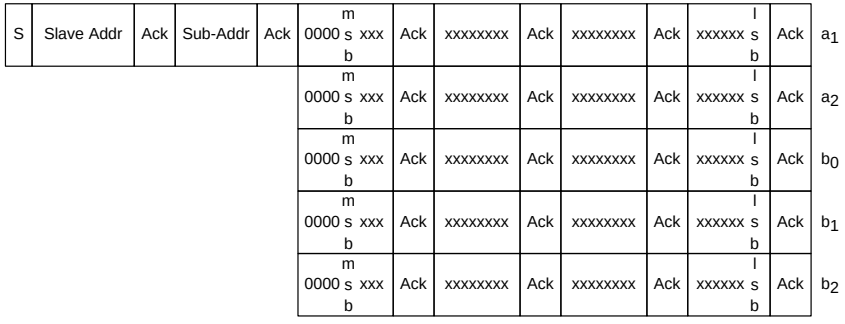
PWRDN	POWER STATUS
0	Active
1	Power-down/sleep

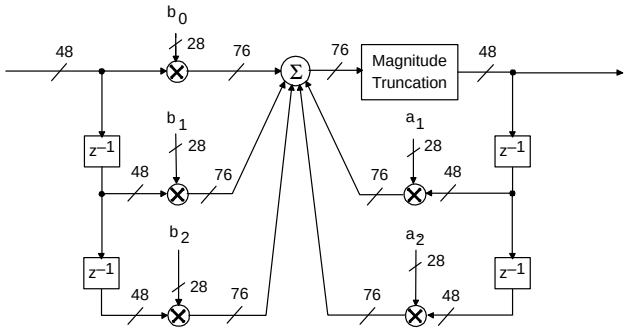
1.7.2 I²C Bus-Controlled Modes

SUBADDRESS(es)	PARAMETER(s)
0x00 – Starting I²C Check Word 0xFC – Ending I²C Check Word	• Check words apply to I²C master mode only • In master I²C mode, the two check words are compared after EEPROM download. If comparison fails, a second attempt is made. If the second comparison fails, the parameters default to the slave default values. • In slave I²C mode, the default value for both check words is: 0x81_42_24_18
Input Mixer 28-Bit Gain Coefficients 0x01 – 0x33 Output Mixer 28-Bit Gain Coefficients 0x84 – 0xA1	**Gain Coefficient (Format = 5.23)**
Effects Block BiQuad Filter Coefficients 0x34–0x4B	NOTE: All gain coefficients 5.23 numbers.
Reverberation Block Gains	

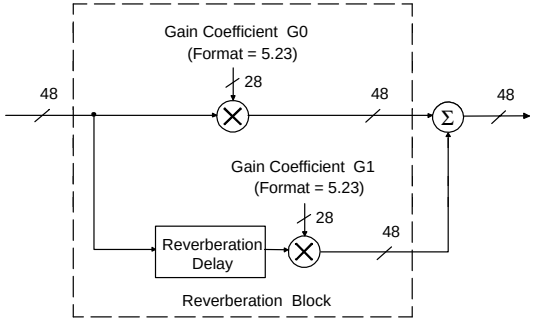








Reverberation Block	Subaddress
Channel 1	0x4C
Channel 2	0x4D
Channel 3	0x4E

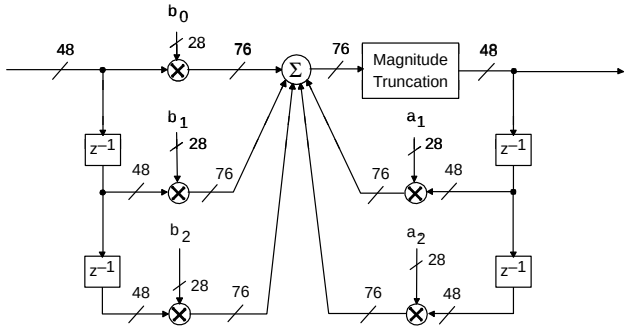


SUBADDRESS(es)	PARAMETER(s)

Cascaded (Twelve/Channel) Main Filter BiQuads

MAIN FILTER BLOCK	Subaddress
Channel 1	0x4F–0x5A
Channel 2	0x5B–0x66
Channel 3	0x67–0x72

S	Slave Addr	Ack	Sub-Addr	Ack	m 0000 s xxx b	Ack	xxxxxxxx	Ack	xxxxxxxx	Ack	xxxxxx l s b	Ack	
					m 0000 s xxx b	Ack	xxxxxxxx	Ack	xxxxxxxx	Ack	xxxxxx l s b	Ack	a_1
					m 0000 s xxx b	Ack	xxxxxxxx	Ack	xxxxxxxx	Ack	xxxxxx l s b	Ack	a_2
					m 0000 s xxx b	Ack	xxxxxxxx	Ack	xxxxxxxx	Ack	xxxxxx l s b	Ack	b_0
					m 0000 s xxx b	Ack	xxxxxxxx	Ack	xxxxxxxx	Ack	xxxxxx l s b	Ack	b_1
					m 0000 s xxx b	Ack	xxxxxxxx	Ack	xxxxxxxx	Ack	xxxxxx l s b	Ack	b_2

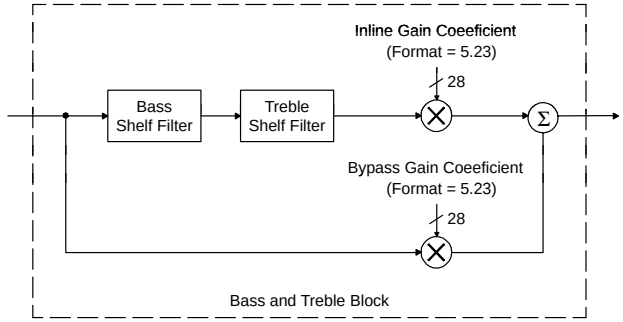


NOTE: All gain coefficients 5.23 numbers

Bass and Treble Gain Coefficients

Channel 1 = 0x73
Channel 2 = 0x74
Channel 3 = 0x75

S	Slave Addr	Ack	Sub-Addr	Ack	m 0000 s xxx b	Ack	xxxxxxxx	Ack	xxxxxxxx	Ack	xxxxxx l s b	Ack	
					m 0000 s xxx b	Ack	xxxxxxxx	Ack	xxxxxxxx	Ack	xxxxxx l s b	Ack	Bypass Gain
					m 0000 s xxx b	Ack	xxxxxxxx	Ack	xxxxxxxx	Ack	xxxxxx l s b	Ack	Inline Gain



Dynamic Range Control (DRC) Mixer Coefficients

S	Slave Addr	Ack	Sub-Addr	Ack	m 0000 s xxx b	Ack	xxxxxxxx	Ack	xxxxxxxx	Ack	xxxxxx l s b	Ack

S	Slave Addr	Ack	Sub-Addr	Ack	m 0000 s xxx b	Ack	xxxxxxxx	Ack	xxxxxxxx	Ack	xxxxxx l s b	Ack	
					m 0000 s xxx b	Ack	xxxxxxxx	Ack	xxxxxxxx	Ack	xxxxxx l s b	Ack	Word2

Word1

CH1
- 0x76 = Mix u to i
- 0x79 = Mix j to i

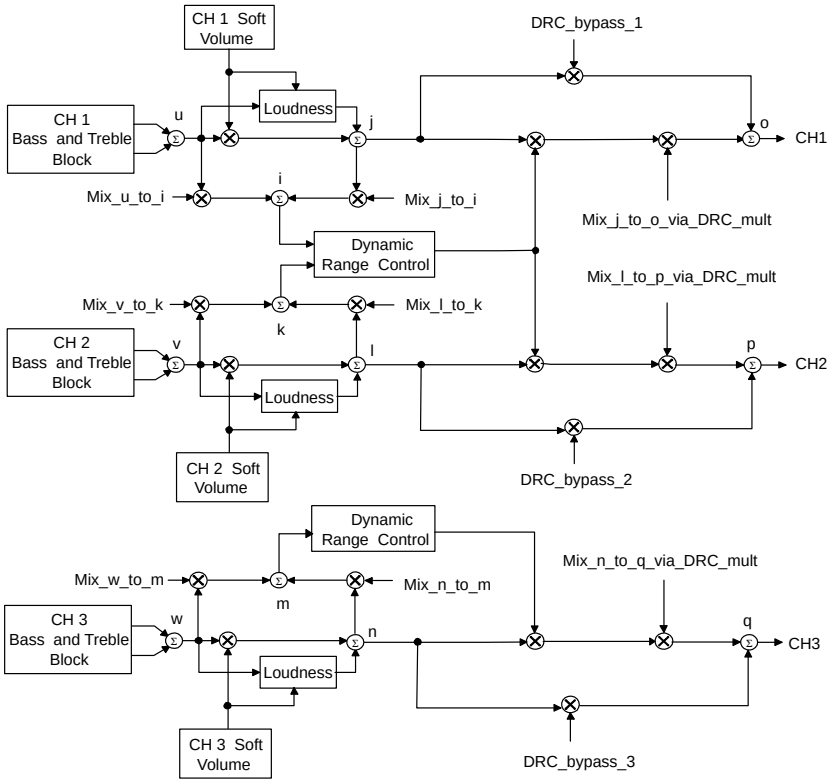
CH2
- 0x77 = Mix v to k
- 0x7A = Mix l to k

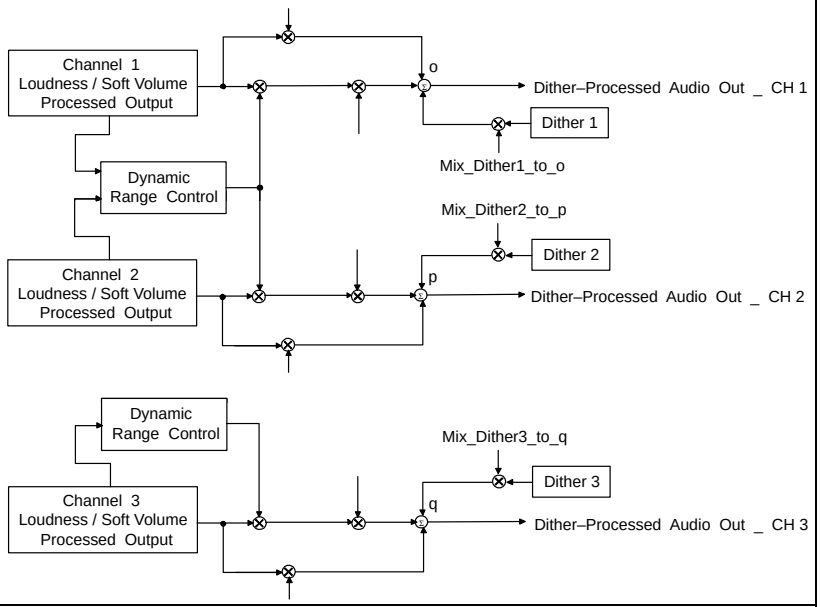
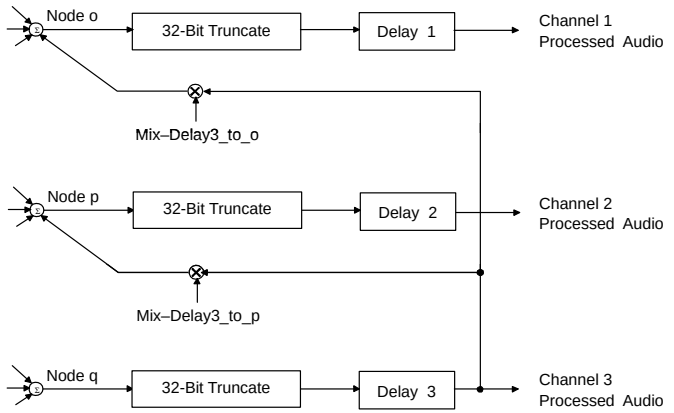
CH3
- 0x78 = Mix w to m
- 0x7B = Mix n to m

CH1– 0x7C
- Word 1 = Mix j to o – Inline
- Word 2 = Mix j to o – Bypass

CH2– 0x7D
- Word 1 = Mix l to p – Inline
- Word 2 = Mix l to p – Bypass

CH1– 0x7E
- Word 1 = Mix n to q – Inline
- Word 2 = Mix n to q – Bypass



SUBADDRESS(es)	PARAMETER(s)
Dither Mix Gain Coefficients S | Slave Addr | Ack | Sub-Addr | Ack | 0000 s xxx m b | Ack | xxxxxxxx | Ack | xxxxxxxx | Ack | xxxxxx s l b | Ack Channel 1 0x7F = Mix Dither 1 to o – 28-Bit Coefficient Channel 2 0x80 = Mix Dither 2 to p – 28-Bit Coefficient Channel 3 0x81 = Mix Dither 3 to q – 28-Bit Coefficient	
Channel 3 to Channel 1 and Channel 2 Mix Gain Coefficients S | Slave Addr | Ack | Sub-Addr | Ack | 0000 s xxx m b | Ack | xxxxxxxx | Ack | xxxxxxxx | Ack | xxxxxx s l b | Ack Channel 1 0x82 = Mix Channel 3 Output to o – 28-Bit Coefficient Channel 2 0x83 = Mix Channel 3 Output to p – 28-Bit Coefficient	

Soft Volume and Loudness Subaddress

Soft Volume

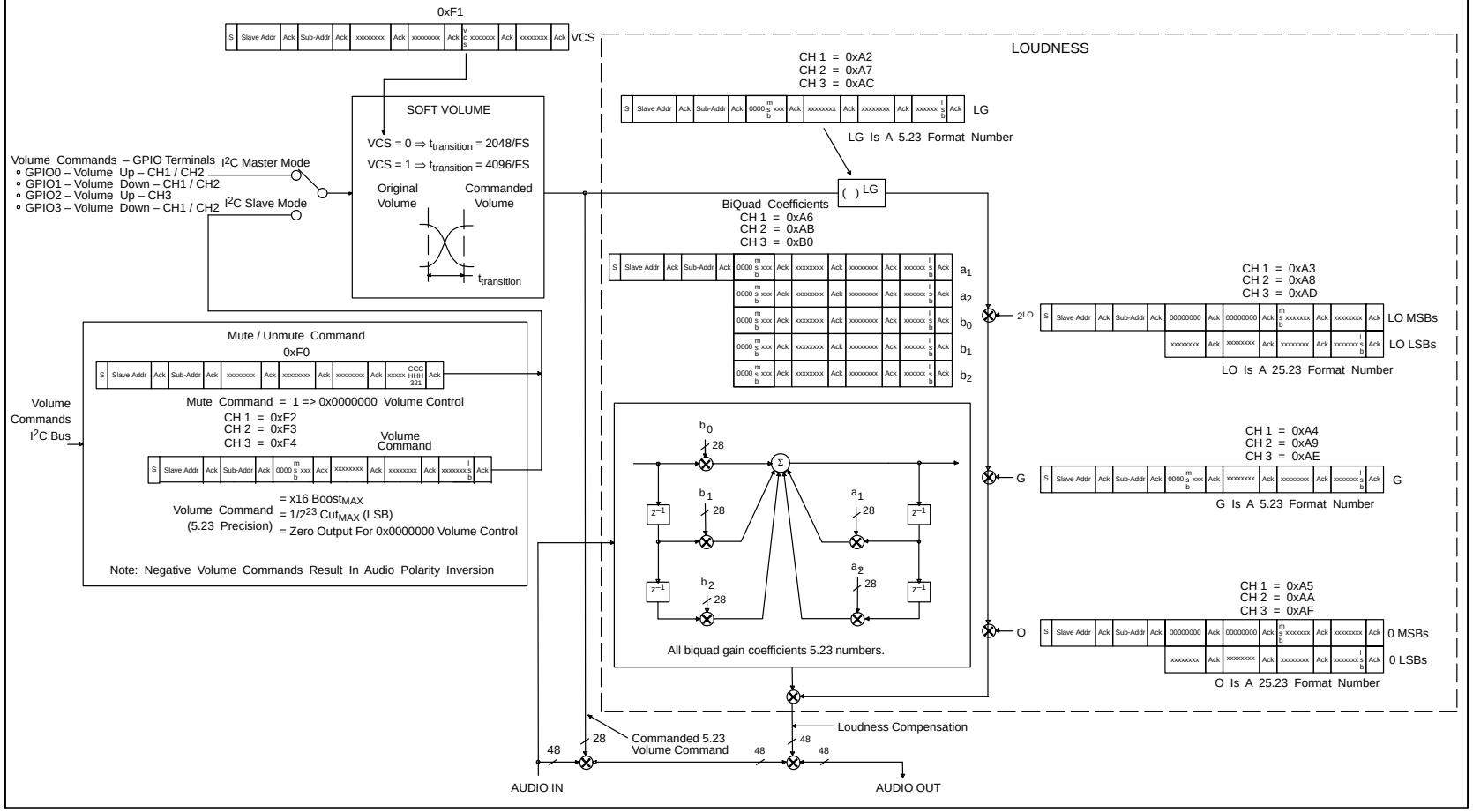
- Mute/Unmute = 0xF0
- Volume Slew Command = 0xF1

Volume Command

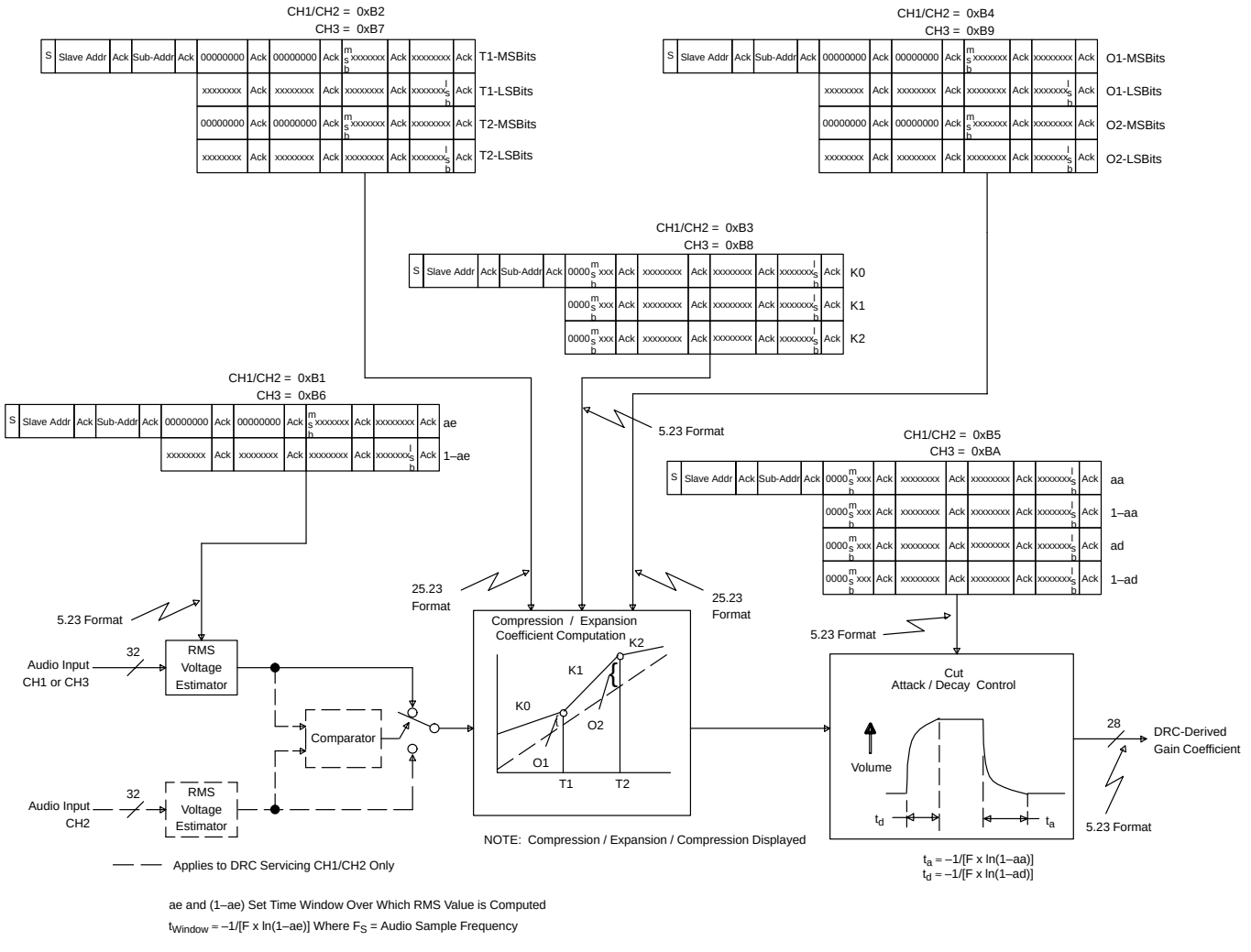
Parameter	Subaddress		
	CH1	CH2	CH3
Volume Command	0xF2	0xF3	0xF4

Loudness

Parameter	Subaddress		
	CH1	CH2	CH3
LG	0xA2	0xA7	0xAC
LO	0xA3	0xA8	0xAD
G	0xA4	0xA9	0xAE
O	0xA5	0xAA	0xAF
BiQuad	0xA6	0xAB	0xB0



Subaddress — Dynamic Range Control (DRC) Block



Spectrum Analyzer/VU Meter

BiQuad 1 to 10 Subaddresses = 0xBC to 0xC5

S	Slave Addr	Ack	Sub-Addr	Ack	0000 msb xxx	Ack	xxxxxxxx	Ack	xxxxxxxx	Ack	xxxxxxx lsb	Ack	
					0000 msb xxx	Ack	xxxxxxxx	Ack	xxxxxxxx	Ack	xxxxxxx lsb	Ack	a_1
					0000 msb xxx	Ack	xxxxxxxx	Ack	xxxxxxxx	Ack	xxxxxxx lsb	Ack	a_2
					0000 msb xxx	Ack	xxxxxxxx	Ack	xxxxxxxx	Ack	xxxxxxx lsb	Ack	b_0
					0000 msb xxx	Ack	xxxxxxxx	Ack	xxxxxxxx	Ack	xxxxxxx lsb	Ack	b_1
					0000 msb xxx	Ack	xxxxxxxx	Ack	xxxxxxxx	Ack	xxxxxxx lsb	Ack	b_2

RMS Window Time Constant Subaddress = 0xBB

S	Slave Addr	Ack	Sub-Addr	Ack	0000 msb xxx	Ack	xxxxxxxx	Ack	xxxxxxxx	Ack	xxxxxxx lsb	Ack	
					0000 msb xxx	Ack	xxxxxxxx	Ack	xxxxxxxx	Ack	xxxxxxx lsb	Ack	asa
					0000 msb xxx	Ack	xxxxxxxx	Ack	xxxxxxxx	Ack	xxxxxxx lsb	Ack	1–asa

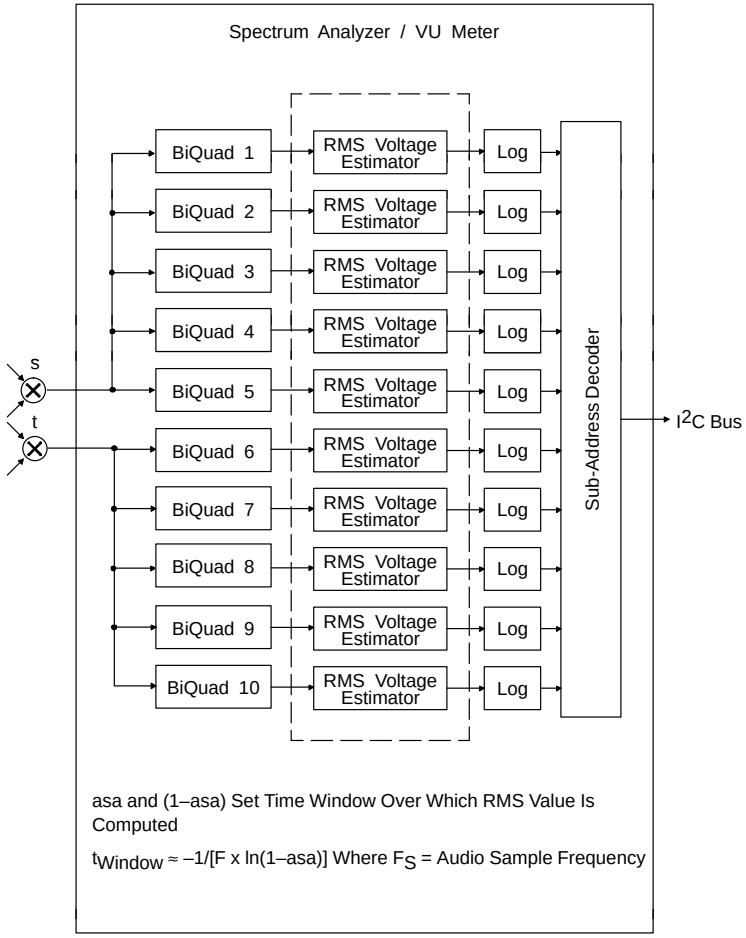
Spectrum Analyzer Output Subaddress = 0xFD

S	Slave Addr	Ack	Sub-Addr	Ack	xxxxx.xxx	Ack	
					xxxxx.xxx	Ack	BiQuad 1
					xxxxx.xxx	Ack	BiQuad 2
					xxxxx.xxx	Ack	BiQuad 3
					xxxxx.xxx	Ack	BiQuad 4
					xxxxx.xxx	Ack	BiQuad 5
					xxxxx.xxx	Ack	BiQuad 6
					xxxxx.xxx	Ack	BiQuad 7
					xxxxx.xxx	Ack	BiQuad 8
					xxxxx.xxx	Ack	BiQuad 9
					xxxxx.xxx	Ack	BiQuad 10

VU Meter Output = 0xFE

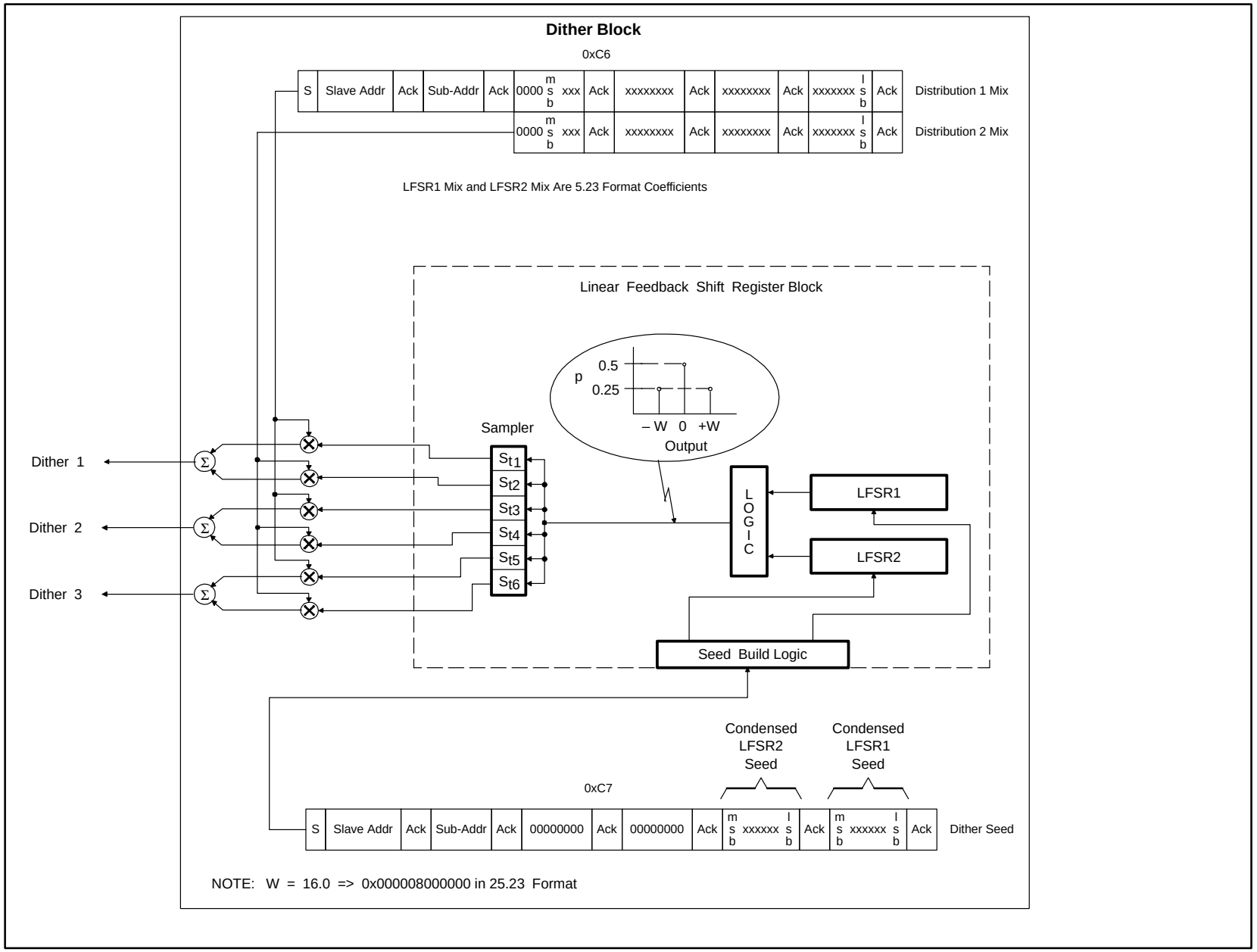
S	Slave Addr	Ack	Sub-Addr	Ack	xxxxx.xxx	Ack	
					xxxxx.xxx	Ack	VU Meter Output 1 (BiQuad 5)
					xxxxx.xxx	Ack	VU Meter Output 1 (BiQuad 6)

Spectrum Analyzer/VU Meter

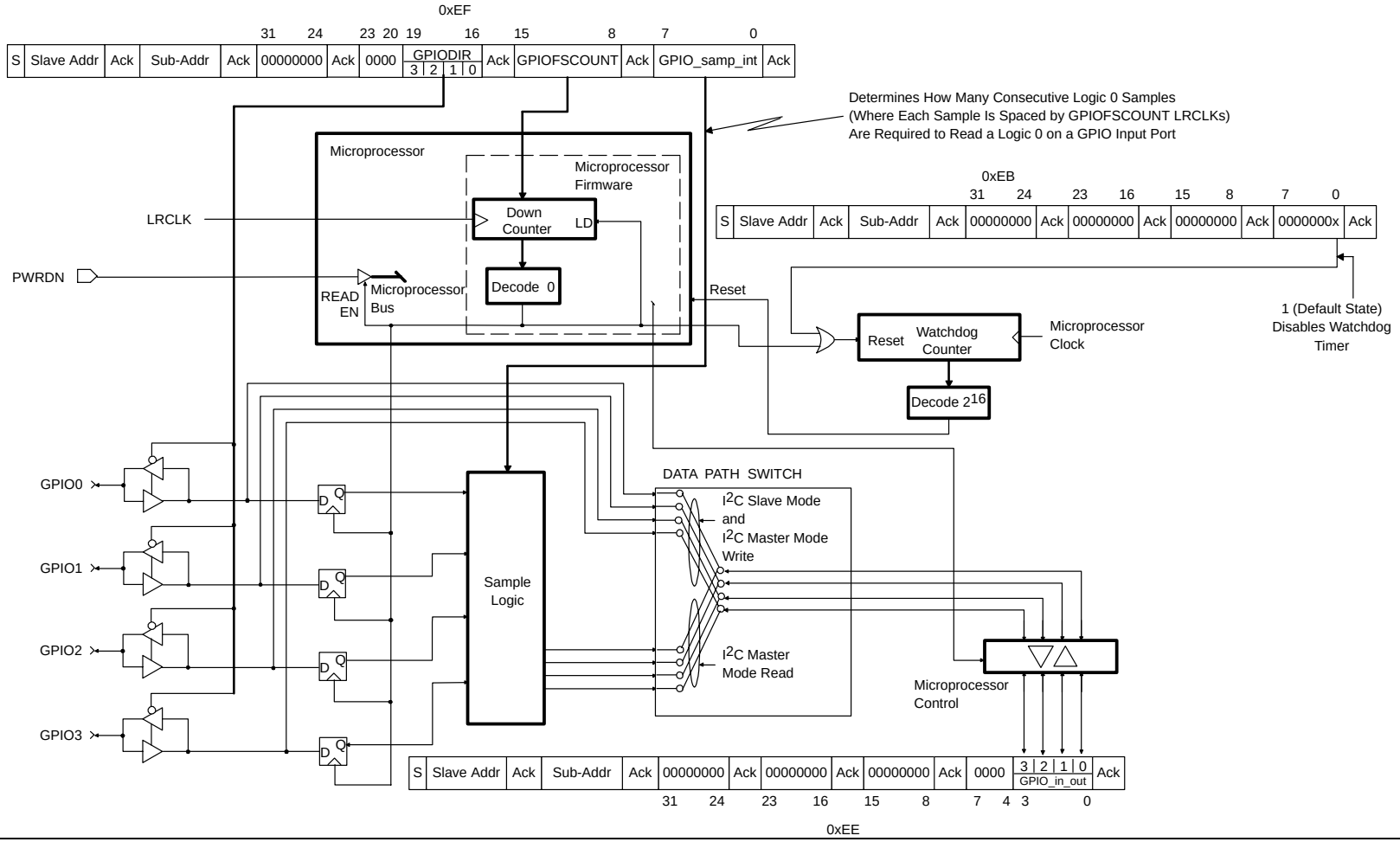


asa and (1–asa) Set Time Window Over Which RMS Value Is Computed

$t_{Window} \approx -1/[F \times \ln(1-asa)]$ Where F_S = Audio Sample Frequency

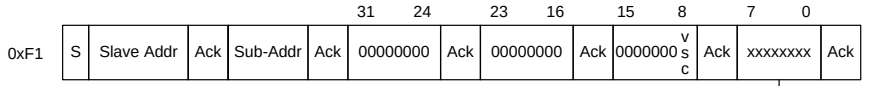

Dither Block
0xC6
S
Slave Addr
Ack
Sub-Addr
Ack
0000 msb xxx
Ack
xxxxxxxx
Ack
xxxxxxxx
Ack
xxxxxxx lsb
Ack
Distribution 1 Mix
0000 msb xxx
Ack
xxxxxxxx
Ack
xxxxxxxx
Ack
xxxxxxx lsb
Ack
Distribution 2 Mix
LFSR1 Mix and LFSR2 Mix Are 5.23 Format Coefficients
Linear Feedback Shift Register Block
p
0.5
0.25
– W 0 +W
Output
Sampler
St1
St2
St3
St4
St5
St6
Dither 1
Dither 2
Dither 3
LOGIC
LFSR1
LFSR2
Seed Build Logic
Condensed LFSR2 Seed
Condensed LFSR1 Seed
0xC7
S
Slave Addr
Ack
Sub-Addr
Ack
00000000
Ack
00000000
Ack
msb xxxxxx lsb
Ack
msb xxxxxx lsb
Ack
Dither Seed
NOTE: W = 16.0 => 0x000008000000 in 25.23 Format

GPIO and Watchdog Timer Subaddresses	
SUBADDRESS(es)	**PARAMETER(s)**
0xC8–0xC9	Factory Test Subaddresses
0xCA–0xCF	SDIN4 Input Mixers
0xD0–0xD1	CH1/CH2 to CH3 *After Effects* Mixers
0xD2–0xEA	Reserved



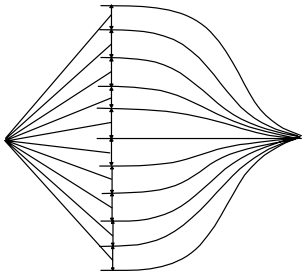
SUBADDRESS(es)	PARAMETER(s)
0xEC–0xED	Reserved/Factory Test Subaddresses
0xEE–0xEG—See Subaddress 0xEB	GPIO Port I/O Values and GPIO Parameters
0xF0—See Subaddress 0xA2	Master Mute/Un-Mute

0xF1—Also See Subaddress 0xA2 and Subaddress 0xF5



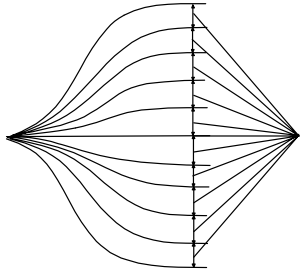
Treble and Bass
Slew Rate
TBLC[7:0]

Bass
Filter Set N



$t_{Transition}$ = TBLC[7:0] x 1/LRCLK

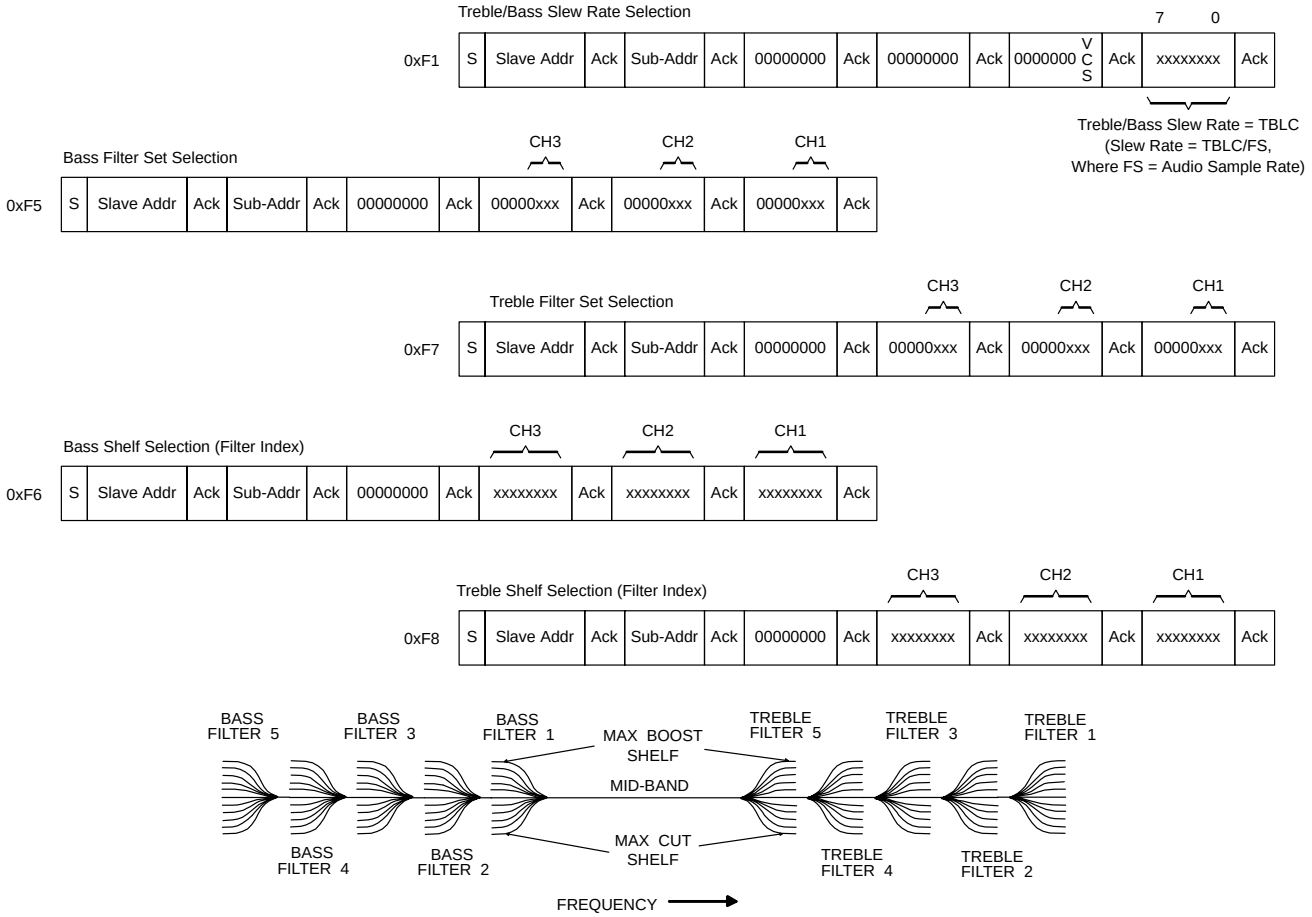
Treble
Filter Set N



$t_{Transition}$ = TBLC[7:0] x 1/LRCLK

0xF2–0xF4—See Subaddress 0xA2	CH1–CH3 Volume CMDS

Subaddress—Bass and Treble Shelf Filter Parameters



Treble & Bass Filter Set Commands

0 => No Change
1 – 5 => Filter Sets 1 – 5
6 – 7 => Illegal (Behavior Indeterminate)

Treble & Bass Filter Shelf Commands

0 => Illegal (Behavior Indeterminate)
1 – 150 => Filter Shelves 1 – 150
1 => +18-dB Boost
•
•
•
150 => –18-dB Cut
151 – 255 => Illegal (Behavior Indeterminate)

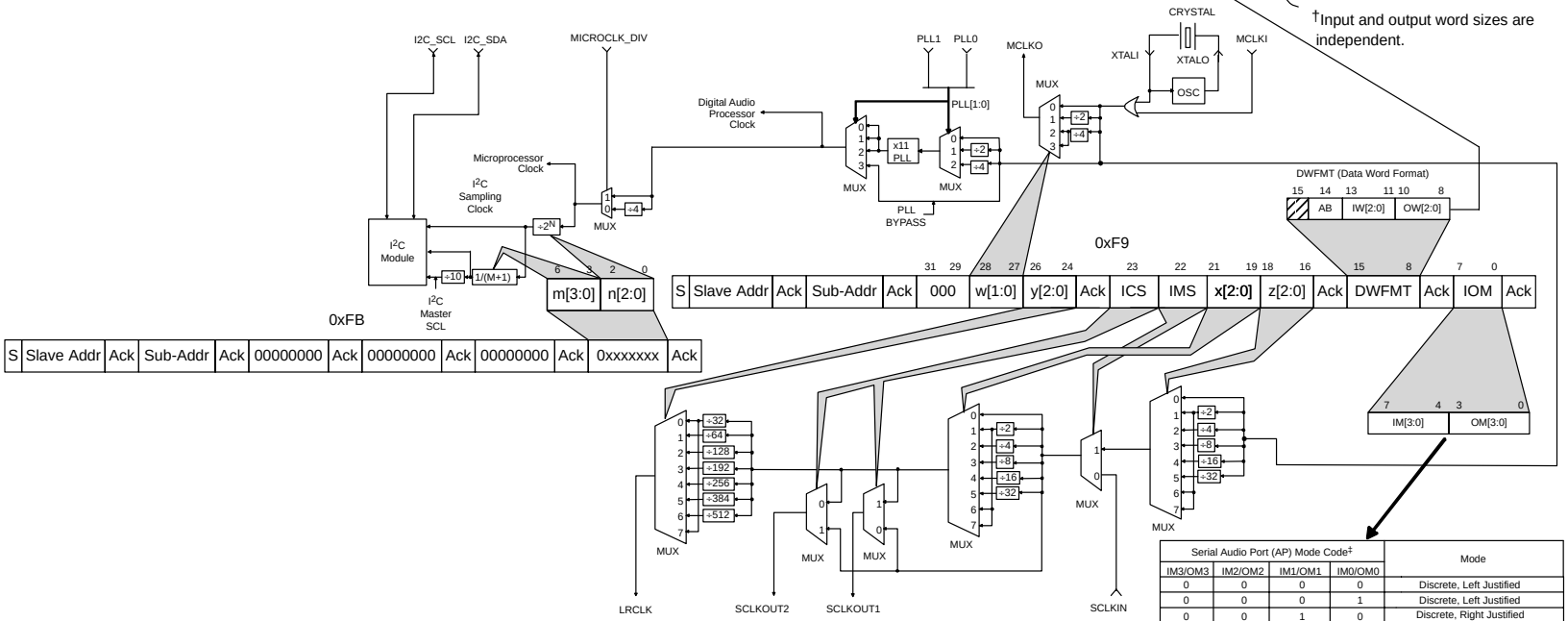
FS (LRCLK)	3-dB CORNERS (kHz)									
	FILTER SET 5		FILTER SET 4		FILTER SET 3		FILTER SET 2		FILTER SET 1	
	BASS	TREBLE	BASS	TREBLE	BASS	TREBLE	BASS	TREBLE	BASS	TREBLE
96 kHz	0.25	6	0.5	12	0.75	18	1	24	1.5	36
88.4 kHz	0.23	5.525	0.46	11.05	0.691	16.575	0.921	22.1	1.381	33.15
64 kHz	0.167	4	0.333	8	0.5	12	0.667	16	1	24
48 kHz	0.125	3	0.25	6	0.375	9	0.5	12	0.75	18
44.1 kHz	0.115	2.756	0.23	5.513	0.345	8.269	0.459	11.025	0.689	16.538
32 kHz	0.083	2	0.167	4	0.25	6	0.333	8	0.5	12
24 kHz	0.063	1.5	0.125	3	0.188	4.5	0.25	6	0.375	9
22.05 kHz	0.057	1.378	0.115	2.756	0.172	4.134	0.23	5.513	0.345	8.269
16 kHz	0.042	1	0.083	2	0.125	3	0.167	4	0.25	6
12 kHz	0.031	0.75	0.063	1.5	0.094	2.25	0.125	3	0.188	4.5
11.025 kHz	0.029	0.689	0.057	1.378	0.086	2.067	0.115	2.756	0.172	4.134

I²S FORMAT, CLOCK MANAGEMENT, AND I²C M AND N ASSIGNMENTS

AB assigns TDM time slots for those TDM outputs involving two TAS3103s. For these output formats, one of the TAS3103 chips must be defined as AB = 0. The other TAS3103 chip must be defined as AB = 1.

Word Size Code†			Word Size
IW2/OW2	IW1/OW1	IW0/OW0	
0	0	0	32 Bit
0	0	1	16 Bit
0	1	0	18 Bit
0	1	1	20 Bit
1	0	0	24 Bit
1	0	1	32 Bit
1	1	0	32 Bit
1	1	1	32 Bit

†Input and output word sizes are independent.

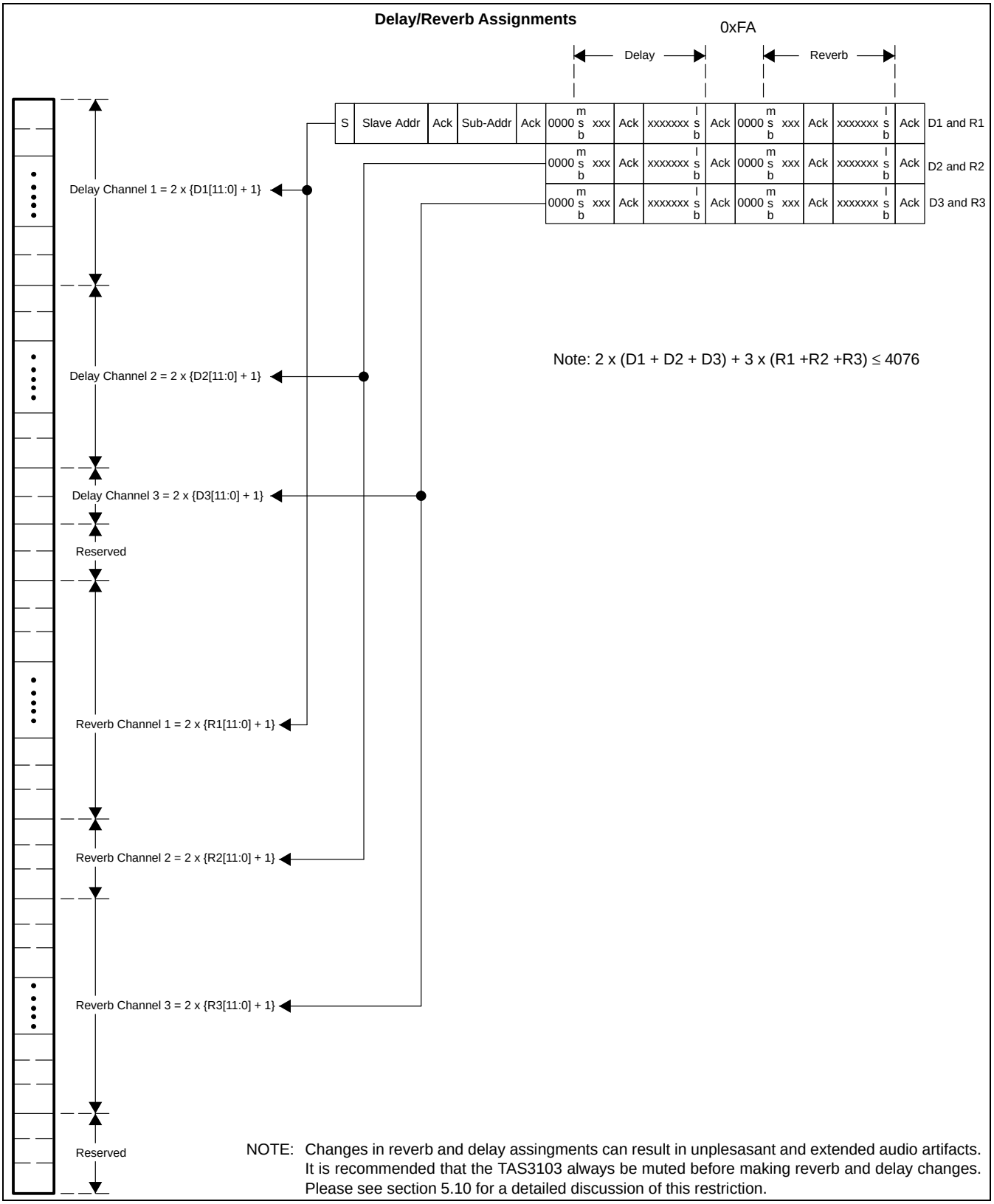


Serial Audio Port (AP) Mode Code‡				Mode
IM3/OM3	IM2/OM2	IM1/OM1	IM0/OM0	
0	0	0	0	Discrete, Left Justified
0	0	0	1	Discrete, Left Justified
0	0	1	0	Discrete, Right Justified
0	0	1	1	Discrete, I²S
0	1	0	0	Discrete, 16 – Bit Packed
0	1	0	1	TDM_LJ_8
0	1	1	0	TDM_LJ_6
0	1	1	1	TDM_LJ_4
1	0	0	0	TDM_I2S_8
1	0	0	1	TDM_I2S_6
1	0	1	0	TDM_I2S_4
1	0	1	1	TDM_20Bit_6
1	1	0	0	6 Ch, Single Chip, Crystal (LJ)
1	1	0	1	6 Ch, Single Chip (LJ)
1	1	1	0	6 Ch, Single Chip, Crystal (I²S)
1	1	1	1	6 Ch, Single Chip, 20 – Bit

‡Input and output mode selections are independent.

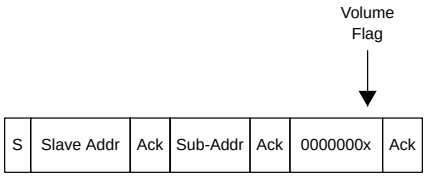
NOTE: F9 must not be updated without first muting all three monaural channels in the TAS3103. Please see Section 2.1.1 for a detailed discussion of this restriction.

Delay/Reverb Assignments



Note: 2 x (D1 + D2 + D3) + 3 x (R1 +R2 +R3) ≤ 4076

NOTE: Changes in reverb and delay assingments can result in unplesasant and extended audio artifacts. It is recommended that the TAS3103 always be muted before making reverb and delay changes. Please see section 5.10 for a detailed discussion of this restriction.

SUB-ADDRESS(ES)	PARAMETER(S)
0xFC—See Subaddress 0x00	Ending I^2C Check Word
0xFD–0xFE—See Subaddress 0xBB	Spectrum Analyzer/VU Meter Ouputs
0xFF—Volume Busy Flag	
	• Volume Flag = 0 ⇒ No volume commands are active. • Volume Flag = 1 ⇒ One or more volume commands are active.

2 Hardware Architecture

Figure 2–1 depicts the hardware architecture of the chip. The architecture consists of five major blocks:

- Input Serial Audio Port (SAP)
- Output Serial Audio Port (SAP)
- DPLL and Clock Management
- Controller
- Digital Audio Processor (DAP)

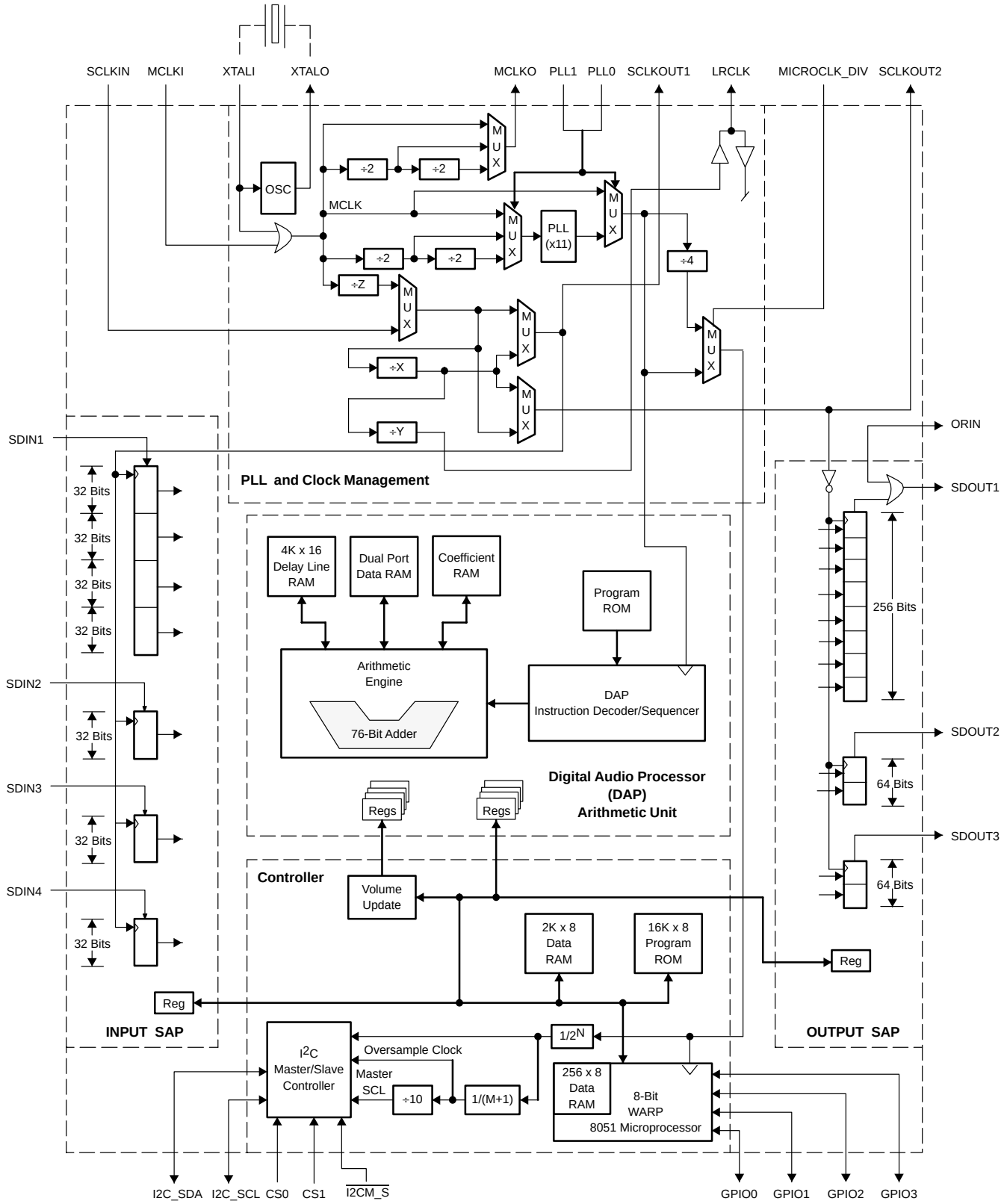


Figure 2–1. TAS3103 Detailed Hardware Block Diagram

2.1 Input and Output Serial Audio Ports (SAPs)

The TAS3103 accepts data in various serial data formats including left/right justified and I^{2}S, 16 through 32 bits, discrete, or TDM. Sample rates from 8 kHz through 96 kHz are supported. Each TAS3103 has four input serial ports and three output serial ports, labeled SDIN[4:1] and SDOUT[3:1] respectively. All ports accommodate stereo data formats, and SDIN1 and SDOUT1 also accommodate time-division multiplex (TDM) data formats. The formats are selectable via I^{2}C commands. All input channels are assigned the same format and all output channels are assigned the same format; and the two formats need not be the same. The TAS3103 can accommodate system architectures that require data format conversions without the need for additional glue logic. If a TDM format is selected for the input port, only SDIN1 is active; the other three input channels cannot be used. If a TDM format is selected for the output port, only SDOUT1 is active; the other two channels cannot be used.

2.1.1 SAP Configuration Options

The TAS3103 serial interface data format options for discrete (stereo) data are detailed in Figure 2–2.

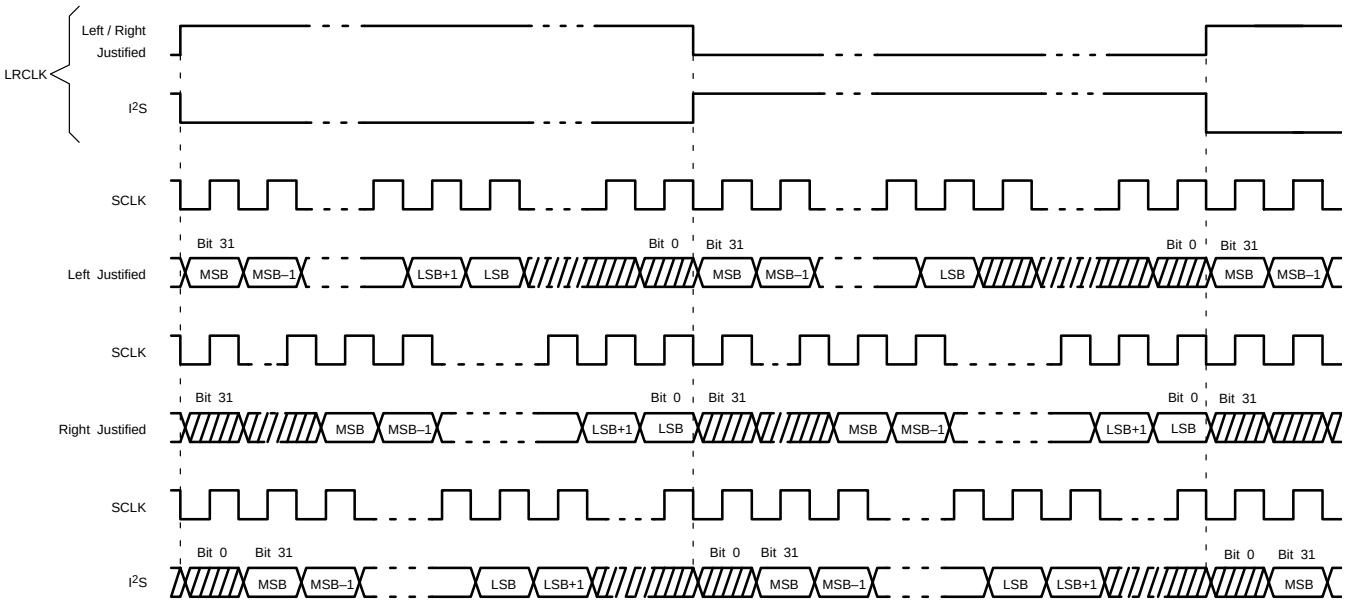


Figure 2–2. Discrete Serial Data Formats

When the TAS3103 is transmitting serial data, it uses the negative edge of SCLK to output a new data bit. The TAS3103 samples incoming serial data on the rising edge of SCLK.

The TDM modes on the TAS3103 only provide left justified and I^{2}S formats, and each word in the TDM data stream adheres to the bit placement shown in Figure 2–2. Figure 2–3 illustrates the output data stream for a 4-channel TDM mode. Two cases are illustrated; an I^{2}S data format case (SAP output mode 1010) and a left-justified data format case (SAP output mode 0111).

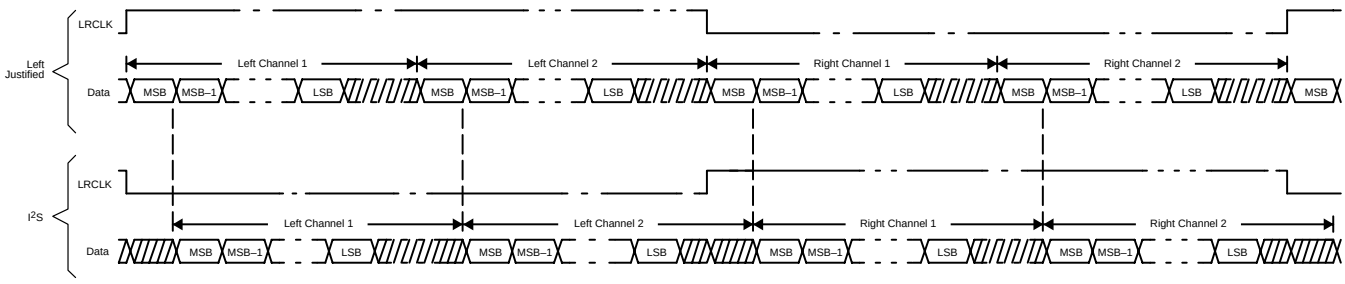


Figure 2–3. Four Channel TDM Serial Data Formats

A 16-bit field contained in the 32-bit word located at I2C subaddress 0xF9 configures both the input and output serial audio ports. Figure 2–4 illustrates the format of this 16-bit field. The data is shown in the transmitted I2C protocol format, and thus, in addition to the data, the start bit S, the slave address, the subaddress, and the acknowledges required by every byte are also shown.

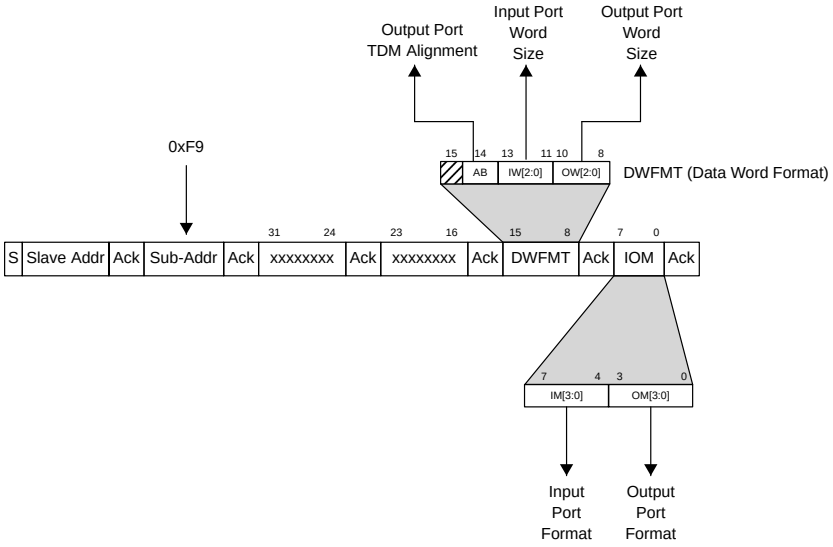
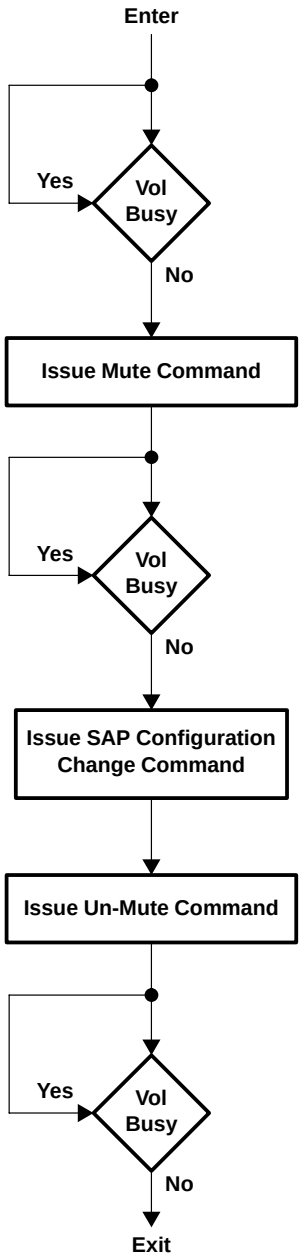


Figure 2–4. SAP Configuration Subaddress Fields

Commands to reconfigure the SAP cannot be issued as standalone commands, but must accompany mute and un-mute commands. The reason for this is that an SAP configuration change while a volume or bas and treble update is taking place can cause the update to not properly be completed. Figure 2–5 shows the recommended procedure for issuing SAP configuration update commands.

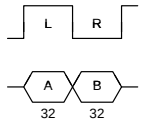
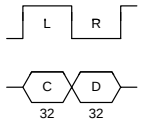
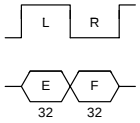
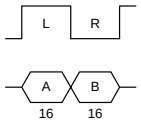
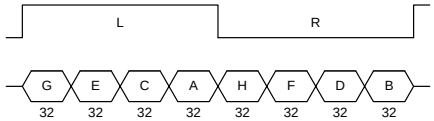
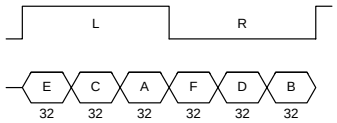
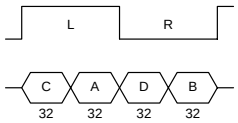
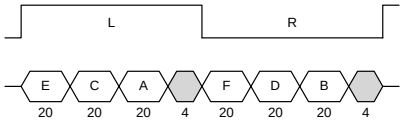
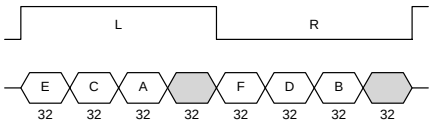


Mute Command = 0x00000007 at sub-address x0F0
Un-mute command = 0x00000000 at sub-address 0xF0
SAP configuration sub-address = 0x59
Volume busy flag = LSB of sub-address 0xFF logic 1 = busy

Figure 2–5. Recommended Procedure for Issuing SAP Configuration Updates

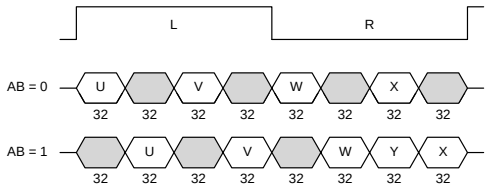
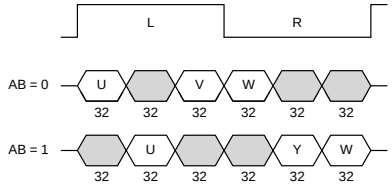
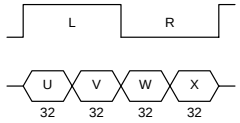
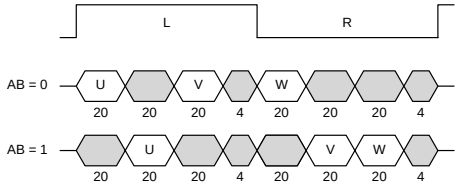
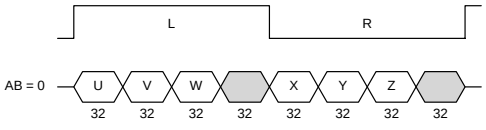
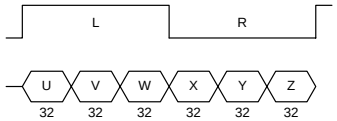
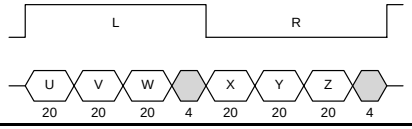
Figure 2–6**,** Figure 2–7, and Figure 2–8 tabularize the formatting and word size options available for the input SAP and output SAP. In these figures, data formats are paired when the only difference between the pair is whether the word placement within the LRCLK period is left justified or I^2S. The TDM formats available include single chip TDM output formats ($SDOUT1_{chipA}$ or $SDOUT1_{chipB}$) and two chip TDM output formats ($SDOUT1_{chipA}$ OR'ed with $SDOUT1_{chipB}$). For two chip TDM output formats, the OR'ing operation is accomplished by routing SDOUT1 from one of the two TAS3103 chips to ORIN of the other TAS3103 chip. The AB bit also comes into play for two chip TDM formats; AB must be set to 1 on one of the two TAS3103 chips and set to 0 on the other TAS3103 chip. For a given connection of SDOUT1 to ORIN, it does not matter which TAS3103 is set up as chip AB = 1, and which chip is set up as chip AB = 0. However, the routing of the processed data to the output registers in the TAS3103 is dependent on which chip is chip AB = 0 and which chip is chip AB = 1. Figure 2–10 and Figure 2–11 illustrate this dependence.

In Figure 2–10 and Figure 2–11, the paired TDM output formats 0101 and 1000 are unique in that each format, in effect, services two distinct industry formats. For these two modes, if register Y in chip AB = 1 is set to zero (by appropriate output mixer coefficient settings), the resulting format is a standard 8 CH TDM format. This option is illustrated in Figure 2–5.

INPUT TYPE	IM[3:0]	FORMAT	WORDSIZE	DATA DISTRIBUTION: A, B, C, D, E, F, G, H = INPUT MIXER INPUTS		
				SDIN1	SDIN2	SDIN3
DISCRETE	000X(1)	Left justified	All options valid			
	0010	Right justified	All options valid			
	0011	I2S	All options valid except 32 bit			
	0100	16-bit packed	IW[2:0] = 001		Not available	Not available
TIME DIVISION MULTIPLEX (TDM)	0101	8 CH transfer, left justified	All options valid		Not available	Not available
	1000	8 CH transfer, I2S	All options valid except 32 bit		Not available	Not available
	0110/1101 (2)(3)	6 CH, left justified	All options valid		Not available	Not available
	1001(3)	6 CH, I2S	All options valid except 32 bit		Not available	Not available
	0111	4 CH, left justified	All options valid		Not available	Not available
	1010	4 CH, I2S	All options valid except 32 bit		Not available	Not available
	1011/1111(4)	6 CH, 20 bit	IW[2:0] = 011		Not available	Not available
	1100	6 CH data, 8 CH transfer, left justified	All options valid		Not available	Not available
	1110	6 CH data, 8 CH transfer, I2S	All options valid except 32 bit		Not available	Not available

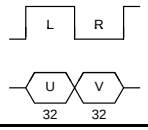
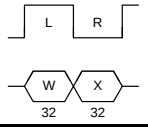
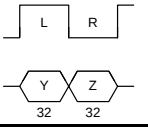
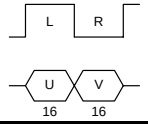
NOTES: 1. Left justified, stereo is the default input format.
2. IM[3:0] modes 0110 and 1101 are identical for the input SAP. OM[3:0] modes 0110 and 1101 do produce different results in the output SAP (see Figure 2–7).
3. If a 6 CH input format is selected, the output format must also be set to 6 CH. When in a 6 CH mode, data format selections—I2S and left justified—for the 6 Ch input SAP can be made independent of the data format selections—I2S and left justified—made for the 6 CH output SAP.
4. IM[3:0] modes 1011 and 1111 are identical for the input SAP. OM[3:0] modes 1011 and 1111 do produce different results in the output SAP (see Figure 2–7).

Figure 2–6. Format Options: Input Serial Audio Port

OUTPUT TYPE	OM[3:0]	FORMAT	WORDSIZE	DATA DISTRIBUTION: U, V, W, X, Y, Z = OUTPUT MIXER OUTPUTS		
				SDOUT1	SDOUT2	SDOUT3
TIME DIVISION MULTIPLEX (TDM)	0101	8 CH, 2 chip, left justified	All options valid		Not available	Not available
	1000	8 CH, 2 chip, I2S	All options valid except 32 bit		Not available	Not available
	0110(1)	6 CH, 2 chip, left justified	All options valid		Not available	Not available
	1001(1)	6 CH, 2 chip, I2S	All options valid except 32 bit		Not available	Not available
	0111	4 CH, left justified	All options valid		Not available	Not available
	1010	4 CH, I2S	All options valid except 32 bit		Not available	Not available
	1011	6 CH, 2 chip, 20 bit	OW[2:0] = 011		Not available	Not available
	1100	6 CH data, 8 CH transfer, left justified	All options valid		Not available	Not available
	1110	6 CH data, 8 CH transfer, I2S	All options valid except 32 bit		Not available	Not available
	1101(1)	6 CH, left justified	All options valid		Not available	Not available
	1111	6 CH, 20 bit	OW[2:0] = 011		Not available	Not available

NOTE 1: If a 6 CH output format is selected, the input format must also be set to 6 CH. When in a 6 CH mode, data format selections—I2S and left justified—for the output SAP can be made independent of the data format selections—I2S and left justified—can be made for the input SAP.

Figure 2–7. TDM Format Options: Output Serial Audio Port

OUTPUT TYPE	OM[3:0]	FORMAT	WORDSIZE	DATA DISTRIBUTION: U, V, W, X, Y, Z = OUTPUT MIXER OUTPUTS		
				SDOUT1	SDOUT2	SDOUT3
DISCRETE	000X(1)	Left justified	All options valid			
	0010	Right justified	All options valid			
	0011	I^2S	All options valid except 32 bit			
	0100	16-bit packed	OW[2:0] = 001		Not available	Not available

NOTE 1: Left justified, stereo is the default input format.

Figure 2–8. Discrete Format Options: Output Serial Audio Port

	SAMPLE SIZE	INPUT IW[2:0]			OUTPUT OW[2:0]		
		IW2	IW1	IW0	OW2	OW1	OW0
	(32)	0	0	0	0	0	0
DEFAULT →	16 Bit	0	0	1	0	0	1
	18 Bit	0	1	0	0	1	0
	20 Bit	0	1	1	0	1	1
	24 Bit	1	0	0	1	0	0
	32 Bit	1	0	1	1	0	1
	(32)	1	1	0	1	1	0
	(32)	1	1	1	1	1	1

(32) ⇒ Reserved for future family members. Selection of 000, 110, or 111 in the TAS3103 selects a 32-bit sample size.

Figure 2–9. Word Size Settings

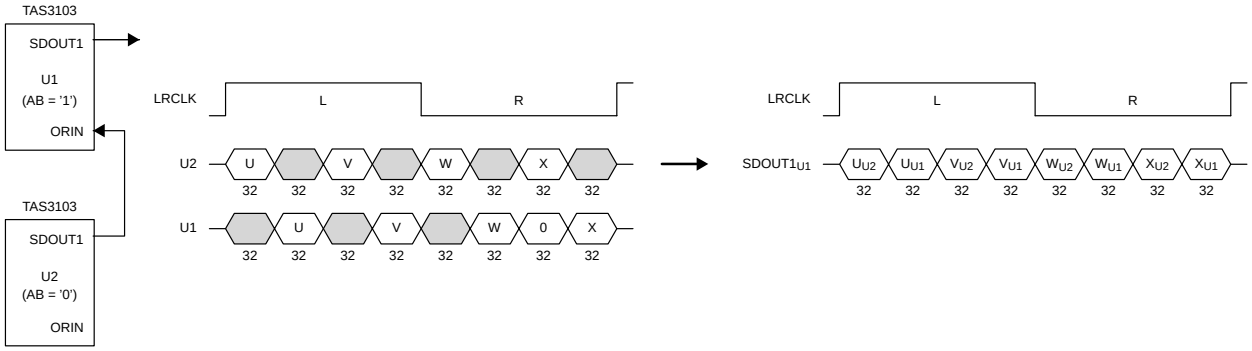


Figure 2–10. 8 CH TDM Format Using SAP Modes 0101 and 1000

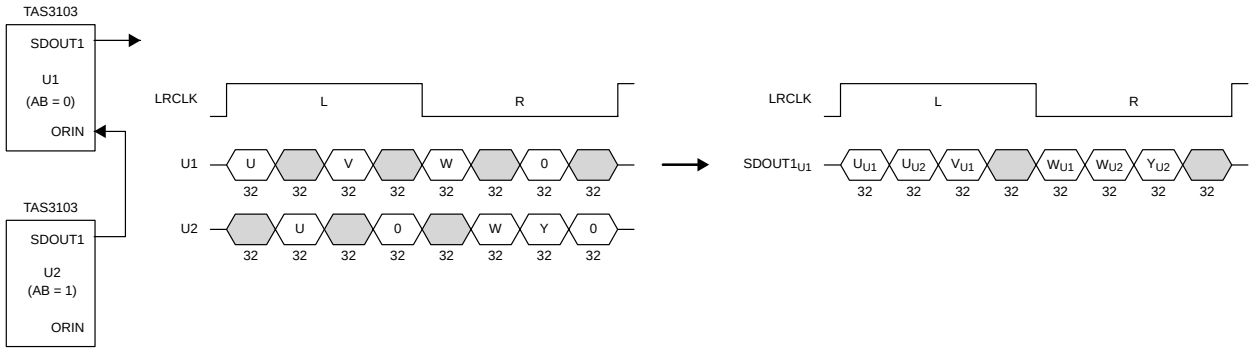


Figure 2–11. 6 CH Data, 8 CH Transfer TDM Format Using SAP Modes 0101 and 1000

For these same two modes, if register X in chip AB = 0 is set to zero, and registers V and X in chip AB = 1 are set to zero, the resulting format is a 6 CH data, 8 CH transfer format. This option is illustrated in Figure 2–6.

The data output format in Figure 2–11 is identical to that realized using data output formats 1100 and 1110 in Figure 2–7. The difference is that SAP modes 1010 and 1000 provide six independent monaural channels to process the data, whereas SAP modes 1100 and 1110 provide only three independent monaural channels to process the data.

2.1.2 Processing Flow—SAP Input to SAP Output

All SAP data format options other than I^2S result in a two-sample delay from input to output, as illustrated in Figure 2–12. Figure 2–12 is also relevant if I^2S formatting is used for both the input SAP and the output SAP (the polarity of LRCLK in Figure 2–12 has to be inverted in this case). However, if I^2S format conversions are performed between input and output, the delay becomes either 1.5 samples or 2.5 samples, depending on the processing clock frequency selected for the digital audio processor (DAP) relative to the sample rate of the incoming data. The input to output delay for an I^2S input format and a non-I^2S output format is illustrated in Figure 2–13(a), and Figure 2–13(b) illustrates the delay for a non-I^2S input format and an I^2S output format. In each case, two distinct input to output delay times are shown: a 1.5 sample delay time if the processing time in the DAP is less than half the sample period, and a 2.5 sample delay time if the processing time in the DAP is greater than half the sample period.

The departure from the two-sample input to output processing delay when I^2S format conversions are performed is due to the use of a common LRCLK. The I^2S format uses the falling edge of LRCLK to begin a sample period, whereas all other formats use the rising edge of LRCLK to begin a sample period. This means that the input SAP and digital audio processor (DAP) operate on sample windows that are 180° out of phase with respect to the sample window used by the output SAP. This phase difference results in the output SAP outputting a new data sample at the midpoint of the sample period used by the DAP to process the data. If the processing cycle completes all processing tasks before the midpoint of the processing sample period, the output SAP outputs this processed data. However, if the processing time extends past the midpoint of the processing sample period, the output SAP outputs the data processed during the previous processing sample period. In the former case, the delay from input to output is 1.5 samples. In the latter case, the delay from input to output is 2.5 samples.

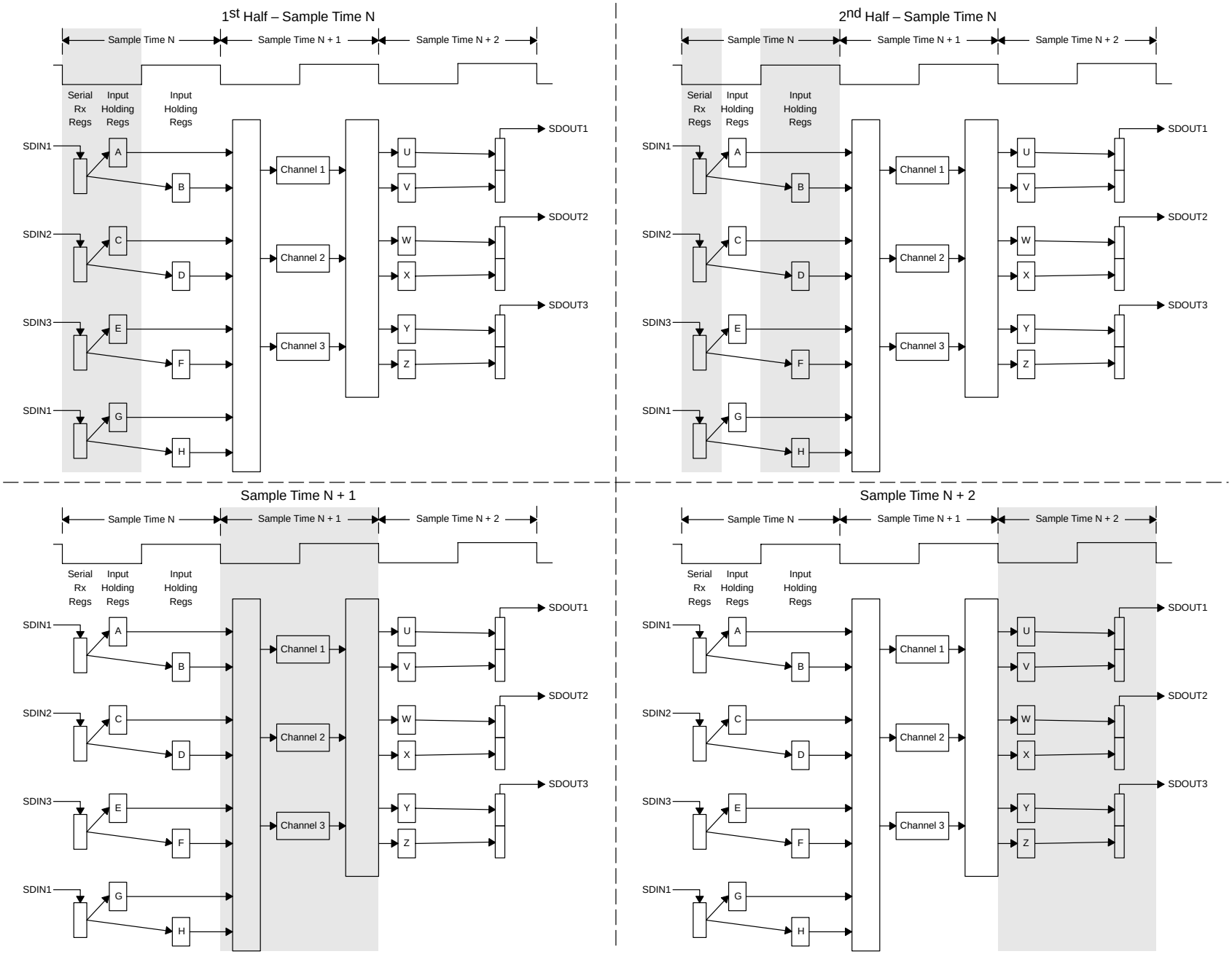
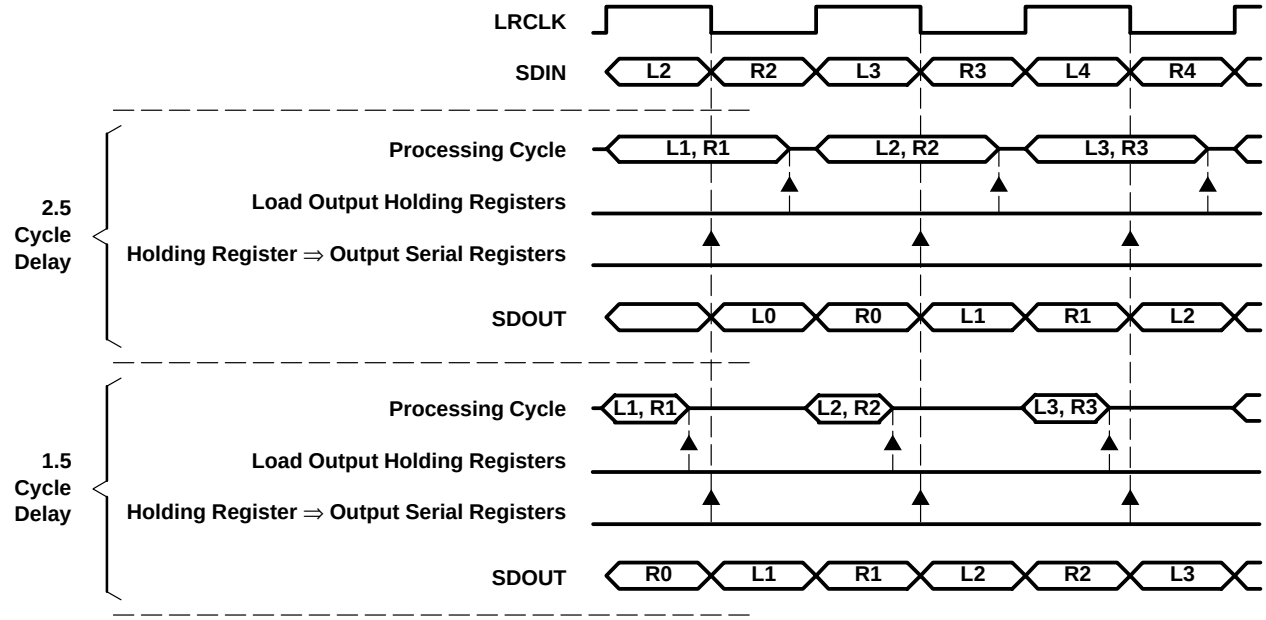
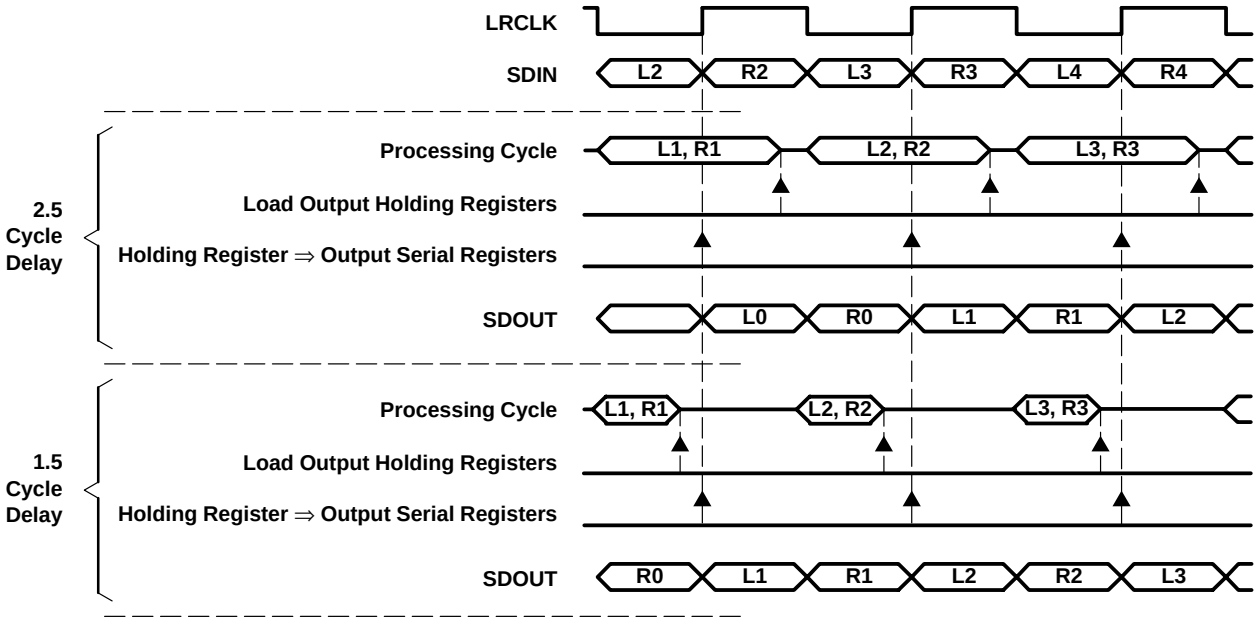


Figure 2–12. SAP Input-to-Output Latency



(a) Left-Justified Input / I^2S Output



(b) I^2S Input / Left-Justified Output

Figure 2–13. SAP Input-to-Output Latency for I^2S Format Conversions

The delay from input to output can thus be either 1.5 or 2.5 sample times when data format conversions are performed that involves the I^2S format. However, which delay time is obtained for a particular application is determinable and fixed for that application, providing care is taken in the selection of MCLKI/XTALI with respect to the incoming sample clock LRCLK.

Table 2–1 lists all viable clock selections for a given audio sample rate (LRCLK). The table only includes those clock choices that allow enough processing throughput to accomplish all tasks within a given sample time ($\tau s = 1/LRCLK$). For each entry in the table, the DAP processing time is given in terms of whether the time is greater than 0.5 τs (resulting in an input to output delay of 2.5 τs), or less than 0.5 τs (resulting in an input to output delay of 1.5 τs).

Table 1 is valid for both master and slave I^2S modes (bit IMS at subaddress 0xF9 determines I^2S master/slave selection—see DPLL and clock management section that follows). For all applications, MCLK must be ≥ 128 LRCLK (FS). In the I^2S master mode, MCLK, SCLK (I^2S bit clock) LRCLK are all harmonically related. Furthermore, in the I^2S master mode, if a master clock value given in Table 2–1 is used, the latency realized in performing I^2S format conversions, 1.5 samples or 2.5 samples, is stable and fixed over the duration of operation. However, greater care must be taken for the I^2S slave mode. In this mode, the device has the proper operational throughput to perform all required computations as long as MCLK is ≥ 128 LRCLK. But there is no longer the requirement that MCLK be harmonically related to SCLK and LRCLK. Values of MCLK could be chosen such that the output dithers between latencies of 1.5 and 2.5 sample times. There may be cases where part of the data stream output exhibits sample time latencies of 1.5 τs and the other portion of the output data stream exhibits sample time latencies of 2.5 τs. To assure that such cases do not happen in the I^2S slave mode, the relationships between MCLK and LRCLK given in Table 2–1 should be followed for data format conversions involving the I^2S format. The MCLKI/XTALI frequencies given in Table 2–1 (if set to within ±5% of the nominal value shown) assure that the DAP processing time falls above 0.5 T_S or below 0.5 τs with enough margin to assure that there is no race condition between the outputting of data and the completion of the processing tasks.

Table 2–1. TAS3103 Throughput Latencies vs MCLK and LRCLK

AUDIO SAMPLE RATE (LRCLK)	MASTER CLOCK(2) (MCLKI/XTALI)	DAP(1) CLOCK (PLL_OUTPUT)	DAP CLOCK Cycles/LRCLK	DAP PROCESSING TIME	THROUGH-PUT DELAY
96 kHz	24.576 MHz, 12.288 MHz	135.168 MHz	1408	> $T_S/2$	2.5 T_S
88.2 kHz	22.5792 MHz, 11.2896 MHz	124.1856 MHz	1408	> $T_S/2$	2.5 T_S
48 kHz	24.576 MHz, 12.288 MHz	135.168 MHz	2816	< $T_S/2$	1.5 T_S
	24.576 MHz, 12.288 MHz, 6.144 MHz	67.584 MHz	1408	> $T_S/2$	2.5 T_S
44.1 kHz	22.5792 MHz, 11.2896 MHz	124.1856 MHz	2816	< $T_S/2$	1.5 T_S
	22.5792 MHz, 11.2896 MHz, 5.6448 MHz	62.0928 MHz	1408	> $T_S/2$	2.5 T_S
32 kHz	16.384 MHz, 8.192 MHz	90.112 MHz	2816	< $T_S/2$	1.5 T_S
	16.384 MHz, 8.192 MHz, 4.096 MHz	45.056 MHz	1408	> $T_S/2$	2.5 T_S
24 kHz	24.576 MHz, 12.2858 MHz	135.168 MHz	5632	< $T_S/2$	1.5 T_S
	24.576 MHz, 12.2858 MHz, 6.144 MHz	67.584 MHz	2816	< $T_S/2$	1.5 T_S
	12.288 MHz, 6.144 MHz, 3.072 MHz	33.792 MHz	1408	> $T_S/2$	2.5 T_S
22.05 kHz	22.5792 MHz, 11.2896 MHz	124.1856 MHz	5632	< $T_S/2$	1.5 T_S
	22.5792 MHz, 11.2896 MHz, 5.6448 MHz	62.0928 MHz	2816	< $T_S/2$	1.5 T_S
	11.2896 MHz, 5.6448 MHz, 2.8224 MHz	31.0464 MHz	1408	> $T_S/2$	2.5 T_S
8 kHz	24.576 MHz, 12.288 MHz	135.168 MHz	16896	< $T_S/2$	1.5 T_S
	24.576 MHz, 12.288 MHz, 6.144 MHz	67.584 MHz	8448	< $T_S/2$	1.5 T_S
	12.288 MHz, 6.144 MHz, 3.072 MHz	33.792 MHz	4224	< $T_S/2$	1.5 T_S
	6.144 MHz, 3.072 MHz, 1.536 MHz	16.896 MHz	2112	> $T_S/2$	2.5 T_S

NOTES: 1. DAP clock is the internal digital audio processor clock. It is equal to 11 × MCLK1/XTALI, 11/2 × MCLKI/XTALI, or 11/4 × MCLKI/XTALI (as determined by a bit field in I^2C subaddress 0xF9). The DAP clock must always be greater than or equal to 1400 F_S (LRCLK).
2. MCLKI must always be less than or equal to 25 MHz. XTALI must always be less than or equal to 20 MHz.

2.2 DPLL and CLock Management

Clock management for the TAS3103 consists of two control structures:

- Master clock management: oversees the selection of the clock frequencies for the microprocessor, the I^2C controller, and the digital audio processor (DAP). The master clock (MCLKI or XTALI) serves as the source for these clocks. In most applications, the master clock is input to an on-chip digital phase lock loop (DPLL), and the DPLL output is used to derive the microprocessor and DAP clocks. A DPLL bypass mode can also be used, in which case the master clock is used to derive the microprocessor and DAP clocks.
- Serial audio port (SAP) clock management: oversees SAP master/slave mode, the settings of SCLKOUT1 and SCLKOUT2, and the setting of LRCLK in the SAP master mode.

Figure 2–14 illustrates the clock circuitry in the TAS3103. The bold lines in Figure 2–14 highlight the default settings at power turn on, or after a reset. Inputs MCLKI and XTALI source the master clock for the TAS3103. Within the TAS3103, these two inputs are combined by an OR gate, and thus only one of these two sources can be active at any one time. The source that is not active must be set to logic 0. In normal operation, the master clock is divided by 1, 2, or 4 (as determined by the logic levels set at input pins PLL0 and PLL1) and then multiplied by 11 in frequency by the on-chip DPLL. The ability to bypass the DPLL is also an option under I^2C command control. The DPLL output (or MCLKI/XTALI if the DPLL is bypassed) is the processing clock used by the digital audio processor (DAP).

The DAP processing clock can also serve as the clock for the on-chip microprocessor, or the DAP clock can be divided by four prior to sending to the microprocessor. The input pin MICROCLK_DIV makes this clock choice. A logic 1 input level on this pin selects the DAP clock for the microprocessor clock; a logic 0 input level on this pin selects the DAP clock/four for the microprocessor clock. The selected microprocessor clock is also used to derive the clocks used by the I^2C control block. Two parameters, N and M, define the clocks used by the I^2C control block. The I^2C control block sampling frequency is set by $1/2^N$, where N can range in value from 0 to 7. A 1/(1 + M) divisor followed by a 1/10 divisor generates the data bit clock (SCL) sampling frequency. This derived SCL clock is only used when the I^2C control block is set to master mode (input pin $\overline{\text{I2CM\_S}}$ = 1). The default value for the I^2C parameter N depends on whether the I^2C controller is in a slave mode ($\overline{\text{I2CM\_S}}$ = 0) or a master mode ($\overline{\text{I2CM\_S}}$ = 1). In the I^2C master mode N = 2 (2^N = 4), which assures that a 100-kHz I^2C data clock (SCL) can be generated when the digital audio processor (DAP) is running at its maximum frequency of 135 MHz. In the I^2C slave mode N = 1 (2^N = 2), which assures the I^2C controller an adequate over-sampling clock when the DAP is running at the minimum clock frequency required to process 8-kHz audio data (approximately 11.2 MHz).

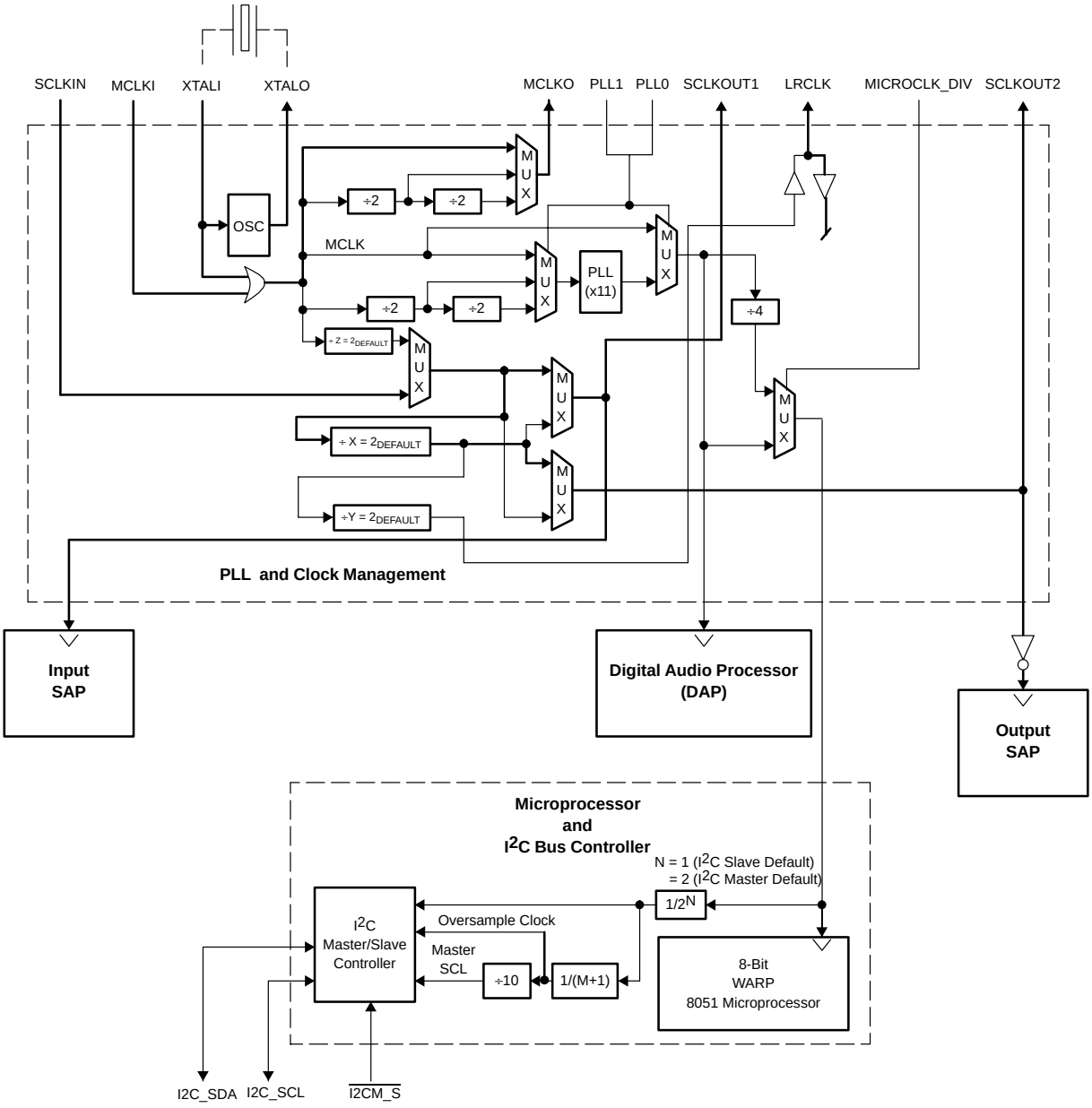


Figure 2–14. DPLL and Clock Management Block Diagram

When the SAP is in the master mode, the serial audio port (SAP) uses the MCLKI/XTALI master clock to derive the serial port clocks SCLKOUT1, SLCKOUT2, and LRCLK. When the SAP is in the slave mode, LRCLK is an input and SCLKOUT2 and SCLKOUT1 are derived from SCLKIN. As shown in Figure 2–14, SCLKOUT1 clocks data into the input SAP and SCLKOUT2 clocks data from the output SAP. Two distinct clocks are required to support TDM to discrete and discrete to TDM data format conversions. Such format conversions also require that SCLKIN be the higher valued bit clock frequency. For TDM in/discrete out format conversions, SCLKIN must be equal to the input bit clock. For discrete in/TDM out format conversions, SCLKIN must be equal to the output bit clock. The frequency settings for SCLKOUT1, SCLKOUT2, and LRCLK in the SAP master mode, as well as the SAP master/slave mode selection, are all controlled by I^{2}C commands.

Table 2–2 lists the default settings at power turn on or after a received reset.

Table 2–2. TAS3103 Clock Default Settings

CLOCK	DEFAULT SETTING
SCLKOUT1	SCLKIN
SCLKOUT2	SCLKIN
LRCLK	Input
MCLKO	MCLKI or XTALI
DAP processing clock	Set by pins PLL0 and PLL1
Microprocessor clock	Set by pin MICROCLK_DIV
I^2C sampling clock	**I^2C master mode** Microprocessor clock/4 **I^2C slave mode** Microprocessor clock/2
I^2C master SCL	I^2C sampling clock/90

The selections provided by the dedicated TAS3103 input pins and the programmable settings provided by I^2C subaddress commands give the TAS3103 a wealth of clocking options. Table 2–1, in the section describing the serial audio port (SAP), lists typical clocking selections for different audio sampling rates. However, the following clocking restrictions must be adhered to:

- MCLKI or XTALI ≥ 128 F_S (NOTE: For some TDM modes, MCLKI or XTALI must be ≥ 256 F_S)
- Microprocessor clock/20 ≥ I^2C SCL clock
- Microprocessor clock ≤ 35 MHz
- I^2C oversample clock/10 ≥ I^2C SCL clock
- XTALI ≤ 12.288 MHz
- MCLKI ≤ 25 MHz

As long as these restrictions are met, all other clocking options are allowed.

2.3 Controller

The controller serves as the interface between the digital audio processor (DAP), the asynchronous I^2C bus interface, and the four general-purpose I/O (GPIO) pins. Included in the controller block is an industry-standard 8051 microprocessor and an I^2C master/slave bus controller.

2.3.1 8051 Microprocessor

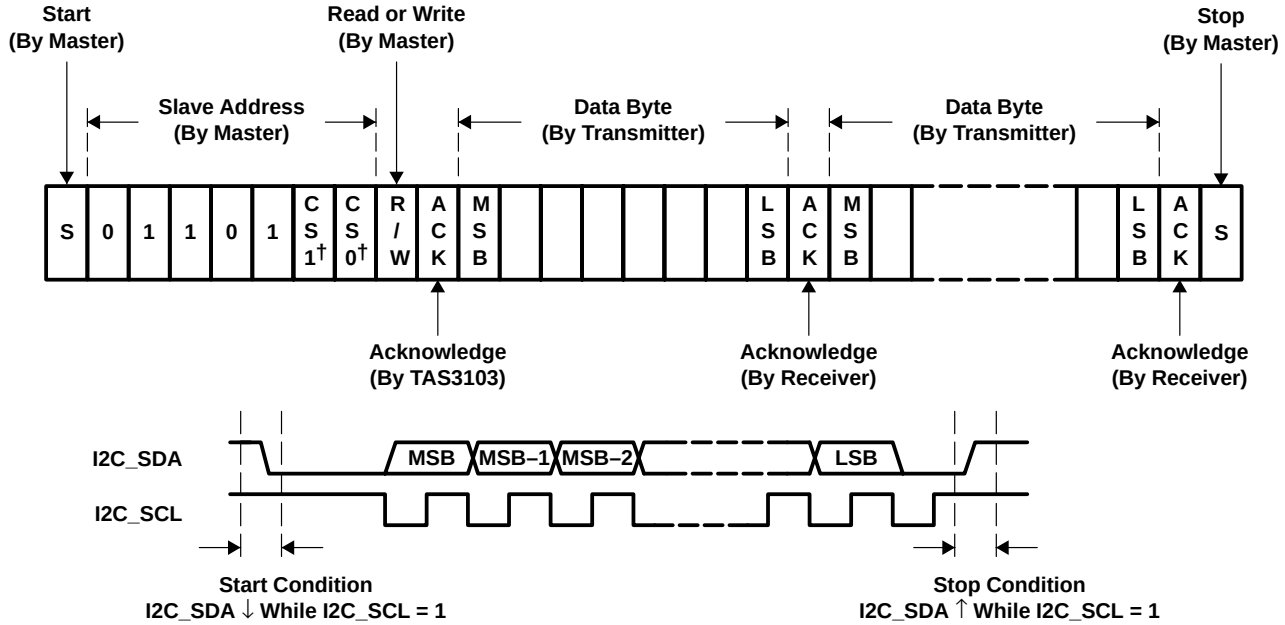
The 8051 microprocessor receives and distributes I^2C write data, retrieves and outputs to the I^2C bus controller the required I^2C read data, and participates in most processing tasks requiring multiframe processing cycles. The microprocessor also controls the flow of data into and out of the GPIO pins, which includes volume control when in the I^2C master mode The microprocessor has its own data RAM for storing intermediate values and queuing I^2C commands, and a fixed program ROM. The microprocessor's program cannot be altered.

2.3.2 I^2C Bus controller

The TAS3103 has a bidirectional, two-wire, I^2C-compatible interface. Both 100K-bps and 400K-bps data transfer rates are supported, and the TAS3103 controller can serve as either a master I^2C device or a slave I^2C device. Master/slave operation is defined by the logic level input into pin $\overline{\text{I2CM\_S}}$ (logic 1 = master mode, logic 0 = slave mode). If this input level is changed, the TAS3103 must be reset.

In the I^2C master mode, data rate transfer is fixed at 100 kHz. In the I^2C slave mode, data rate transfer is determined by the master device. However, the setting of I^2C parameter N at subaddress 0xF8 (see the *PLL and Clock Management* section) does play a role in setting the data transfer rate. In the I^2C slave mode, bit rates other than (and including) the I^2C-specific 100K-bps and 400K-bps bit rates can be obtained, but N must always be set so that the over-sample clock into the I^2C master/slave controller is at least a factor of 10 higher in frequency than SCL.

The I2C communication protocol for the I2C slave mode is shown in Figure 2–15.



† Bits CS1 and CS0 in the TAS3103 slave address are compared to the logic levels on pins CS0 and CS1 for address verification. This provides the ability to address up to four TAS3103 chips on the same I2C bus.

Figure 2–15. I2C Slave Mode Communication Protocol

In the slave mode, the I2C bus is used to:

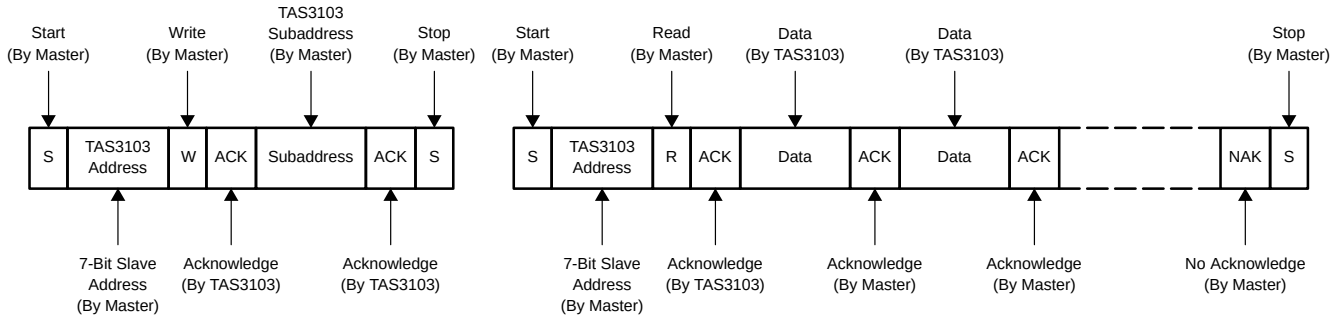
- Update coefficient values and output data to those GPIO ports configured as output.
- Read status flags, input data from those GPIO ports configured as inputs and retrieve spectrum analyzer/VU meter data.

In the master mode, the I2C bus is used to download a user-specific configuration from an I2C compatible EEPROM.

In the slave mode only, specific registers and memory locations in the TAS3103 are accessible with the use of I2C subaddresses. There are 256 such I2C subaddresses. The protocol required to access a specific subaddress is presented in Figure 2–16.

As shown in Figure 2–16, a read transaction requires that the master device first issue a write transaction to give the TAS3103 the subaddress to be used in the read transaction that follows. This subaddress assignment write transaction is then followed by the read transaction. For write transactions, the subaddress is supplied in the first byte of data written, and this byte is followed by the data to be written. For write transactions, the subaddress must always be included in the data written. There cannot be a separate write transaction to supply the subaddress, as was required for read transactions. If a subaddress assignment only write transaction is followed by a second write transaction supplying the data, erroneous behavior results. The first byte in the second write transaction is interpreted by the TAS3103 as another subaddress replacing the one previously written.

I²C Read Transaction



I²C Write Transaction

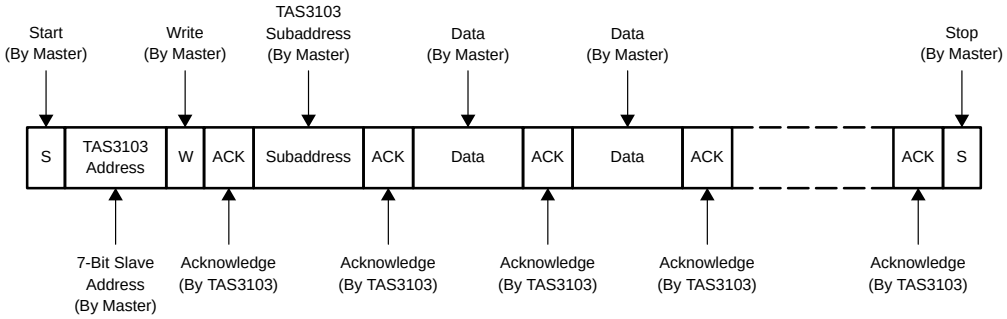


Figure 2–16. I²C Subaddress Access Protocol

2.3.2.1 I²C Master Mode Operation

The TAS3103 uses the master mode to download an operational configuration. The configuration downloaded must contain data for all 256 subaddresses, with spacer data supplied for those subaddresses that are GPIO subaddresses, read-only subaddresses, factory-test subaddresses, or unused (reserved) subaddresses. The spacer data must always be assigned the value zero. Table 2–3 organizes the 256 subaddresses (and their corresponding EEPROM addresses) into sequential blocks, with each block containing either valid data or spacer data.

Table 2–3 also illustrates that the subaddresses and their corresponding EEPROM memory addresses do not directly correlate. This is because many subaddresses are assigned more than one 32-bit word. For example, there is a unique subaddress for each biquad filter in the TAS3103, but each subaddress is assigned five 32-bit coefficients—resulting in twenty bytes of memory being assigned to each biquad subaddress.

The TAS3103, in the I²C master mode, can execute a complete download without requiring any wait states. After the TAS3103 has downloaded all 2367 bytes of coefficient and spacer data, the I²C bus is disabled and cannot be used to update coefficient values or retrieve status or spectrum/VU meter data. Volume control is available in the master mode via the four GPIO pins.

Table 2–3. I²C EEPROM Data

DATA TYPE		EEPROM BYTE ADDRESSES	SUB-ADDRESS(es)
Valid data	Starting I²C check word	0x00–0x03	0x00
	Input mixers—set 1	0x04–0xD3	0x01–0x33
	Effects block Bi-Quads	0xD4–0x29B	0x34–0x4B
	Reverb block mixers	0x29C–0x2C7	0x4C–0x4E
	CH1 Bi-Quads	0x2C8–0x3B7	0x4F–0x5A
	CH2 Bi-Quads	0x3B8–0x4A7	0x5B–0x66
	CH3 Bi-Quads	0x4A8–0x597	0x67–0x72
	Bass and treble inline/bypass mixers	0x5980x5AF	0x73–0x75
	DRC mixers	0x5B0–0x5DF	0x76–0x7E
	Dither input mixers	0x5E0–0x5EB	0x7F–0x81
	CH3 (sub-woofer) To CH 1/2 (L/R) mixers	0x5EC–0x5F3	0x82–0x83
	Spectrum analyzer/VU meter mixers	0x5F4–0x60B	0x84–0x89
	Output mixers	0x60C–0x66B	0x8A–0xA1
	CH1 loudness parameters	0x66C–0x697	0xA2–0xA6
	CH2 loudness parameters	0x698–0x6C3	0xA7–0xAB
	CH3 loudness parameters	0x6C4–0x6EF	0xAC–0xB0
	CH 1/2 DRC parameters	0x6F0–0x733	0xB1–0xB5
	CH3 DRC parameters	0x734–0x777	0xB6–0xBA
	Spectrum analyzer parameters	0x778–0x847	0xBB–0xC5
	Dither output mixers	0x848–0x84F	0xC6
	Dither speed	0x850–0x853	0xC7
Factory Test Data (EEPROM spacer data)		0x854–0x85F	0xC8–0xC9
Valid data	Input mixers—set 2	0x860–0x87F	0xCA–0xD1
Spacer Data		0x880–0x8E3	0xD2–0xEA
Valid data	Watchdog timer enable	0x8E4–0x8E7	0xEB
Factory Test Data (EEPROM spacer data)		0x8E8–0x8F3	0xEC–0xED
Valid data	GPIO port parameters	0x8F4–0x8FB	0xEE–0xEF
	Volume parameters	0x8FC–0x90F	0xF0–0xF4
	Bass/treble filter selections	0x910–0x91F	0xF5–0xF8
	I²S command word	0x920–0x923	0xF9
	Delay/reverb settings	0x924–0x92F	0xFA
	I²C M and N	0x930–0x933	0xFB
	Ending I²C check word	0x934–0x937	0xFC
Read Only Data (EEPROM spacer data)		0x938–0x943	0xFD–0xFF

NOTE: EEPROM organization must be big endian–MS byte of data word allocated to the lowest address in memory.

The I²C master mode also utilizes the starting and ending I²C check words to verify a proper EEPROM download. The first 32-bit data word received from the EEPROM, the starting I²C check word at subaddress 0x00, is stored and compared against the 32-bit data word received for subaddress 0xFC, the ending I²C check word. These two data words must be equal as stored in the EEPROM. If the two words do not match when compared in the TAS3103, the TAS3103 conducts another parameter download from the EEPROM. If the comparison check again fails, the TAS3103 discards all downloaded parameters and set all parameters to the default values listed in the subaddress table presented in the Appendix. In the I²C slave mode, these default values are used to initialize the TAS3103 at power turnon or after a reset.

2.3.2.2 I2C Slave Mode Operation

The I2C slave mode is the mode that must be used if it is required to change configuration parameters (other than volume via the GPIO pins for the I2C master mode) during operation. The I2C slave mode is also the only I2C mode that provides access to the spectrum analyzer and VU meter outputs. Configuration downloads from a master device can be used to replace the I2C master mode EEPROM download.

For I2C read commands, the TAS3103 responds with data, a byte at a time, starting at the subaddress assigned, as long as the master device continues to respond with acknowledges. If a given subaddress does not use all 32 bits, the unused bits are read as logic 0. I2C write commands, however, are treated in accordance with the data assignment for that address space. If a write command is received for a biquad subaddress, the TAS3103 expects to see five 32-bit words. If fewer than five data words have been received when a stop command (or another start command) is received, the data received is discarded. If a write command is received for a mixer coefficient, the TAS3103 expects to see only one 32-bit word.

Supplying a subaddress for each subaddress transaction is referred to as random I2C addressing. The TAS3103 also supports sequential I2C addressing. For write transactions, if a subaddress is issued followed by data for that subaddress and the fifteen subaddresses that follow, a sequential I2C write transaction has taken place, and the data for all 16 subaddresses is successfully received by the TAS3103. For I2C sequential write transactions, the subaddress then serves as the start address and the amount of data subsequently transmitted, before a stop or start is transmitted, determines how many subaddresses are written to. As was true for random addressing, sequential addressing does require that a complete set of data be transmitted. If only a partial set of data is written to the last subaddress, the data for the last subaddress is discarded. However, all other data written is accepted; just the incomplete data is discarded.

The GPIO subaddresses and most reserved read-only and factory test subaddresses require the downloading of four bytes of zero-valued spacer data in order to proceed to the next subaddress. However, there are five exceptions to this rule and Table 2–4 lists the subaddresses of these five exceptions and the number of zero-valued bytes that must be written.

Table 2–4. Four Byte Write Exceptions—Reserved and Factory-Test I2C Subaddresses

SUB-ADDRESS	NUMBER OF ZERO-VALUED BYTES THAT MUST BE WRITTEN
0xC9	8
0xED	8
0xFD	10 (0xA)
0xFE	2
0xFF	1

The TAS3103 can always receive sequential I2C addressing write data without issuing wait states. If it is desired to download data to all subaddresses using one sequential write transaction, spacer data for the reserved, GPIO, read-only, and factory-test subaddresses must be supplied as per Table 2–3 and Table 2–4.

The TAS3103 also supports sequential read transactions. When an I2C subaddress assignment write transaction is followed by a read transaction, the TAS3103 outputs the data for that subaddress, and then continue to output data for the subaddresses that follow as long as the master continues to issue data received acknowledges. Except for two exceptions, the TAS3103 outputs four bytes of zero-valued data for reserved and factory-test subaddresses. The subaddresses of the exceptions, and the number of bytes supplied by the TAS3103 for each exception, are given in Table 2–5. If a GPIO port is assigned as an output port, a logic 0 bit value is supplied by the TAS3103 for this GPIO port in response to a read transaction at subaddress 0xEE.

Table 2–5. Four Byte Read Exceptions—Reserved and Factory-Test I2C Subaddresses

SUB-ADDRESS	NUMBER BYTES SUPPLIED BY TAS3103
0xC9	8
0xED	8

NOTE: Table 2–5 does not include read-only subaddresses and thus does not include subaddresses 0xFD, 0xFE, and 0xFF. When read, these read-only subaddresses output 10, 2, and 1 byte respectively.

Thus, for all reserved and factory-test subaddresses, except subaddresses OxC9 and 0xED, the master device must issue four data received acknowledges for the four bytes of zero-valued data. For subaddresses OxC9 and 0xED, the master device must issue eight data received acknowledges for the eight bytes of zero-valued data.

Sequential read transactions do not have restrictions on outputting only complete subaddress data sets. If the master does not issue enough data received acknowledges to receive all the data for a given subaddress, the master device simply does not receive all the data. If the master device issues more data received acknowledges than required to receive the data for a given subaddress, the master device simply receives complete or partial sets of data, depending on how many data received acknowledges are issued, from the subaddress(es) that follow.

I^2C read transactions, both sequential and random, can impose wait states. For the standard I^2C mode (SCL = 100 kHz), worst-case wait state times, for an 8-MHz microprocessor clock, is on the order of 2 microseconds. Nominal wait state times, for the same 8-MHz microprocessor clock, is on the order of 1 microsecond. For the fast I^2C mode (SCL = 400 KHz), and the same 8-MHz microprocessor clock, worst-case wait state times can extend up to 10.5 microseconds in duration. Nominal wait state times for this same case lie in a range from 2 microseconds to 4.6 microseconds. Increasing the microprocessor clock frequency lowers the wait state times, and, for the standard I^2C mode, a higher microprocessor clock can totally eliminate the presence of wait states. For example, increasing the microprocessor clock to 16 MHz results in no wait states. For the fast I^2C mode, higher microprocessor clocks shortens the wait state times encountered, but does not totally eliminate their presence.

2.4 Digital Audio Processor (DAP) Arithmetic Unit

The digital audio processor (DAP) arithmetic unit is a fixed-point computational engine consisting of an arithmetic unit and data and coefficient memory blocks. Figure 2–17 is a block diagram of the arithmetic unit.

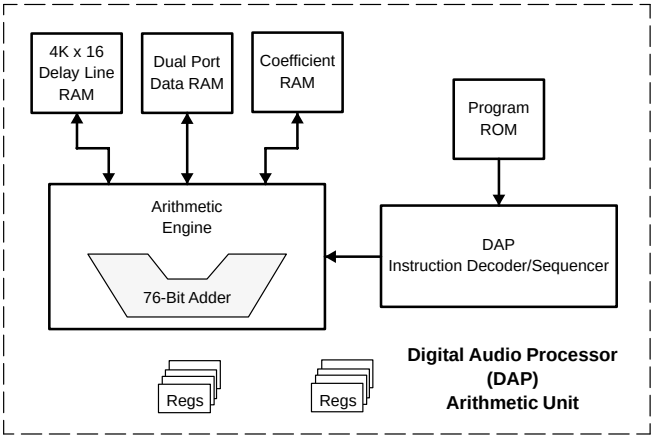


Figure 2–17. Digital Audio Processor Arithmetic Unit Block Diagram

The DAP arithmetic unit is used to implement all firmware functions—soft volume, loudness compensation, bass and treble processing, dynamic range control, channel filtering, 3D effects, input and output mixing, spectrum analyzer, VU meter, and dither.

Figure 2–18 shows the data word structure of the DAP arithmetic unit. Eight bits of overhead or guard bits are provided at the upper end of the 48-bit DAP word, and 8 bits of computational precision or noise bits are provided at the lower end of the 48-bit word. The incoming digital audio words are all positioned with the most significant bit abutting the 8-bit overhead/guard boundary. The sign bit in bit 39 indicates that all incoming audio samples are treated as signed data samples.

CAUTION: Audio data into the TAS3103 is always treated as signed data.

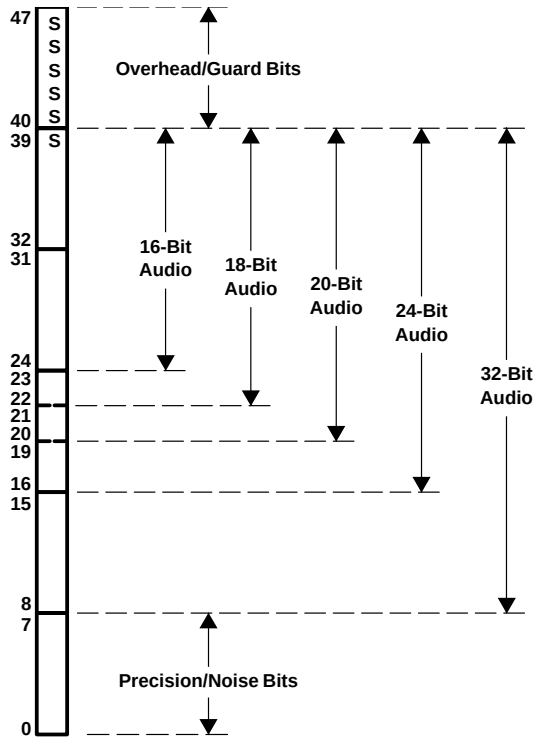


Figure 2–18. DAP Arithmetic Unit Data Word Structure

The arithmetic engine is a 48-bit (25.23 format) processor consisting of a general-purpose 76-bit arithmetic logic unit and function-specific arithmetic blocks. Multiply operations (excluding the function-specific arithmetic blocks) always involve 48-bit DAP words and 28-bit coefficients (usually I^2C programmable coefficients). If a group of products are to be added together, the 76-bit product of each multiplication is applied to a 76-bit adder, where a DSP-like multiply-accumulate (MAC) operation takes place. Biquad filter computations use the MAC operation to maintain precision in the intermediate computational stages.

To maximize the linear range of the 76-bit ALU, saturation logic is not used. Intermediate overflows are then permitted in multiply-accumulate operations, but it is assumed that subsequent terms in the multiply-accumulate computation flow corrects the overflow condition. The biquad filter structure used in the TAS3103 is the direct form I structure and has only one accumulation node. With this type of structure, intermediate overflow is allowed as long as the designer of the filters has assured that the final output is bounded and does not overflow. Figure 2–19 shows a bounded computation that experiences intermediate overflow condition. 16-bit arithmetic is used for ease of illustration.

The DAP memory banks include a dual port data RAM for storing intermediate results, a coefficient RAM, a 4K x 16 RAM for implementing the delay stages, and a fixed program ROM. Only the coefficient RAM, assessable via the I^2C bus, is available to the user.

	8-Bit ALU Operation (Without Saturation)		
	10110111	**(–73)**	**–73**
	+ 11001101	**(–51)**	**+ –51**
	10000100	**(–124)**	**–124**
	+ 11010011	**(–45)**	**+ –45**
Rollover →	**01010111**	**(57)**	**–169**
	+ 00111011	**(59)**	**+ 59**
	10010010	**(–110)**	**–110**

Figure 2–19. DAP ALU Operation With Intermediate Overflow

The DAP processing clock is set by pins PLL0 and PLL1, in conjunction with the source clock XTALI or MCLKI. The DAP operates at speeds up to 136 MHz, which is sufficient to process 96-kHz audio.

2.5 Reset

The reset circuitry in the TAS3103 is shown in Figure 2–20. A reset is initiated by inputting logic 0 on the reset pin $\overline{\text{RST}}$. A reset is also issued at power turnon by the internal 1.8-V regulator sub-system.

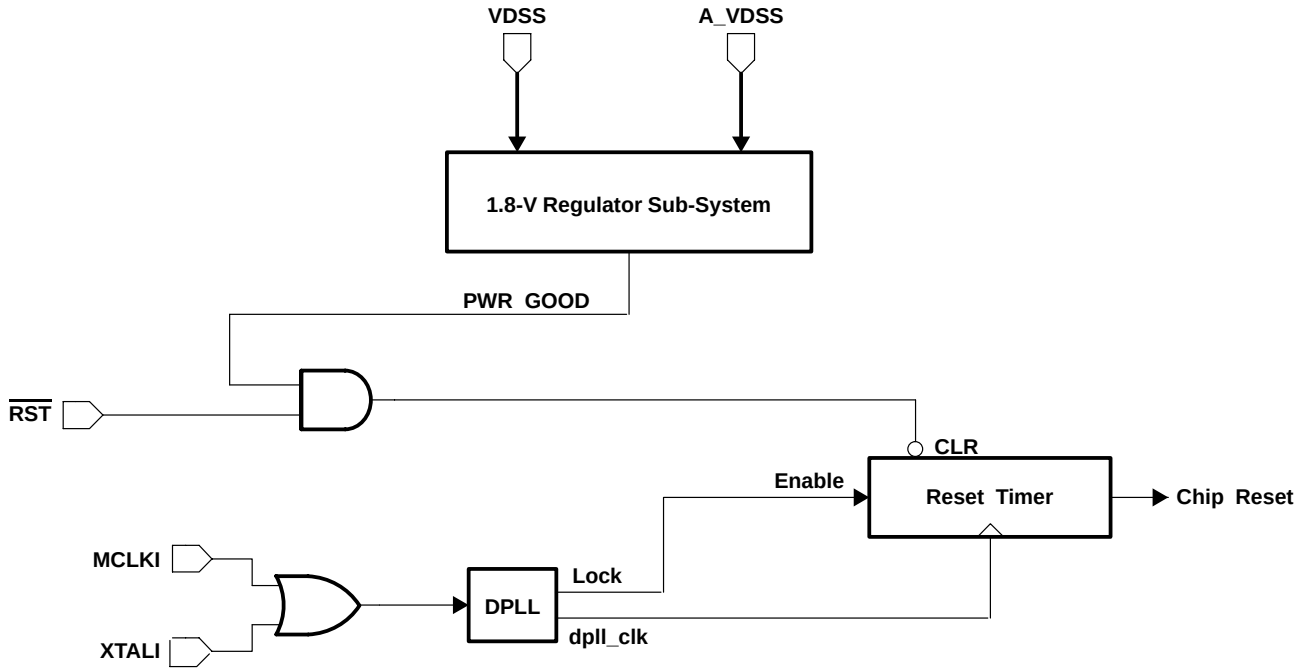


Figure 2–20. TAS3103 Reset Circuitry

At power turnon, the internal 1.8-V regulator sub-system issues an internal reset that remains active until regulation is reached. The duration of this signal assures that all reset activities are conducted at power turnon. This means that the external reset pin $\overline{\text{RST}}$ does not require an RC time constant derived external reset to assure that a reset is applied at power turn-on. The reset pin $\overline{\text{RST}}$ can then be used exclusively for exception resets, saving the cost and size impact of additional RC components. However, since $\overline{\text{RST}}$ is an asynchronous clear, it can respond to narrow negative signal transitions. Some applications, therefore, might require a high-frequency capacitor on the $\overline{\text{RST}}$ pin in order to remove unwanted noise excursions.

2.6 Power Down

Setting the PWRDN pin to logic 1 enables power down. Power down stops all clocks in the TAS3103, but preserves the state of the TAS3103. When PWRDN is deactivated (set to logic 0) after a period of activation, the TAS3103 resumes the processing of audio data upon receiving the next LRCLK (indicating a new sample of audio data is available for processing). The configuration of the TAS3103 and all programmable parameters are retained during power down.

There is a time lag between setting PWRDN to logic 1 and entering the power down state. Normally, PWRDN is sampled every GPIOFSCOUNT LRCLK periods (see the *subaddress 0xEF and the watchdog timer and GPIO ports* sections). This means that a time lag as great as GPIOFSCOUNT(1/LRCLK) could exist between the activation of PWRDN (setting to logic 1) the time at which the microprocessor recognizes that the PWRDN pin has been activated. Normally, upon recognizing that the PWRDN pin has been activated, the TAS3103 enters the power-down state approximately 80 microprocessor clock cycles later. However, if a soft volume update is in progress, the TAS3103 waits until the soft volume update is complete before entering the power down state. For this case then, the worst

case time lag between recognizing the activation of pin PWRDN and entering the power down would be 4096 LRCLK periods, assuming a volume slew rate selection (bit VSC of I^2C subaddress 0xF1) of 4096 and the issuance of a volume update immediately preceding the reading of pin PWRDN. The worst case time lag between setting PWRDN to logic 1 and entering the power down state is then:

$$\text{power} - \text{down} - \text{time lag}_{\text{Worst-Case}} = \frac{4096 + \text{GPIOFSCOUNT}}{\text{LRCLK}} + \frac{80}{\text{Microprocessor-Clock}}$$

There is also a time lag between deactivating PWRDN (setting PWRDN to logic 0) and exiting the power down state. This time lag is set by the time it takes the internal digital PLL to stabilize, and this time, in turn, is set by the master clock frequency (MCLKI or XTALI) and the PLL output clock frequency. For a 135-MHz PLL output clock and a 24.576 MCLKI, the time lag is approximately 25 microseconds. For an 11.264-MHz PLL output clock and a 1.024-MHz MCLKI, the time lag is approximately 360 microseconds.

Power consumption in the power-down state is approximately 12 mW.

2.7 Watchdog Timer

There is a watchdog timer in the TAS3103 that monitors the microprocessor activity. If the microprocessor ever ceases to execute its stored program, the watchdog timer fires and resets the TAS3103. This capability was included in the TAS3103 for factory test purposes and has little use in applications. The program structure used in the microprocessor assures that the microprocessor always executes its stored program unless a hardware failure occurs.

The watchdog timer is governed by the parameter GPIOFSCOUNT in subaddress 0xEF and the LSB of the 32-bit word at subaddress 0xEB. The default value of the LSB of the 32-bit word at subaddress 0xEB is 1 and this value disables the watchdog timer. The GPIOFSCOUNT is also used in other functions and balancing the needs of these other functions regarding GPIOFSCOUNT with the requirements of the watchdog timer is an involved process. For this reason, it is strongly recommended that the LSB of the 32-bit word at subaddress 0xEB remain a 1. If an application does require use of the watchdog timer, it is requested that the user contact an application engineer in the Digital Audio Department of Texas Instruments for details in properly using this feature.

2.8 General-Purpose I/O (GPIO) Ports

The TAS3103 has four general-purpose I/O (GPIO) ports. Figure 2–21 is a block diagram of the GPIO circuitry in the TAS3103.

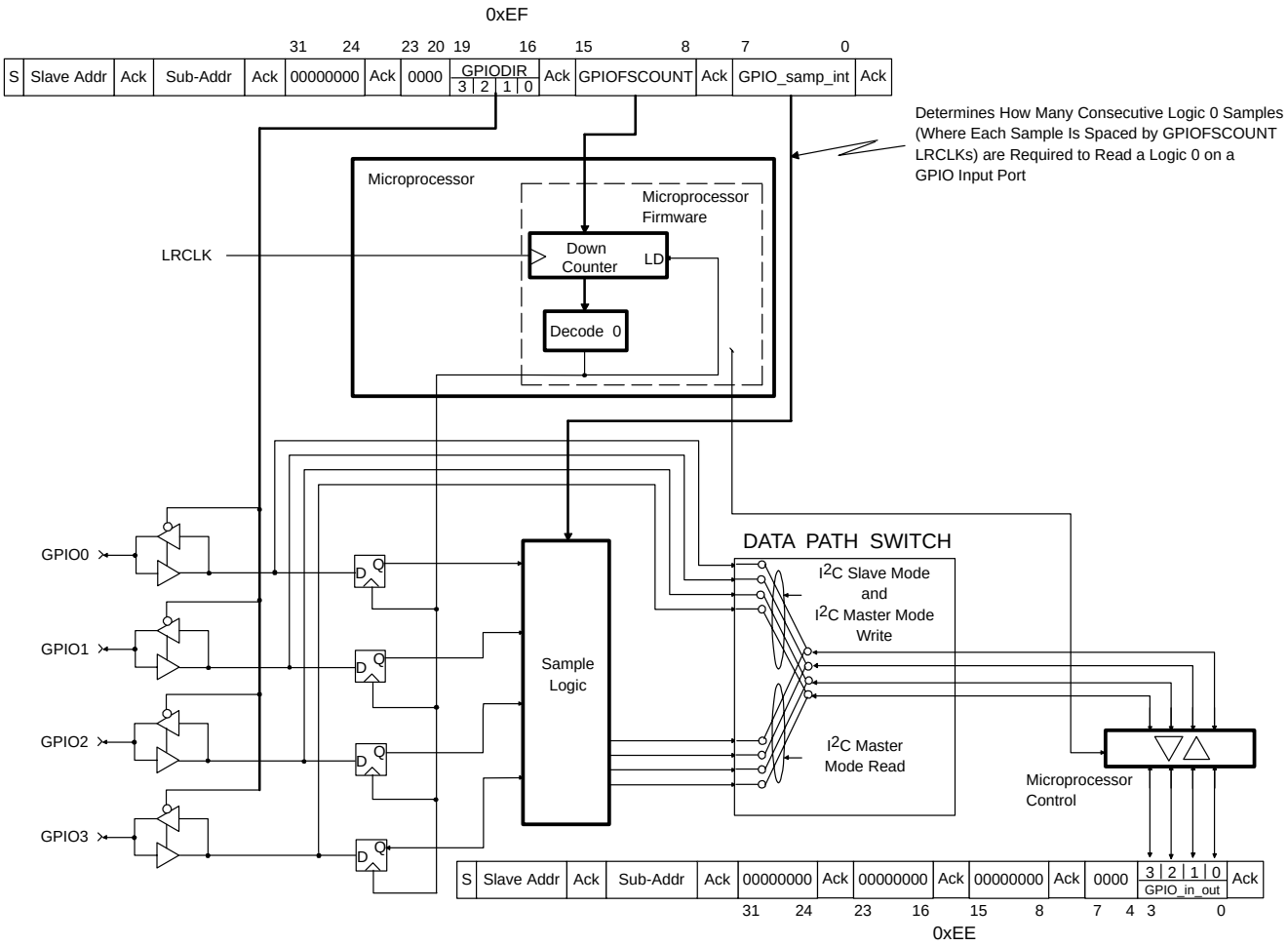


Figure 2–21. GPIO Port Circuitry

2.8.1 GPIO Functionality—I²C Master Mode

In the I²C master mode, the GPIO ports are strictly input ports and are used to control volume. Table 2–6 lists the functionality of each GPIO port in the I²C master mode. Bit field GPIOFSCOUNT (15:8) of I²C subaddress 0xEF governs the rate at which the GPIO pins are sampled for a volume update. The sample rate is:

$$f_{GPIO\_Port} = \frac{LRCLK}{GPIOFSCOUNT}$$

Table 2–6. GPIO Port Functionality—I²C Master Mode

GPIO PORT	FUNCTION
GPIO0 (pin 18)	Volume up—CH1 and CH2
GPIO1 (pin 19)	Volume down—CH1 and CH2
GPIO2 (pin 20)	Volume up—CH3
GPIO3 (pin 21)	Volume down—CH3

GPIOFSCOUNT also governs the rate at which the power down pin PWRDN is sampled and the rate at which the watchdog counter is reset. GPIOFSCOUNT then cannot be independently used to tune the volume adjustment. For this reason, bit field GPIO_samp_int of the same I²C subaddress (0xEF) is included to provide the ability to adjust the responsiveness (or sluggishness) of the volume switches.

Each GPIO port has a weak pullup to VDDS. A volume control switch then typically switches the signal line to the GPIO port between ground and an open circuit. The parameter GPIO_samp_int sets how many consecutive GPIO port

samples must be logic 0 before a logic 0 is read. A read logic 0 on a given GPIO port is interpreted as a command to increase or decrease volume. If a logic 0 is read, and the signal level into the GPIO port remains at logic 0 for another GPIO_samp_int consecutive samples, a second logic 0 value is read.

For each logic 0 read, the volume is increased or decreased 0.5 dB. After two consecutive logic 0 readings, each logic 0 reading that follows results in the volume level increasing or decreasing 5 dB instead of 0.5 dB. Figure 2–22 shows an example of activating a volume switch. For the example in Figure 2–22, GPIOFSCOUNT is set to 3 and GPIO_samp_int is set to 2. It is also noted in Figure 2–22 that the parameter GPIO_samp_int only comes into play on logic 0 valued samples. As soon as the GPIO sample goes to logic 1, the audio updating ceases.

2.8.2 GPIO Functionality—I^{2}C Slave Mode

In the I^{2}C slave mode, the GPIO ports can be used as true general-purpose ports. Each port can be individually programmed, via the I^{2}C bus, to be either an input or an output port. The default assignment for all GPIO ports, in the I^{2}C slave mode, is an input port.

When a given GPIO port is programmed as an output port, by setting the appropriate bit in the bit field GPIODIR (19:16) of subaddress 0xEF to logic 1, the logic level output is set by the logic level programmed into the appropriate bit in bit field GPIO_in_out (3:0) of subaddress 0xEE. The I^{2}C bus then controls the logic output level for those GPIO ports assigned as output ports.

When a given GPIO port is programmed as an input port by setting the appropriate bit in bit field GPIODIR (19:16) of subaddress 0xEF to logic 0, the logic input level into the GPIO port is written to the appropriate bit in bit field GPIO_in_out (3:0) of subaddress 0xEE. The I^{2}C bus can then be used to read bit field GPIO_in_out to determine the logic levels at the input GPIO ports. Whether a given bit in the bit field GPIO_in_out is a bit to be read via the I^{2}C bus or a bit to be written to via the I^{2}C bus is strictly determined by the corresponding bit setting in bit field GPIODIR.

In the I^{2}C slave mode, the GPIO input ports are read every GPIOFSCOUNT LRCLKs, as was the case in the I^{2}C master mode. However, parameter GPIO_samp_int does not have a role in the I^{2}C slave mode. If a GPIO port is assigned as an output port, a logic 0 bit value is supplied by the TAS3103 for this GPIO port in response to a read transaction at subaddress 0xEE.

If the GPIO ports are left in their power turnon state default state, they are input ports with a weak pullup on the input to VDSS.

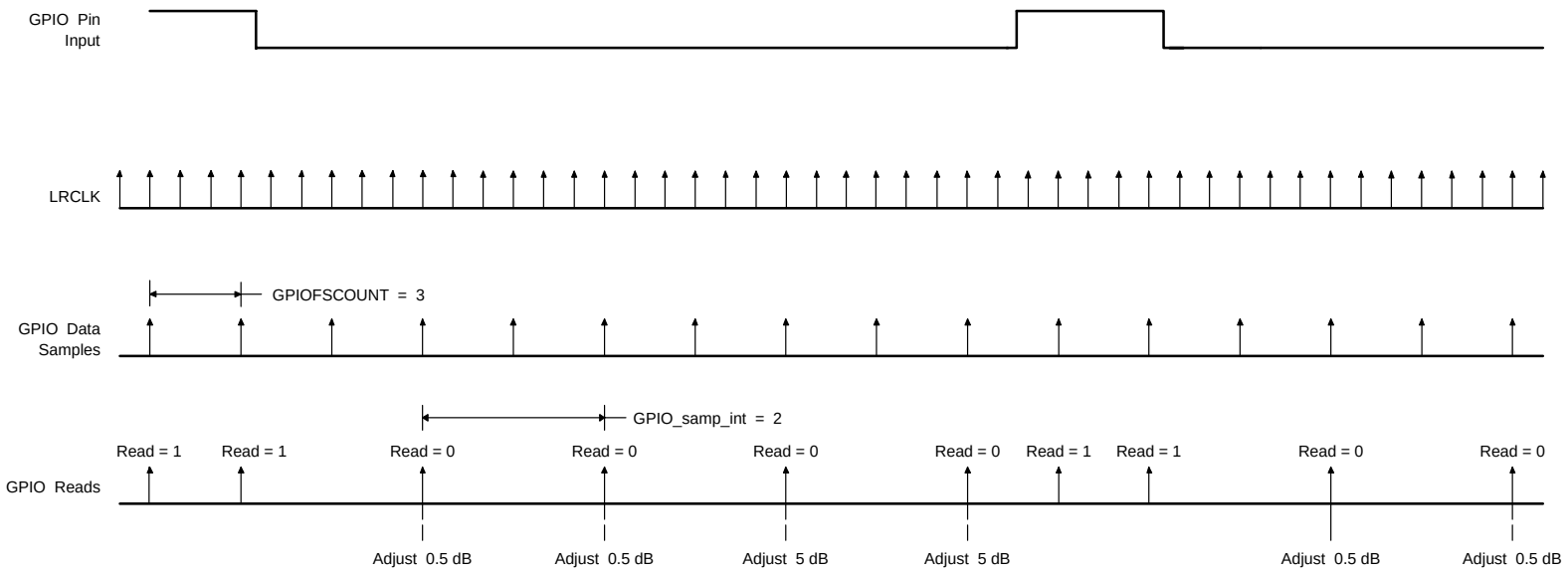


Figure 2–22. Volume Adjustment Timing—Master I^{2}C Mode

3 Firmware Architecture

3.1 Input Crossbar Mixers

3.2 3D Effects Block

3.3 BiQuad Filters

3.4 Treble and Bass Management

3.5 Soft Volume/Loudness Management

3.6 Dynamic Range Control (DRC)

The DRC provides both compression and expansion capabilities over three separate and definable regions of audio signal levels. Programmable threshold levels set the boundaries of the three regions. Within each of the three regions a distinct compression or expansion transfer function can be established and the slope of each transfer function is determined by programmable parameters. The offset (boost or cut) at the two boundaries defining the three regions can also be set by programmable offset coefficients. The DRC implements the composite transfer function by computing a 5.23 format gain coefficient from each sample output from the rms estimator. This gain coefficient is then applied to a mixer element, whose other input is the audio data stream. The mixer output is the DRC-adjusted audio data.

There are two distinct DRC blocks in the TAS3103. One DRC services two monaural channels - CH1 and CH2. This DRC computes rms estimates of the audio data streams on both CH1 and CH2. The two estimates are then compared on a sample-by-sample basis, and the larger of the two is used to compute the compression/expansion gain coefficient. The gain coefficient is then applied to both CH1 and CH2 audio. The other DRC services only monaural channel CH3. This DRC also computes an rms estimate of the signal level on CH3, and this estimate is used to compute the compression/expansion gain coefficient applied to CH3 audio.

Figure 3–1 shows the positioning of the DRC block in the TAS3103 processing flow. As seen, the DRC input can come from either before or after soft volume control and loudness processing, or can be a weighted combination of both. The mixers feeding the DRC control the selection of which audio data stream or combination thereof, is input into the DRC. The mixers also provide a means of gaining or attenuating the signal level into the DRC. If the DRC setup is referenced to the 0-dB level at the TAS3103 input, the coefficient values for these mixers must be taken into account. Discussions and examples that follow further explore the role the mixers play in setting up the transfer function of the DRC.

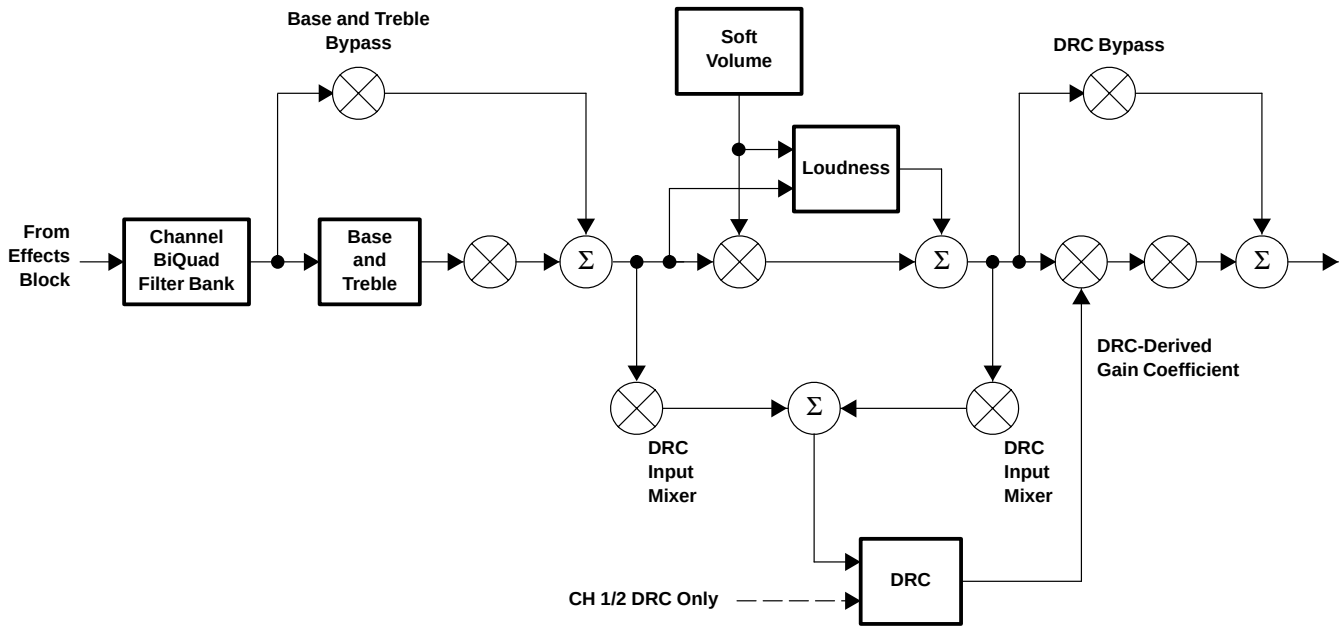


Figure 3–1. DRC Positioning in TAS3103 Processing Flow

Figure 3–2 illustrates a typical DRC transfer function.

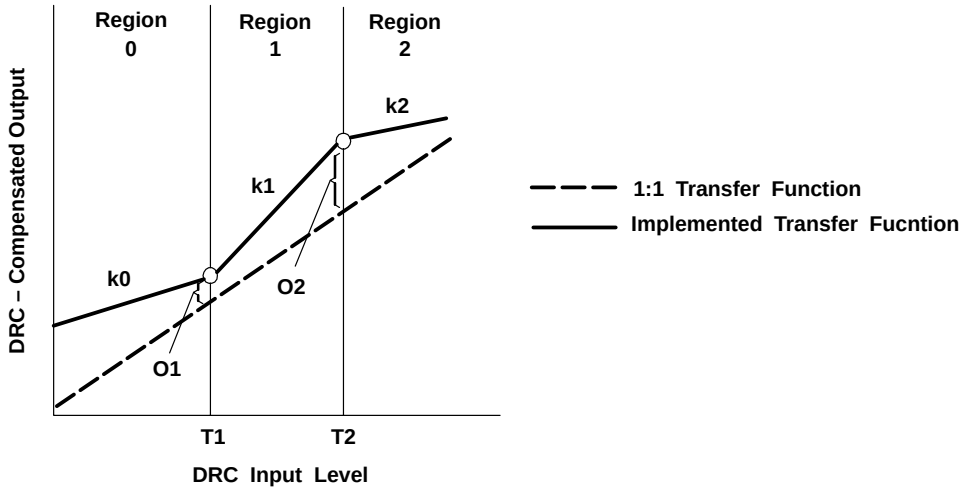


Figure 3–2. Dynamic Range Compression (DRC) Transfer Function Structure

The three regions shown in Figure 3–2 are defined by three sets of programmable coefficients:

- Thresholds T1 and T2—define region boundaries.
- Offsets O1 and O2—define the DRC gain coefficient settings at thresholds T1 and T2 respectively.
- Slopes k0, k1, and k2—define whether compression or expansion is to be performed within a given region. The magnitudes of the slopes define the degree of compression or expansion to be performed.

The three sets of parameters are all defined in logarithmic space and adhere to the following rules:

- The maximum input sample into the DRC is referenced at 0 dB. All values below this maximum value then have negative values in logarithmic (dB) space.
- The samples input into the DRC are 32-bit words and consist of the upper 32 bits of the 48-bit word format used by the digital audio processor (DAP). The 48-bit DAP word is derived from the 32-bit serial data

received at the serial audio receive port by adding 8 bits of headroom above the 32-bit word and 8 bits of computational precision below the 32-bit word. If the audio processing steps between the SAP input and the DRC input results in no accumulative boost or cut, the DRC would operate on the 8 bits of headroom and the 24 MSBs of the audio sample. Under these conditions, a 0-dB (maximum value) audio sample (0x7FFFFFFF) is seen at the DRC input as a –48-dB sample (8 bits x –6.02 dB/bit = –48 dB).

- Thresholds T1 and T2 define, in dB, the boundaries of the three regions of the DRC, as referenced to the rms value of the data into the DRC. Zero valued threshold settings reference the maximum valued rms input into the DRC and negative valued thresholds reference all other rms input levels. Positive valued thresholds have no physical meaning and are not allowed. In addition, zero valued threshold settings are not allowed.

Although the DRC input is limited to 32-bit words, the DRC itself operates using the 48-bit word format of the DAP. The 32-bit samples input into the DRC are placed in the upper 32 bits of this 48-bit word space. This means that the threshold settings must be programmed as 48-bit (25.23 format) numbers.

CAUTION:
Zero valued and positive valued threshold settings are not allowed and cause unpredictable behavior if used.

- Offsets O1 and O2 define, in dB, the attenuation (cut) or gain (boost) applied by the DRC-derived gain coefficient at the threshold points T1 and T2 respectively. Positive offsets are defined as cuts, and thus boost or gain selections are negative numbers. Offsets must be programmed as 48-bit (25.23 format) numbers.
- Slopes k0, k1, and k2 define whether compression or expansion is to be performed within a given region, and the degree of compression or expansion to be applied. Slopes are programmed as 28-bit (5.23 format) numbers.

3.6.1 DRC Implementation

Figure 3–3 shows the three elements comprising the DRC: (1) an rms estimator, (2) a compression/expansion coefficient computation engine, and (3) an attack/decay controller.

- RMS estimator—This DRC element derives an estimate of the rms value of the audio data stream into the DRC. For the DRC block shared by CH1 and CH2, two estimates are computed - an estimate of the CH1 audio data stream into the DRC, and an estimate of the CH2 audio data stream into the DRC. The outputs of the two estimators are then compared, sample-by-sample, and the larger valued sample is forwarded to the compression/expansion coefficient computation engine.

  Two programmable parameters, ae and (1 – ae), set the effective time window over which the rms estimate is made. For the DRC block shared by CH1 and CH2, the programmable parameters apply to both rms estimators. The time window over which the rms estimation is computed can be determined by:

$$t_{window} = \frac{1}{F_S \, \ell n(1 - ae)}$$

- Compression/expansion coefficient computation—This DRC element converts the output of the rms estimator to a logarithmic number, determines the region that the input resides, and then computes and outputs the appropriate coefficient to the attack/decay element. Seven programmable parameters—T1, T2, O1, O2, k0, k1, and k2—define the three compression/expansion regions implemented by this element.
- Attack/decay control—This DRC element controls the transition time of changes in the coefficient computed in the compression/expansion coefficient computation element. Four programmable parameters define the operation of this element. Parameters ad and 1 – ad set the decay or release time constant to be used for volume boost (expansion). Parameters aa and 1 – aa set the attack time constant to be used for volume cuts. The transition time constants can be determined by:

$$t_a = \frac{1}{F_S \, \ell n(1 - aa)} \qquad t_d = \frac{1}{F_S \, \ell n(1 - ad)}$$

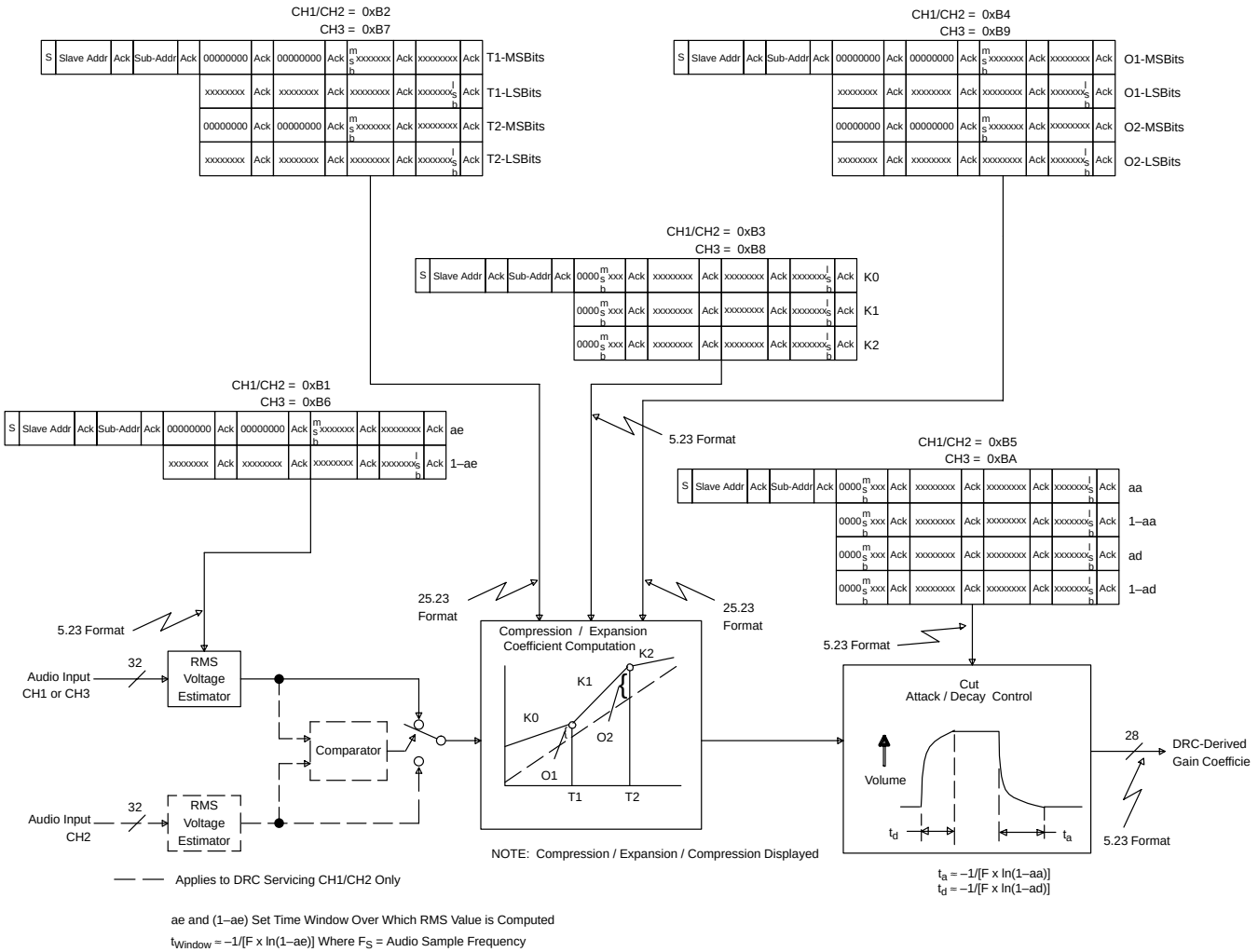


Figure 3–3. DRC Block Diagram

3.6.2 Compression/Expansion Coefficient Computation Engine Parameters

There are seven programmable parameters assigned to each DRC block: two threshold parameters - T1 and T2, two offset parameters - O1 and O2, and three slope parameters - k0, k1, and k2. The threshold parameters establish the three regions of the DRC transfer curve, the offsets anchor the transfer curve by establishing known gain settings at the threshold levels, and the slope parameters define whether a given region is a compression or an expansion region.

The audio input stream into the DRC must pass through DRC-dedicated programmable input mixers. These mixers are provided to scale the 32-bit input into the DRC to account for the positioning of the audio data in the 48-bit DAP word and the net gain or attenuation in signal level between the SAP input and the DRC. The selection of threshold values must take the gain (attenuation) of these mixers into account. The DRC implementation examples that follow illustrate the effect these mixers have on establishing the threshold settings.

T2 establishes the boundary between the high-volume region and the mid-volume region. T1 establishes the boundary between the mid-volume region and the low-volume region. Both thresholds are set in logarithmic space, and which region is active for any given rms estimator output sample is determined by the logarithmic value of the sample.

Threshold T2 serves as the fulcrum or pivot point in the DRC transfer function. O2 defines the boost (> 0dB) or cut (< 0 dB) implemented by the DRC-derived gain coefficient for an rms input level of T2. If O2 = 0 dB, the value of the derived gain coefficient is 1.0 (0x00, 80, 00, 00 in 5.23 format). k2 is the slope of the DRC transfer function for rms input levels above T2, and k1 is the slope of the DRC transfer function for rms input levels below T2 (and above T1). The labeling of T2 as the fulcrum stems from the fact that there cannot be a discontinuity in the transfer function at T2. The user can, however, set the DRC parameters to realize a discontinuity in the transfer function at the boundary defined by T1. If no discontinuity is desired at T1, the value for the offset term O1 must obey the following equation.

$$O1_{\text{No Discontinuity}} = (T1 - T2) \times k1 + O2$$

T1 and T2 are the threshold settings in dB, k1 is the slope for region 1, and O2 is the offset in dB at T2. If the user chooses to select a value of O1 that does not obey the above equation, a discontinuity at T1 is realized.

Going down in volume from T2, the slope k1 remains in effect until the input level T1 is reached. If, at this input level, the offset of the transfer function curve from the 1:1 transfer curve does not equal O1, there is a discontinuity at this input level as the transfer function is snapped to the offset called for by O1. If no discontinuity is wanted, O1 and/or k1 must be adjusted so that the value of the transfer curve at the input level T1 is offset from the 1:1 transfer curve by the value O1. The examples that follow illustrate both continuous and discontinuous transfer curves at T1.

Going down in volume from T1, starting at the offset level O1, the slope k0 defines the compression/expansion activity in the lower region of the DRC transfer curve.

3.6.2.1 Threshold Parameter Computation

For thresholds,

$$T_{dB} = -6.0206T_{INPUT} = -6.0206T_{SUB\_ADDRESS\_ENTRY}$$

If, for example, it is desired to set T1 = -64dB, then the sub-address entry required to set T1 to -64 dB is:

$$T1_{SUB\_ADDRESS\_ENTRY} = \frac{-64}{-6.0206} = 10.63$$

From Figure 3–3, it can be seen that T1 is entered as a 48-bit number in 25.23 format. Therefore:

T1 = 10.63 = 0_1010.1010_0001_0100_0111_1010_111
= 0x00000550A3D7 in 25.23 format

3.6.2.2 Offset Parameter Computation

The offsets set the boost or cut applied by the DRC-derived gain coefficient at the threshold point. An equivalent statement is that offsets represent the departure of the actual transfer function from a 1:1 transfer at the threshold point. Offsets are 25.23 formatted 48-bit logarithmic numbers. They are computed by the following equation.

$$O_{INPUT} = \frac{O_{DESIRED} + 24.0824\ dB}{6.0206}$$

Gains or boosts are represented as negative numbers; cuts or attenuation are represented as positive numbers. For example, to achieve a boost of 21 dB at threshold T1, the I^2C coefficient value entered for O1 must be:

$$O1_{INPUT} = \frac{-21\ dB + 24.0824\ dB}{6.0206} = 0.51197555$$

$$= 0.1000\_0011\_0001\_1101\_0100$$

$$= 0x00000041886A \text{ in } 25.23 \text{ format}$$

More examples of offset computations are included in the following examples.

3.6.2.3 Slope Parameter Computation

In developing the equations used to determine the sub-address input value required to realize a given compression or expansion within a given region of the DRC, the following convention is adopted.

DRC Transfer = Input Increase : Output Increase

If the DRC realizes an output increase of n dB for every dB increase in the rms value of the audio into the DRC, a 1:n expansion is being performed. If the DRC realizes a 1 dB increase in output level for every n dB increase in the rms value of the audio into the DRC, a n:1 compression is being performed.

For 1:n expansion, the slope k can be found by:

$k = n - 1$

For n:1 compression, the slope k can be found by: $k = \frac{1}{n} - 1$

In both expansion (1:n) and compression (n:1), n is implied to be greater than 1. Thus, for expansion:

$k = n - 1$ means $k > 0$ for $n > 1$. Likewise, for compression, $k = \frac{1}{n} - 1$ means $-1 < k < 0$ for $n > 1$. Thus, it appears that k must always lie in the range $k > -1$.

The DRC imposes no such restriction and k can be programmed to values as negative as –15.999. To determine what results when such values of k are entered, it is first helpful to note that the compression and expansion equations for k are actually the same equation. For example, a 1:2 expansion is also a 0.5:1 compression.

$$0.5 \text{ Compression} \Rightarrow k = \frac{1}{0.5} - 1 = 1$$

$$1:2 \text{ Expansion} \Rightarrow k = 2 - 1 = 1$$

As can be seen, the same value for k is obtained either way. The ability to choose values of k less than –1 allows the DRC to implement negative slope transfer curves within a given region. Negative slope transfer curves are usually not associated with compression and expansion operations, but the definition of these operations can be expanded to include negative slope transfer functions. For example, if k = –4

$$\text{Compression Equation: } k = -4 = \frac{1}{n} - 1 \Rightarrow n = -\frac{1}{3} \Rightarrow -0.3333 : 1 \text{ compression}$$

$$\text{Expansion Equation: } k = -4 = n - 1 \Rightarrow n = -3 \Rightarrow 1 : -3 \text{ expansion}$$

With k = –4, the output decreases 3 dB for every 1 dB increase in the rms value of the audio into the DRC. As the input increases in volume, the output decreases in volume.

3.6.3 DRC Compression/Expansion Implementation Examples

The following four examples illustrate the steps that must be taken to calculate the DRC compression/expansion coefficients for a specified DRC transfer function. The first example is an expansion/compression/expansion implementation without discontinuities in the transfer function and represents a typical application. This first example also illustrates one of the three modes of DRC saturation—32-bit dynamic range limitation saturation. The second example is a compression/expansion/compression implementation. There is no discontinuity at T1 and 32-bit dynamic range saturation occurs at low volume levels into the DRC. Example 2 also illustrates another form of DRC saturation—maximum gain saturation. Example 3 illustrates the concept of infinite compression. Also, in Example 3, 32-bit dynamic range saturation occurs at low volume levels and the third form of DRC saturation is illustrated—minimum gain saturation. Example 4 illustrates the ability of the DRC to realize a negative slope transfer function. This example also illustrates two of the three forms of saturation—32-bit dynamic range saturation at low volume levels and minimum gain saturation.

CAUTION:

The examples presented all exhibit some form of DRC saturation. This is not intended to imply that all (or most) DRC transfer implementation exhibit some form of saturation. Most practical implementations do not exhibit saturation. The examples are chosen to explain by example the three types of saturation that can be encountered. But the phenomenon of saturation can also be used to advantage in that it effectively provides a means to implement more than three zones or regions of operation. If saturation is intended, the regions exhibiting the transfer characteristic set by k0, k1, and k2 provide three regions and the regions exhibiting saturation provide the additional regions of operation.

3.6.3.1 Example 1—Expansion/Compression/Expansion Transfer Function With 32-Bit Dynamic Range Saturation

For this example, the following transfer characteristics are chosen.

- Threshold point 2: T2 = –26 dB, O2 = 30 dB
- Threshold point 1: T1 = –101 dB, O1 = –7.5 dB
- Region 0 slope: k0 = 0.05 ≥ 1:1.05 Expansion
- Region 1 slope: k1 = –0.5 ≥ 2:1 Compression
- Region 2 slope: k2 = 0.1 ≥ 1:1.1 Expansion

The thresholds T1 and T2 are typically referenced, by the user, to the 0-dB signal level into the TAS3103. But to determine the equivalent threshold point at the DRC input, it is necessary to take into account the processing gain (or loss) between the TAS3103 SAP input and the DRC. Assume, as an example, the processing gain structure shown in Figure 3–4. Inputting the data below the 8-bit headroom in the 48-bit DAP word and then routing only the upper 32 bits of the 48-bit word into the DRC, results in a 48-dB (8 bits x 6 dB/bit = 48 dB) attenuation of the signal level into the DRC. Channel processing gain and use of the dedicated mixer into the DRC can revise this apparent 48-dB attenuation in signal level into the DRC. In Figure 3–4, the 24 mixer gain into the DRC, coupled with a net channel gain of 0 dB, changes the net 48-dB attenuation of the signal level into the DRC to a net attenuation of 24 dB.

For slopes:

Region 0 = 1:1.05 Expansion ≥ k0 = 1.05 – 1 = 0.05
= 00000.0000_1100_1100_1100_1100_110
= 0x0066666 in 5.23 format

Region 1 = 2:1 Compression ≥ k1 = 1/2 – 1 = -0.5
= 11111.1000_0000_0000_0000_0000_000
= 0xFC00000 in 5.23 format

Region 2 = 1:1.1 Expansion ≥ k2 = 1.1 – 1 = 0.1
= 00000.0001_1001_1001_1001_1001_100
= 0x00CCCCC in 5.23 format

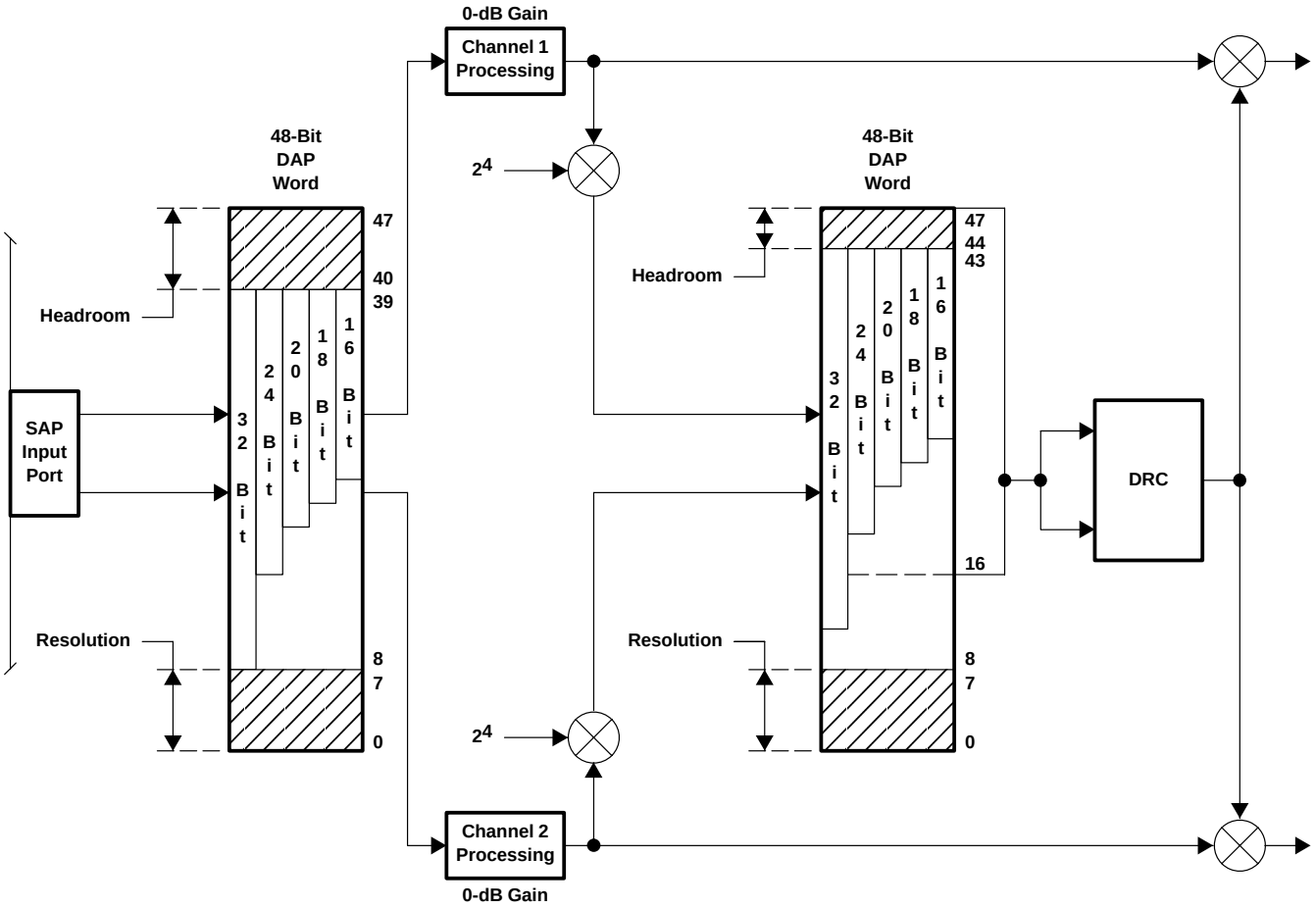


Figure 3–4. DRC Input Word Structure for 0-dB Channel Processing Gain

The resulting DRC transfer function for the above parameters is shown in Figure 3–5. The threshold T2 is set at the DRC rms input level of –50 dB, which corresponds to a –26-dB rms signal level at the SAP input. The DRC-compensated output at T2 is cut 30 dB with respect to the 1:1 transfer function (O2 = 30 dB). The threshold T1 is set at the DRC rms input level of –125 dB, which corresponds to a –101-dB rms signal level at the SAP input. The DRC-compensated output at T1 is boosted by 7.5 dB with respect to the 1:1 transfer function (O1 = –7.5 dB).

For thresholds, $T_{dB} = -6.0206T_{INPUT} = -6.0206T_{SUB\_ADDRESS\_ENTRY}$.

Therefore,

$T2 = –26\text{ dB} –24\text{ dB} = –50\text{ dB} \geq T2_{INPUT}$ = –50/–6.0206 = 8.30482
= 01000.0100_1110_0000_1000_1010_111
= 0x000004270457 in 25.23 format

$T1 = –101\text{ dB} –24\text{ dB} = –125\text{ dB} \geq T1_{INPUT}$ = –125/–6.0206 = 20.76205
= 010100.1100_0011_0001_0101_1011_010
= 0x00000A618ADA in 25/23 format

For offsets, $O_{INPUT} = \frac{1}{6.0206}\left[O_{dB} + 24.0824\right]$.

Therefore, $O2_{INPUT} = \frac{1}{6.0206}[30 + 24.0824] = 8.982892$
= 01000.1111_1011_1001_1110_1100_111
= 0x0000047DCF67 in 25.23 format

$$O1_{INPUT} = \frac{1}{6.0206}[-7.5 + 24.0824] = 2.754277$$
$$= 010.1100\_0001\_0001\_1000\_0100\_110$$
$$= 0x000001608C26 \text{ in } 25.23 \text{ format}$$

For input levels above the T2 threshold, the transfer function exhibits a 1:1.1 expansion. For input levels below T2, the transfer function exhibits a 2:1 compression. Also, by definition, it is seen that there is no discontinuity in the transfer function at T2. When the 2:1 compression curve in region 1 intersects the T1 threshold level, the output level is 7.5 dB above the 1:1 transfer, an offset value identical to O1. Thus, there is no discontinuity at T1. For input levels below T1, the transfer function exhibits a 1:1.05 expansion.

DRC rms input levels below –192 dB fall below the 32-bit precision of the DRC input (32 bits x –6 dB/bit = –192 dB). This means that for levels below –192 dB, the DRC sees a constant input level of 0, and thus the computed DRC gain coefficient remains fixed at the value computed when the input was at –192 dB. The transfer function then has a 1:1 slope below the –192-dB input level and is offset from the 1:1 transfer curve by the offset present at the –192-dB input level.

The change from a 1:1.05 expansion to a 1:1 transfer below –192 dB is the result of 32-bit dynamic range saturation at the DRC input. This type of saturation always occurs at a DRC input level of –192 dB. However, the input level at which this type of saturation occurs depends on the channel gain. For this example, the saturation occurs at an input level of –168 dB (–192-dB DRC input + 48 dB 8-bit headroom –24-dB mixer gain into DRC).

3.6.3.2 Example 2—Compression/Expansion/Compression Transfer Function With Maximum Gain Saturation and 32-Bit Dynamic Range Saturation

The transfer function parameters for this example are given in Table 3–1. In setting the threshold levels it is assumed that the net processing gain between the SAP input and the DRC is 0 dB. This is the same as Example 1 except that the gain of the mixer into the DRC is set to 1 instead of 2^4. Because of the 8-bit headroom in the 48-bit DAP word, the upper eight bits of the 32-bit DRC input word are zero, resulting in 0-dB signal levels at the SAP input being seen as –48-dB signal levels at the DRC.

Figure 3–5 shows the DRC transfer function resulting from the parameters given in Table 3–1. At threshold level T2 (–70 dB), O2 specifies a boost of 30 dB. But the signed 5.23 formatted gain coefficient only provides a 24-dB boost capability (5 integer bits = Sxxxx $\geq 2^4 \times$ 6 dB/octave = 24 dB). Internally, the DRC operates in 48-bit space and thus computes a 30-dB boost. But the 5.23 formatted gain coefficient saturates or clips at 24 dB. The transfer curve thus resides 24 dB above the 1:1 transfer curve at T2.

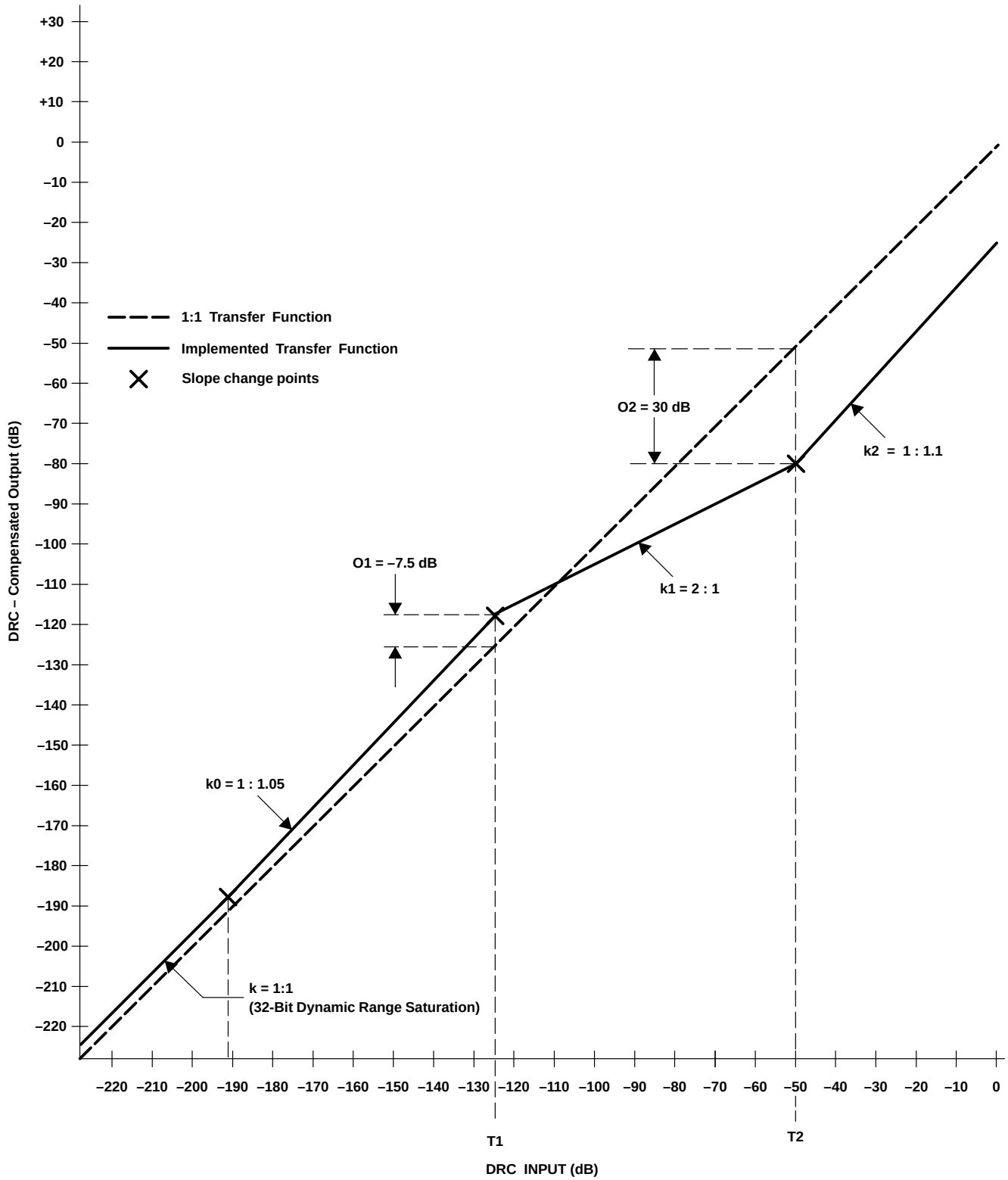


Figure 3–5. DRC Transfer Curve—Example 1

The transfer curve remains a constant 24 dB above the 1:1 transfer curve for input levels above and below T2 until the computed DRC gain coefficient falls within the dynamic range of a 5.23 format number. For input levels above T2, k2 implements a 5:1 compression, At an input level 7.5 dB above T2 (–62.5 dB), the DRC transfer curve has risen 7.5/5 = 1.5 dB. The boost at this point is 30 dB - (7.5 dB - 1.5 dB) = 24 dB. The DRC has come out of gain saturation. For input levels above –62.5 dB, the transfer curve exhibits 5:1compression.

Table 3–1. DRC Example 2 Parameters

DRC PARAMETER	REQUIRED (SPECIFIED) VALUE (NET $GAIN_{SAP\ Input\text{-}DRC}$ = 0 dB)	I^2C COEFFICIENT VALUE
T2	$-22\ dB_{Input} \geq -70\ dB_{DRC}$	–70/–6.0206= 11.626748 = $0x000005D03948_{25.23\ Format}$
T1	$-102\ dB_{Input} \geq -150\ dB_{DRC}$	–150/–6.0206 = 24.91446 = $0x00000C750D09_{25.23\ Format}$
O2	–30 dB	(–30 + 24.0824)/6.0206 = –0.982892 = $0xFFFFFF823098_{25.23\ Format}$
O1	50 dB	(50 + 24.0824)/6.0206 = 12.304820 = $0x000006270458_{25.23\ Format}$
k2	5:1 Compression	(1/5) – 1 = –0.8 = $0xF99999A_{5.23\ Format}$
k1	1:2 Expansion	2 – 1 = 1 = $0x0800000_{5.23\ Format}$
k0	2:1 Compression	(1/2) – 1 = –0.5 = $0xFC00000_{5.23\ Format}$

For input levels below T2, k1 implements a 1:2 expansion. With a 1:2 expansion in effect, the transfer curve has dropped 12 dB at an input level 6 dB below T2. The boost at this level is 30 dB – (12 dB – 6 dB) = 24 dB. The DRC gain coefficient has again come out of saturation. For input levels below –76 dB and above –150 dB, the transfer curve exhibits a 1:2 expansion.

At T1 (-150 dB), the transfer curve is 50 dB below the 1:1 transfer curve. Since O1 = 50 dB, there is no discontinuity in the transfer function. For inputs below –150 dB, k0 implements a 2:1 compression. The change from a 2:1 compression to a 1:1 transfer at –192 dB is due to 32-bit dynamic range saturation at the DRC input.

3.6.3.3 Example 3—1:1 Transfer/Infinite Compression With Minimum Gain Saturation, 32-Bit Dynamic Range Saturation, and Equal Threshold Settings (T1=T2)

The DRC transfer function parameters for this example are given in Table 3–2. In addition to illustrating minimum gain saturation, this example also illustrates the operation of the DRC when T1 and T2 are set equal.

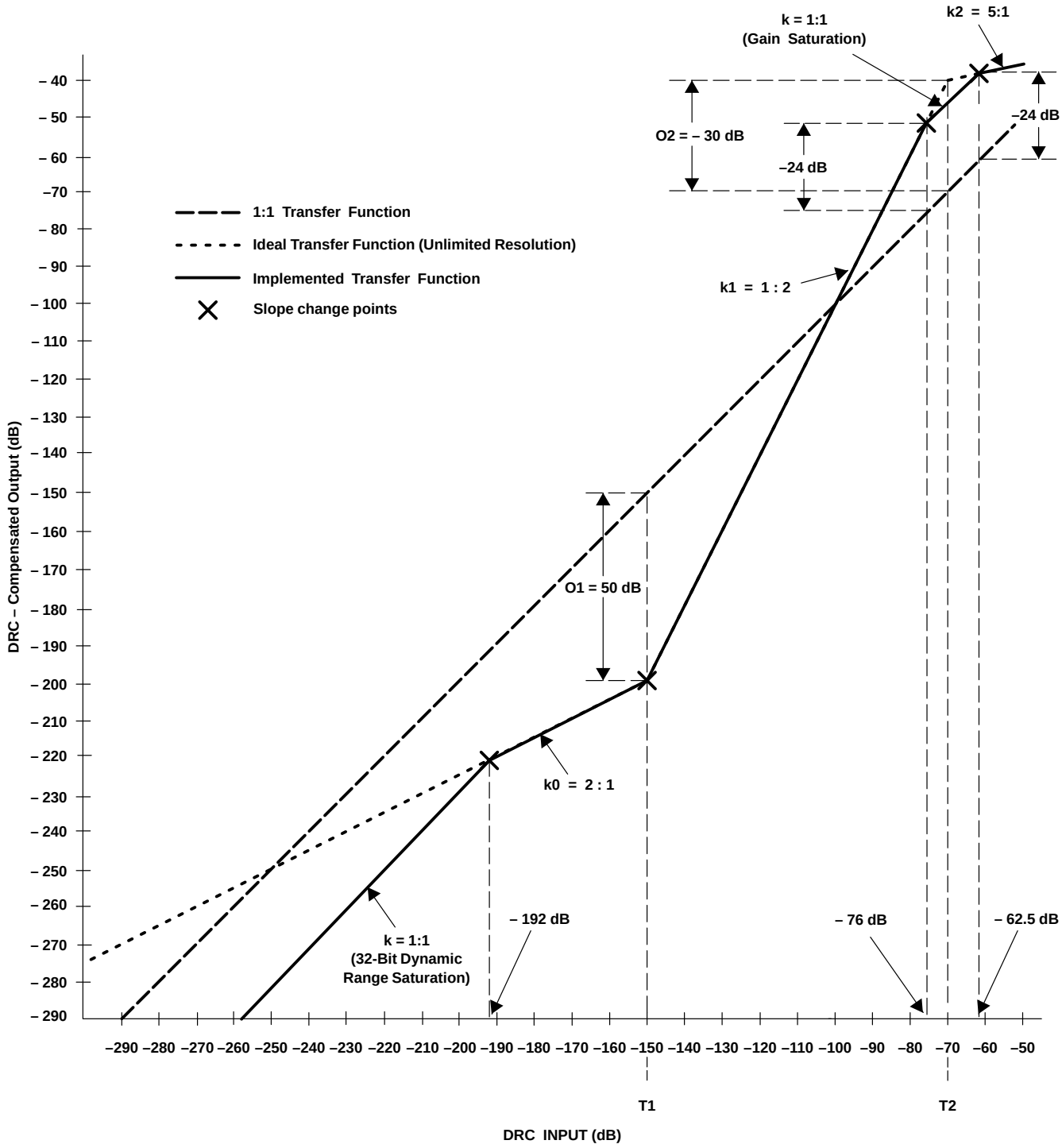


Figure 3–6. DRC Transfer Curve—Example 2

When T1 and T2 are set equal, the following questions arise:

- If O1 ≠ O2, what roles do O1 and O2 have?
- Which slope parameter, k0 or k1, has control of the transfer function for input levels below the common threshold point?
- Does k2 control the transfer function for inputs above the common threshold point?

This example addresses and answers those questions.

Table 3–2. DRC Example 3 Parameters

DRC PARAMETER	REQUIRED (SPECIFIED) VALUE (NET GAIN$_{\text{SAP Input-DRC}}$ = 0 dB)	I^{2}C COEFFICIENT VALUE
T1 and T2	–148.7 dB$_{\text{Input}}$ ≥ –172.7 dB$_{\text{DRC}}$	–172.7/–6.0206 = 28.684849 = 0x00000E57A91F$_{25.23\ \text{Format}}$
O2	–20 dB	(–20 + 24.0824)/6.0206 = 0.678072 = 0x00000056CB0F$_{25.23\ \text{Format}}$
O1	10 dB	(10 + 24.0824)/6.0206 = 5.660964 = 0x000002D49A78$_{25.23\ \text{Format}}$
k2	∞:1 Compression	(1/∞) – 1 = –1 = 0xF800000$_{5.23\ \text{Format}}$
k1	1:1 Transfer	(1/1) – 1 = 1 = 0 = 0x0000000$_{5.23\ \text{Format}}$
k0	2:1 Compression	(1/2) – 1 = –0.5 = 0xFC00000$_{5.23\ \text{Format}}$

For this example it is assumed that a net processing gain of 2^4 (24 dB) is realized from the SAP input and the DRC (which is identical to the net processing gain assumed for Example 1). The 2^4 gain results in reducing the 8-bit headroom in the 48-bit DAP word to a headroom of four bits. The 32-bit data into the DRC then resides in bits 27:0, which means that the data level into the DRC is down 24 dB with respect to the input level at the SAP. Data input into the TAS3103 (SAP) at a level of –148.7 dB is seen as a –148.7 dB – 24 dB = –172.7-dB signal at the DRC. T1 and T2 must be set to –172.7 dB to realize a common threshold point at an incoming signal level of –148.7 dB.

Figure 3–7 shows the transfer function resulting from entering the I^{2}C coefficient values given in Table 3–2. At the T1/T2 threshold, a discontinuity of 30 dB is observed. For inputs above the threshold, the transfer curve is horizontal (infinite compression), and the horizontal line starts 20 dB above the 1:1 transfer curve at the threshold point. Thus, for cases when T1 = T2, O2 governs the offset with regard to the starting point of the transfer curve above the common threshold point and k2 determines the slope of the transfer curve. For inputs below the common threshold point, the transfer curve exhibits a 2:1 compression and starts 10 dB below the 1:1 transfer curve. Thus, O1 sets the offset at the threshold point for the transfer curve at and below the common threshold point and k0 determines the slope of this curve. Slope parameter k1 plays no role when T1 = T2. The value of 0 (1:1 transfer) used in this example for k1 could be changed to any value and the resulting transfer function would not be altered. The change from a 2:1 compression to a 1:1 transfer at –192 dB is due to 32-bit dynamic range saturation at the DRC input.

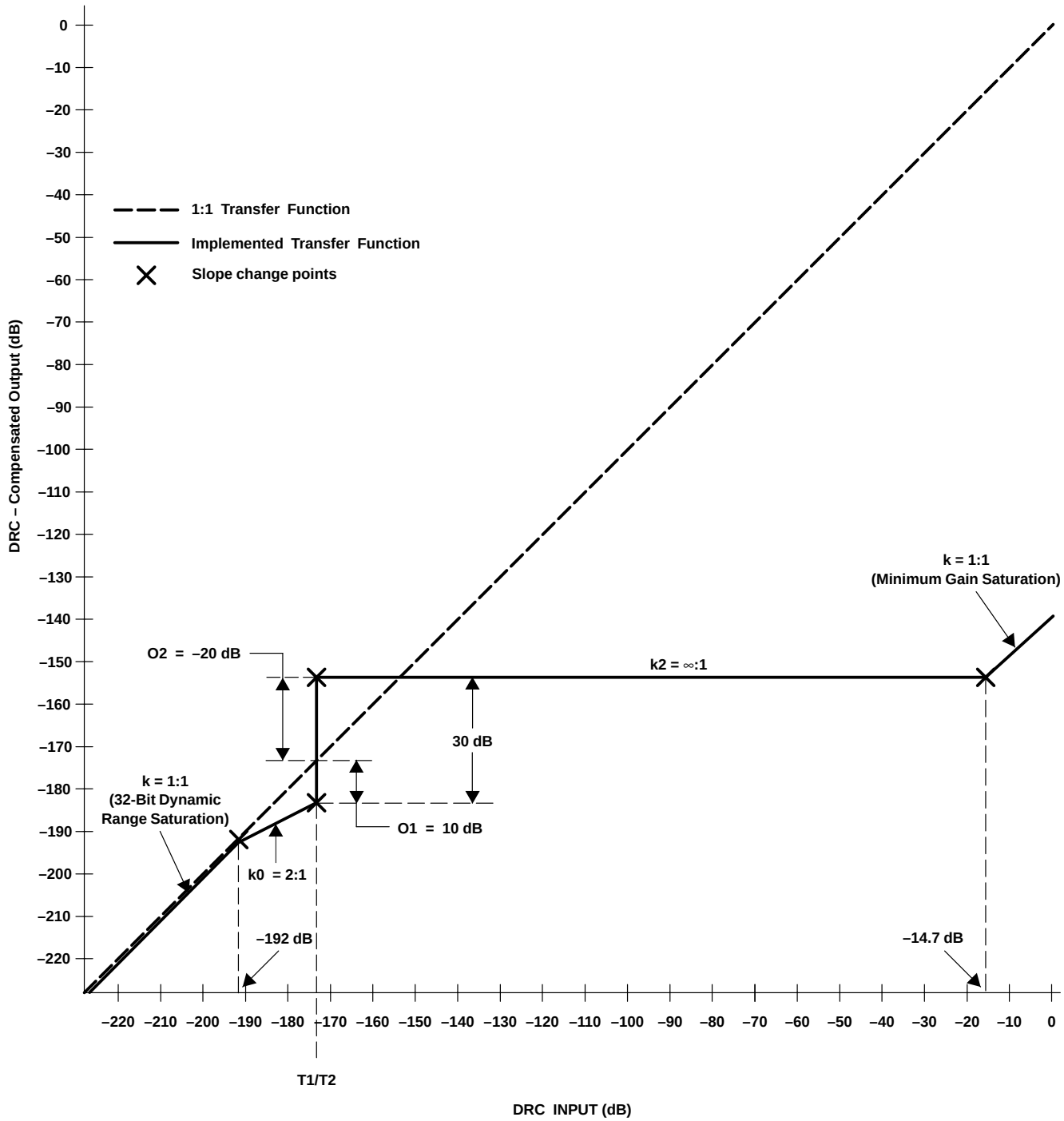


Figure 3–7. DRC Transfer Curve—Example 3

The horizontal slope of the transfer curve above the common threshold point does not remain horizontal indefinitely. At a point 158 dB above the common threshold point (–14.7-dB DRC input level), the transfer function has gone from a boost of 20 dB to a cut of 138 dB. A cut of 138 dB is the maximum cut possible for a 5.23 format gain coefficient ($2^{-23} \geq 23$ octaves $\times$ 6 dB/octave = 138 dB). Thus, at a DRC input level of –14.7 dB, minimum gain saturation has been reached. For inputs above this saturation point, the DRC-derived gain coefficient remains constant at the minimum gain value (2^{-23}), and the transfer function exhibits a 1:1 transfer slope.

3.6.3.4 Example 4—Expansion/Cut/Expansion With Gain Saturation and 32-Bit Dynamic Range Saturation

The three previous examples restricted the slope factor k to lie in the range $k \geq -1$. This example illustrates the transfer characteristic obtained using a value of k less than –1. For this example it is assumed that the net processing gain into the DRC is 0 dB. This means that the 8-bit headroom in the 48-bit DAP processing word structure does not contain data. Since the DRC receives the upper 32 bits of this 48-bit word, data at the DRC is down 48 dB (8 bits x 6 dB/ bit = 48 dB) with respect to the signal level at the SAP input (TAS3103 input). The transfer function parameters for this example are given in Table 3–3. Figure 3–8 shows the transfer function resulting from entering the I^2C coefficient values given in Table 3–3.

At the threshold point T2 (–70 dB), the transfer function is 100 dB below the 1:1 transfer slope (O2 = 100 dB). For input levels above T2, the transfer function exhibits a 1:1.4 expansion. For input levels below T2, the transfer function exhibits a negative slope; for every dB the input decreases, the output increases by 1 dB. At an input level 62 dB below T2 (–132 dB), the transfer curve has risen 62 dB, for a net boost of 124 dB. The transfer curve at this input level is 24 dB above the 1:1 transfer curve. This boost value puts the DRC-derived gain coefficient into gain saturation. For input levels below –132 dB, the gain coefficient remains constant at maximum gain and the transfer function exhibits a 1:1 transfer slope, parallel to the 1:1 transfer curve but 24 dB above it.

At T1 (-150 dB), the transfer curve snaps back to the 1:1 transfer curve since O1 = 0 dB. The DRC gain coefficient is no longer in gain saturation and for inputs below –150 dB, the transfer function exhibits a 1:1.5 expansion. The change from a 1:1.5 expansion to a 1:1 transfer below –192 dB is the result of 32-bit dynamic range saturation.

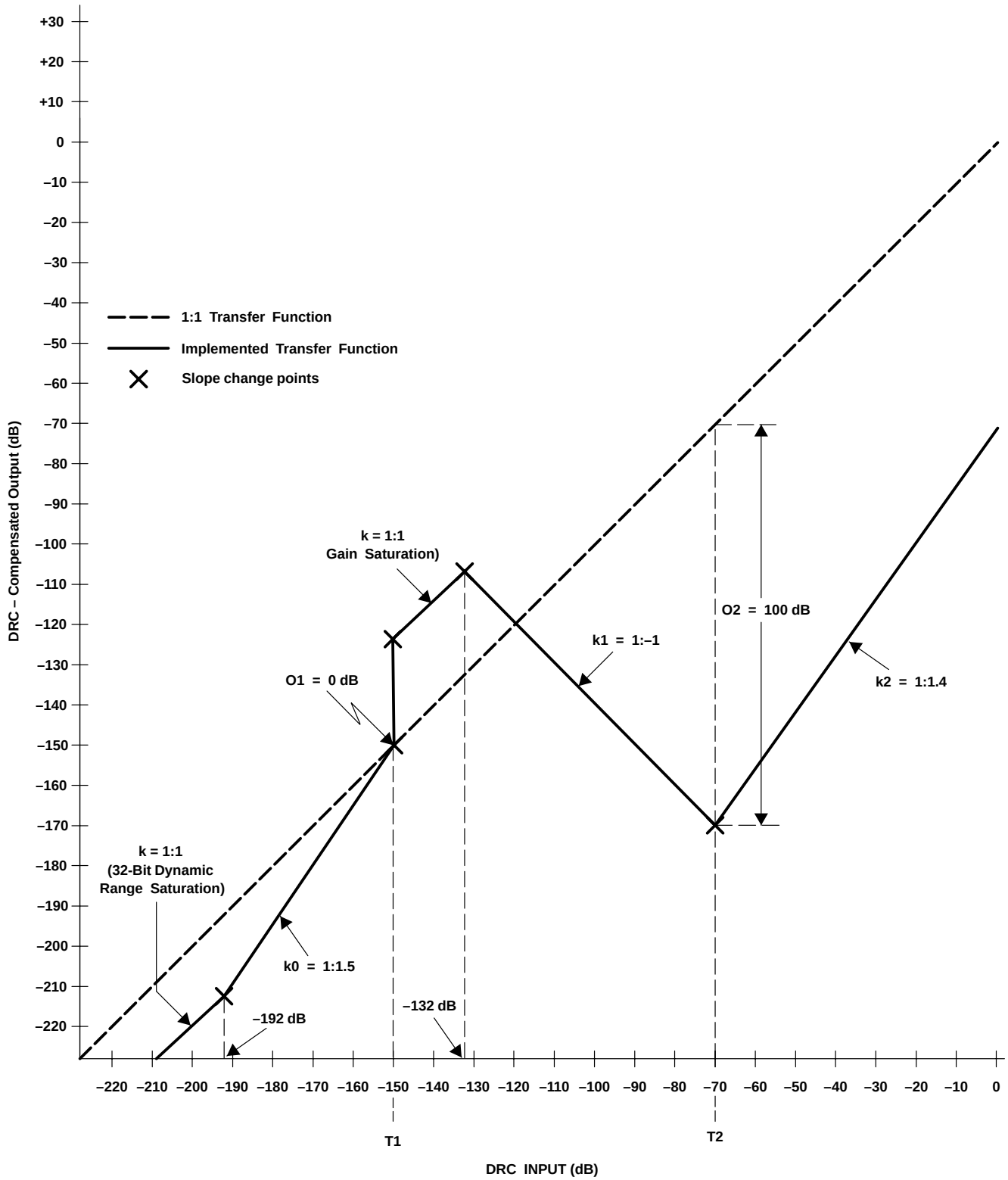


Figure 3–8. DRC Transfer Curve—Example 4

Table 3–3. DRC Example 4 Parameters

DRC PARAMETER	REQUIRED (SPECIFIED) VALUE (NET GAIN$_{\text{SAP Input-DRC}}$ = 0 dB)	I^2C COEFFICIENT VALUE
T2	–22 $dB_{Input} \geq$ –70 dB_{DRC}	–70/–6.0206= 11.626748 = 0x000005D03948$_{25.23\ Format}$
T1	–102 $dB_{Input} \geq$ –150 dB_{DRC}	–150/–6.0206 = 24.91446 = 0x00000C750D09$_{25.23\ Format}$
O2	100 dB	(100 + 24.0824)/6.0206 = 20.609640 = 0x00000A4E08B0$_{25.23\ Format}$
O1	0 dB	(0 + 24.0824)/6.0206 = 4.000000 = 0x000002000000$_{25.23\ Format}$
k2	1:1.4 Expansion	1.4 – 1 = 0.4 = 0X0333333$_{5.23\ Format}$
k1	1:–1 Transfer	(1/–1) – 1 = –1 –1 = –2 = 0XF000000$_{5.23\ Format}$
k0	1:1.5 Expansion	1.5 – 1 = 0.5 = 0x0400000$_{5.23\ Format}$

3.7 Spectrum Analyzer/VU Meter

3.8 Adjustable Dither Block

3.9 Output Crossbar Multiplexer

4 Electrical Specifications

4.1 Absolute Maximum Ratings Over Operating Temperature Ranges (unless otherwise noted)†

Supply voltage range: VDDS . . . . . –0.3 to 3.6 V
A_VDDS . . . . . –0.3 to 3.6 V
Input voltage range, V_I: 3.3-V LVCMOS . . . . . –0.5 V to VDDS + 0.5 V
1.8-V LVCMOS . . . . . –0.5 V to DVDD(1) + 0.5 V
Output voltage range, V_O: 3.3-V LVCMOS . . . . . –0.5 V to VDDS + 0.5 V
1.8-V LVCMOS . . . . . –0.5 V to DVDD(1) + 0.5 V
Input clamp curent, I_{IK} (V_I < 0 or V_I > DVDD) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > DVDD) . . . . . ±20 mA
Operating free-air temperature . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: DVDD is a 1.8-V supply derived from regulators internal to the TAS3103 chip. DVDD is routed to pin 29 (DVDD_BYPASS_CAP) to provide access to external filter capacitors, but should not be used to source power to external devices.

DISSIPATION RATING TABLE (Low-k Board, 125°C Junction)

PACKAGE	$T_A \leq 25°C$ POWER RATING	OPERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DBT	0.82 W	8.21 mW/°C	0.451 mW

4.2 Recommended Operating Conditions

		MIN	NOM	MAX	UNITS
Digital supply voltage, VDDS		3	3.3	3.6	V
Analog supply voltage, A_VDDS		3	3.3	3.6	V
High-level input voltage, V_{IH}	3.3-V LVCMOS	0.7 VDDS		VDDS	V
	1.8-V LVCMOS (XTALI)	0.7 DVDD		DVDD	
Low-level input voltage, V_{IL}	3.3-V LVCMOS	0		0.3 VDDS	V
	1.8-V LVCMOS (XTALI)	0		0.3 DVDD	
Input voltage, V_I	3.3-V LVCMOS	0		VDDS	V
	1.8-V LVCMOS (XTALI)	0		DVDD	
Output voltage, V_O	3.3-V LVCMOS	0.8 VDDS		VDDS	V
	1.8-V LVCMOS (XTALO)	0.8 DVDD		DVDD	
Operating ambient air temperature range, T_A		0		70	°C
Operating junction temperature range, T_J		0		115	°C

4.3 Electrical Characteristics Over Recommended Operating Conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{OH}	High-level output voltage	3.3-V LVCMOS	I_{OH} = –4 mA	0.8 VDDS			V
		1.8-V LVCMOS (XTALO)	I_{OH} = –0.55 mA	0.8 DVDD			
V_{OL}	Low-level output voltage	3.3-V LVCMOS	I_{OL} = 4 mA			0.22 VDDS	V
		1.8-V LVCMOS (XTALO)	I_{OL} = 0.75 mA			0.22 DVDD	
I_{OZ}	High-impedance output current	3.3-V LVCMOS				±20	µA
I_{IL}	Low-level input current	3.3-V LVCMOS	$V_I = V_{IL}$			±1	µA
		1.8-V LVCMOS (XTALI)	$V_I = V_{IL}$			±1	
I_{IH}	High-level input current	3.3-V LVCMOS	$V_I = V_{IH}$			±1	µA
		1.8-V LVCMOS (XTALI)	$V_I = V_{IH}$			±1	
I_{DD}	Input supply current	Digital supply voltage, DVDD	DSP clock = 135 MHz		TBD		mA
			DSP clock = 67.5 MHz		TBD		
			DSP clock = 33.75 MHz		TBD		
			Power down		TBD		µA
		Analog supply voltage, AVDD	Normal		TBD		mA
			Power down		TBD		µA

4.4 TAS3100 Timing Characteristics

4.4.1 Master Clock Signals Over Recommended Operating Conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$f_{(XTALI)}$	Frequency, XTALI		2.8		20	MHz
$t_{c(1)}$	Cycle time, XTALI	See Note 2	50		357	ns
$f_{(MCLKI)}$	Frequency, MCLKI ($1/t_{c(2)}$)		2.8		50	MHz
$t_{w(MCLKI)}$	Pulse duration, MCLKI high	See Note 3	H_{MCLKI} – TBD	H_{MCLKI}	H_{MCLKI} + TDB	ns
$f_{(MCLKO)}$	Frequency, MCLKO ($1/t_{c(3)}$)	C_L = 50 pF	2.8		50	MHz
$t_{r(MCLKO)}$	Rise time, MCLKO				TDB	ns
$t_{f(MCLK)}$	Fall time, MCLKO				TDB	ns
$t_{w(MCLKO)}$	Pulse duration, MCLKO high	See Note 3	H_{MCLKO} – TDB	H_{MCLKO}	H_{MCLKO} + TDB	ns
$t_{d(MI–MO)}$	Delay time, MCLKI rising edge to MCLKO rising edge	See Note 4 and Note 5			TBD	ns

NOTES: 2. Typical duty cycle is 50/50.
3. HMCLKI = 1 /2MCLKI
4. Only applies when MCLKI is selected as master source clock.
5. Also applies to MCLKO falling edge when MCLKO = MCLKI/2 or MCLKI/4

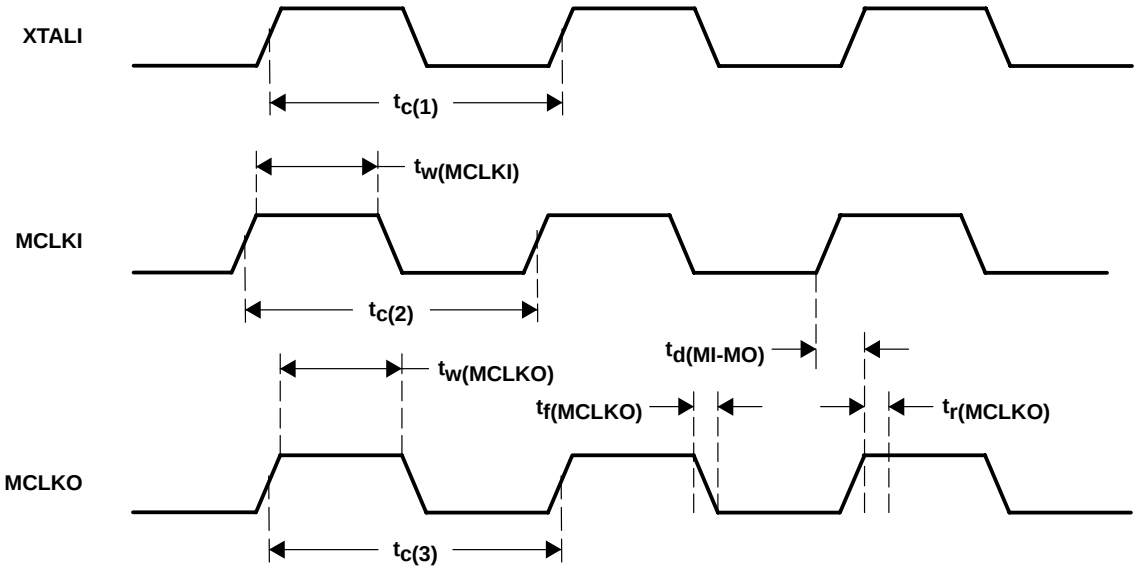


Figure 4–1. Master Clock Signals Timing Waveforms

4.4.2 Control Signals Over Recommended Operating Conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$t_{w1(L)}$	Pulse duration, $\overline{RST}$ low		TBD			µs
t_{pd1}	Propagation delay, PWRDN high to power down state asserted		TBD			µs
t_{pd2}	Propagation delay, PWRDN low to power down state deasserted		TBD			µs

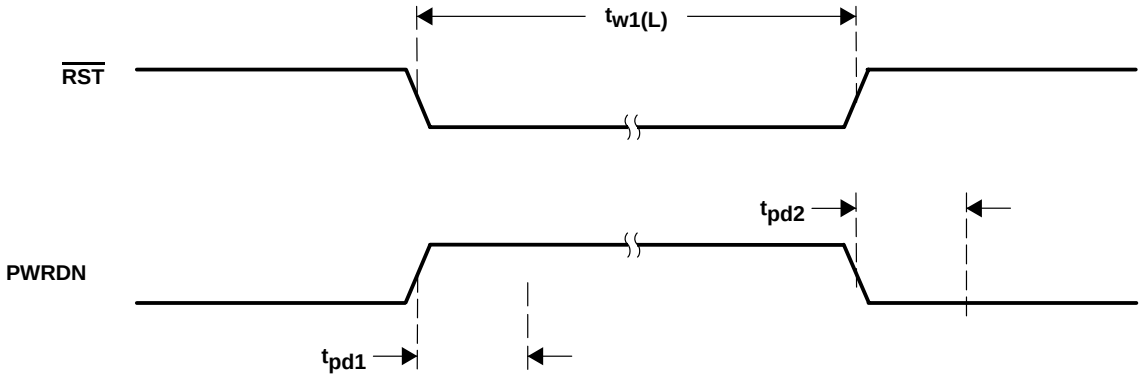


Figure 4–2. Control Signals Timing Waveforms

4.4.3 Serial Audio Port Slave Mode Over Recommended Operating Conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNITS
f_{LRCLK}	Frequency, LRCLK (F_S)			8		96	kHz
	Pulse duration, LRCLK high		See Note 6	H_{LRCLK} – TDB	H_{LRCLK}	H_{LRCLK} + TDB	ns
f_{SCLKIN}	Frequency, SCLKIN		See Note 2	$(32)F_S$		25	MHz
t_{cyc}	Cycle time, SCLKIN		See Note 2	40		$1/(32)F_S$	ns
t_{pd1}	Propagation delay, SCLKIN falling edge to SDOUT		C_L = 30 pF			10	ns
t_{su1}	Setup time, LRCLK to SCLKIN rising edge			5			ns
t_{h1}	Hold time, LRCLK from SCLKIN rising edge			5			ns
t_{su2}	Setup time, SDIN to SCLKIN rising edge			5			ns
t_{h2}	Hold time, SDIN from SCLKIN rising edge			5			ns
t_{pd2}	Propagation delay, SCLKIN falling edge to SCLKOUT2 falling edge	SCLKOUT2 = SCLKIN	C_L = 30 pF	TBD			ns
		SCLKOUT2 < SCLKIN	C_L = 30 pF	TBD			ns

NOTES: 2. Typical duty cycle is 50/50.
6. $H_{LRCLK} = 1/2f_{LRCLK}$

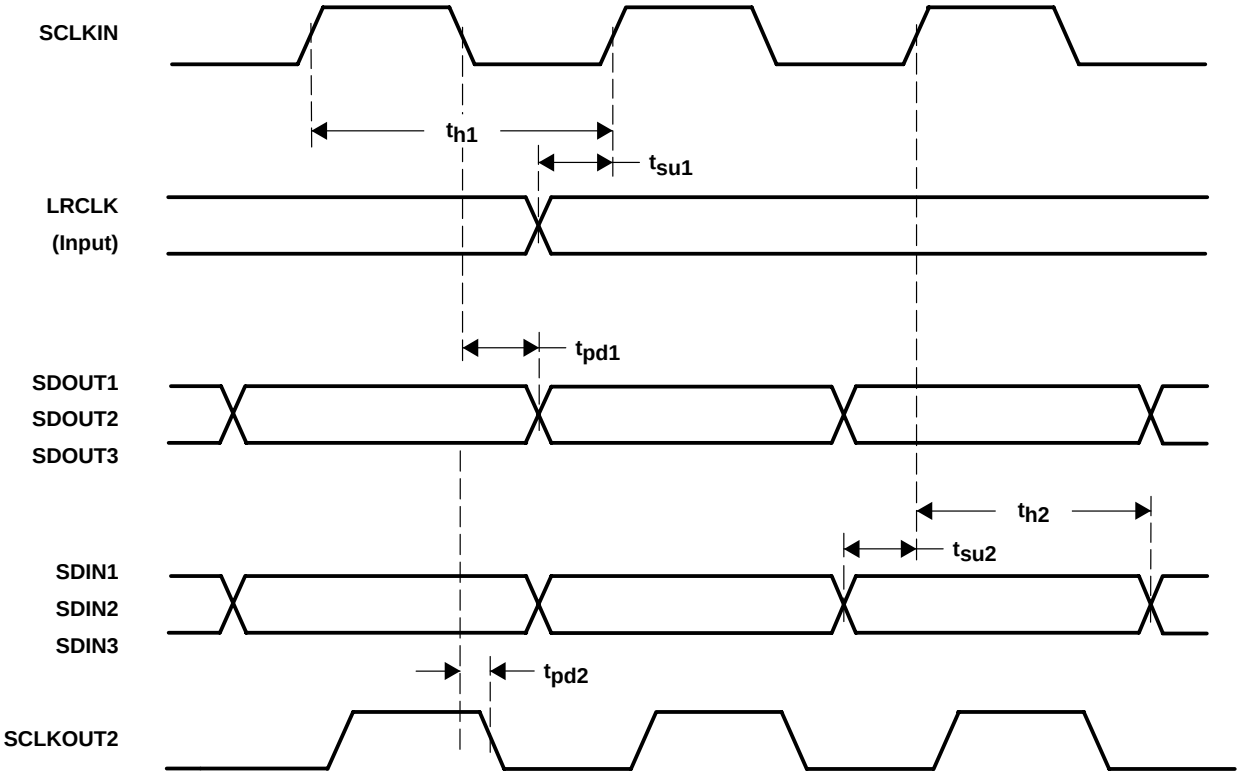


Figure 4–3. Serial Audio Port Slave Mode Timing Waveforms

4.4.4 Serial Audio Port Master Mode Over Recommended Operating Conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$f_{(LRCLK)}$	Frequency LRCLK		8		96	kHz
$t_{r(LRCLK)}$	Rise time, LRCLK	C_L = 30 pF			TBD	ns
$t_{f(LRCLK)}$	Fall time, LRCLK	C_L = 30 pF			TBD	ns
$f_{(SCLKOUT)}$	Frequency ($1/t_{cyc}$), SCLKOUT1/SCLKOUT2	C_L = 50 pF, See Note 2	(32)F_S		25	MHz
$t_{r(SCLKOUT)}$	Rise time, SCLKOUT1/SCLKOUT2	C_L = 30 pF			TDB	ns
$t_{f(SCLKOUT)}$	Fall time, SCLKOUT1/SCLKOUT2	C_L = 30 pF			TDB	ns
$t_{pd1(SCLKOUT1)}$	Propagation delay, SCLKOUT1 falling edge to LRCLK edge				10	ns
$t_{pd1(SCLKOUT2)}$	Propagation delay, SCLKOUT2 falling edge to LRCLK edge				10	ns
t_{pd2}	Propagation delay, SCLKOUT2 falling edge to SDOUT	C_L = 30 pF			10	ns
t_{su}	Setup time, SDIN to SCLKOUT1 rising edge		5			ns
t_h	Hold time, SDIN from SCLKOUT1 rising edge		5			ns
t_{sk}	Skew time, SCLKOUT1 to SCLKOUT2	C_L = 30 pF	TBD		TBD	ns

NOTE 2: Typical duty cycle is 50/50.

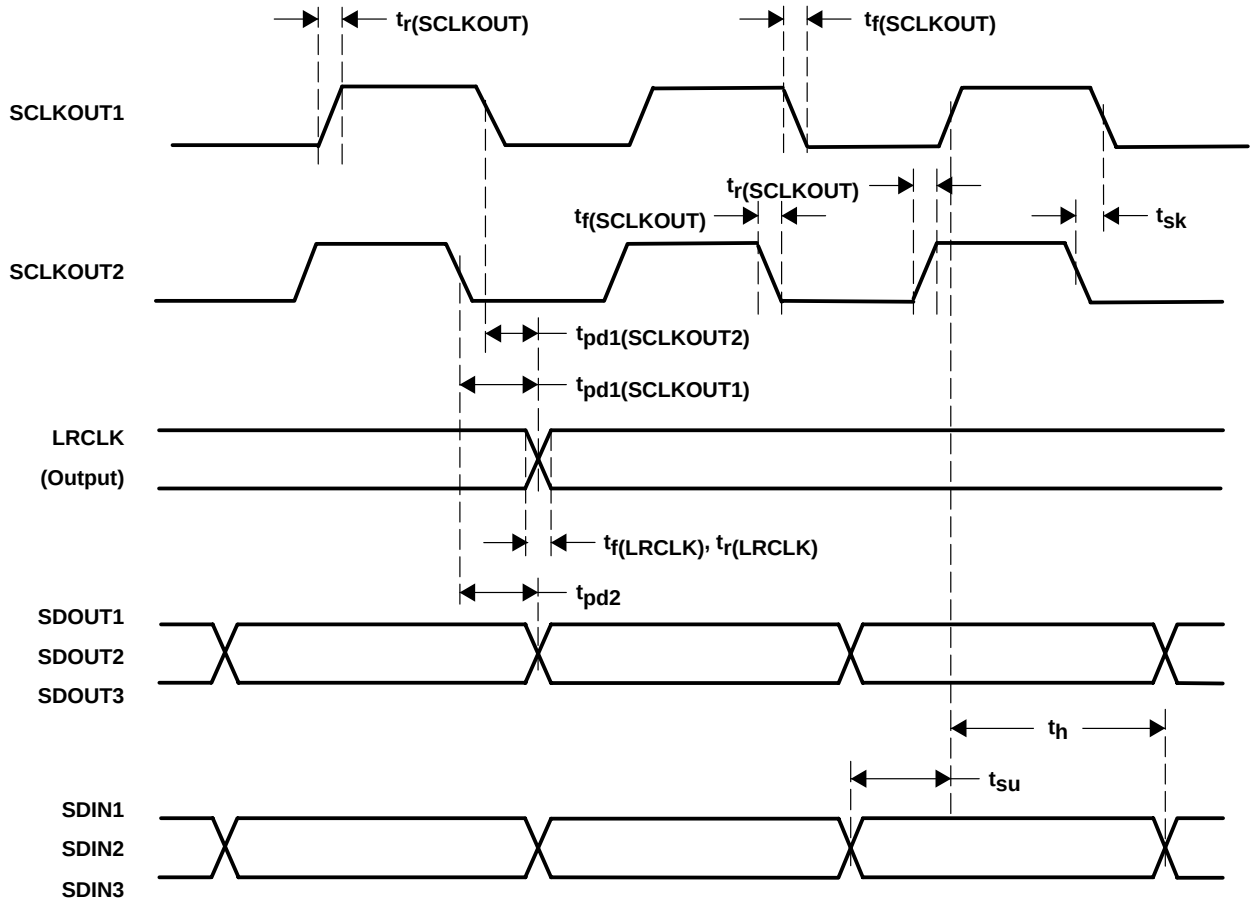


Figure 4–4. TAS3100 Serial Audio Port Master Mode Timing Waveforms

4.4.5 I²C Interface Signals Over Recommended Operating Conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	STANDARD MODE		FAST MODE		UNITS
			MIN	MAX	MIN	MAX	
f_{SCL}	Frequency, SCL		0	100	0	400	kHz
$t_{w(H)}$	Pulse duration, SCL high		4		0.6		µs
$t_{w(L)}$	Pulse duration, SCL low		4.7		1.3		µs
t_r	Rise time, SCL and SDA			1000		300	ns
t_f	Fall time, SCL and SDA			300		300	ns
t_{su1}	Setup time, SDA to SCL		250		100	-	ns
t_{h1}	Hold time, SCL to SDA output	See Note 7	0	TDB	0	TDB	ns
$t_{(buf)}$	Bus free time between stop and start condition		4.7		1.3		µs
t_{su2}	Setup time, SCL to start condition		4.7		0.6		µs
t_{h2}	Hold time, start condition to SCL		4		0.6		µs
t_{su3}	Setup time, SCL to stop condition		4		0.6		µs
C_L	Load capacitance for each bus line			400		400	pF

NOTE 7: When SDA is an input, a 10X or greater internal sampling of SDA (as set by proper selection of N in sub-address 0xFE) can accommodate a skew between SDA and the falling edge of SCL of up to 300 ns.

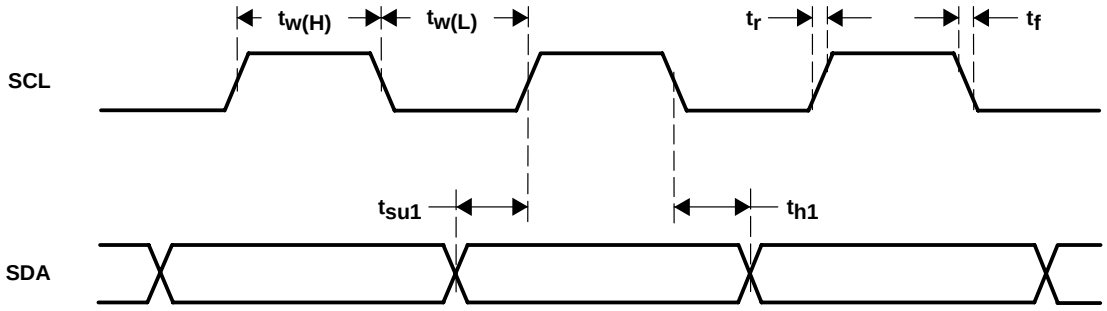


Figure 4–5. I²C SCL and SDA Timing Waveforms

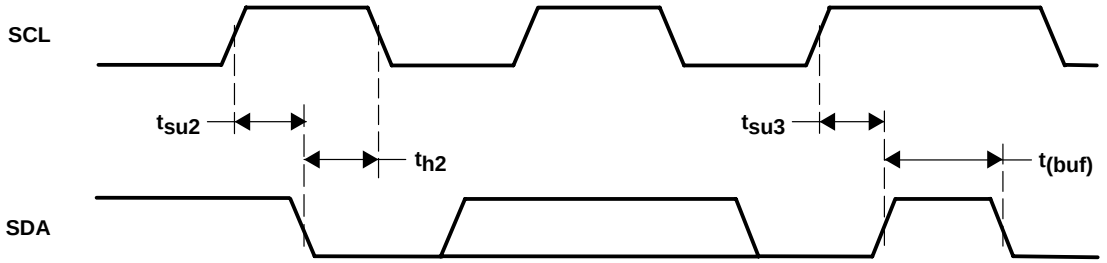


Figure 4–6. I²C Start and Stop Conditions Timing Waveforms

Appendix A

A.1 I2C Subaddress Table

SUBADDRESS (0xSS)	REGISTER NAME	NUMBER OF 4-BYTE WORDS	CONTENTS (u Indicates Unused Bits)	INITIALIZATION VALUE
0x00	Starting I2C check word	1	SCW(31:24), SCW(23:16), SCW(15:8), SCW(7:0)	0x81, 0x42, 0x24, 0x18
0x01	Mix A to a	1	u(31:28)A_a(27:24), A_a(23:16), A_a(15:8), A_a(7:0)	0x00, 0x80, 0x00, 0x00
0x02	Mix A to b	1	u(31:28)A_b(27:24), A_b(23:16), A_b(15:8), A_b(7:0)	0x00, 0x00, 0x00, 0x00
0x03	Mix A to c	1	u(31:28)A_c(27:24), A_c(23:16), A_c(15:8), A_c(7:0)	0x00, 0x00, 0x00, 0x00
0x04	Mix A to d	1	u(31:28)A_d(27:24), A_d(23:16), A_d(15:8), A_d(7:0)	0x00, 0x00, 0x00, 0x00
0x05	Mix A to e	1	u(31:28)A_e(27:24), A_e(23:16), A_e(15:8), A_e(7:0)	0x00, 0x00, 0x00, 0x00
0x06	Mix A to f	1	u(31:28)A_f(27:24), A_f(23:16), A_f(15:8), A_f(7:0)	0x00, 0x00, 0x00, 0x00
0x07	Mix B to a	1	u(31:28)B_a(27:24), B_a(23:16), B_a(15:8), B_a(7:0)	0x00, 0x00, 0x00, 0x00
0x08	Mix B to b	1	u(31:28)B_b(27:24), B_b(23:16), B_b(15:8), B_b(7:0)	0x00, 0x80, 0x00, 0x00
0x09	Mix B to c	1	u(31:28)B_c(27:24), B_c(23:16), B_c(15:8), B_c(7:0)	0x00, 0x00, 0x00, 0x00
0x0A	Mix B to d	1	u(31:28)B_d(27:24), B_d(23:16), B_d(15:8), B_d(7:0)	0x00, 0x00, 0x00, 0x00
0x0B	Mix B to e	1	u(31:28)B_e(27:24), B_e(23:16), B_e(15:8), B_e(7:0)	0x00, 0x00, 0x00, 0x00
0x0C	Mix B to f	1	u(31:28)B_f(27:24), B_f(23:16), B_f(15:8), B_f(7:0)	0x00, 0x00, 0x00, 0x00
0x0D	Mix C to a	1	u(31:28)C_a(27:24), C_a(23:16), C_a(15:8), C_a(7:0)	0x00, 0x00, 0x00, 0x00
0x0E	Mix C to b	1	u(31:28)C_b(27:24), C_b(23:16), C_b(15:8), C_b(7:0)	0x00, 0x00, 0x00, 0x00
0x0F	Mix C to c	1	u(31:28)C_c(27:24), C_c(23:16), C_c(15:8), C_c(7:0)	0x00, 0x00, 0x00, 0x00
0x10	Mix C to d	1	u(31:28)C_d(27:24), C_d(23:16), C_d(15:8), C_d(7:0)	0x00, 0x00, 0x00, 0x00
0x11	Mix C to e	1	u(31:28)C_e(27:24), C_e(23:16), C_e(15:8), C_e(7:0)	0x00, 0x00, 0x00, 0x00
0x12	Mix C to f	1	u(31:28)C_f(27:24), C_f(23:16), C_f(15:8), C_f(7:0)	0x00, 0x40, 0x00, 0x00
0x13	Mix D to a	1	u(31:28)D_a(27:24), D_a(23:16), D_a(15:8), D_a(7:0)	0x00, 0x00, 0x00, 0x00
0x14	Mix D to b	1	u(31:28)D_b(27:24), D_b(23:16), D_b(15:8), D_b(7:0)	0x00, 0x00, 0x00, 0x00
0x15	Mix D to c	1	u(31:28)D_c(27:24), D_c(23:16), D_c(15:8), D_c(7:0)	0x00, 0x00, 0x00, 0x00
0x16	Mix D to d	1	u(31:28)D_d(27:24), D_d(23:16), D_d(15:8), D_d(7:0)	0x00, 0x00, 0x00, 0x00
0x17	Mix D to e	1	u(31:28)D_e(27:24), D_e(23:16), D_e(15:8), D_e(7:0)	0x00, 0x00, 0x00, 0x00
0x18	Mix D to f	1	u(31:28)D_f(27:24), D_f(23:16), D_f(15:8), D_f(7:0)	0x00, 0x40, 0x00, 0x00
0x19	Mix E to a	1	u(31:28)E_a(27:24), E_a(23:16), E_a(15:8), E_a(7:0)	0x00, 0x00, 0x00, 0x00
0x1A	Mix E to b	1	u(31:28)E_b(27:24), E_b(23:16), E_b(15:8), E_b(7:0)	0x00, 0x00, 0x00, 0x00
0x1B	Mix E to c	1	u(31:28)E_c(27:24), E_c(23:16), E_c(15:8), E_c(7:0)	0x00, 0x00, 0x00, 0x00
0x1C	Mix E to d	1	u(31:28)E_d(27:24), E_d(23:16), E_d(15:8), E_d(7:0)	0x00, 0x00, 0x00, 0x00
0x1D	Mix E to e	1	u(31:28)E_e(27:24), E_e(23:16), E_e(15:8), E_e(7:0)	0x00, 0x00, 0x00, 0x00
0x1E	Mix E to f	1	u(31:28)E_f(27:24), E_f(23:16), E_f(15:8), E_f(7:0)	0x00, 0x00, 0x00, 0x00
0x1F	Mix F to a	1	u(31:28)F_a(27:24), F_a(23:16), F_a(15:8), F_a(7:0)	0x00, 0x00, 0x00, 0x00

SUBADDRESS (0xSS)	REGISTER NAME	NUMBER OF 4-BYTE WORDS	CONTENTS (u Indicates Unused Bits)	INITIALIZATION VALUE
0x20	Mix F to b	1	u(31:28)F_b(27:24), F_b(23:16), F_b(15:8), F_b(7:0)	0x00, 0x00, 0x00, 0x00
0x21	Mix F to c	1	u(31:28)F_c(27:24), F_c(23:16), F_c(15:8), F_c(7:0)	0x00, 0x00, 0x00, 0x00
0x22	Mix F to d	1	u(31:28)F_d(27:24), F_d(23:16), F_d(15:8), F_d(7:0)	0x00, 0x00, 0x00, 0x00
0x23	Mix F to e	1	u(31:28)F_e(27:24), F_e(23:16), F_e(15:8), F_e(7:0)	0x00, 0x00, 0x00, 0x00
0x24	Mix F to f	1	u(31:28)F_f(27:24), F_f(23:16), F_f(15:8), F_f(7:0)	0x00, 0x00, 0x00, 0x00
0x25	Mix a to c	1	u(31:28)a_c(27:24), a_c(23:16), a_c(15:8), a_c(7:0)	0x00, 0x00, 0x00, 0x00
0x26	Mix b to c	1	u(31:28)b_c(27:24), b_c(23:16), b_c(15:8), b_c(7:0)	0x00, 0x00, 0x00, 0x00
0x27	Mix a to g	1	u(31:28)a_g(27:24), a_g(23:16), a_g(15:8), a_g(7:0)	0x00, 0x00, 0x00, 0x00
0x28	Mix b to h	1	u(31:28)b_h(27:24), b_h(23:16), b_h(15:8), b_h(7:0)	0x00, 0x00, 0x00, 0x00
0x29	Mix a to d via BQ and Rev/D	1	u(31:28)a_d(27:24), a_d(23:16), a_d(15:8), a_d(7:0)	0x00, 0x80, 0x00, 0x00
0x2A	Mix a to e via BQ and Rev/D	1	u(31:28)a_e(27:24), a_e(23:16), a_e(15:8), a_e(7:0)	0x00, 0x00, 0x00, 0x00
0x2B	Mix b to d via BQ and Rev/D	1	u(31:28)b_d(27:24), b_d(23:16), b_d(15:8), b_d(7:0)	0x00, 0x00, 0x00, 0x00
0x2C	Mix b to e via BQ and Rev/D	1	u(31:28)b_e(27:24), b_e(23:16), b_e(15:8), b_e(7:0)	0x00, 0x80, 0x00, 0x00
0x2D	Mix g to d via BQ	1	u(31:28)g_d(27:24), g_d(23:16), g_d(15:8), g_d(7:0)	0x00, 0x00, 0x00, 0x00
0x2E	Mix g to e via BQ	1	u(31:28)g_e(27:24), g_e(23:16), g_e(15:8), g_e(7:0)	0x00, 0x00, 0x00, 0x00
0x2F	Mix h to d via BQ	1	u(31:28)h_d(27:24), h_d(23:16), h_d(15:8), h_d(7:0)	0x00, 0x00, 0x00, 0x00
0x30	Mix h to e via BQ	1	u(31:28)h_e(27:24), h_e(23:16), h_e(15:8), h_e(7:0)	0x00, 0x00, 0x00, 0x00
0x31	Mix c to d via BQ	1	u(31:28)c_d(27:24), c_d(23:16), c_d(15:8), c_d(7:0)	0x00, 0x00, 0x00, 0x00
0x32	Mix c to e via BQ	1	u(31:28)c_e(27:24), c_e(23:16), c_e(15:8), c_e(7:0)	0x00, 0x00, 0x00, 0x00
0x33	Mix f to g and h	1	u(31:28)f_gh(27:24), f_gh(23:16), f_gh(15:8), f_gh(7:0)	0x00, 0x00, 0x00, 0x00
0x34	a_de path, biquad 1	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x35	a_de path, biquad 2	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x36	a_de path, biquad 3	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00

SUBADDRESS (0xSS)	REGISTER NAME	NUMBER OF 4-BYTE WORDS	CONTENTS (u Indicates Unused Bits)	INITIALIZATION VALUE
0x37	a_de path, biquad 4	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x38	b_de path, biquad 1	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x39	b_de path, biquad 2	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x3A	b_de path, biquad 3	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x3B	b_de path, biquad 4	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x3C	g_de path, biquad 1	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x3D	g_de path, biquad 2	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00

SUBADDRESS (0xSS)	REGISTER NAME	NUMBER OF 4-BYTE WORDS	CONTENTS (u Indicates Unused Bits)	INITIALIZATION VALUE
0x3E	g_de path, biquad 3	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x3F	g_de path, biquad 4	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x40	h_de path, biquad 1	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x41	h_de path, biquad 2	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x42	h_de path, biquad 3	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x43	h_de path, biquad 4	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x44	c_de path, biquad 1	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00

SUBADDRESS (0xSS)	REGISTER NAME	NUMBER OF 4-BYTE WORDS	CONTENTS (u Indicates Unused Bits)	INITIALIZATION VALUE
0x45	c_de path, biquad 2	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x46	c_de path, biquad 3	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x47	c_de path, biquad 4	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x48	f_CH3 path, biquad 1	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x49	f_CH3 path, biquad 2	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x4A	f_CH3 path, biquad 3	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x4B	f_CH3 path, biquad 4	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00

SUBADDRESS (0xSS)	REGISTER NAME	NUMBER OF 4-BYTE WORDS	CONTENTS (u Indicates Unused Bits)	INITIALIZATION VALUE
0x4C	a_de path, Reverb Gain Rg0	2	u(31:28)Rg0(27:24), Rg0(23:16), Rg0(15:8), Rg0(7:0)	0x00, 0x80, 0x00, 0x00
	a_de path, Reverb Gain Rg1		u(31:28)Rg1(27:24), Rg1(23:16), Rg1(15:8), Rg1(7:0)	0x00, 0x00, 0x00, 0x00
0x4D	b_de path, Reverb Gain Rg0	2	u(31:28)Rg0(27:24), Rg0(23:16), Rg0(15:8), Rg0(7:0)	0x00, 0x80, 0x00, 0x00
	b_de path, Reverb Gain Rg1		u(31:28)Rg1(27:24), Rg1(23:16), Rg1(15:8), Rg1(7:0)	0x00, 0x00, 0x00, 0x00
0x4E	f_CH3 path, Reverb Gain Rg0	2	u(31:28)Rg0(27:24), Rg0(23:16), Rg0(15:8), Rg0(7:0)	0x00, 0x80, 0x00, 0x00
	f_CH3 path, Reverb Gain Rg1		u(31:28)Rg1(27:24), Rg1(23:16), Rg1(15:8), Rg1(7:0)	0x00, 0x00, 0x00, 0x00
0x4F	CH1 biquad 1	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x50	CH1 biquad 2	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x51	CH1 biquad 3	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x52	CH1 biquad 4	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x53	CH1 biquad 5	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x54	CH1 biquad 6	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00

SUBADDRESS (0xSS)	REGISTER NAME	NUMBER OF 4-BYTE WORDS	CONTENTS (u Indicates Unused Bits)	INITIALIZATION VALUE
0x55	CH1 biquad 7	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x56	CH1 biquad 8	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x57	CH1 biquad 9	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x58	CH1 biquad 10	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x59	CH1 biquad 11	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x5A	CH1 biquad 12	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x5B	CH2 biquad 1	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00

SUBADDRESS (0xSS)	REGISTER NAME	NUMBER OF 4-BYTE WORDS	CONTENTS (u Indicates Unused Bits)	INITIALIZATION VALUE
0x5C	CH2 biquad 2	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x5D	CH2 biquad 3	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x5E	CH2 biquad 4	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x5F	CH2 biquad 5	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x60	CH2 biquad 6	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x61	CH2 biquad 7	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x62	CH2 biquad 8	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00

SUBADDRESS (0xSS)	REGISTER NAME	NUMBER OF 4-BYTE WORDS	CONTENTS (u Indicates Unused Bits)	INITIALIZATION VALUE
0x63	CH2 biquad 9	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x64	CH2 biquad 10	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x65	CH2 biquad 11	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x66	CH2 biquad 12	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x67	CH3 biquad 1	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x68	CH3 biquad 2	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x69	CH3 biquad 3	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00

SUBADDRESS (0xSS)	REGISTER NAME	NUMBER OF 4-BYTE WORDS	CONTENTS (u Indicates Unused Bits)	INITIALIZATION VALUE
0x6A	CH3 biquad 4	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x6B	CH3 biquad 5	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x6C	CH3 biquad 6	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x6D	CH3 biquad 7	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x6E	CH3 biquad 8	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x6F	CH3 biquad 9	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x70	CH3 biquad 10	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00

SUBADDRESS (0xSS)	REGISTER NAME	NUMBER OF 4-BYTE WORDS	CONTENTS (u Indicates Unused Bits)	INITIALIZATION VALUE
0x71	CH3 biquad 11	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x72	CH3 biquad 12	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0x73	Bass and treble bypass 1	2	u(31:28)BTby1(27:24), BTby1(23:16), BTby1(15:8), BTby1(7:0)	0x00, 0x80, 0x00, 0x00
	Bass and treble inline 1		u(31:28)BT1(27:24), BT1(23:16), BT1(15:8), BT1(7:0)	0x00, 0x00, 0x00, 0x00
0x74	Bass and treble bypass 2	2	u(31:28)BTby2(27:24), BTby2(23:16), BTby2(15:8), BTby2(7:0)	0x00, 0x80, 0x00, 0x00
	Bass and treble inline 2		u(31:28)BT2(27:24), BT2(23:16), BT2(15:8), BT2(7:0)	0x00, 0x00, 0x00, 0x00
0x75	Bass and treble bypass 3	2	u(31:28)BTby3(27:24), BTby3(23:16), BTby3(15:8), BTby3(7:0)	0x00, 0x80, 0x00, 0x00
	Bass and treble inline 3		u(31:28)BT3(27:24), BT3(23:16), BT3(15:8), BT3(7:0)	0x00, 0x00, 0x00, 0x00
0x76	Mix u to i	1	u(31:28)u_i(27:24), u_i(23:16), u_i(15:8), u_i(7:0)	0x00, 0x00, 0x00, 0x00
0x77	Mix v to k	1	u(31:28)v_k(27:24), v_k(23:16), v_k(15:8), v_k(7:0)	0x00, 0x00, 0x00, 0x00
0x78	Mix w to m	1	u(31:28)w_m(27:24), w_m(23:16), w_m(15:8), w_m(7:0)	0x00, 0x00, 0x00, 0x00
0x79	Mix j to i	1	u(31:28)j_i(27:24), j_i(23:16), j_i(15:8), j_i(7:0)	0x00, 0x00, 0x00, 0x00
0x7A	Mix l to k	1	u(31:28)l_k(27:24), l_k(23:16), l_k(15:8), l_k(7:0)	0x00, 0x00, 0x00, 0x00
0x7B	Mix n to m	1	u(31:28)n_m(27:24), n_m(23:16), n_m(15:8), n_m(7:0)	0x00, 0x00, 0x00, 0x00
0x7C	Mix j to o via DRC mult	2	u(31:28)j_o(27:24), j_o(23:16), j_o(15:8), j_o(7:0)	0x00, 0x00, 0x00, 0x00
	DRC bypass 1		u(31:28)DRC_{by1}(27:24), DRC_{by1}(23:16), DRC_{by1}(15:8), DRC_{by1}(7:0)	0x00, 0x80, 0x00, 0x00
0x7D	Mix l to p via DRC mult	2	u(31:28)l_p(27:24), l_p(23:16), l_p(15:8), l_p(7:0)	0x00, 0x00, 0x00, 0x00
	DRC bypass 2		u(31:28)DRC_{by2}(27:24), DRC_{by2}(23:16), DRC_{by2}(15:8), DRC_{by2}(7:0)	0x00, 0x80, 0x00, 0x00
0x7E	Mix n to q via DRC mult	2	u(31:28)n_q(27:24), n_q(23:16), n_q(15:8), n_q(7:0)	0x00, 0x00, 0x00, 0x00
	DRC bypass 3		u(31:28)DRC_{by3}(27:24), DRC_{by3}(23:16), DRC_{by3}(15:8), DRC_{by3}(7:0)	0x00, 0x80, 0x00, 0x00
0x7F	Mix dither1 to o	1	u(31:28)Dth1_o(27:24), Dth1_o(23:16), Dth1_o(15:8), Dth1_o(7:0)	0x00, 0x00, 0x00, 0x00
0x80	Mix dither2 to p	1	u(31:28)Dth2_p(27:24), Dth2_p(23:16), Dth2_p(15:8), Dth2_p(7:0)	0x00, 0x00, 0x00, 0x00
0x81	Mix dither3 to q	1	u(31:28)Dth3_q(27:24), Dth3_q(23:16), Dth3_q(15:8), Dth3_q(7:0)	0x00, 0x00, 0x00, 0x00
0x82	Mix delay3 to o	1	u(31:28)Dth3_o(27:24), Dth3_o(23:16), Dth3_o(15:8), Dth3_o(7:0)	0x00, 0x00, 0x00, 0x00
0x83	Mix delay3 to p	1	u(31:28)Dth3_p(27:24), Dth3_p(23:16), Dth3_p(15:8), Dth3_p(7:0)	0x00, 0x00, 0x00, 0x00
0x84	Mix o to r	1	u(31:28)o_r(27:24), o_r(23:16), o_r(15:8), o_r(7:0)	0x00, 0x40, 0x00, 0x00
0x85	Mix o to s	1	u(31:28)o_s(27:24), o_s(23:16), o_s(15:8), o_s(7:0)	0x00, 0x00, 0x00, 0x00
0x86	Mix p to r	1	u(31:28)p_r(27:24), p_r(23:16), p_r(15:8), p_r(7:0)	0x00, 0x40, 0x00, 0x00

SUBADDRESS (0xSS)	REGISTER NAME	NUMBER OF 4-BYTE WORDS	CONTENTS (u Indicates Unused Bits)	INITIALIZATION VALUE
0x87	Mix p to t	1	u(31:28)p_t(27:24), p_t(23:16), p_t(15:8), p_t(7:0)	0x00, 0x00, 0x00, 0x00
0x88	Mix q to r	1	u(31:28)q_r(27:24), q_r(23:16), q_r(15:8), q_r(7:0)	0x00, 0x00, 0x00, 0x00
0x89	Mix r to s and t	1	u(31:28)r_st(27:24), r_st(23:16), r_st(15:8), r_st(7:0)	0x00, 0x80, 0x00, 0x00
0x8A	Mix z to Z	1	u(31:28)z_Z(27:24), z_Z(23:16), z_Z(15:8), z_Z(7:0)	0x00, 0x00, 0x00, 0x00
0x8B	Mix z to Y	1	u(31:28)z_Y(27:24), z_Y(23:16), z_Y(15:8), z_Y(7:0)	0x00, 0x00, 0x00, 0x00
0x8C	Mix z to X	1	u(31:28)z_X(27:24), z_X(23:16), z_X(15:8), z_X(7:0)	0x00, 0x00, 0x00, 0x00
0x8D	Mix z to W	1	u(31:28)z_W(27:24), z_W(23:16), z_W(15:8), z_W(7:0)	0x00, 0x00, 0x00, 0x00
0x8E	Mix z to V	1	u(31:28)z_V(27:24), z_V(23:16), z_V(15:8), z_V(7:0)	0x00, 0x00, 0x00, 0x00
0x8F	Mix z to U	1	u(31:28)z_U(27:24), z_U(23:16), z_U(15:8), z_U(7:0)	0x00, 0x80, 0x00, 0x00
0x90	Mix y to Z	1	u(31:28)y_Z(27:24), y_Z(23:16), y_Z(15:8), y_Z(7:0)	0x00, 0x00, 0x00, 0x00
0x91	Mix y to Y	1	u(31:28)y_Y(27:24), y_Y(23:16), y_Y(15:8), y_Y(7:0)	0x00, 0x00, 0x00, 0x00
0x92	Mix y to X	1	u(31:28)y_X(27:24), y_X(23:16), y_X(15:8), y_X(7:0)	0x00, 0x00, 0x00, 0x00
0x93	Mix y to W	1	u(31:28)y_W(27:24),y_W(23:16), y_W(15:8), y_W(7:0)	0x00, 0x00, 0x00, 0x00
0x94	Mix y to V	1	u(31:28)y_V(27:24), y_V(23:16), y_V(15:8), y_V(7:0)	0x00, 0x80, 0x00, 0x00
0x95	Mix y to U	1	u(31:28)y_U(27:24), y_U(23:16), y_U(15:8), y_U(7:0)	0x00, 0x00, 0x00, 0x00
0x96	Mix x to Z	1	u(31:28)x_Z(27:24), x_Z(23:16), x_Z(15:8), x_Z(7:0)	0x00, 0x00, 0x00, 0x00
0x97	Mix x to Y	1	u(31:28)x_Y(27:24), x_Y(23:16), x_Y(15:8), x_Y(7:0)	0x00, 0x00, 0x00, 0x00
0x98	Mix x to X	1	u(31:28)x_X(27:24), x_X(23:16), x_X(15:8), x_X(7:0)	0x00, 0x00, 0x00, 0x00
0x99	Mix x to W	1	u(31:28)x_W(27:24), x_W(23:16), x_W(15:8), x_W(7:0)	0x00, 0x80, 0x00, 0x00
0x9A	Mix x to V	1	u(31:28)x_V(27:24), x_V(23:16), x_V(15:8), x_V(7:0)	0x00, 0x00, 0x00, 0x00
0x9B	Mix x to U	1	u(31:28)x_U(27:24), x_U(23:16), x_U(15:8), x_U(7:0)	0x00, 0x00, 0x00, 0x00
0x9C	Mix r to Z	1	u(31:28)r_Z(27:24), r_Z(23:16), r_Z(15:8), r_Z(7:0)	0x00, 0x00, 0x00, 0x00
0x9D	Mix r to Y	1	u(31:28)r_Y(27:24), r_Y(23:16), r_Y(15:8), r_Y(7:0)	0x00, 0x00, 0x00, 0x00
0x9E	Mix r to X	1	u(31:28)r_X(27:24), r_X(23:16), r_X(15:8), r_X(7:0)	0x00, 0x80, 0x00, 0x00
0x9F	Mix r to W	1	u(31:28)r_W(27:24), r_W(23:16), r_W(15:8), r_W(7:0)	0x00, 0x00, 0x00, 0x00
0xA0	Mix r to V	1	u(31:28)r_V(27:24), r_V(23:16), r_V(15:8), r_V(7:0)	0x00, 0x00, 0x00, 0x00
0xA1	Mix r to U	1	u(31:28)r_U(27:24), r_U(23:16), r_U(15:8), r_U(7:0)	0x00, 0x00, 0x00, 0x00
0xA2	CH1 Loudness Log_2 G	1	u(31:28)LG(27:24), LG(23:16), LG(15:8), LG(7:0)	0x00, 0x40, 0x00, 0x00
0xA3	CH1 Loudness Log_2 O	2	u(31:24), u(23:16), $LO_{47:40}$(15:8), $LO_{39:32}$(7:0)	0x00, 0x00, 0x00, 0x00
			$LO_{31:24}$(31:24), $LO_{23:16}$(23:16), $LO_{15:8}$(15:8), $LO_{7:0}$(7:0)	0x00, 0x00, 0x00, 0x00
0xA4	CH1 Loudness G	1	u(31:28)G(27:24), G(23:16), G(15:8), G(7:0)	0x00, 0x00, 0x00, 0x00
0xA5	CH1loudness O	2	u(31:24), u(23:16), $O_{47:40}$(15:8), $O_{39:32}$(7:0)	0x00, 0x00, 0x00, 0x00
			$O_{31:24}$(31:24), $O_{23:16}$(23:16), $O_{15:8}$(15:8), $O_{7:0}$(7:0)	0x00, 0x00, 0x00, 0x00

SUBADDRESS (0xSS)	REGISTER NAME	NUMBER OF 4-BYTE WORDS	CONTENTS (u Indicates Unused Bits)	INITIALIZATION VALUE
0xA6	CH1 loudness biquad	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0xA7	CH2 loudness $\log_2$ G	1	u(31:28)LG(27:24), LG(23:16), LG(15:8), LG(7:0)	0x00, 0x40, 0x00, 0x00
0xA8	CH2 loudness $\log_2$ O	2	u(31:24), u(23:16), $LO_{47:40}$(15:8), $LO_{39:32}$(7:0)	0x00, 0x00, 0x00, 0x00
			$LO_{31:24}$(31:24), $LO_{23:16}$(23:16), $LO_{15:8}$(15:8), $LO_{7:0}$(7:0)	0x00, 0x00, 0x00, 0x00
0xA9	CH2 loudness G	1	u(31:28)G(27:24), G(23:16), G(15:8), G(7:0)	0x00, 0x00, 0x00, 0x00
0xAA	CH2 loudness O	2	u(31:24), u(23:16), $O_{47:40}$(15:8), $O_{39:32}$(7:0)	0x00, 0x00, 0x00, 0x00
			$O_{31:24}$(31:24), $O_{23:16}$(23:16), $O_{15:8}$(15:8), $O_{7:0}$(7:0)	0x00, 0x00, 0x00, 0x00
0xAB	CH2 loudness biquad	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0xAC	CH3 loudness $\log_2$ G	1	u(31:28)LG(27:24), LG(23:16), LG(15:8), LG(7:0)	0x00, 0x40, 0x00, 0x00
0xAD	CH3 loudness $\log_2$ O	2	u(31:24), u(23:16), $LO_{47:40}$(15:8), $LO_{39:32}$(7:0)	0x00, 0x00, 0x00, 0x00
			$LO_{31:24}$(31:24), $LO_{23:16}$(23:16), $LO_{15:8}$(15:8), $LO_{7:0}$(7:0)	0x00, 0x00, 0x00, 0x00
0xAE	CH3 loudness G	1	u(31:28)G(27:24), G(23:16), G(15:8), G(7:0)	0x00, 0x00, 0x00, 0x00
0xAF	CH3 loudness O	2	u(31:24), u(23:16), $O_{47:40}$(15:8), $O_{39:32}$(7:0)	0x00, 0x00, 0x00, 0x00
			$O_{31:24}$(31:24), $O_{23:16}$(23:16), $O_{15:8}$(15:8), $O_{7:0}$(7:0)	0x00, 0x00, 0x00, 0x00
0xB0	CH3 loudness biquad	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0xB1	CH1/2 DRCE ae	2	u(31:28)ae(27:24), ae(23:16), ae(15:8), ae(7:0)	0x00, 0x80, 0x00, 0x00
	CH1/2 DRCE 1-ae		u(31:28)1-ae(27:24), 1-ae(23:16), 1-ae(15:8), 1-ae(7:0)	0x00, 0x00, 0x00, 0x00
0xB2	CH1/2 DRCE T1	4	u(31:24), u(23:16), $T1_{47:40}$(15:8), $T1_{39:32}$(7:0)	0x00, 0x00, 0x00, 0x00
			$T1_{31:24}$(31:24), $T1_{23:16}$(23:16), $T1_{15:8}$(15:8), $T1_{7:0}$(7:0)	0x00, 0x00, 0x00, 0x01
	CH1/2 DRCE T2		u(31:24), u(23:16), $T2_{47:40}$(15:8), $T2_{39:32}$(7:0)	0x00, 0x00, 0x00, 0x00
			$T2_{31:24}$(31:24), $T2_{23:16}$(23:16), $T2_{15:8}$(15:8), $T2_{7:0}$(7:0)	0x00, 0x00, 0x00, 0x01
0xB3	CH1/2 k0’	3	u(31:28)k0’(27:24), k0’(23:16), k0’(15:8), k0’(7:0)	0x00, 0x00, 0x00, 0x00
	CH1/2 k1’		u(31:28)k1’(27:24), k1’(23:16), k1’(15:8), k1’(7:0)	0x00, 0x00, 0x00, 0x00
	CH1/2 k2’		u(31:28)k2’(27:24), k2’(23:16), k2’(15:8), k2’(7:0)	0x00, 0x00, 0x00, 0x00

SUBADDRESS (0xSS)	REGISTER NAME	NUMBER OF 4-BYTE WORDS	CONTENTS (u Indicates Unused Bits)	INITIALIZATION VALUE
0xB4	CH1/2 DRCE O1	4	u(31:24), u(23:16), $O1_{47:40}$(15:8), $O1_{39:32}$(7:0)	0x00, 0x00, 0x00, 0x00
			$O1_{31:24}$(31:24), $O1_{23:16}$(23:16), $O1_{15:8}$(15:8), $O1_{7:0}$(7:0)	0x01, 0xFF, 0xFF, 0xFF
	CH1/2 DRCE O2		u(31:24), u(23:16), $O2_{47:40}$(15:8), $O2_{39:32}$(7:0)	0x00, 0x00, 0x00, 0x00
			$O2_{31:24}$(31:24), $O2_{23:16}$(23:16), $O2_{15:8}$(15:8), $O2_{7:0}$(7:0)	0x01, 0xFF, 0xFF, 0xFF
0xB5	CH1/2 DRCE aa	4	u(31:28)aa(27:24), aa(23:16), aa(15:8), aa(7:0)	0x00, 0x80, 0x00, 0x00
	CH1/2 DRCE 1-aa		u(31:28)1-aa(27:24), 1-aa(23:16), 1-aa(15:8), 1-aa(7:0)	0x00, 0x00, 0x00, 0x00
	CH1/2 DRCE ad		u(31:28)ad(27:24), ad(23:16), ad(15:8), ad(7:0)	0x00, 0x80, 0x00, 0x00
	CH1/2 DRCE 1-ad		u(31:28)1-ad(27:24), 1-ad(23:16), 1-ad(15:8), 1-ad(7:0)	0x00, 0x00, 0x00, 0x00
0xB6	CH3 DRCE ae	2	u(31:28)ae(27:24), ae(23:16), ae(15:8), ae(7:0)	0x00, 0x80, 0x00, 0x00
	CH3 DRCE 1-ae		u(31:28)1-ae(27:24), 1-ae(23:16), 1-ae(15:8), 1-ae(7:0)	0x00, 0x00, 0x00, 0x00
0xB7	CH3 DRCE T1	4	u(31:24), u(23:16), $T1_{47:40}$(15:8), $T1_{39:32}$(7:0)	0x00, 0x00, 0x00, 0x00
			$T1_{31:24}$(31:24), $T1_{23:16}$(23:16), $T1_{15:8}$(15:8), $T1_{7:0}$(7:0)	0x00, 0x00, 0x00, 0x01
	CH3 DRCE T2		u(31:24), u(23:16), $T2_{47:40}$(15:8), $T2_{39:32}$(7:0)	0x00, 0x00, 0x00, 0x00
			$T2_{31:24}$(31:24), $T2_{23:16}$(23:16), $T2_{15:8}$(15:8), $T2_{7:0}$(7:0)	0x00, 0x00, 0x00, 0x01
0xB8	CH3 k0’	3	u(31:28)k0’(27:24), k0’(23:16), k0’(15:8), k0’(7:0)	0x00, 0x00, 0x00, 0x00
	CH3 k1’		u(31:28)k1’(27:24), k1’(23:16), k1’(15:8), k1’(7:0)	0x00, 0x00, 0x00, 0x00
	CH3 k2’		u(31:28)k2’(27:24), k2’(23:16), k2’(15:8), k2’(7:0)	0x00, 0x00, 0x00, 0x00
0xB9	CH3 DRCE O1	4	u(31:24), u(23:16), $O1_{47:40}$(15:8), $O1_{39:32}$(7:0)	0x00, 0x00, 0x00, 0x00
			$O1_{31:24}$(31:24), $O1_{23:16}$(23:16), $O1_{15:8}$(15:8), $O1_{7:0}$(7:0)	0x01, 0xFF, 0xFF, 0xFF
	CH3 DRCE O2		u(31:24), u(23:16), $O2_{47:40}$(15:8), $O2_{39:32}$(7:0)	0x00, 0x00, 0x00, 0x00
			$O2_{31:24}$(31:24), $O2_{23:16}$(23:16), $O2_{15:8}$(15:8), $O2_{7:0}$(7:0)	0x01, 0xFF, 0xFF, 0xFF
0xBA	CH3 DRCE aa	4	u(31:28)aa(27:24), aa(23:16), aa(15:8), aa(7:0)	0x00, 0x80, 0x00, 0x00
	CH3 DRCE 1-aa		u(31:28)1-aa(27:24), 1-aa(23:16), 1-aa(15:8), 1-aa(7:0)	0x00, 0x00, 0x00, 0x00
	CH3 DRCE ad		u(31:28)ad(27:24), ad(23:16), ad(15:8), ad(7:0)	0x00, 0x80, 0x00, 0x00
	CH3 DRCE 1-ad		u(31:28)1-ad(27:24), 1-ad(23:16), 1-ad(15:8), 1-ad(7:0)	0x00, 0x00, 0x00, 0x00
0xBB	Spectrum analyzer asa	2	u(31:28)asa(27:24), asa(23:16), asa(15:8), asa(7:0)	0x00, 0x80, 0x00, 0x00
	Spectrum analyzer 1-asa		u(31:28)1-asa(27:24), 1-asa(23:16), 1-asa(15:8), 1-asa(7:0)	0x00, 0x00, 0x00, 0x00
0xBC	Spectrum analyzer BQ1	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00

SUBADDRESS (0xSS)	REGISTER NAME	NUMBER OF 4-BYTE WORDS	CONTENTS (u Indicates Unused Bits)	INITIALIZATION VALUE
0xBD	Spectrum analyzer BQ2	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0xBE	Spectrum analyzer BQ3	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0xBF	Spectrum analyzer BQ4	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0xC0	Spectrum analyzer BQ5	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0xC1	Spectrum analyzer BQ6	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0xC2	Spectrum analyzer BQ7	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0xC3	Spectrum analyzer BQ8	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00

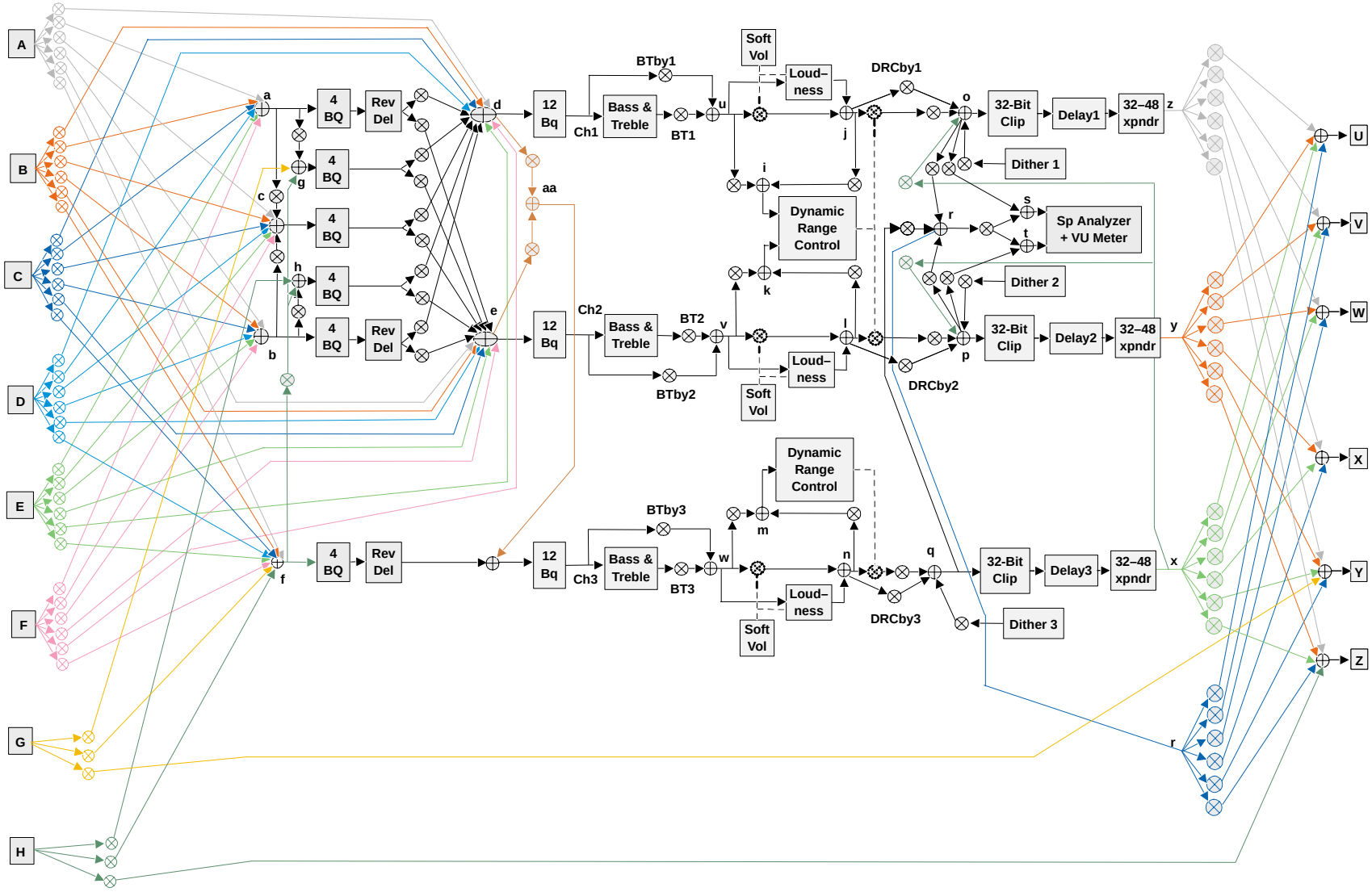
SUBADDRESS (0xSS)	REGISTER NAME	NUMBER OF 4-BYTE WORDS	CONTENTS (u Indicates Unused Bits)	INITIALIZATION VALUE
0xC4	Spectrum analyzer BQ9	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0xC5	Spectrum analyzer BQ10	5	u(31:28)a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b0(27:24), b0 (23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00, 0x00
			u(31:28)b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00, 0x00
			u(31:28)b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
0xC6	Dither LFSR1 mix	2	u(31:28)LFSR1(27:24), LFSR1(23:16), LFSR1(15:8), LFSR1(7:0)	0x00, 0x80, 0x00, 0x00
	Dither LFSR2 mix		u(31:28)LFSR2(27:24), LFSR2(23:16), LFSR2(15:8), LFSR2(7:0)	0x00, 0x80, 0x00, 0x00
0xC7	Dither seed	1	u(31:24), u(23:16), LFSR2_SEED(15:8), LFSR1_SEED(7:0)	0x00, 0x00, 0x22, 0x49
0xC8	Factory test	1	u(31:24), u(23:16), u(15:8), u(7:0)	N/A
0xC9	Factory test	2	u(31:24), u(23:16), u(15:8), u(7:0)	N/A
			u(31:24), u(23:16), u(15:8), u(7:0)	N/A
0xCA	Mix G to g	1	u(31:28)G_g(27:24), G_g(23:16), G_g(15:8), G_g(7:0)	0x00, 0x00, 0x00, 0x00
0xCB	Mix G to f	1	u(31:28)G_f(27:24), G_f(23:16), G_f(15:8), G_f(7:0)	0x00, 0x00, 0x00, 0x00
0xCC	Mix G to Y	1	u(31:28)G_Y(27:24), G_Y(23:16), G_Y(15:8), G_Y(7:0)	0x00, 0x00, 0x00, 0x00
0xCD	Mix H to h	1	u(31:28)H_h(27:24), H_h(23:16), H_h(15:8), H_h(7:0)	0x00, 0x00, 0x00, 0x00
0xCE	Mix H to f	1	u(31:28)H_f(27:24), H_f(23:16), H_f(15:8), H_f(7:0)	0x00, 0x00, 0x00, 0x00
0xCF	Mix H to Z	1	u(31:28)H_Z(27:24), H_Z(23:16), H_Z(15:8), H_Z(7:0)	0x00, 0x00, 0x00, 0x00
0xD0	Mix d to aa	1	u(31:28)d_aa(27:24), d_aa(23:16), d_aa(15:8), d_aa(7:0)	0x00, 0x00, 0x00, 0x00
0xD1	Mix e to aa	1	u(31:28)e_aa(27:24), e_aa(23:16), e_aa(15:8), e_aa(7:0)	0x00, 0x00, 0x00, 0x00
0xD2	Reserved	1	u(31:24), u(23:16), u(15:8), u(7:0)	N/A
0xD3	Reserved	1	u(31:24), u(23:16), u(15:8), u(7:0)	N/A
0xD4	Reserved	1	u(31:24), u(23:16), u(15:8), u(7:0)	N/A
0xD5	Reserved	1	u(31:24), u(23:16), u(15:8), u(7:0)	N/A
0xD6	Reserved	1	u(31:24), u(23:16), u(15:8), u(7:0)	N/A
0xD7	Reserved	1	u(31:24), u(23:16), u(15:8), u(7:0)	N/A
0xD8	Reserved	1	u(31:24), u(23:16), u(15:8), u(7:0)	N/A
0xD9	Reserved	1	u(31:24), u(23:16), u(15:8), u(7:0)	N/A
0xDA	Reserved	1	u(31:24), u(23:16), u(15:8), u(7:0)	N/A
0xDB	Reserved	1	u(31:24), u(23:16), u(15:8), u(7:0)	N/A
0xDC	Reserved	1	u(31:24), u(23:16), u(15:8), u(7:0)	N/A
0xDD	Reserved	1	u(31:24), u(23:16), u(15:8), u(7:0)	N/A

SUBADDRESS (0xSS)	REGISTER NAME	NUMBER OF 4-BYTE WORDS	CONTENTS (u Indicates Unused Bits)	INITIALIZATION VALUE
0xDE	Reserved	1	u(31:24), u(23:16), u(15:8), u(7:0)	N/A
0xDF	Reserved	1	u(31:24), u(23:16), u(15:8), u(7:0)	N/A
0xE0	Reserved	1	u(31:24), u(23:16), u(15:8), u(7:0)	N/A
0xE1	Reserved	1	u(31:24), u(23:16), u(15:8), u(7:0)	N/A
0xE2	Reserved	1	u(31:24), u(23:16), u(15:8), u(7:0)	N/A
0xE3	Reserved	1	u(31:24), u(23:16), u(15:8), u(7:0)	N/A
0xE4	Reserved	1	u(31:24), u(23:16), u(15:8), u(7:0)	N/A
0xE5	Reserved	1	u(31:24), u(23:16), u(15:8), u(7:0)	N/A
0xE6	Reserved	1	u(31:24), u(23:16), u(15:8), u(7:0)	N/A
0xE7	Reserved	1	u(31:24), u(23:16), u(15:8), u(7:0)	N/A
0xE8	Reserved	1	u(31:24), u(23:16), u(15:8), u(7:0)	N/A
0xE9	Reserved	1	u(31:24), u(23:16), u(15:8), u(7:0)	N/A
0xEA	Reserved	1	u(31:24), u(23:16), u(15:8), u(7:0)	N/A
0xEB	Watchdog timer enable	1	u(31:24), u(23:16), u(15:8), u(7:1)R1(0)	0x00, 0x00, 0x00, 0x01
0xEC	Factory test	1	u(31:24), u(23:16), u(15:8), u(7:0)	N/A
0xED	Factory test	2	u(31:24), u(23:16), u(15:8), u(7:0)	N/A
			u(31:24), u(23:16), u(15:8), u(7:0)	N/A
0xEE	GPIO port I/O value	1	u(31:24), u(23:16), u(15:8), u(7:4)GPIO_in_out(3:0)	0x00, 0x00, 0x00, 0x0X(1)
0xEF	GPIO parameters	1	u(31:24), u(23:20)GPIODIR(19:16), GPIOFSCOUNT(15:8), GPIO_samp_int(7:0)	0x00, 0x0F, 0x6E, 0x6D
0xF0	Master mute/unmute	1	(31:24), u(23:16), u(15:8), u(7:3)CH3M_U(2)CH2M_U(1)CH1M_U(0)	0x00, 0x00, 0x00, 0x00
0xF1	Vol, T and B slew rates	1	u(31:24), u(23:16), u(15:9)VSC(8), TBLC(7:0)	0x00, 0x00, 0x00, 0x40
0xF2	CH1 volume (5.23 precision)	1	u(31:28)Vol1(27:24), Vol1(23:16), Vol1(15:8), Vol1(7:0)	0x00, 0x00, 0x00, 0x00
0xF3	CH2 volume (5.23 precision)	1	u(31:28)Vol2(27:24), Vol2(23:16), Vol2(15:8), Vol2(7:0)	0x00, 0x00, 0x00, 0x00
0xF4	CH3 volume (5.23 precision)	1	u(31:28)Vol3(27:24), Vol3(23:16), Vol3(15:8), Vol3(7:0)	0x00, 0x00, 0x00, 0x00
0xF5	Bass filter set (1-5)	1	u(31:24), u(23:19)CH3Bs(18:16), u(15:11) CH2Bs(10:8), u(7:3)CH1Bs(2:0),	0x00, 0x03, 0x03, 0x03
0xF6	Bass filter index	1	u(31:24), CH3Bf(23:16), CH2Bf(15:8), CH1Bf(7:0)	0x00, 0x72, 0x72, 0x72
0xF7	Treble filter set (1-5)	1	u(31:24), u(23:19)CH3Ts(18:16), u(15:11) CH2Ts(10:8), u(7:3)CH1Ts(2:0),	0x00, 0x03, 0x03, 0x03
0xF8	Treble filter index	1	u(31:24), CH3Tf(23:16), CH2Tf(15:8), CH1Tf(7:0)	0x00, 0x72, 0x72, 0x72
0xF9	I^2S command word	1	MLRCLK(31:24), SCLK(23:16), DWFMT(15:8), IOM(7:0)	0x01, 0x01, 0x09, 0x11
0xFA	Delay/reverb times–CH1	3	u(31:28)D1(27:24), D1(23:16), u(15:12)R1(11:8), R1(7:0)	0x00, 0x00, 0x00, 0x00
	Delay/reverb times–CH2		u(31:28)D2(27:24), D2(23:16), u(15:12)R2(11:8), R2(7:0)	0x00, 0x00, 0x00, 0x00
	Delay/reverb times–CH3		u(31:28)D3(27:24), D3(23:16), u(15:12)R3(11:8), R3(7:0)	0x00, 0x00, 0x00, 0x00
0xFB	I^2C M and N	1	u(31:24), u(23:16), u(15:8), u(7)M(6:3)N(2:0)	0x00, 0x00, 0x00, 0x41
0xFC	Ending I^2C check word	1	ECW(31:24), ECW(23:16), ECW(15:8), ECW(7:0)	0x81, 0x42, 0x24, 0x18

SUBADDRESS (0xSS)	REGISTER NAME	NUMBER OF 4-BYTE WORDS	CONTENTS (u Indicates Unused Bits)	INITIALIZATION VALUE
0xFD	Spectrum analyzer output 1	2.5	SA1(7:0)	(Always data dependent)
	Spectrum analyzer output 2		SA2(7:0)	(Always data dependent)
	Spectrum analyzer output 3		SA3(7:0)	(Always data dependent)
	Spectrum analyzer output 4		SA4(7:0)	(Always data dependent)
	Spectrum analyzer output 5		SA5(7:0)	(Always data dependent)
	Spectrum analyzer output 6		SA6(7:0)	(Always data dependent)
	Spectrum analyzer output 7		SA7(7:0)	(Always data dependent)
	Spectrum analyzer output 8		SA8(7:0)	(Always data dependent)
	Spectrum analyzer output 9		SA9(7:0)	(Always data dependent)
	Spectrum analyzer output 10		SA10(7:0)	(Always data dependent)
0xFE	VU meter output 1 (SA5)	0.5	SA5(7:0)	(Always data dependent)
	VU meter output 2 (SA6)		SA6(7:0)	(Always data dependent)
0xFF	Flag register	0.25	u(7:1)VolBusy(0)	N/A

NOTE 1: GPIO ports are initialized to be read ports. The initial input values read then are dependent on what is connected to the GPIO pins. If a given GPIO pin is left unconnected, the internal pull-up results in a logic 1 being read.

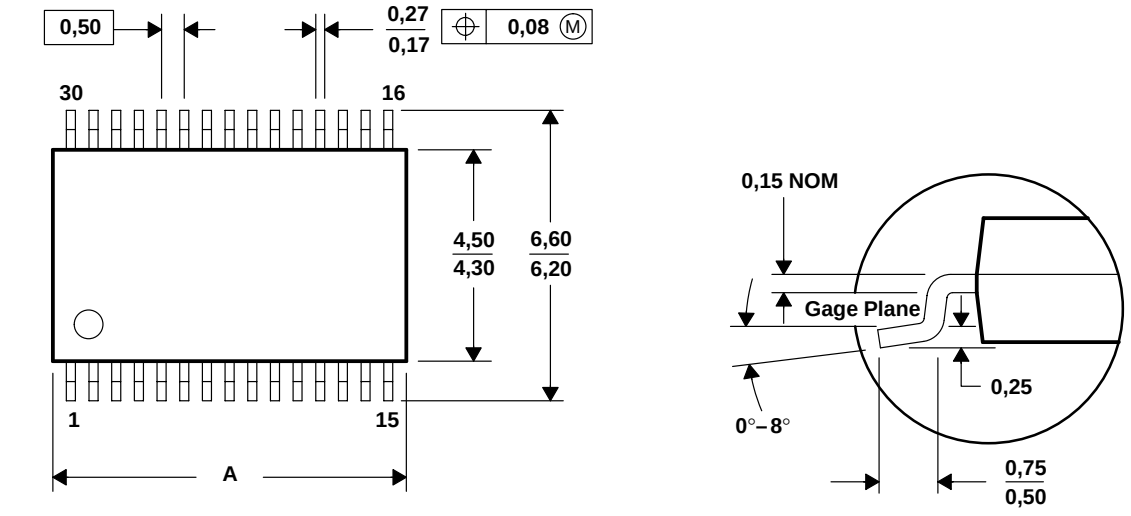
A.2 TAS3103 Firmware Block Diagram



Appendix B
Mechanical Information

DBT (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

30 PINS SHOWN



DIM \ PINS **	20	24	28	30	38	44	50
A MAX	5,10	6,60	7,90	7,90	9,80	11,10	12,60
A MIN	4.90	6,40	7,70	7,70	9,60	10,90	12,40

4073252/E 02/02

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-153