FEATURE

AUDIO DELAY LINES

Don't do now what you can put off for a few milliseconds. Need to delay a signal? Tim Orr shows you how to do it and suggests some applications for analogue delay lines.

THERE ARE MANY natural phenomena which are 'caused' by time delays. All acoustic instruments and, in fact, everything in acoustics is time related. It is, therefore, hardly surprising that several manufacturers produce electronic time delay integrated circuits. These are called analogue delay lines or sometimes, 'bucket brigade delay lines' as this accurately describes their operation.

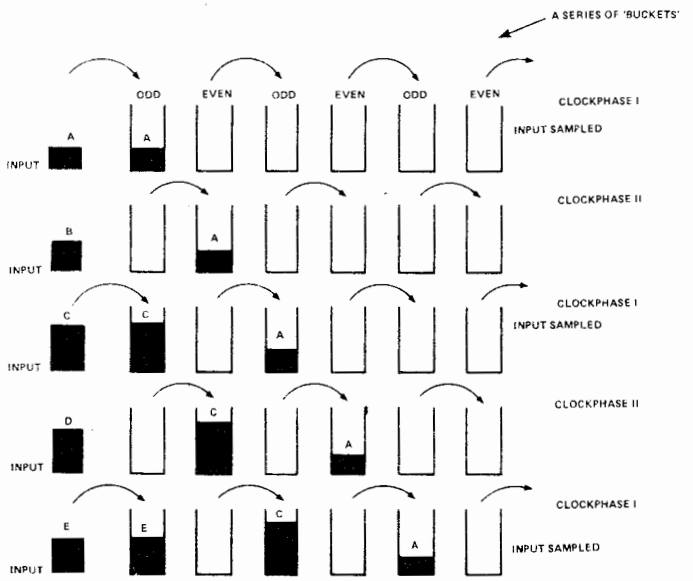


Fig. 1. Bucket Brigade delay lines.

Quantum Buckets

The device can be thought of as being a series of buckets containing water. (Actually it is a series of capacitors containing charge.) The signal presented to the input fills up the first bucket to the level of that signal. This occurs on phase I of a controlling clock signal. On the second clock (phase II), all the *odd* buckets tip their water into the *even* buckets. No input sampling occurs on clock phase II. On the next clock phase (phase I) the input is sampled and all the *even* buckets tip their water into the *odd* buckets. In this way a signal propogates down the delay line which represents the input signal as a series of 'samples'. The buckets are really analogue sample and hold units and the tipping is done with electronic switches. This technique is a cross between analogue and digital processes. The cross between analogue and digital processes. The charge stored (which is proportional to the input voltage) is truly analogue, but it is quantised into small units of time and so, in that sense, it is digital. If the delay line is, say, 512 stages long and the clock frequency is 512 Hz, then the delay time will be:

$$\frac{\text{number of stages}}{2 \times \text{clock frequency}} = 0.5 \text{ sec}$$

That is, after 0.5 sec a waveform representing the input signal of 0.5 sec earlier will appear at the output. In the example shown in Fig. 1, this signal would only appear at the output for the duration of clock phase II. To fill in the gaps, a second delay line connected in parallel with the first, but clocked in antiphase, is used, so that a delayed output signal appears on both clock phases.

Delay lines would seem to solve a myriad of electronic problems but with every solution comes a host of new problems. First, the maximum bandwidth of the delayed signal is proportional to the clock frequency. As the signal is sampled, then the 'sampling theorem' says that the signal bandwidth must be less than half the sampling frequency, which, for practical purposes, means about one-third. So, if you want to delay an audio signal of 10 kHz bandwidth by 1 second, then the number of stages delay needed is 60,000. This will cost you a few hundred dollars in delay lines. If you choose a lower clock frequency requiring fewer delay lines then you will have to make do on a reduced bandwidth. If this bandwidth is not controlled by use of an external lowpass filter, then a phenomenon called aliasing occurs which makes the delayed signal sound as if it has been 'ring modulated'. A typical delay line structure is shown in Fig. 2. A lowpass filter is used to band limit the input signal which prevents the aliasing effects. A second filter is used to recover the quantised output from the delay line by rejecting all the unwanted high harmonics.

The input signal level is always larger than that of the output signal because the buckets are leaky, although the leaks occur in both positive and negative directions. Also, the slower the clock frequency the longer the leakage time is and so the loss is greater. This is a major noise generating mechanism. The noise is broad band, being strong in low frequencies (just the area you are listening to), and becomes louder and more bassy as the

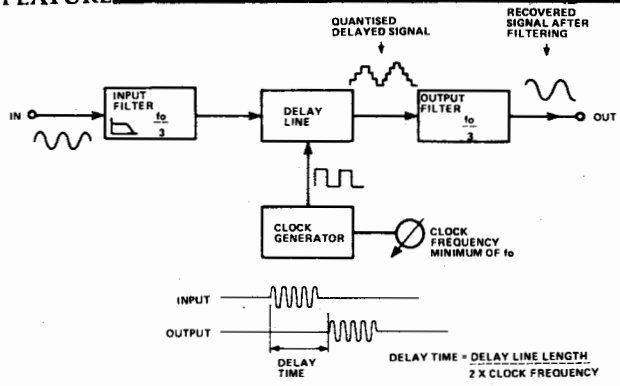


Fig. 2. Block diagram of a typical delay line system.

clock frequency is reduced. This results in signal to noise ratios of about 70dB for maximum frequencies. To overcome the poor performance at low frequencies a noise reduction system such as a compander can be used. The distortion caused by delay lines is typically about 1% and the overload characteristics are not at all good. Heavy overloads can cause the delay lines to stop producing any output at all. The solution is to limit the input level, with some simple sort of diode limiting. One other gremlin is that the output DC level varies with clock frequency which causes some awkward break-through effects. However, once you are fully aware of the limitations of delay lines, it is possible to design a wide range of interesting devices. Delay lines work surprisingly well when you consider that they move a very small packet of charge through several hundred memory stages with a corruption of only one part in 10,000 to 100,000!

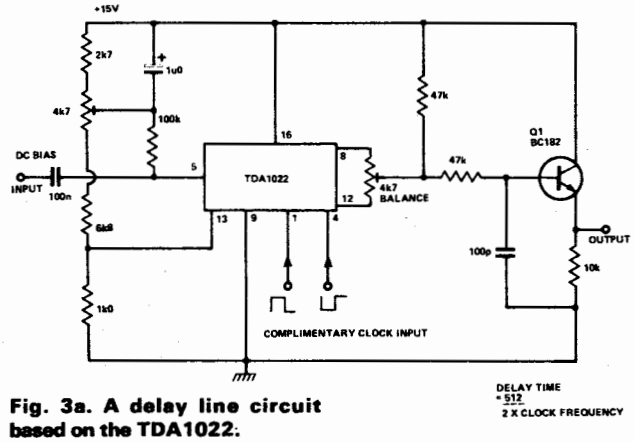


Fig. 3a. A delay line circuit based on the TDA1022.

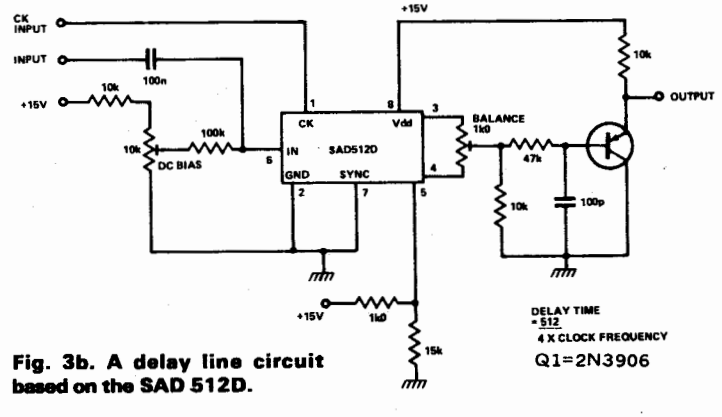


Fig. 3b. A delay line circuit based on the SAD 512D.

Some Delay Line Circuits

Two delay line circuits are shown in Fig. 3. The top one uses a delay line made by Mullard/Signetics. A two phase clock is needed. A preset adjusts the input DC bias so that when the device is overloaded, the clipping is symmetrical. A balance control on the output balances the two outputs for a minimum clock breakthrough. This preset is particularly useful when long delay times with audible clock frequencies are used.

The second delay line is the SAD512D made by Reticon. This device has the same two preset controls but only requires a single clock signal. There is a complementary clock generator (a divide by two flip flop) on the actual IC. The input clock must therefore be twice the calculated frequency.

If long delay times are needed, then there is the Reticon R5101 which will give you a 1 second delay at about 500 Hz bandwidth. This device gives a superb automatic double tracking effect (50 mS at 10 kHz bandwidth) but unfortunately it's rather expensive.

Clock Generators

A selection of clock generator circuits is given in Fig. 4. Circuit A is a standard CMOS relaxation oscillator. The IC costs only about 50¢ and generates complementary square waves; the minimum frequency of operation is about 1 MHz (with a suitable timing capacitor) and the manual control range is about 50 to 1. It is not very practical to voltage control the frequency of this oscillator.

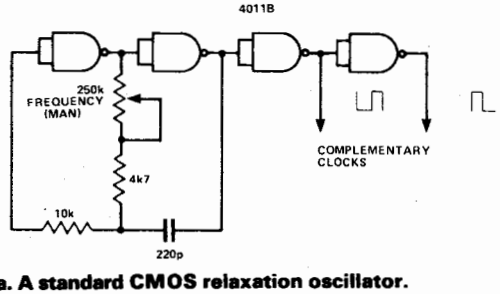


Fig. 4a. A standard CMOS relaxation oscillator.

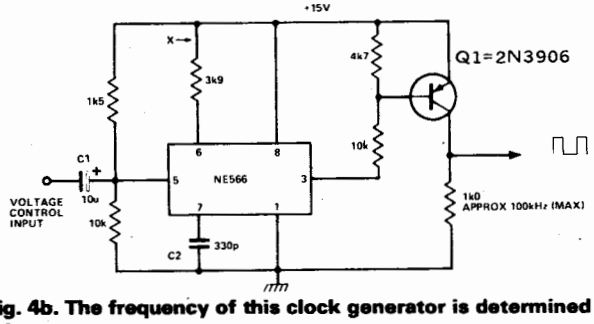


Fig. 4b. The frequency of this clock generator is determined by C1.

Circuit B uses an NE566 which is a voltage controllable oscillator IC. The frequency may be controlled via the capacitor C1 or by interposing a potentiometer or a controlled current source at point X. The output square wave needs to be level shifted and this is done with Q1. The maximum frequency using this circuit should be limited to about 100 kHz. For higher operation up to 1 MHz, a faster level shifter is needed.

Circuit C uses a CMOS Schmitt trigger and a couple of transistors. This oscillator can readily be controlled by a current generator. The output waveform is a short positive going pulse. A divide by two flip flop converts

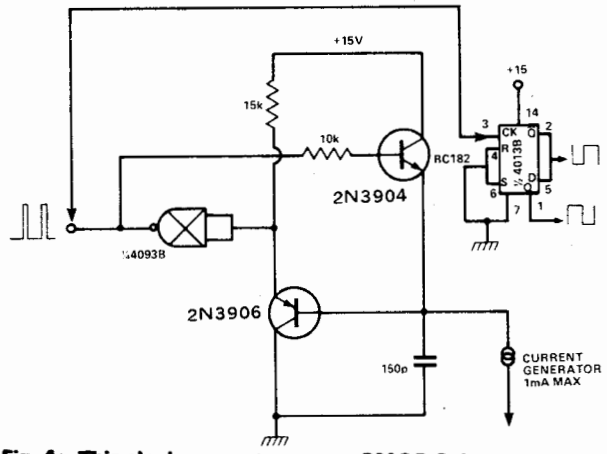


Fig. 4c. This clock generator uses a CMOS Schmitt trigger. The flip flop produces a pair of complementary square waves.

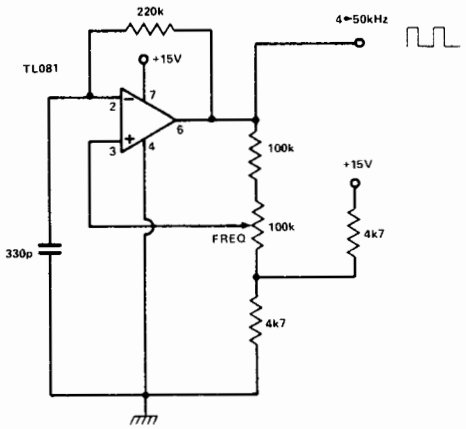
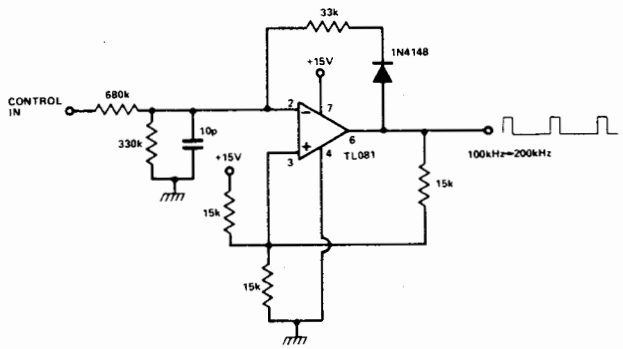


Fig. 4d. (above) and Fig. 4e. (below) show circuits using fast slew rate op. amps.



this pulse into a pair of complementary square waves.

Circuits D and E employ the fast slew rate (13 V/uS) of the Texas BI FET Op Amp range. This enables them to oscillate at high frequencies and to generate square waves with fast edges. Circuit D is a manual control device and circuit E is voltage controllable.

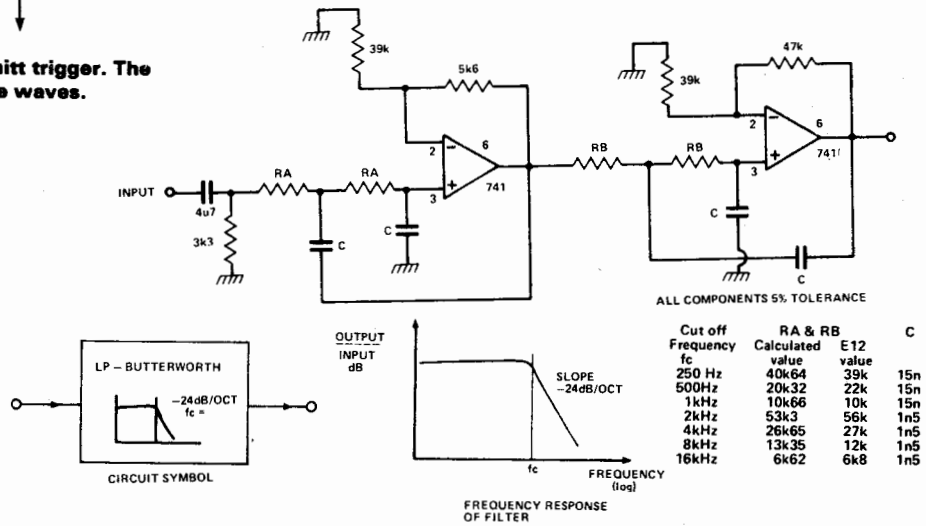
DIY Design

A 'do it yourself' lowpass filter chart is shown in Fig. 5. This filter is a 4th order Butterworth design. The roll-off slope is 24 dB/octave. This means that signals one octave above the cut-off frequency are attentuated by 24 dB (×0.06), at two octaves the attenuation is 48 dB (×0.004), etc. Also the filter has a pass band gain of 8.3 dB (×2.6).

The design procedure for constructing delay line systems is as follows.

1. Select the correct length delay line for the job in hand. Decide on the signal bandwidth needed.
2. Design the low pass filters to have a cut-off frequency equal to the signal bandwidth.
3. Select a suitable clock oscillator that will generate the correct output (single or complementary) at a high enough frequency. Select a voltage controlled design if it is needed. Calculate the required clock frequency.

The following examples show delay line systems. The boxes depicting delay lines include suitable filters.



Cut off Frequency fc	RA & RB Calculated value	RA & RB E12 value	C
250 Hz	40k64	39k	15n
500Hz	20k32	22k	15n
1kHz	10k66	10k	15n
2kHz	53k3	56k	1n5
4kHz	26k65	27k	1n5
8kHz	13k35	12k	1n5
16kHz	6k62	6k8	1n5

Fig. 5. A do-it-yourself design for a fourth order Butterworth filter.

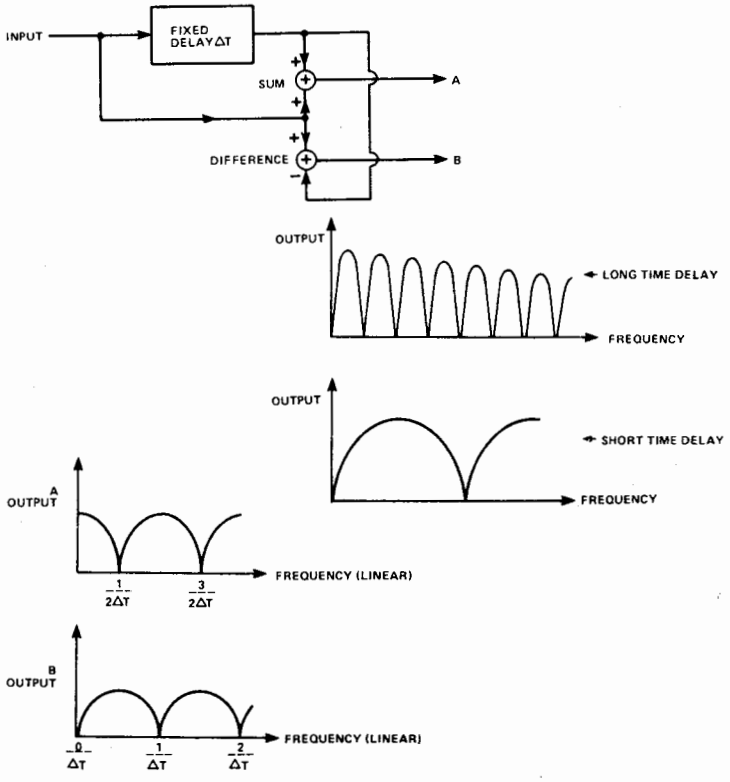


Fig. 6. By taking the sum and difference between the original and delayed signal, a comb filter response is generated. The noteches are spaced at 1/(ΔT) Hz, where ΔT is the delay time.

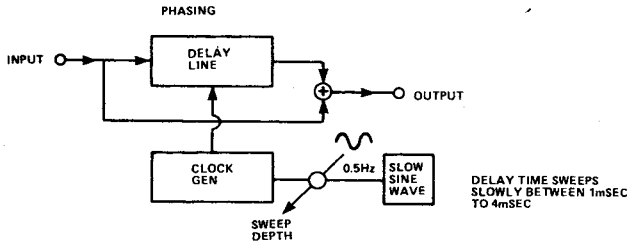


Fig. 7. Note that a long time delay produces lots of notches, a short time delay, only a few. A very popular musical effect is phasing. This uses a slowly sweeping comb filter. That is, the delay time, and hence the notch spacing, are modulated with a slow moving sine wave.

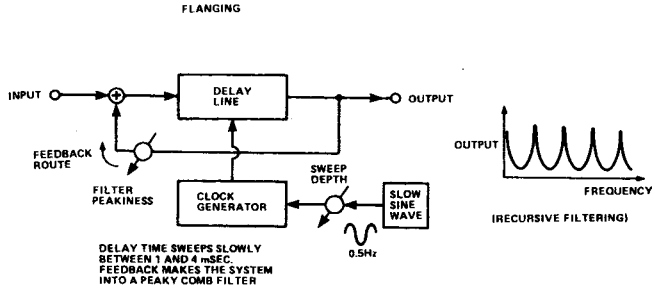


Fig. 8. Flanging is another similar effect, except that feedback is applied around the delay line. When this feedback is in phase with the input, a peak in the frequency response is generated. A pot is used to control the feedback and hence the amount of 'peakyness' of the filter. Flanging produces very strong colouration of the sound.

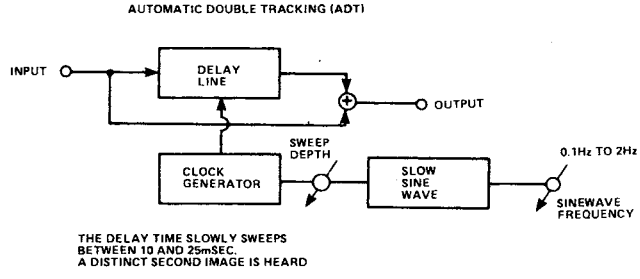
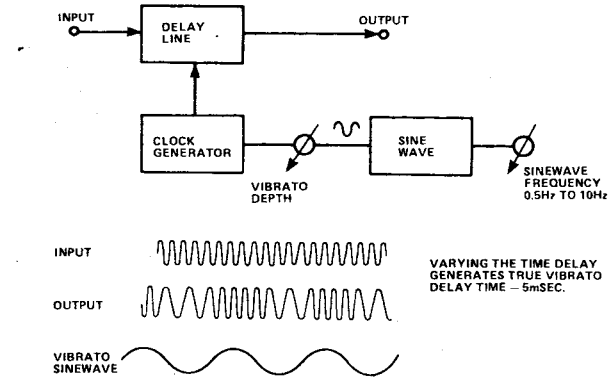


Fig. 9. Automatic double tracking (ADT) is used to add depth and a chorus quality to solo singers and musicians. The delay time is relatively long so that a distinct second image is heard. This image is slowly swept backwards and forwards in time thus adding to the chorus quality. It is such a useful effect that even my singing sounds good!



10 shows a 'true vibrato' system. This produces a real uency modulation acting upon all of the input signal. By lly modulating the clock generator frequency the time delay nilarly modulated. This causes the output signal to be ressed and expanded in time, resulting in vibrato.

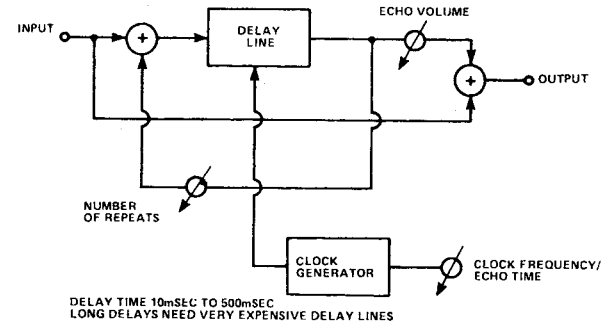


Fig. 11. All electronic echo is obtainable using long delay lines, although you generally have to trade off bandwidth for echo time. Electronic echo systems usually have three controls: time delay, echo volume and repeat level. This last control enables you to vary the echo from a single slap back echo to a long series of repeats.

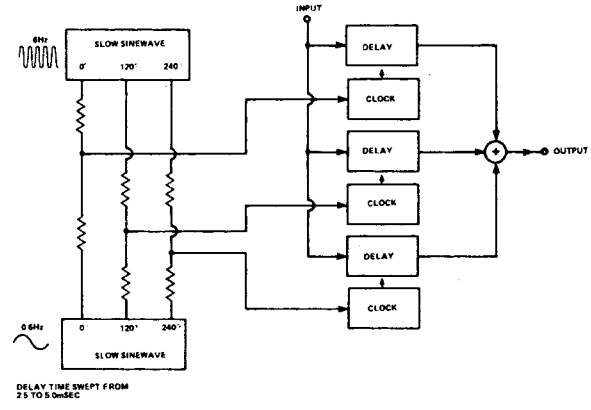


Fig. 12. Electronic string machines nearly always have a chorus/ensemble generator. This is a device that causes complex phasing on the string signal that converts it from a rather flat electronic signal to a rich string-like sound. This is done with three delay lines that have their delay times modulated by three low frequency sine-waves.

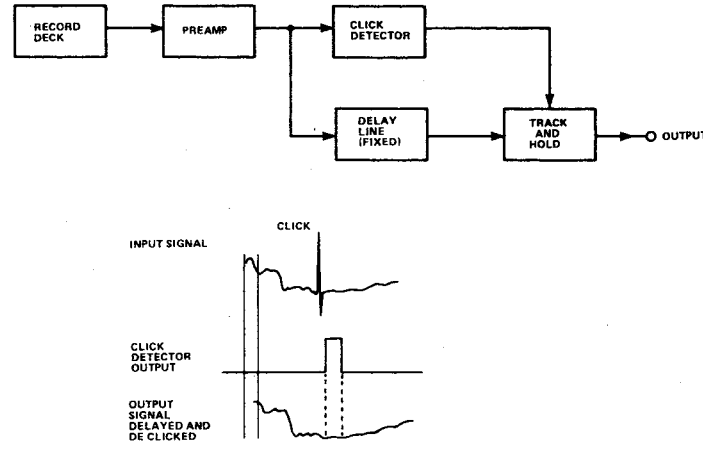


Fig. 13. It is possible to remove record scratches and clicks using a delay line. A scratch on a record is a relatively easy signal to discriminate from the music. However, once the scratch has been detected, the sound of the scratch has already left the loudspeakers and so it is too late to do anything about it. However if the sound is delayed then the scratch can be 'snipped out' using a track and hold circuit. The resulting gap is far less objectionable than the original scratch.

analogue delay line

There are numerous applications requiring the use of an audio delay line, for example phasing and vibrato units, echo and reverberation units, and sophisticated loudspeakers with active time-delay compensation. One of the simplest ways to achieve this electronically is to use an analogue (bucket brigade) shift register. There are various types on the market and a particularly interesting one is the Reticon SAD 512, which has 512 stages and a built-in clock buffer. The clock buffer enables it to be driven from a simple, single-phase clock circuit such as a CMOS multivibrator.

Figure 1 shows a delay line utilising the SAD 512. Input signals to the device must be positive with respect to the 0 V pin, so the AF input signal is first fed to an inverting amplifier, IC2, which has a positive DC offset adjustable by P1. The clock generator is an astable multivibrator using CMOS NAND gates (N1 and N2) and its frequency may be varied between 10 kHz and 100 kHz by means of P3. The clock buffer of the SAD 512 divides the clock input frequency by two, so the sampling frequency, f_c, of the SAD 512, varies between 5 kHz and 50 kHz. The delay produced by the circuit is $n/2f_c$, where n is the number of stages in the IC. The delay may therefore be varied between 5.12 ms and 51.2 ms. To obtain longer delays several SAD 512s may, of course, be cascaded very easily, since no special clock drive circuit is required.

To minimise clock noise the outputs from the final and penultimate stages of the IC are summed by R7, R8 and P2. However, if the circuit is to be used with the minimum clock frequency then clock noise will still be audible, and the lowpass filter circuit shown in figure 2 should be connected to the output. This consists of a fourth-order Butterworth filter with a turnover frequency of 2.5 kHz and an ultimate slope of −24 dB/octave. Of course, if low clock frequencies are to be employed then the maximum frequency of the input signal must be restricted to half the sampling frequency. This can be achieved by connecting the filter circuit of figure 2 at the input of the delay line, as shown in figure 3.

To set up the circuit the clock frequency is lowered until it becomes audible. P2 is then adjusted until clock noise is at a minimum. The clock frequency is then raised and a signal fed in. The signal level is increased until distortion becomes apparent, whereupon P1 is adjusted to minimise distortion. This procedure (increasing the signal level and adjusting P1) is repeated until no further improvement is obtained. Alternatively, if an oscilloscope is available, P1 may be adjusted so that the waveform clips symmetrically when the circuit is overloaded by a large signal.

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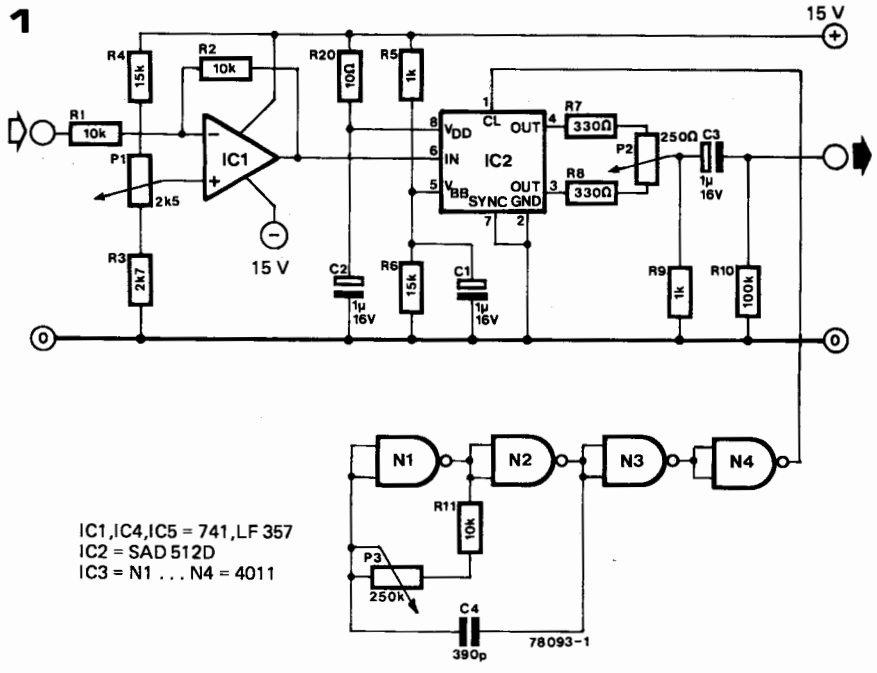
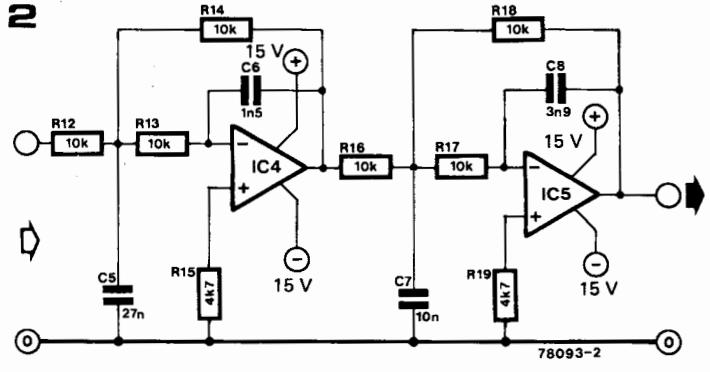


IC1,IC4,IC5 = 741,LF 357
IC2 = SAD 512D
IC3 = N1 . . . N4 = 4011

2



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