Audio Time Delay Systems

CONCLUDED

Build a Digital Audio Delay Line

Computer-type RAM memory and both A/D and D/A converters are used in this second approach

BY JOHN NEVES, STEVE KOLUPAEV, AND DEBBIE DELAHANTY

IN the first two parts of this series, we described an audio delay system based on analog techniques using bucket-brigade devices as the principal active elements. This month we will concentrate on the use of digital techniques to achieve the same purpose.

The project described here uses A/D (analog-to-digital) and D/A (digital-to-analog) converters, random access memory (RAM), and a time base that provides the necessary synchronization for the digital system as well as determining the length of the delay.

Overall Operation. As shown in Fig. 1, the audio input is fed to a filter and amplifier combination that attenuates frequencies above 10 kHz (to prevent aliasing problems) and scales the signal level for the A/D converter.

An 8-bit A/D converter performs a companding conversion that increases the digital signal resolution to an equivalent 11 bits plus sign, giving a dynamic range of approximately 70 dB. The converter operates under the control of synchronization pulses from the clock/controller. Digital information at the output of the A/D converter passes to a 4096 (4K in computer jargon) × 8-bit RAM as a series of 8-bit "words." Timed by pulses from the clock/controller, the stream of digital words cycles through a desired number of memory locations, up to the maximum of 4096. At any point in the cycle, as an old sample is read from the data latch and passed to the D/A converter, a new sample is written into the memory.

The length of delay is determined by the number of memory locations through which each sample passes and the length of each sampling interval. (The number of locations traversed is set by the manual switches.) For example, if the sampling frequency is 25 kHz, one sampling interval is 1/25,000 second or 40 microseconds. Therefore, if all 4096 memory locations are used, the total delay will be 4096 × 40 (μs) or 163.84 milliseconds. A 20-kHz rate would give a delay of 204.8 milliseconds.

Setting the memory address counter to some number between 1 and 4096 by means of the thumbwheel switches allows the delay to be varied while holding the sampling rate constant. Since the sampling rate also determines system bandwidth, changing the delay in this fashion does not affect frequency response. The fact that digital data is not degraded as it passes through the RAM means that the noise and distortion content of the output signal is also independent of the delay.

After the user-selected storage period, the digital data is read out of the memory and temporarily stored in a latch circuit that holds the digital data steady for the following D/A converter. Upon receipt of an appropriate timing pulse, the latch passes the digital data to the D/A converter where it is converted back into analog form. This analog sig-

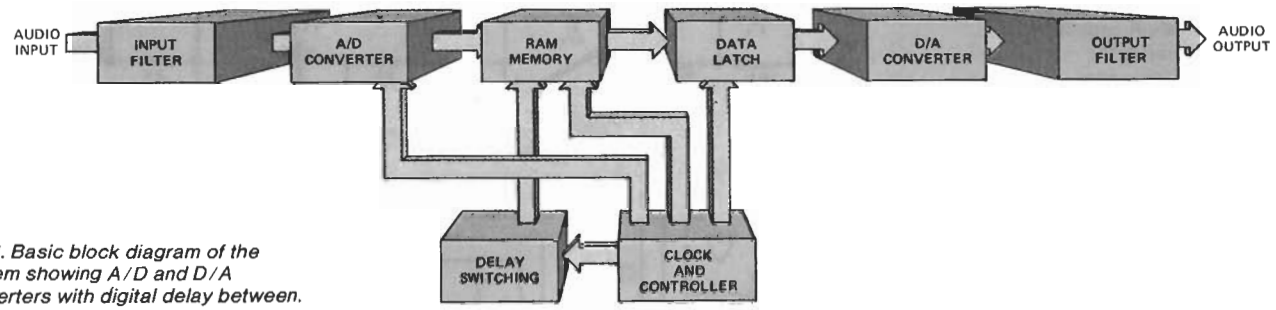


Fig. 1. Basic block diagram of the system showing A/D and D/A converters with digital delay between.

nal, now delayed, is filtered to remove any sampling components above 10 kHz that may be present. After filtering, the audio signal is amplified to bring it up to a level (about 1 volt) that can drive an audio amplifier.

Like the analog unit, the digital delay system is intended to be used with one or two auxiliary power amplifiers and loudspeakers. Ideally, there should be two delay units, one per channel. The signal should be delivered to your listening area at a level about 10 dB below that of the undelayed sound. For reasons detailed in Part 2, less expensive speakers and amplifiers can be used for the delayed sound channels.

To further economize, a single amplifier, speaker, and delay unit can be used. Audio from the two main channels can be resistively mixed and fed to a single delay unit as shown in Fig. 2.

The length of the delay produced by the unit can be adjusted in small increments to tailor it to the acoustics of your listening area. Start with about 20 milliseconds and experiment from there. Provision has been made to feed some of the output signal back to the input to generate reverberation. But if there is too much feedback, oscillation will occur.

Circuit Description. Due to its complexity, the circuit has been broken up into small, functional units. The individual circuits are interconnected by mating "letters-in-a-circle."

Input Filter and A/D Conversion. As shown in Fig. 3, *IC1A* and *IC1B* form a low-pass filter that amplifies all signals below 10 kHz. A comparator formed by *IC1C* monitors the amplified signal and turns on *LED1* when the audio reaches the optimum four volts peak-to-peak.

The amplified signal from IC1B (pin 7) is passed to an A/D converter consisting of *IC2A, IC18, IC22, IC24* and two of the gates in *IC23*. Timed by a "start conversion" pulse from the clock/controller, the incoming analog audio is converted into 8-bit binary code that is presented to the RAM for temporary storage. The converter performs a companding action, making the resolution of the digital signal equivalent to an 11-bit word plus sign. Dynamic range is thus approximately 70 dB.

Memory and Latch. This circuit, shown in Fig. 4, uses eight conventional 4096 (bits) by 1 (bit) static RAMs (IC3 through *IC10*) arranged to form a 4096 (bits) × 8 (bits) array. Static RAM is used to avoid the refresh cycles needed by dynamic RAM.

Each RAM element has its own unique address identified by the "*An*" (*n* stands for a digit) symbol above each RAM address line pin. Each RAM also has one pin (pin 8, R/$\overline{W}$) that enables the RAM to accept data when the signal on this pin is in one logic state, and output the data when the pin is in the opposite logic state. Thus, under control of pulses from the clock/controller, the RAM can read in external data, or write out the data contained within its cells. The eight bits of data passed out of the RAM go to a pair of four-input data latches (*IC11* and *IC12*) that hold the data in their internal flip-flops until a properly timed pulse from the clock/controller causes it to pass to the D/A converter.

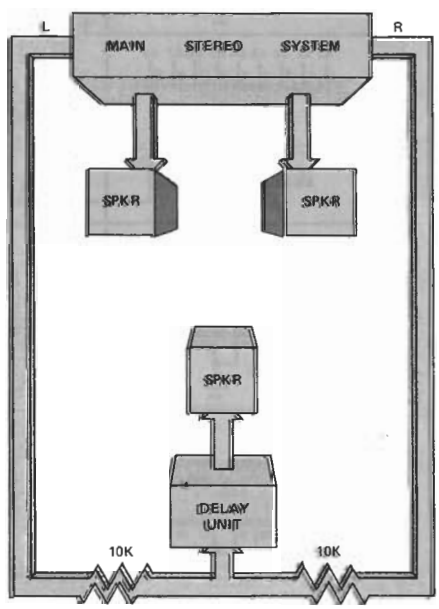


Fig. 2. Audio signals from the two main channels are mixed in resistors and applied to delay unit and a single speaker. Delay is adjusted to suit acoustics.

D/A Converter and Output Stages. The data from the RAM/latch circuit is applied to *IC13*, a D/A converter, as shown in Fig. 5. The reconstructed output signal from the D/A converter is almost identical to the filtered analog input, except that it is multiplied by a small scaling factor (due to amplification), contains a small amount of "quantization" noise caused by the D/A conversion, and, of course, is delayed.

After amplification in *IC25A* brings the signal up to about 1-volt peak-to-peak, the analog signal is passed through an active low-pass filter composed of *IC25B* and *IC25C*. The filter cuts off at 10 kHz, and attenuates any sampling frequency components that may remain in the signal. The output of *IC25C* is then used to drive the external audio amplifier.

Clock and Controller. The system clock, implemented by *IC19* in Fig. 6, is the basic timing control for the system. Its main element is a vco (voltage-controlled oscillator) whose frequency is determined by the setting of *R21*. Varying the clock rate allows the user to experiment with effects such as vibrato, flanging, or frequency modulation. Keep in mind that the vco not only affects delay time but system bandwidth as well.

Counter *IC17* accepts the clock signal and is configured to generate the four timed trigger pulses used by the A/D converter, RAM memory, and data latch. The four outputs are buffered by elements of *IC20* and *IC21* to convert the low-current CMOS outputs of *IC17* into signals capable of driving TTL.

As shown in Fig. 6, the four timing pulses are identified as P1, P2, P3, and P4. Pulse P1 commands the start of an A/D conversion in *IC18* (Fig. 3), while P2 increments (by 1) the memory address counter of Fig. 7. The resulting memory address points to the oldest stored sample. A new conversion will be completed eight clock pulses after P1.

The RAM is normally in the read mode, which means that the memory

(Figures 3 and 4 are on page 70. Text continues on page 73.)

PARTS LIST

C1,C4,—0.005-μF capacitor
C2—220-pF capacitor
C13—470-pF capacitor
C5—10-μF, 16-V electrolytic
C6,C7,C19—0.1-μF ceramic capacitor
C8 through C11,C16 through C18—1-μF, Mylar, tantalum, or electrolytic
C12—0.033-μF disc capacitor
C3,C14—0.001-μF, Mylar or ceramic
C15—330-pF ceramic capacitor
C20—47-pF ceramic capacitor
C21,C22—5000-μF, 20-V electrolytic
D1—1N914 diode
D2 through D5—1N4002 or similar diode
IC1,IC25—LM324 quad op amp
IC2—LM311N comparator
IC3 through IC10—4K × 1 static RAM, MM5257, TI4044, EMM4044, IM7141, MCM2141, 4104, 2613, HM4315, HM4847, or similar
IC11, IC12—7475, 74LS75, four-bit latch
IC13,IC22—DAC-76, DAC-88 companding D/A converter (Precision Monolithics or American MicroDevices)
IC14,IC15,IC16—74193, 74LS193 up-down synchronous 4-bit counter
IC17—4017 CMOS decade counter
IC18—DM2502 successive approximation register (National or American MicroDevices)
IC19—4046 CMOS phase-locked loop
IC20—4010 CMOS-TTL buffer
IC21—74LS00 quad two-input NAND gate
IC23—7486, 74LS86 quad exclusive-OR
IC24—7474, 74LS74 D flip-flop
IC26—320T-12, negative 12-volt regulator
IC27—340T-12, positive 12-volt regulator
IC28—340T-5, positive 5-volt regulator
J1,J2—Phono connector
LED1—Light emitting diode
The following are ¼-watt, 5% resistors unless otherwise noted:
R1—47 kΩ
R2—18 kΩ
R3—39 kΩ
R4,R23,R28 through R39,R40,R41—10 kΩ
R5—680 kΩ
R6—3.3 kΩ
R7,R10,R25—22 kΩ
R8—820Ω
R9,R18,R20—4.7 kΩ
R11,R24—51 kΩ
R12,R13,R15,R16,R26,R27—2.7 kΩ
R14—500Ω potentiometer
R17,R19—13 kΩ
R21—10 kΩ potentiometer
R22—2.2 kΩ
R42—33 kΩ
R43,R44,R45—100 kΩ potentiometer
S1—Spst switch
T1—24-V CT, 1-A (1.5-A for stereo)
Misc.—Hex 2-digit thumbwheel switch (2) or 16-pin DIP switches, suitable enclosure (Mod-U-Box MBS 4-10-10 available from Intra Fab, 425 Queens Lane, San Jose, CA 95112 or similar), knobs, press-on type, mounting hardware, etc.

Note: The following are available from Videoart, Box 10327, Stanford, CA 94305: etched and drilled pc board at $18; DM2502 successive approximation register at $6.80; DAC-88 converter at $7.50; set of eight memory ICs at $50. California residents please add 6.5% sales tax.

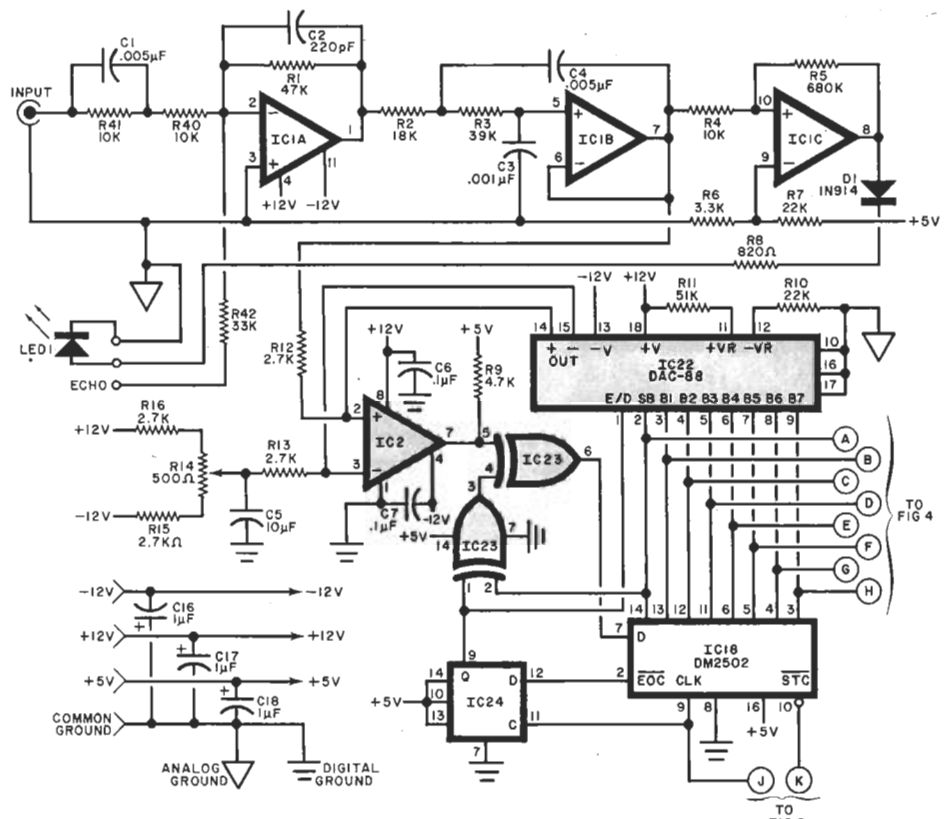


Fig. 3. Input filter and A/D conversion circuits. The input is filtered and amplified first and then converted to 8-bit binary code at the output to Fig. 4. A companding action makes the output equivalent to an 11-bit word plus sign.

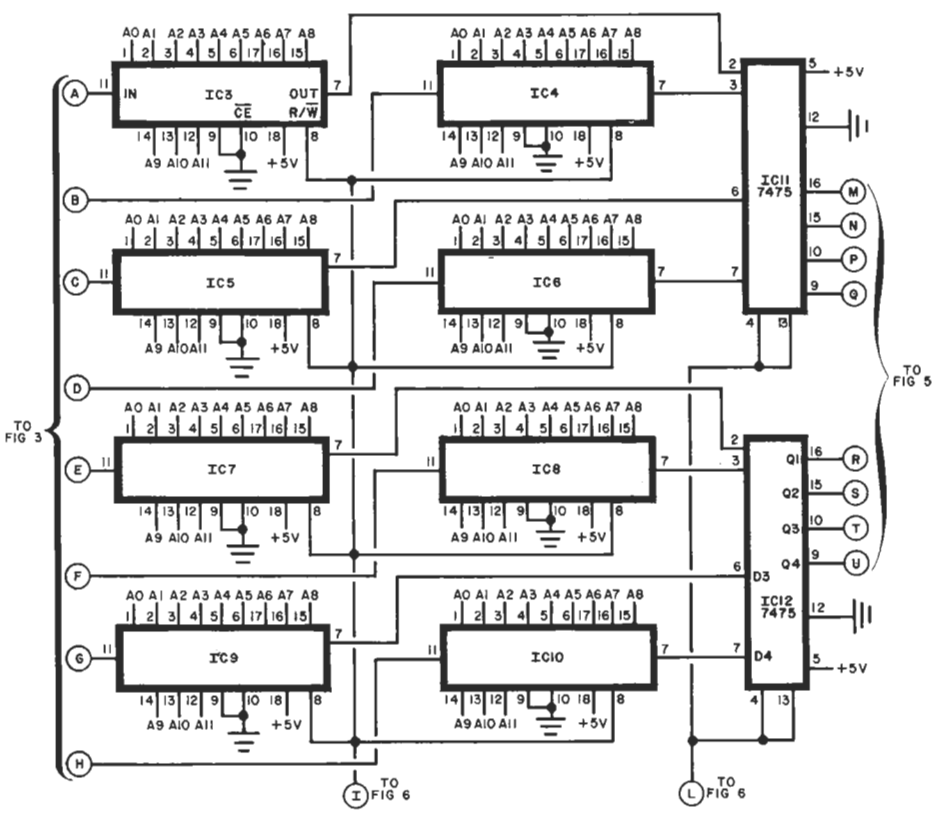


Fig. 4. Memory and latch circuits. Eight static RAM units (IC3 through IC10) are used to form a 4096 by 8 array. Each RAM can read in or write out data as determined by pulses from the clock/controller. Output is held in latches IC11 and IC12.

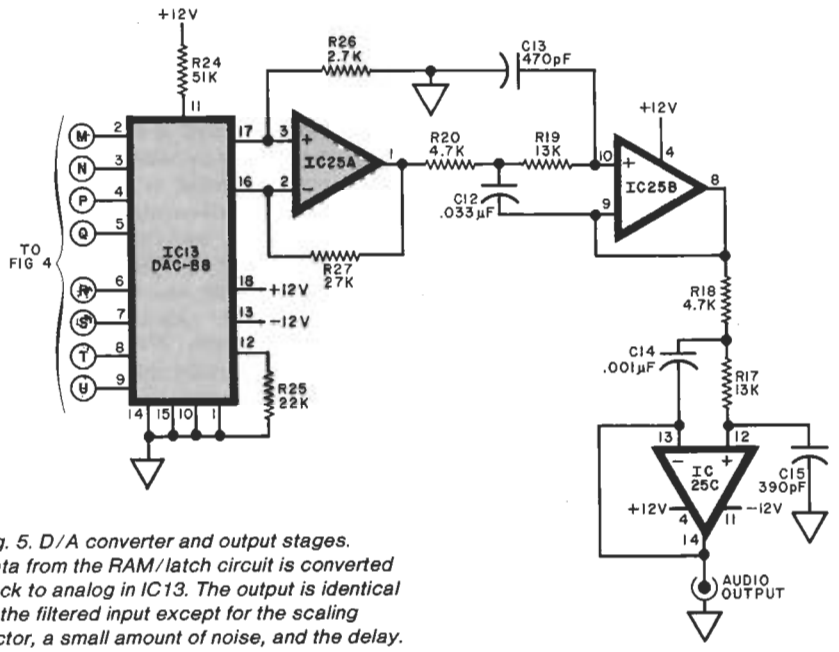


Fig. 5. D/A converter and output stages. Data from the RAM/latch circuit is converted back to analog in IC13. The output is identical to the filtered input except for the scaling factor, a small amount of noise, and the delay.

constantly displays the 8-bit code stored at the address pointed to by the memory address counter at its output. The third pulse, P3, is applied to the data latches (Fig. 4), causing them to load the result of the read operation and hold it stable for D/A conversion by *IC13* (Fig. 5), which takes place in less than one microsecond. The last pulse, P4, causes a memory write operation that overwrites the old sample with the 8-bit code currently available at the A/D converter output.

Delay Switching. The delay switching uses three ICs to select the RAM memory addresses dialed in via the user-accessible switches as shown in Fig. 7.

Programmable counters *IC14*, *IC15*, and *IC16* are cascaded with the clock input presented to *IC16*. Its "carry" output drives *IC15*, which in turn drives *IC14*. These counters can be preset to any desired modulo output by entering the control data on the input pins—in this case, voltage or ground from the user-selectable switches connected to *S2* and *S3*. Thus, the outputs of each IC will agree with the manually preset count, independent of the clock frequency. Since there are 12 address lines, the count can reach a maximum of $2^{11} + 2^{10} + 2^9 \ldots + 2^0 = 2^{12} - 1 = 4095$ and the delayed bits can pass through any desired number of memory locations.

Power Supply. The power supply, shown in Fig. 8, uses a full-wave rectifier in conjunction with −12, +12, and +5-volt regulators. The system draws 450 mA at +5 volts, and about 20 mA from each of the 12-volt supplies.

The 5-volt power requirement can be reduced by using "LS" or "C" versions of *IC11*, *IC12*, *IC14*, *IC15* and *IC16*. Do not use "L" devices because these usually have different pinouts. Regulators *IC27* and *IC28* should be supplied with heat sinks.

Construction. Given the complexity of the circuit, construction is best implemented by using either Wire-Wrap Techniques or a printed circuit board. In the former case, care should be exercised concerning the ground connections. As shown in the schematics, the analog digital grounds should be isolated from each other and merge only at the power supply common point.

Due to their size, etching and drilling guides and component layout for a double-sided pc board for the project are not reproduced here, but can be obtained by sending a self-addressed 9-by-12 envelope with two units of first-class postage to Dept. DDL, Editorial, POPULAR ELECTRONICS, One Park Ave., New York, NY 10016.

Outputs of the address counters (*IC14*, *IC15*, and *IC16*) should be kept as short as possible and as far away as possible from the input and output op amps. The use of IC sockets is recommended, and the proper installation of polarized elements must be observed.

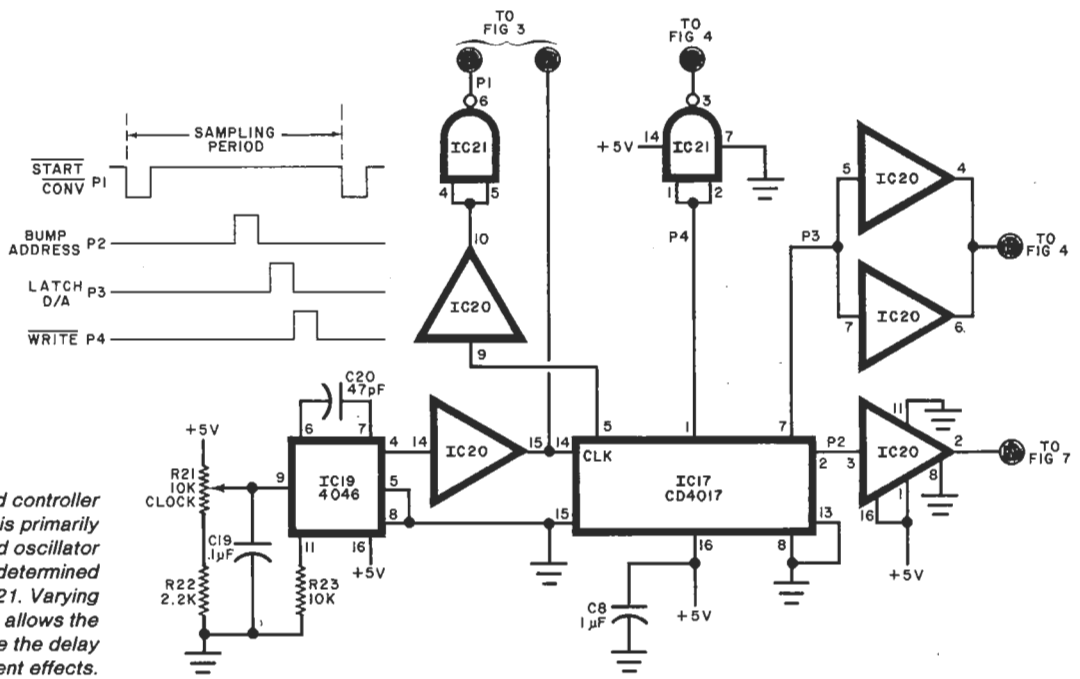


Fig. 6. Clock and controller circuits. This is primarily a voltage-controlled oscillator whose frequency is determined by the setting of R21. Varying the clock rate allows the user to change the delay and get different effects.

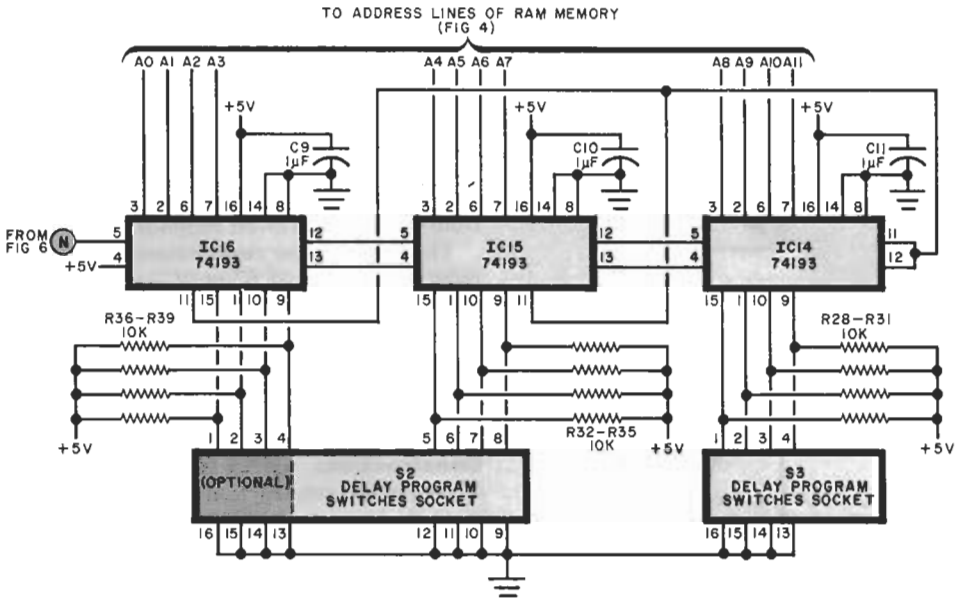


Fig. 7. Delay switching circuits. Three ICs are used to select the RAM memory addresses dialed in by the program switches S2 and S3.

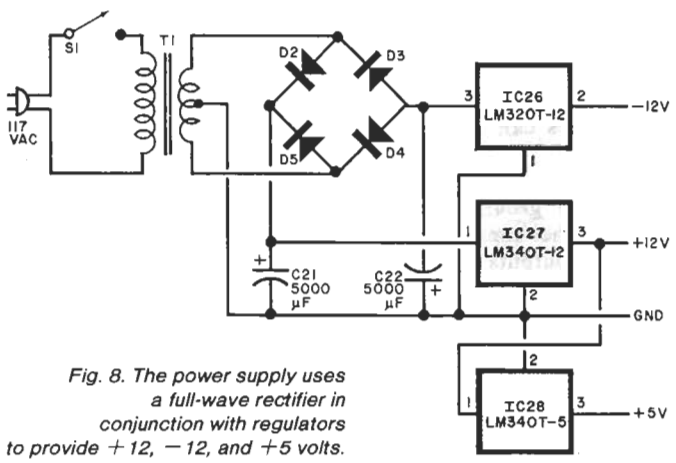
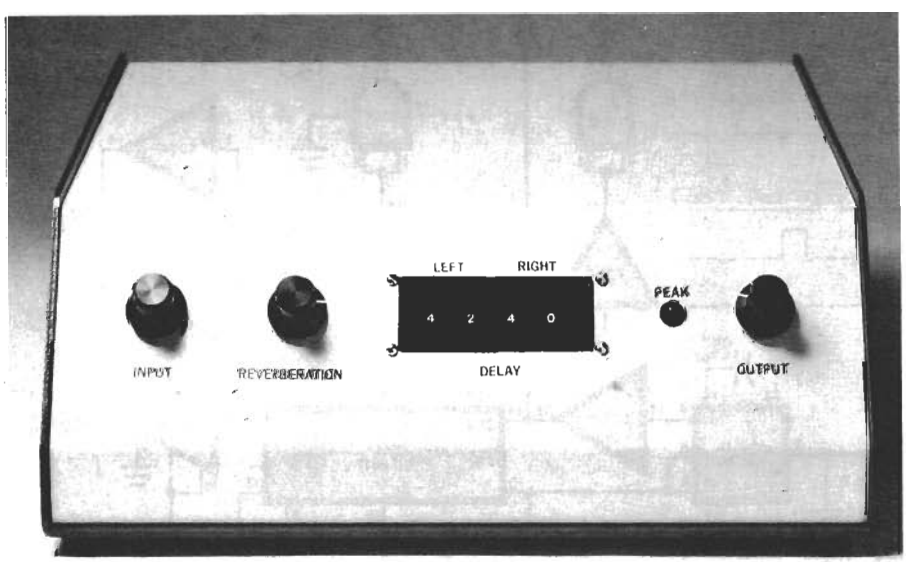


Fig. 8. The power supply uses a full-wave rectifier in conjunction with regulators to provide +12, −12, and +5 volts.



Front view of prototype showing input, output, and reverberation adjustments (see Fig. 9 on next page) and thumbwheel switches to determine delay for two channels.

After the board is completed, it can be installed in a suitable metal enclosure and interconnected as shown in Fig. 9. Although this illustrations shows a pair of thumbwheel switches used to select the delay, DIP switches, such as those used in computer boards, can be substituted. The input gain control, *R43*, output gain control, *R44*, reverberation control, *R45*, audio connectors, *J1* and *J2*, peak indicator, *LED1*, and the two delay-select switches can be mounted on the front panel. For stereo, dual potentiometers are used for *R43* through *R45*, along with two sets of thumbwheel switches and two peak indicator LEDs.

Adjustment. With the delay unit connected to an audio system as shown in Fig. 2, set *R14* and *R21* to their center positions. Place the delay switches (*S2* and *S3*) in the minimum configuration (all switches open). Then adjust echo (reverb) potentiometer *R45* for its minimum resistance, and the audio input control (*R43*) to its center rotation position.

Apply a 1-kHz sine-wave signal to the audio input (*J1*), and an oscilloscope to the *J2* audio output connector. With power turned on, adjust output control *R44* for a convenient scope display.

Increase the audio input level, either by adjusting *R43* or the audio signal generator's level control, until some clipping is noted on the output waveform. Successively adjust the input level and *R14* to obtain a symmetrically clipped sine wave. Then reduce the input level to just below clipping, so that a clean sine wave is displayed.

Increase the sine-wave input frequency to 5 kHz and adjust *R21* to minimize any serrated edges on the displayed waveform. Besides reducing noise, this adjustment also controls the sampling frequency (and bandwidth).

If an oscilloscope is not available, you can perform these adjustments by ear. Preset switches *S2* and *S3* for the desired amount of delay. Use a source of actual program material in place of the signal generator and your ears as "distortion monitors." Adjust the potentiometers for best audible performance. The results obtained by this method will, of course, be less accurate, but will be useful if care is taken in performing the adjustments.

With proper audio input levels, a 4-volt peak-to-peak signal should be seen at pin 7 of *IC1B* (A/D converter input). If you should require more gain, the value of *R1* (feedback resistor for *IC1A*) can be increased.

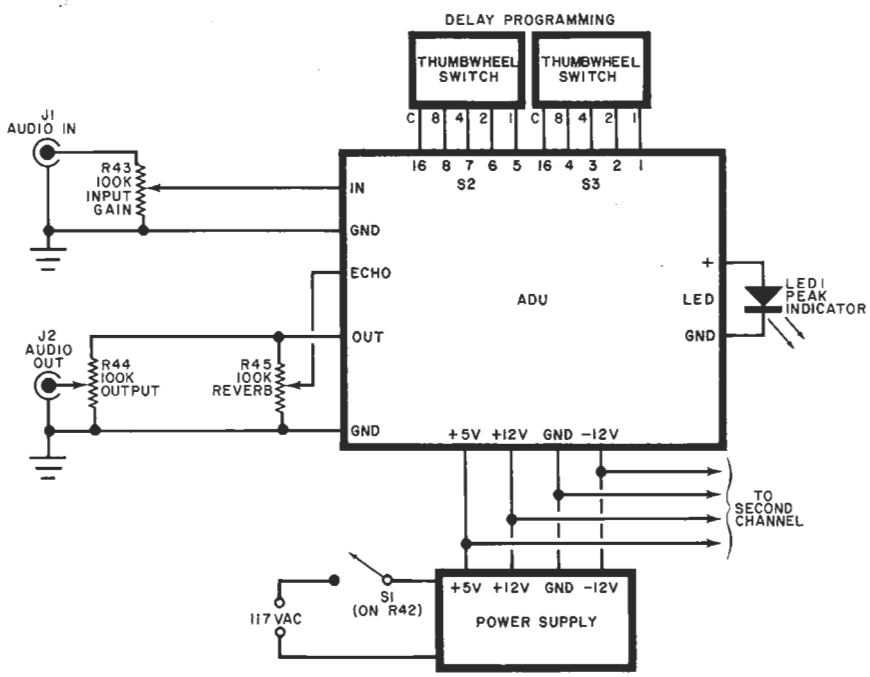
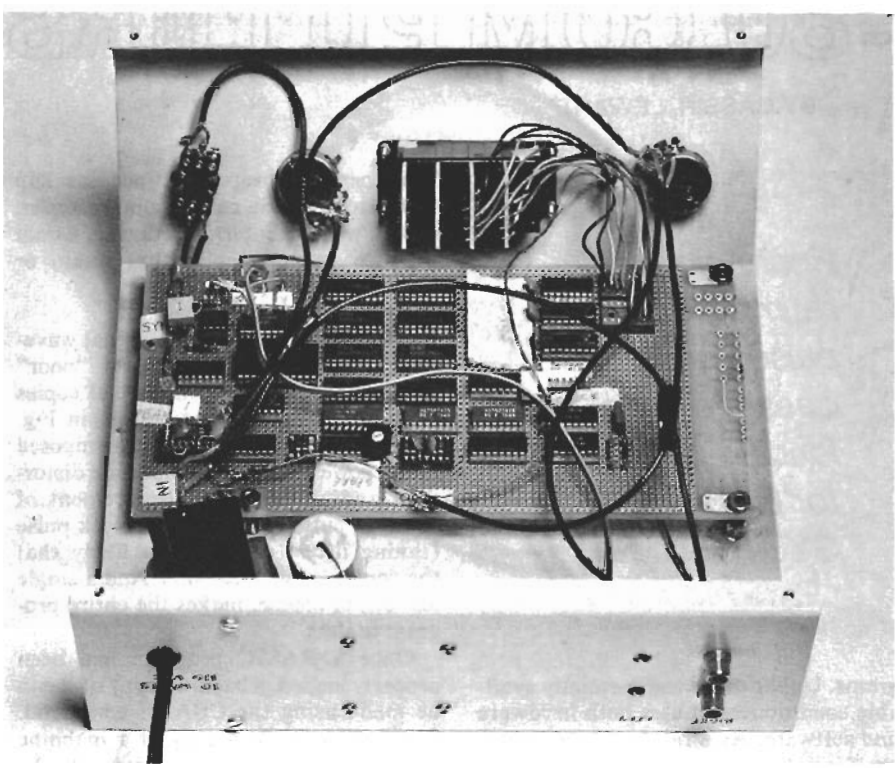


Fig. 9. Schematic of components that are not mounted on the printed circuit board. See photos below and on previous page for ways in which to locate the components.

The memory address counter (*IC14*, *IC15*, *IC16*) can be checked by setting *S2* and *S3* for maximum delay. This causes each of these IC's to count down by 16. An oscilloscope or frequency counter can then be connected to the A0 through A11 outputs of these ICs to note the decreasing frequencies.

A scope can also be used to follow the audio signal through to the A/D converter. The digital outputs of *IC18* vary with the applied audio signal. If a dc voltage level from zero to about 1 volt is applied to the input, the bit changes can be observed as the input voltage level is changed. Zero volts will produce all zeroes and 1 volt will create all ones, with 254 binary states between the two. ◇



Internal view of prototype shows arrangement of board and components on front panel.

BUILDING THIS CIRCUIT IS NOT RECOMMENDED

THE TECHNOLOGY IS TOO OLD - MUCH BETTER IS NOW AVAILABLE

THIS CIRCUIT IS PRESENTED ONLY BECAUSE STUDY OF IT CAN GIVE A PERSON BETTER UNDERSTANDING OF THE THEORY BEHIND MODERN TECHNOLOGY