Envelope Generator

By Jeff Macanley

ALTHOUGH the ADSR envelope generator has become standard there are occasions when a simpler and cheaper alternative is desirable.

The accompanying circuit shows such a device. The basis is the humble flip flop, IC2, half a 4013B. When a positive going pulse is applied to the set input the Q output goes high allowing C1 to charge via the attack pot, RV1, and D1. Notice, though, that the reset pin is connected back across C1: in consequence, as soon as the voltage across this component exceeds about 50% of the supply voltage, the flop flop resets, reverse-biasing D1.

C1 now discharges through the decay pot and D2. With the values shown both attack and decay are variable from a few milliseconds to several seconds. The two current limiting resistors should not be left out because the maximum current that can be drawn from the Q output is only about 10mA peak.

If negative triggering is required the inverter circuit shown can be employed. This has the advantage of allowing the device to be triggered from open collector devices. IC1 can be any inverting CMOS gate, NAND or NOR, with unused inputs wired to +ve (NAND) or 0V (NOR); it can even be an inverter gate! Note that supply connections to IC1 and 2 will need to be added. ■