BVO-16 & BVO-16LC CHIPSET

TRIGAUDIO

Super Low-Cost Multi-Effects DSP chipset

BV-Series DSP

16 FIX EFFECTS

Features

- Stereo performance sound quality
- 16 internal ROM programs of effects such as reverbs, echo, phaser, chorus, flanger, etc.
- Integrated the major components, control interfaces, and strengthen the electronic circuit design, also with the display circuit, for example 7-segment LED, that can save your bom cost
- 20/27bit digital signal processing with 24 bit AD/ DA converters 48kHz sample rates supports
- Programs run at 128 instructions per word clock. (6 MIPS @ 48 khz sampling frequency)
- 32k location Static Ram provides over 0.68 sec ofdelay at 48 kHz sampling frequency
- 2 input and 2 output
- low power 5V operation
- Competitive price
- ROHS compliant (PB-free)

Specification

Analog Input	2
Maximum Input Level	2.8Vp-P Max
Analog Output	2
Maximum Output	2.8Vp-P Max
Digital Processor	(DSP)20/27 Bit, (AD/DA): 24 Bit 192khz
S/N Ratio(A-Weighting)	>95 dB
THD+N	0.08%
Frequency Response	20 Hz - 20 Khz (+/- 2 dB)
Power Supply	5V 90ma (Without Display)

Binary Code and Program Chart

1.	0000	Small Hall	9.	1000	Phaser
2.	0001	Big Hall	10.	1001	Flanger
3.	0010	Room 1	11.	1010	Echo
4.	0011	Chamber Reverb-Church	12.	1011	Chorus
5.	0100	Revers Reverb-Reverse	13.	1100	Early Reflection
6.	0101	Gated Reverb-Gated	14.	1101	Big-Ambience
7.	0110	Room2	15.	1110	Stereo Delay
8.	0111	Spring Reverb	16.	1111	Slap Delay

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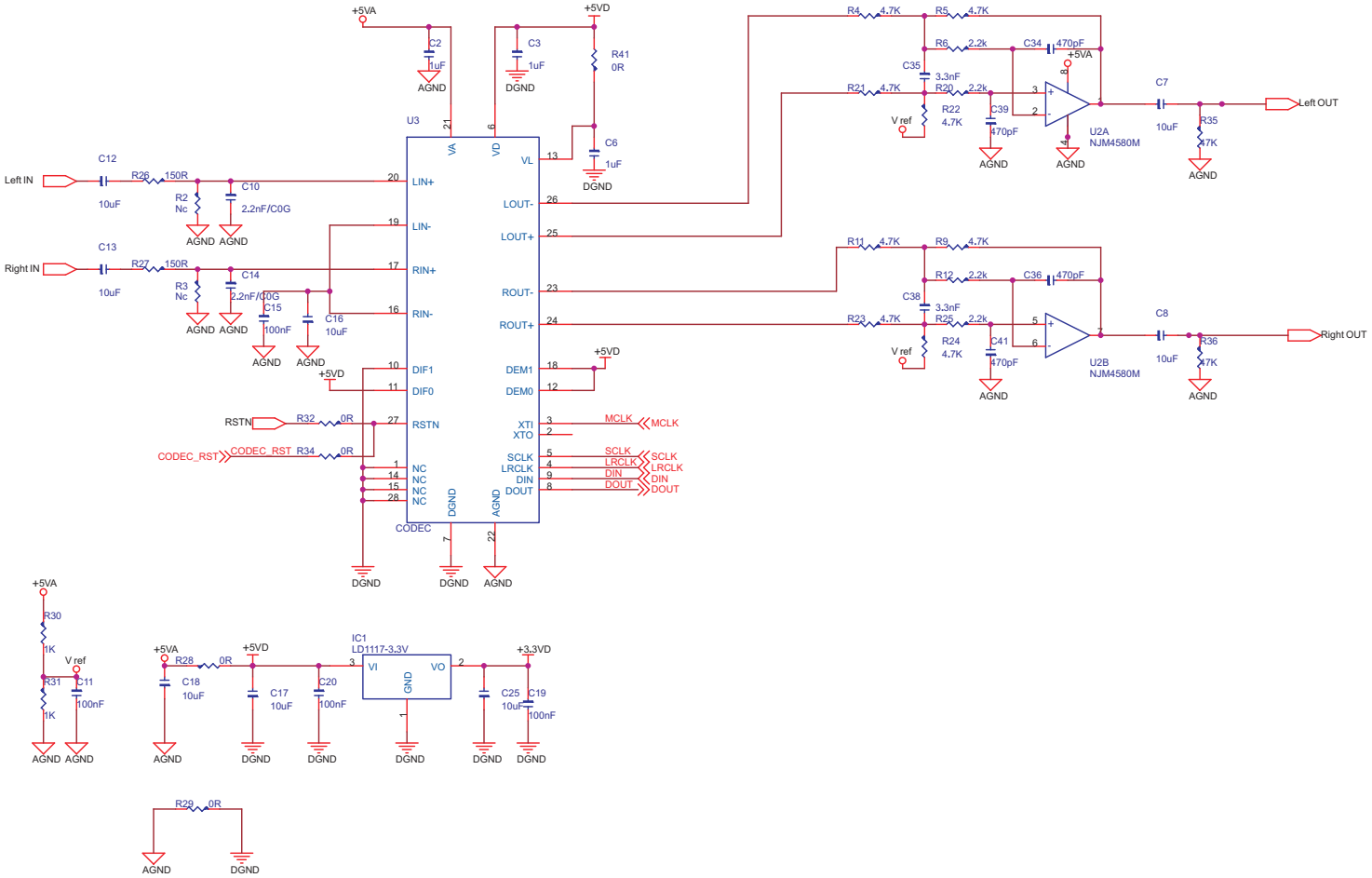
BVO-16&BVO-16LC Chipset Circuit (1-1)



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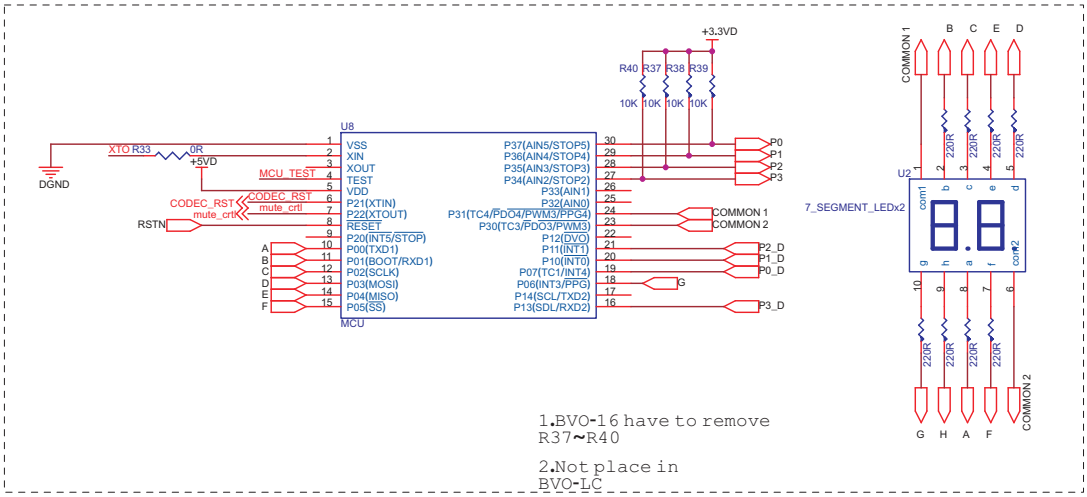
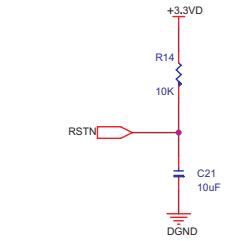
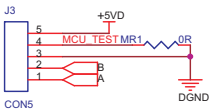
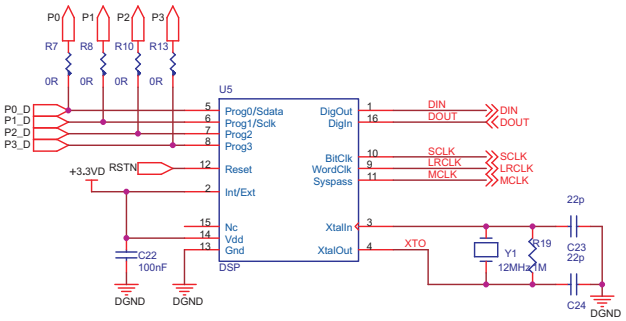
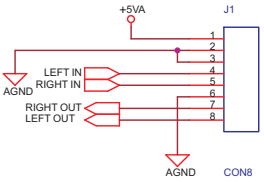
BVO-16&BVO-16LC Control and Display Circuit (1-2)

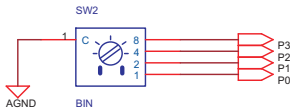


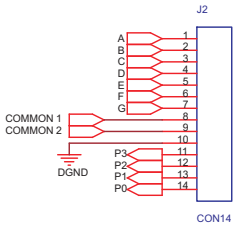












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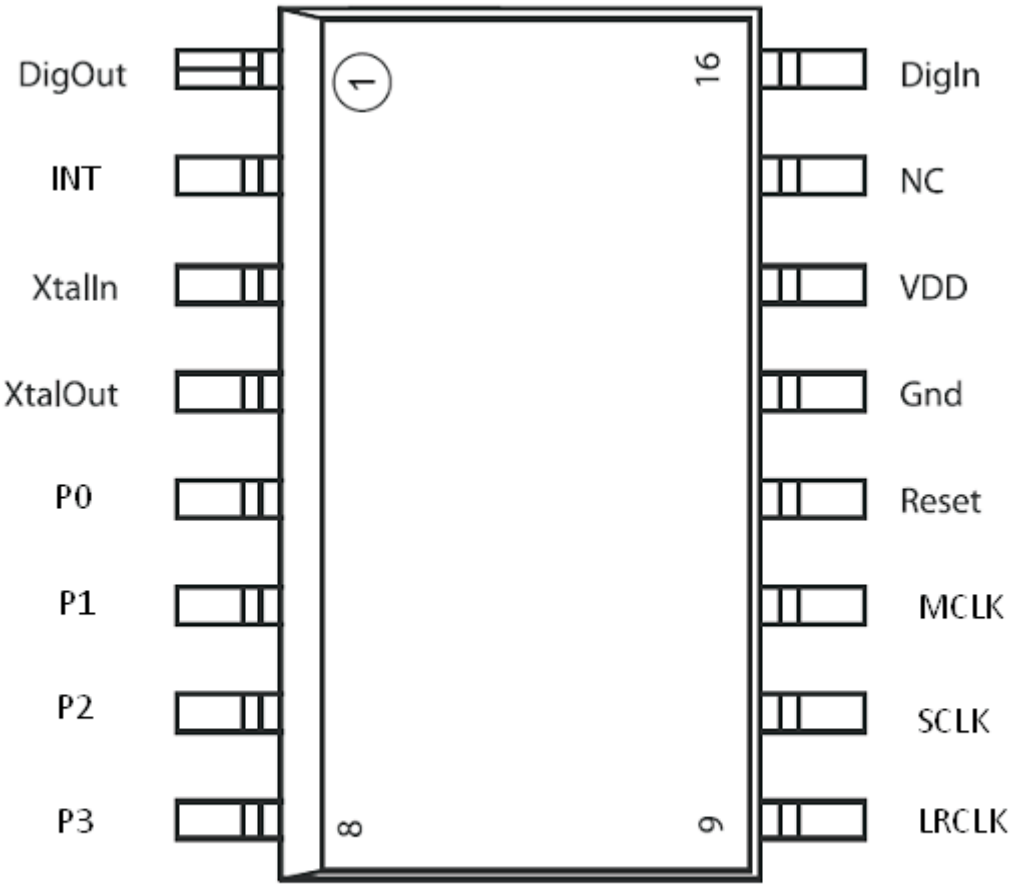
BVO-16&BVO-16LC Detail Item Description

DSP TA-1105 main chip



16 pin SOIC
300mils wide

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Pin Connection Description

Pin#	Name	PinType	Description
1	DigOut	Output	Digital serial output for stereo DAC
2	Int	Input	
3	XtalIn	Input	12.288 MHz crystal input
4	XtalOut	Output	12.288MHzcrystaloutput
5	P0	Input	
6	P1	Input	
7	P2	Input	
8	P3	Input	
9	WCLK	Output	Word clock output
10	BITCLK	Output	Bit clock output
11	LRCLK	Output	LR clock output
12	Reset	Input	Active low reset
13	Gnd	Ground	Ground connection
14	Vdd	Power	Vdd power pin
15	NC		
16	DigIn	Input	Digital serial input for stereo ADC

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Electrical characteristics and operating conditions

Parameter	Description	Condition	Min	Typ	Max	Units
VDD	Supply Voltage		3.0	3.3	3.6	V
Idd	Supply Current			24		mA
Gnd	Ground			0.0		V
Fs	Sample Rate		20	48		kHz

Outputs digout, sysclk, bictlk, wordclk

Parameter	Description	Condition	Min	Typ	Max	Units
V_{OH}	Logic "1" output voltage	Unloaded	2.9	_	_	V
V_{OL}	Logic "0" output voltage	Unloaded	_	0	0.6	V

Inputs digin, int/ext, prog0/sdata, prog1/sclk, prog2, prog3 reset

Parameter	Description	Condition	Min	Typ	Max	Units
VIH	Logic "1" input voltage		2.0	_	5.0	V
VIL	Logic "0" input voltage		0.0	_	0.3*Vdd	V

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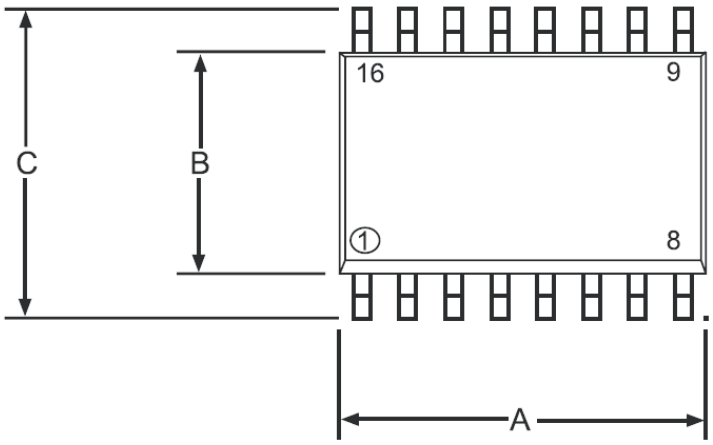
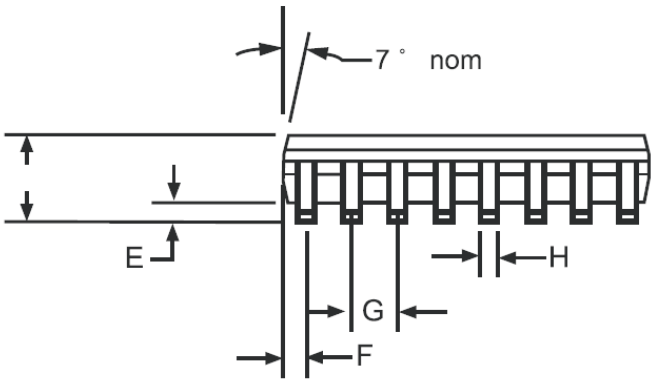
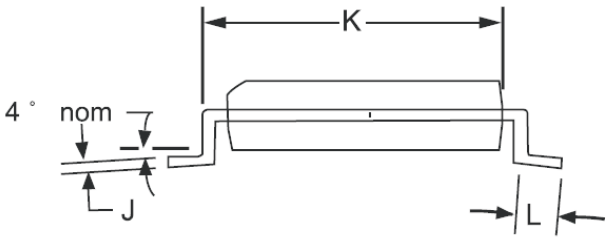
Package Dimensions





Dimensions (Typical)	Inches	Milllimeters
A	.406”	10.31
B	.295”	7.49
C	.407”	10.34
D	.100”	2.50
E	.008”	0.20
F	.025”	0.64
G	.050”	1.27
H	.017”	0.42
J	.011”	0.27
K	.340”	8.66
L	.033”	0.83

Note:
Dimension “A” does not include mold flash, proportions or gate burrs.



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24-BIT Stereo Audio Codec 6880

Features

***100 dB Dynamic Range A/D Converters *100 dB Dynamic Range D/A Converters *105 dB DAC Signal-to-Noise Ratio (EIAJ)**

***Differential Inputs / Outputs *On-chip Anti-aliasing and Output Smoothing Filters *De-emphasis for 32, 44.1 and 48 kHz**

***Supports Master and Slave Modes *Single +5 V power supply *On-Chip Crystal Oscillator *3 - 5 V Digital Interface**

ANALOG CHARACTERISTICS (T_A = 25° C; VA, VD = +5 V; Full Scale Input Sine wave, 997 Hz; Fs = 48 kHz; Measurement Bandwidth is 20 Hz to 20 kHz; Local components as shown in Figures 4 and 5; SPI® mode, Format 0, unless otherwise specified.)

Parameter	Symbol	6880 Min	6880 Typ	6880 Max	Unit
Analog Input Characteristics					
ADC Resolution		-	-	24	Bits
Total Harmonic Distortion	THD	-	0.003	-	%
Dynamic Range A-weighted unweighted		95 92	100 97	- -	dB
Total Harmonic Distortion + Noise (Note 1)	THD+N	-	-92	-87	dB
Interchannel Isolation (1 kHz)		-	90	-	dB
Interchannel Gain Mismatch		-	-	0.1	dB
Offset Error with High Pass Filter		-	-	0	LSB
Full Scale Input Voltage (Differential)		1.9	2.0	2.1	Vrms
Gain Drift		-	100	-	ppm/°C
Input Resistance		10	-	-	kΩ
Input Capacitance		-	-	15	pF
Common Mode Input Voltage		-	2.3	-	V
A/D Decimation Filter Characteristics					
Passband (Note 2)		0	-	21.8	kHz
Passband Ripple		-	-	±0.01	dB
Stopband (Note 2)		30	-	6114	kHz
Stopband Attenuation (Note 3)		80	-	-	dB
Group Delay (Fs = Output Sample Rate) (Note 4)	t_{gd}	-	15/Fs	-	s
Group Delay Variation vs. Frequency	Δt_{gd}	-	-	0	µs
High Pass Filter Characteristics					
Frequency Response -3 dB (Note 2) -0.1 dB		- -	3.7 20	- -	Hz
Phase Deviation @ 20 Hz (Note 2)		-	10	-	Degree
Passband Ripple		-	-	0	dB

Notes:
1. Referenced to typical full-scale differential input voltage (2 Vrms).
2. Filter characteristics scale with output sample rate. For output sample rates, Fs, other than 48 kHz, the 0.01 dB passband edge is 0.4535x Fs and the stopband edge is 0.625x Fs.
3. The analog modulator samples the input at 6.144 MHz for an Fs equal to 48 kHz. There is no rejection of input signals which are multiples of the sampling frequency (n x 6.144 MHz ±21.8 kHz where n = 0,1,2,3...).
4. Group delay for Fs = 48 kHz, t_{gd} = 15/48 kHz = 312 µs.

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ANALOG CHARACTERISTICS (CONTINUED)

Parameter	Symbol	6880 Min	6880 Typ	6880 Max	Unit
Analog Output Characteristics - Minimum Attenuation, 10 kΩ, 100 pF load; unless otherwise specified.					
DAC Resolution		-	-	24	Bits
Signal-to-Noise, Idle-Channel Noise (CS4221 only) DAC muted, A-weighted		97	105	-	dB
Dynamic Range DAC not muted, A-weighted DAC not muted, unweighted		95 92	100 97	- -	dB
Total Harmonic Distortion	THD	-	0.003	-	%
Total Harmonic Distortion + Noise	THD+N	-	-92	-87	dB
Interchannel Isolation (1 kHz)		-	90	-	dB
Interchannel Gain Mismatch		-	-	0.1	dB
Attenuation Step Size All Outputs		0.35	0.5	0.65	dB
Programmable Output Attenuation Span		110	113.5	-	dB
Differential Offset Voltage		-	±10	-	mV
Common Mode Output Voltage		-	2.4	-	V
Full Scale Output Voltage		1.8	1.9	2.0	Vrms
Gain Drift		-	100	-	ppm/°C
Out-of-Band Energy Fs/2 to 2 Fs		-	-60	-	dBFs
Analog Output Load Resistance Capacitance		10 -	- -	- 100	kΩ pF
Combined Digital and Analog Filter Characteristics					
Frequency Response10 Hz to 20 kHz		-	±0.1	-	dB
Deviation from Linear Phase		-	±0.5	-	Degree
Passband: to 0.01 dB corner (Notes 5 and 6)		0	-	21.8	kHz
Passband Ripple (Note 6)		-	-	±0.01	dB
Stopband (Notes 5 and 6)		26.2	-	-	kHz
Stopband Attenuation (Note 7)		70	-	-	dB
Group Delay (Fs = Input Word Rate)	t_{gd}	-	16/Fs	-	s
Power Supply					
Power Supply Current VA VD VL Total Power Down		- - - -	46 9 3 0.4	60 20 5 -	mA
Power Supply Rejection Ratio 1 kHz		-	65	-	dB

Notes:
5. The passband and stopband edges scale with frequency. For input word rates, Fs, other than 48 kHz, the 0.01 dB passband edge is 0.4535x Fs and the stopband edge is 0.5465x Fs.
6. Digital filter characteristics.
7. Measurement bandwidth is 10 Hz to 3 Fs.

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DIGITAL CHARACTERISTICS (T_A = 25° C; VA, VD = 4.75V - 5.25V)

Parameter		Symbol	Min	Max	Unit
High-level Input Voltage	VL = 5V VL = 3V	V_{IH} V_{IH}	2.8 2.0	VL + 0.3 VL + 0.3	V V
Low-level Input Voltage		V_{IL}	-0.3	0.8	V
High-level Output Voltage at I_O = -2.0 mA		V_{OH}	VL - 1.0	-	V
Low-level Output Voltage at I_O = 2.0 mA		V_{OL}	-	0.5	V
Input Leakage Current	Digital Inputs		-	10	µA
Output Leakage Current	High Impedance Digital Outputs		-	10	µA

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0 V, all voltages with respect to 0 V.)

Parameter		Symbol	Min	Max	Unit
Power Supplies	Digital Analog	VD VA	-0.3 -0.3	6.0 6.0	V
Input Current	(Note 8)		-	±10	mA
Analog Input Voltage	(Note 9)		-0.7	VA + 0.7	V
Digital Input Voltage	(Note 9)		-0.7	VD + 0.7	V
Ambient Temperature	Power Applied		-55	+125	°C
Storage Temperature			-65	+150	°C

RECOMMENDED OPERATING CONDITIONS

(AGND, DGND = 0 V, all voltages with respect to 0 V.)

Parameter		Symbol	Min	Typ	Max	Unit
Power Supplies	Digital Analog Digital | VA - VD |	VD VA VL	4.75 4.75 2.7 -	5.0 5.0 5.0 -	5.25 5.25 5.25 0.4	V
Ambient Operating Temperature		T_A	-10	25	70	°C

Notes: 8. Any pin except supplies. Transient currents of up to 100 mA on the analog input pins will not cause SCR latch-up.

9. The maximum over or under voltage is limited by the input current.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

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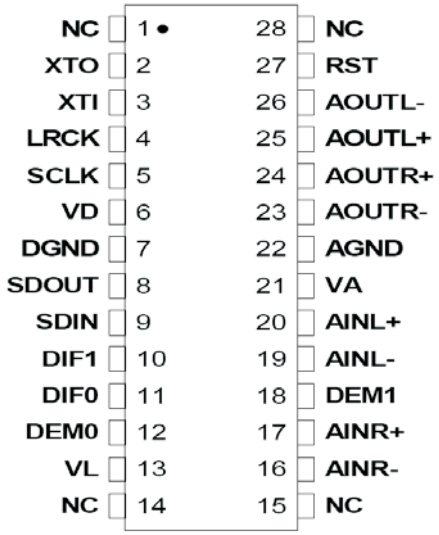
Pin Connection Description



NC	1,14,15, 28	**No Connect** - These pins are not connected internally and should be tied to DGND to minimize noise coupling.
XTI, XTO	2,3	**Crystal Connections (*Input/Output*)** - Input and output connections for the crystal used to clock the CS4220. Alternatively, a clock may be input into XTI. This is the clock source for the delta-sigma modulator and digital filters. The frequency of this clock must be either 256x, 384x, or 512x Fs in Slave Mode and 256x in Master Mode.

Fs (kHz)	XTI (MHz)		
	256x	384x	512x
32	8.1920	12.2880	16.3840
44.1	11.2896	16.9344	22.5792
48	12.2880	18.4320	24.5760

LRCK	4	**Left/Right Clock (*Input*)** - Determines which channel is currently being input/output of the serial audio data pins SDIN/SDOUT. The frequency of the Left/Right clock must be equal to the input sample rate. Although the outputs for each ADC channel are transmitted at different times, Left/Right pairs represent simultaneously sampled analog inputs. The required relationship between the left/right clock, serial clock and serial data is defined by the DIF1-0 pins.
SCLK	5	**Serial Data Clock (*Input*)** - Clocks the individual bits of the serial data into the SDIN pin and out of the SDOUT pin. The required relationship between the left/right clock, serial clock and serial data is defined by the DIF1-0 pins.
VD	6	**Digital Power (*Input*)** - Positive power supply for the digital section. Typically 5.0 VDC.
DGND	7	**Digital Ground (*Input*)** - Digital ground for the digital section.
SDOUT	8	**Serial Data Output (*Output*)** - Two's complement MSB-first serial data is output on this pin. The required relationship between the left/right clock, serial clock and serial data is defined by the DIF1-0 pins.
SDIN	9	**Serial Data Input (*Input*)** - Two's complement MSB-first serial data is input on this pin. The required relationship between the left/right clock, serial clock and serial data is defined by the DIF1-0 pins.

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DIF0, DIF1	10,11	**Digital Interface Format (*Input*)** - The required relationship between the left/right clock, serial clock and serial data is defined by the Digital Interface Format.

DIF1	DIF0	DESCRIPTION	FORMAT	FIGURE
0	0	I^2S, up to 24-bit data	0	8
0	1	Left Justified, up to 24-bit data	1	9
1	0	Right Justified, 24-bit Data	2	10
1	1	Right Justified, 20-bit Data	3	11

DEM0, DEM1	12,18	**De-Emphasis Select (*Input*)** - Controls the activation of the standard 50/15 µs de-emphasis filter. 32, 44.1, or 48 kHz sample rate selection defined in Table

DEM0	DEM1	De-Emphasis
0	0	32 kHz
0	1	44.1 kHz
1	0	48 kHz
1	1	Disabled

VL	13	**Digital Logic Power (*Input*) -** Positive power supply for the digital interface section. Typically 3.0 to 5.0 VDC.
AINR-, AINR+	16,17	**Differential Right Channel Analog Input (*Input*)** - The full scale analog input level (differential) is specified in the Analog Characteristics specification table and may be AC coupled or DC coupled into the device.
AINL-, AINL+	19,20	**Differential Left Channel Analog Input (*Input*)** - The full scale analog input level (differential) is specified in the Analog Characteristics specification table and may be AC coupled or DC coupled into the device.
VA	21	**Analog Power (*Input*)** - Positive power supply for the analog section. Nominally +5 Volts.
AGND	22	**Analog Ground (*Input*)** - Analog ground reference.
AOUTR-, AOUTR+	23, 24	**Differential Right Channel Analog Output (*Output*) -** The full scale analog output level (differential) is specified in the Analog Characteristics specification table.
AOUTL-, AOUTL+	25, 26	**Differential Left Channel Analog Output (*Output*) -** The full scale analog output level (differential) is specified in the Analog Characteristics specification table.
$\overline{\text{RST}}$	27	**Reset (*Input*)** - When low, the device enters a low power mode and all internal registers are reset, including the control port. When high, the control port becomes operational and normal operation will occur.

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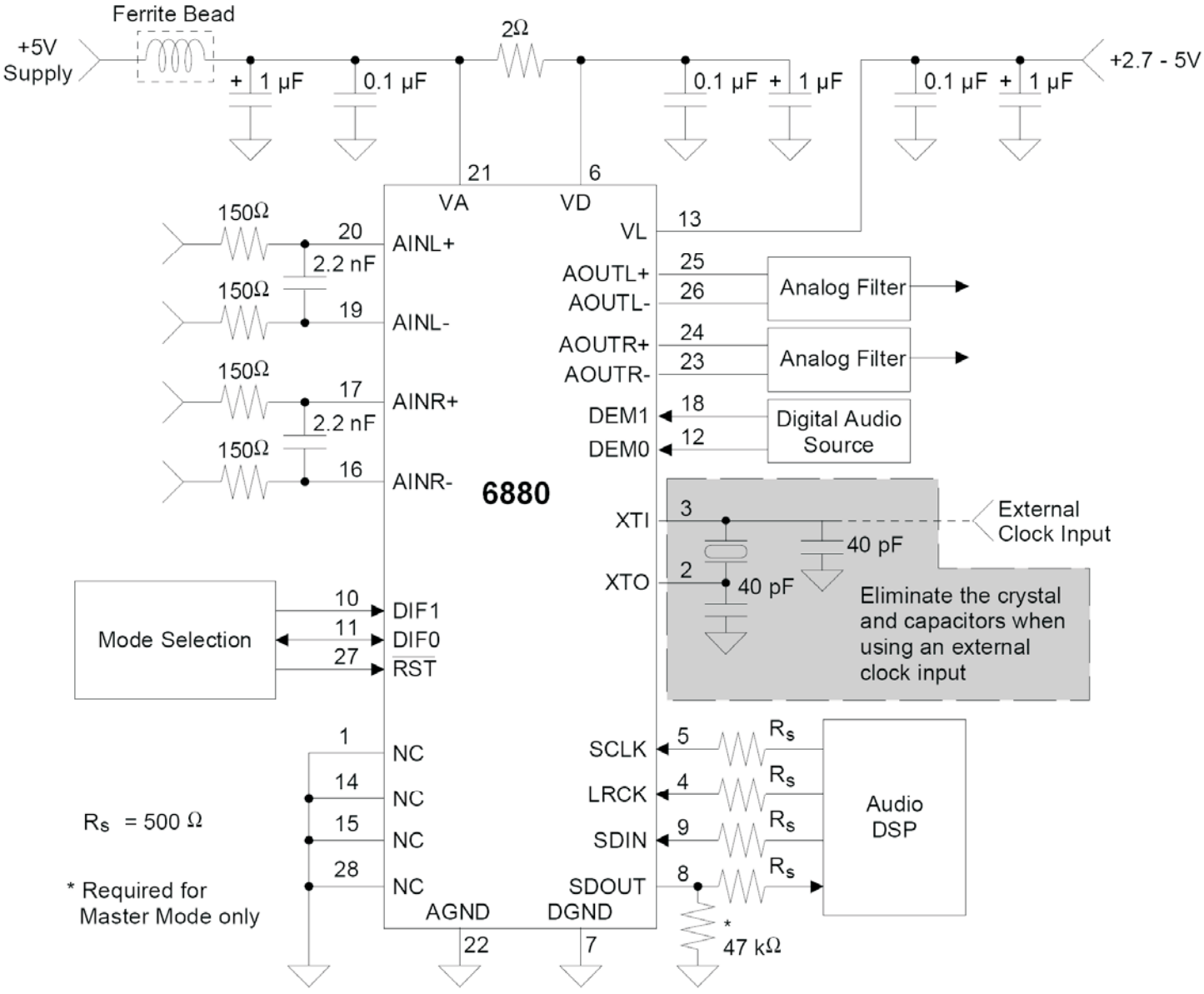

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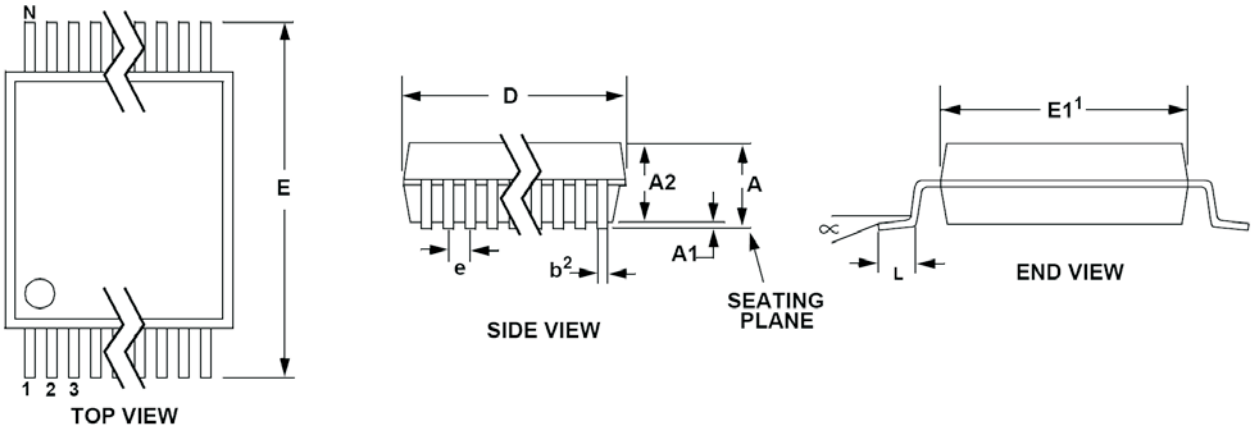
Package Dimensions

28L SSOP PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.084	--	--	2.13	
A1	0.002	0.006	0.010	0.05	0.15	0.25	
A2	0.064	0.069	0.074	1.62	1.75	1.88	
b	0.009	--	0.015	0.22	--	0.38	2,3
D	0.390	0.4015	0.413	9.90	10.20	10.50	1
E	0.291	0.307	0.323	7.40	7.80	8.20	
E1	0.197	0.209	0.220	5.00	5.30	5.60	1
e	0.022	0.026	0.030	0.55	0.65	0.75	
L	0.025	0.0354	0.041	0.63	0.90	1.03	
∝	0°	4°	8°	0°	4°	8°	

JEDEC #: MO-150

Controlling Dimension is Millimeters

Notes:
1. "D" and "E1" are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.
2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.
3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

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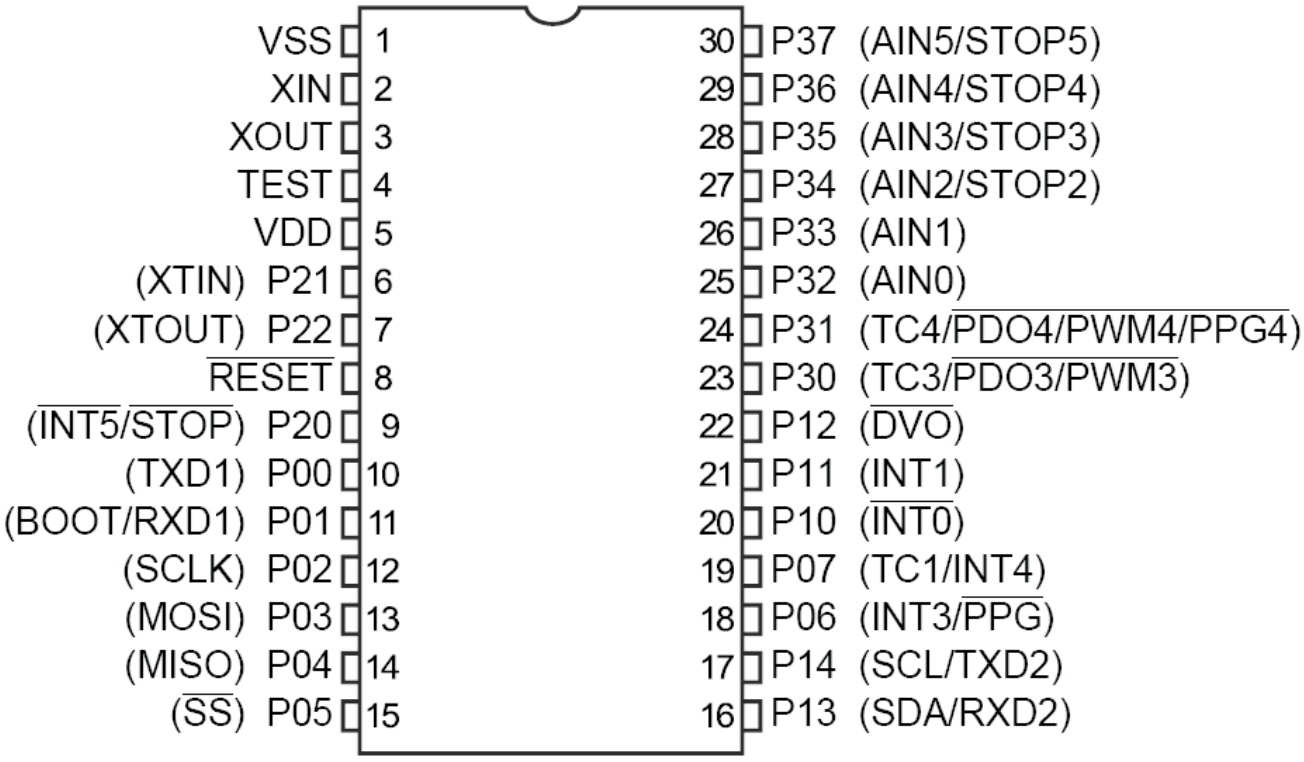
MCU CHIP

Pin Assignment



7F., No.578, Ruiguang Rd., Neihu Dist., Taipei City 11492, Taiwan
E-mail : info@trigaudio.com Tel : +886-2-7721-5586 ext.21~25 Fax : +886-2-7721-5867
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Pin Names and Functions

Pin Name	Pin Number	Input/Output	Functions
P07 TC1 INT4	19	IO I I	PORT07 TC1 input External interrupt 4 input
P06 INT3 $\overline{PPG}$	18	IO I O	PORT06 External interrupt 3 input PPG output
P05 $\overline{SS}$	15	IO I	PORT05 SEI master/slave select input
P04 MISO	14	IO IO	PORT04 SEI master input, slave output
P03 MOSI	13	IO IO	PORT03 SEI master input, slave output
P02 SCLK	12	IO IO	PORT02 SEI serial clock input/output pin
P01 RXD1 BOOT	11	IO I I	PORT01 UART data input 1 Serial PROM mode control input
P00 TXD1	10	IO O	PORT00 UART data output 1
P14 SCL TXD2	17	IO IO O	PORT14 I2C bus clock UART data output 2
P13 SDA RXD2	16	IO IO I	PORT13 I2C bus data UART data input 2
P12 $\overline{DVO}$	22	IO O	PORT12 Divider Output
P11 INT1	21	IO I	PORT11 External interrupt 1 input
P10 $\overline{INT0}$	20	IO I	PORT10 External interrupt 0 input
P22 XTOUT	7	IO O	PORT22 Resonator connecting pins(32.768kHz) for inputting external clock
P21 XTIN	6	IO I	PORT21 Resonator connecting pins(32.768kHz) for inputting external clock
P20 $\overline{STOP}$ $\overline{INT5}$	9	IO I I	PORT20 STOP mode release signal input External interrupt 5 input

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Pin Name	Pin Number	Input/Output	Functions
P37 AIN5 STOP5	30	IO I I	PORT37 Analog Input5 STOP5
P36 AIN4 STOP4	29	IO I I	PORT36 Analog Input4 STOP4
P35 AIN3 STOP3	28	IO I I	PORT35 Analog Input3 STOP3
P34 AIN2 STOP2	27	IO I I	PORT34 Analog Input2 STOP2
P33 AIN1	26	IO I	PORT33 Analog Input1
P32 AIN0	25	IO I	PORT32 Analog Input0
P31 TC4 $\overline{\text{PDO4/PWM4/PPG4}}$	24	IO I O	PORT31 TC4 input PDO4/PWM4/PPG4 output
P30 TC3 $\overline{\text{PDO3/PWM3}}$	23	IO I O	PORT30 TC3 input PDO3/PWM3 output
XIN	2	I	Resonator connecting pins for high-frequency clock
XOUT	3	O	Resonator connecting pins for high-frequency clock
$\overline{\text{RESET}}$	8	I	Reset signal
TEST	4	I	Test pin for out-going test. Normally, be fixed to low.
VDD	5	I	+5V
VSS	1	I	0(GND)

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DC Characteristics

(V_{SS} = 0 V, Topr = -40 to 85 °C)

Parameter	Symbol	Pins	Condition		Min	Typ.	Max	Unit
Hysteresis voltage	V_{HS}	Hysteresis input	V_{DD} = 5.0V		-	0.9	-	V
Input current	I_{IN1}	TEST	V_{DD} = 5.5 V, V_{IN} = 5.5 V/0 V		-	-	±2	μA
	I_{IN2}	Sink open drain, tri - state port						
	I_{IN3}	$\overline{RESET}$	V_{DD} = 5.5 V, V_{IN} = 5.5 V					
Input resistance	R_{IN1}	$\overline{RESET}$ pull - up	V_{DD} = 5.5 V, V_{IN} = 0 V		100	200	450	kΩ
	R_{IN2}	$\overline{PORT}$ pull - up	V_{DD} = 5.5 V, V_{IN} = 0 V		50	100	200	kΩ
Output leakage current	I_{LO0}	P0,P1,P2,P3	V_{DD} = 5.5 V, V_{OUT} = 5.3 V/0.2 V		-	-	±2	μA
Output high voltage	V_{OH}	P0,P1,P2,P3	V_{DD} = 4.5 V, I_{OH} = -0.7 mA		4.1	-	-	V
Output low voltage	V_{OL}	Except P0	V_{DD} = 4.5 V, I_{OL} = 1.6 mA		-	-	0.4	
Output low current	I_{OL}	High current port (P0 Port)	V_{DD} = 4.5 V, V_{OL} = 1.0 V		-	20	-	mA
Supply current in NORMAL1, 2 modes	I_{DD}		V_{DD} = 5.5 V V_{IN} = 5.3 V/0.2 V fc = 16 MHz fs = 32.768 kHz	When a program operates on flash memory (Note4,5)	-	12.5	20	mA
				When a program operates on RAM	-	7.5	14	
Supply current in IDLE 0, 1, 2 modes					-	5.5	9	
Supply current in SLOW1 mode			V_{DD} = 3.0 V V_{IN} = 2.8 V/0.2 V fs = 32.768 kHz	When a program operates on flash memory (Note4,5)	-	22	65	μA
				When a program operates on RAM (FLSSTB<FSTB>= 0)	-	21	30	
				When a program operates on RAM (FLSSTB<FSTB>= 1)	-	16	25	
Supply current in SLEEP1 mode					-	14	22	
Supply current in SLEEP0 mode					-	12	20	
Supply current in STOP mode			V_{DD} = 5.5 V V_{IN} = 5.3 V/0.2 V		-	10	20	
Peak current of inter-mittent operation (Note4,5)	I_{DDP-P}		V_{DD} = 5.5 V		-	10	-	mA
			V_{DD} = 3.0 V		-	2	-	

Note 1: Typical values show those at Topr = 25 C and VDD = 5 V.

Note 2: Input current (IIN3): The current through pull-up or pull-down resistor is not included.

Note 3: The supply currents of SLOW2 and SLEEP2 modes are equivalent to those of IDLE0, IDLE1 and IDLE2 modes.

Note 4: When a program is executing in the flash memory or when data is being read from the flash memory, the flash memory operates in an intermittent manner, causing peak currents in the operation current, as shown in Figure 21-1.In this case, the supply current IDD (in NORMAL1, NORMAL2 and SLOW1 modes) is defined as the sum of the average peak current and MCU current.

Note 5: When designing the power supply, make sure that peak currents can be supplied. In SLOW1 mode, the difference between the peak current and the average current becomes large.

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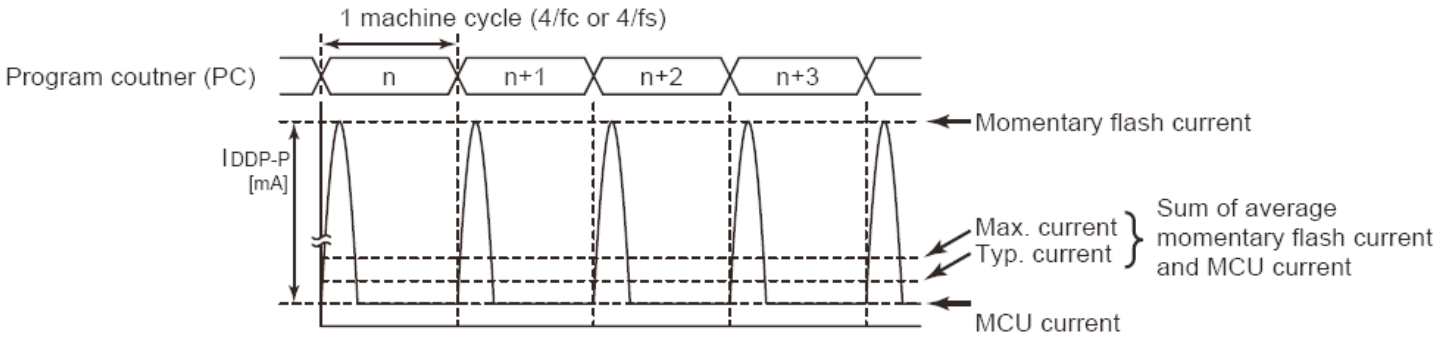

Figure 21-1 Intermittent Operation of Flash Memory

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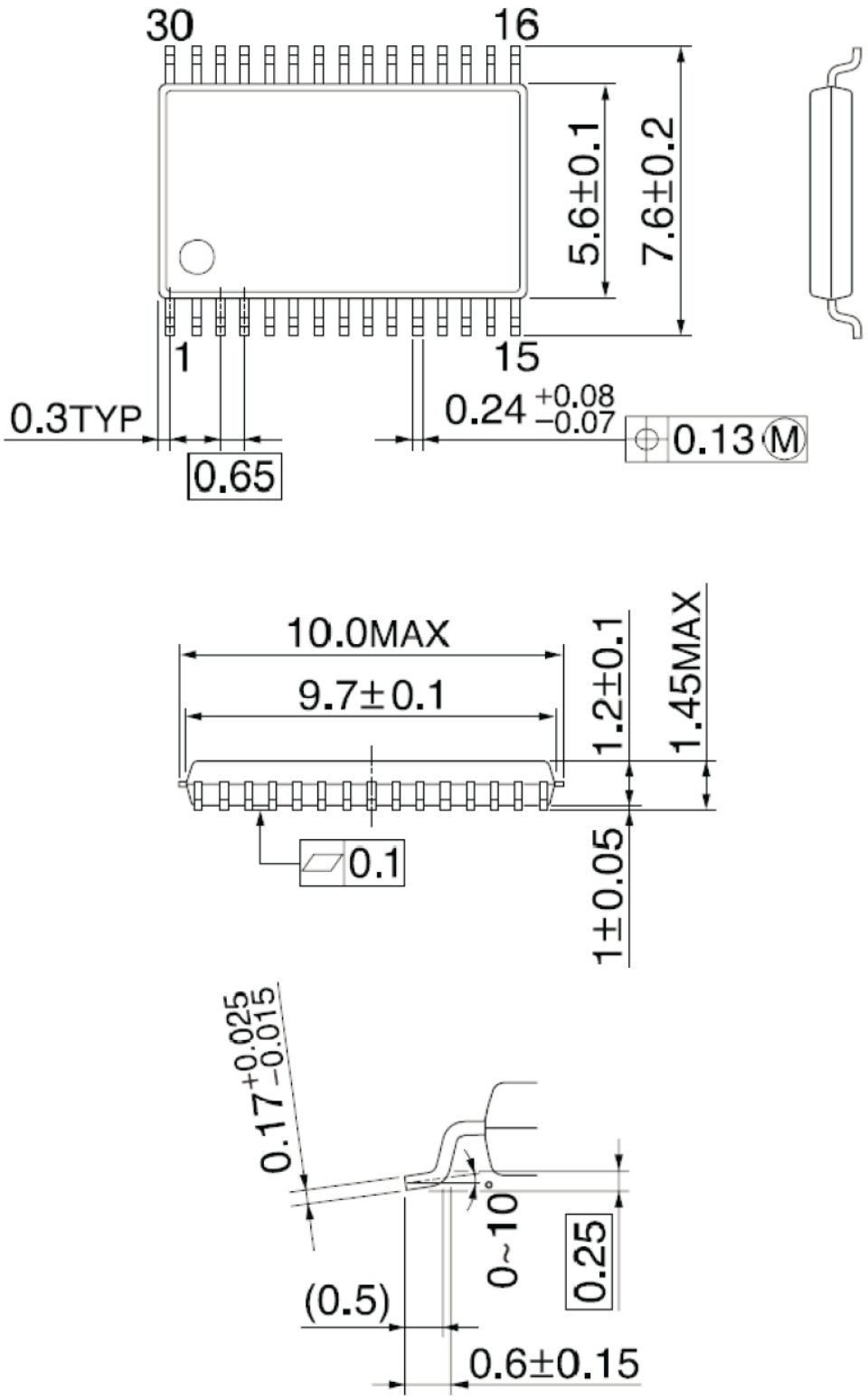
Package Dimensions

SSOP30-P-56-1.65 Rev 02 Unit : mm



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