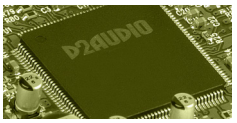
D2AUDIO D2-814xx DATA SHEET

DAE-1 for manufacturers of High-Performance Class-D Audio Amplifiers for use with D2Audio X-Series Reference Designs



PRELIMINARY

Complete Class-D Amplifier Controller SOC

- Digital switching controller
- Flexible audio input sources
- Multiple controller synchronization
- Bridge and Non-Bridged output topologies
- Stand-alone or micro-controller boot option
- 4 Channels

High-Performance Sound

- Unique performance for each part number
- Superior Dynamic Range
- >110 dB SNR, <0.1% THD+N
- 20Hz-20kHz +/-0.5dB frequency response

Graceful Protection and Recovery

- Complete short-circuit, over-current, and over-voltage fault protection

Pure Digital Path

- Digital audio inputs which support I^2S and Left-Justified formats with Linear PCM (32-192 kHz, 16-24-bit)
- Digital audio input which supports S/PDIF format with Linear PCM (32kHz-192kHz, 16-24 bit)

Multiple Part Offerings

- 144-pin LQFP, 4 channel PWM Controller with Integrated Digital Audio Engine with Full-Bridge or Half-Bridge Design Support intended for Ultra High-End Performance Reference Designs
- 128-pin LQFP, 4 channel PWM Controller with Integrated Digital Audio Engine with Full-Bridge or Half-Bridge Design Support intended for Mid-End Performance Reference Designs

System Control Support

- Reference Design Dependant

The D2Audio™ D2-814xx is a fully self-contained 4 channel digital amplifier controller System-On-Chip (SOC). The D2-814xx enables rapid system design for manufacturers of home theater receivers, multi-room distributed audio systems, and powered speakers.

The D2-814xx contains a high-performance digital switching controller to play any input source on any output channel.

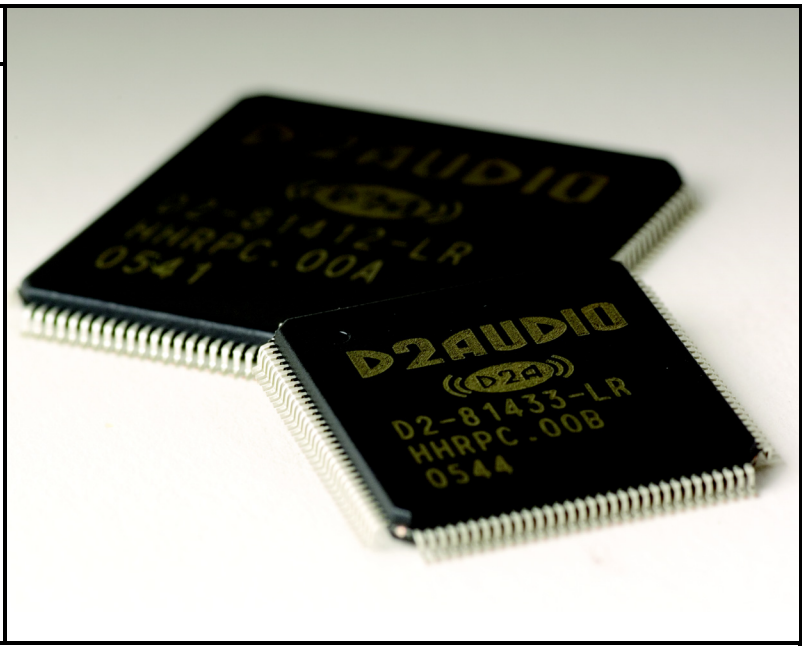
A configurable audio signal processor provides equalization, volume control, tone control, and compression for each channel, also crossover and power limiting for powered speaker applications

The D2-814xx includes 4-channels I^2S/Left-Justified inputs (16-24-bit, 32-192 kHz), optional S/PDIF receiver (16-24-bit).

Boot options include: Self-boot from external serial ROM, asynchronous SCI slave boot, and serial slave boot from host uCon.

D2AUDIO D2-814xx

- **Powerful Digital Audio Management - Reference Design Dependant SRC, Routing, Mixing, Multiple Digital Audio I/O, Tone Control, Parametric EQ, Compression**
- **Reduced Audio System Cost for manufacturers of Class-D Audio amplifiers**
- **Audio Processing features enable optimized speaker performance and delivers dramatically improved sound quality**
- **Minimum Development Cost/Risk/ Time-to-Market**
- **Pure Digital Path**
- **Superior Dynamic Range**
- **>110dB SNR, <0.1% THD+N**
- **20Hz - 20kHZ +/-0.5dB frequency response**



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Nuclear and Medical Applications

D2Audio products are not authorized for use as critical components in life support systems, equipment used in hazardous environments or nuclear control systems without the express written consent of D2Audio Corporation.

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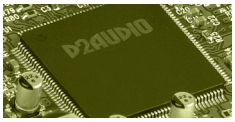
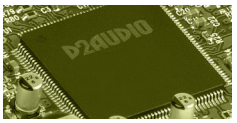


PRELIMINARY

PRELIMINARY

1 D2-814XX ARCHITECTURE



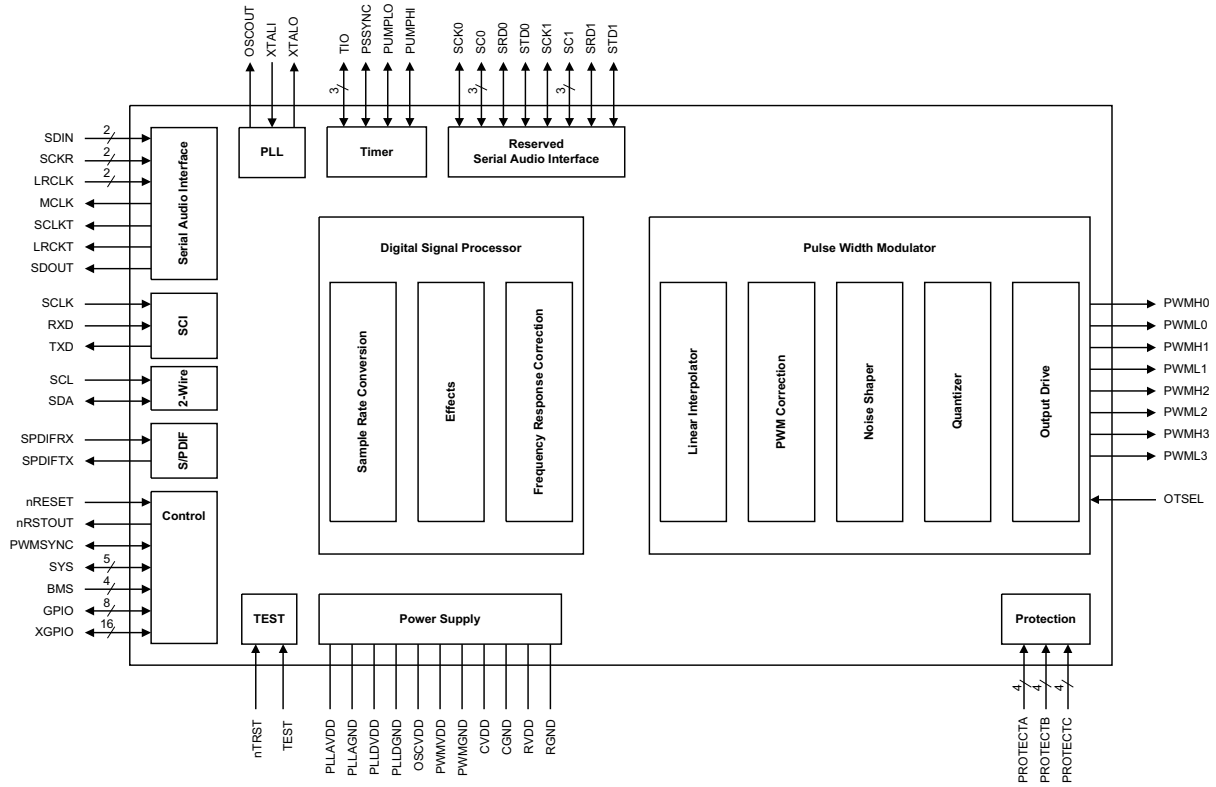


FIGURE 1: D2-814xx Block Diagram (144-pin package)

2 D2-814XX SIGNAL FLOW

The D2-814xx supports a wide variety of signal flows that are fully programmable and are reference design dependant. The D2-814xx IC is to only be used as part of a licensed Reference Design Platform (RDP) package from D2Audio Corporation. The designer should note that each Reference Design Platform (RDP) package has a set signal flow, which is handled by the specified firmware and associated performance level, which is determined primarily by the surrounding components used in the design. Please refer to the specific D2Audio Digital Amplifier Datasheet for the design-specific signal flows and corresponding register set.

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PRELIMINARY

3 SPECIFICATIONS

3.1 ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Supply Voltage RVDD, PWMVDD		-0.3	4.0	V
Supply Voltage CVDD, PLLAVDD, PLLDVDD, OSCVDD		-0.3	2.4	V
Input Voltage, any input but XTALI		-0.3	RVDD+0.3	V
Input Voltage XTALI		-0.3	OSCVDD+0.3	V
Input Current, any pin but supplies		-	+/-10	mA
Operating Temperature, note 1	T_{MAX}	-10	+85	°C
Junction Temperature, note 1	T_{JNC}	-	+125	°C
Storage Temperature, note 1	T_{STG}	-55	+150	°C
Note 1: For both 128-pin LQFP and 144-pin LQFP				

TABLE 1: Absolute Maximum Ratings

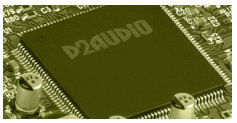
3.2 PIN CHARACTERISTICS

T_A=25 degrees C, CVDD=PLLAVDD=PLLDVDD=OSCVDD=1.8V +/-5%, RVDD=PWMVDD=3.3V +/-10%. All grounds at 0.0V. All voltages referenced to ground.

Parameter	Symbol	Min	Typ	Max	Unit
High Level Input Drive Voltage, note 1	V_{IH}	2.0	-	-	V
Low Level Input Drive Voltage, note 1	V_{IL}	-	-	0.8	V
High Level Output Drive Voltage, note 2 Iout = -Pad Drive	V_{OH}	RVDD - 0.3	-	-	V
Low Level Output Drive Voltage, note 2 Iout = +Pad drive	V_{OL}	-	-	0.3	V
High Level Input Drive Voltage, note 3	V_{IHX}	0.7	-	OSCVDD	V
Low Level Input Drive Voltage, note 3	V_{ILX}	-	-	0.3	V
High Level Output Drive Voltage OSCOUT pin	V_{OHO}	PLLDVDD - 0.3	-	-	V
Low Level Output Drive Voltage OSCOUT pin	V_{OLO}	-	-	0.3	V
Input Leakage Current	I_{IN}	-		+/- 10	uA
Input Capacitance	C_{IN}	-	9	-	pF
Output Capacitance	C_{OUT}	-	9	-	pF
Note 1: All input pins except XTALI Note 2: All digital output pins Note 3: For XTALI input overdrive operation only					

TABLE 2: Pin Characteristics

3.3 POWER REQUIREMENTS



Typical supply currents measured at T_A=25 degrees C, PLL at 300MHz, OSC at 27MHz, core running at 150MHz with typical audio data traffic. Minimum supply currents are measured in full power down configuration.

Parameter	Symbol	Min	Typ	Max	Unit
Core Supply Pins	CVDD	1.7	1.8	1.9	V
		0.01	300		mA
Digital I/O Pad Ring Supply Pins	RVDD	3.0	3.3	3.6	V
		0.01	10		mA
PWM I/O Pad Ring Supply Pins	PWMVDD	3.0	3.3	3.6	V
		0.01	5		mA
Analog Supply Pins (PLL)	PLLAVDD	1.7	1.8	1.9	V
		0.01	10		mA
	PLLDVDD	1.7	1.8	1.9	V
		0.01	2		mA
	OSCVDD	1.7	1.8	1.9	V
		0.01	4		mA

TABLE 3: Power Requirements

3.4 THERMAL CHARACTERISTICS

Package Type	Airflow	Theta J_a	Theta J_c	Unit
128-Pin LQFP	0	56.5	17.6	°C/W
	1 m/s	50.9		
	2 m/s	48.9		
144-Pin LQFP	0	59.1	17.8	°C/W
	1 m/s	52.8		
	2 m/s	50.5		

TABLE 4: Thermal Characteristics

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PRELIMINARY

3.5 SWITCHING CHARACTERISTICS - SERIAL AUDIO PORT

T_A = 25°C, CVDD=PLLAVDD=PLLDVDD=OSCVDD=1.8V +/-5%, RVDD=PWMVDD=3.3V +/-10%. All grounds at 0.0V. All voltages referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
t_cSCLK	SCKRx frequency - SCKR0, SCKR1			12.5	MHz
t_wSCLK	SCKRx pulse width (high and low) - SCKR0, SCKR1	40			ns
t_sLRCLK	LRCKRx setup to SCLK rising - LRCKR0, LRCKR1	20			ns
t_hLRCLK	LRCKRx hold from SCLK rising - LRCKR0, LRCKR1	20			ns
t_sSDI	SDINx setup to SCLK rising - SDIN0, SDIN1	20			ns
t_hSDI	SDINx hold from SCLK rising - SDIN0, SDIN1	20			ns
t_dSDO	SDOUTx delay from SCLK falling			20	ns

TABLE 5: Serial Audio Port Timing

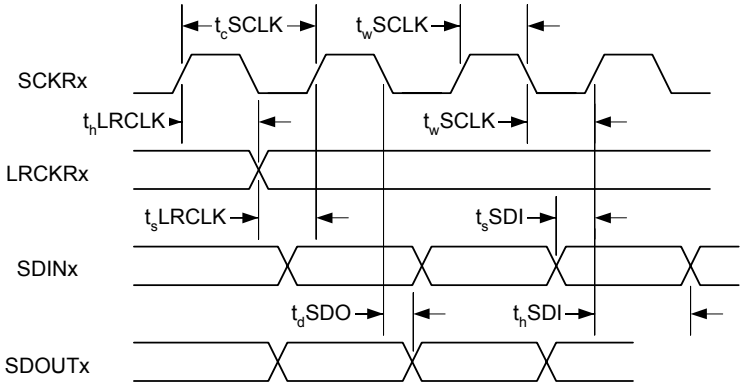


FIGURE 2: Serial Audio Port Timing

3.5.1 SERIAL AUDIO INTERFACE (SAI PORTS)

The D2-814xx IC contains one SAI port for each pair of channels. Each input can support an individually selectable sample rate from 32kHz to 192kHz. All digital audio inputs are 3.3V CMOS logic. The SAI port is designed to interface with standard digital audio components and to accept I^2S or Left-Justified data formats. Note: This port is entirely independent from the Reserved SAI port. The Reserved SAI port may or may not be used in a particular design.

For I^2S format, the left channel data is read when LRCK is low. For the Left-Justified format, the left channel data is read when LRCK is high. Either format requires data to be valid on the rising edge of SCLK and sent MSB-first on SDIN with 32 bits of data per channel. Each set of digital inputs runs asynchronously to the others and may accept different sample rates and formats.

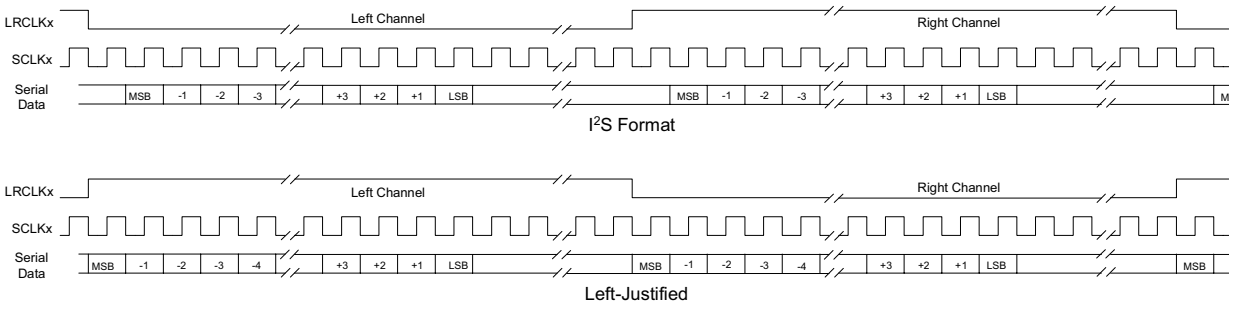
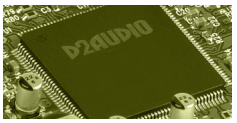


FIGURE 3: SAI port Data Formats

3.6 SWITCHING CHARACTERISTICS - 2-WIRE INTERFACE



T_A = 25°C, CVDD=PLLAVDD=PLLDVDD=OSCVDD=1.8V +/-5%, RVDD=PWMVDD=3.3V +/-10%. All grounds at 0.0V. All voltages referenced to ground.

Symbol	Description	Min	Max	Unit
fSCL	SCL frequency		100	kHz
t_{buf}	Bus free time between transmissions	4.7		us
t_{wlow}SCLx	SCL clock low	4.7		us
t_{whigh}SCLx	SCL clock high	4.0		us
t_sSTA	Setup time for a (repeated) Start	4.7		us
t_hSTA	Start condition Hold time	4.0		us
t_hSDAx	SDA hold from SCL falling (see note)	0		us
t_sSDAx	SDA setup time to SCL rising	250		ns
t_dSDAx	SDA output delay time from SCL falling		3.5	us
t_r	Rise time of both SDA and SCL		1	us
t_f	Fall time of both SDA and SCL		300	ns
t_sSTO	Setup time for a Stop condition	4.7		us
Note: Data must be held sufficient time to bridge the 300ns transition time of SCL				

TABLE 6: 2-Wire Interface Port Timing

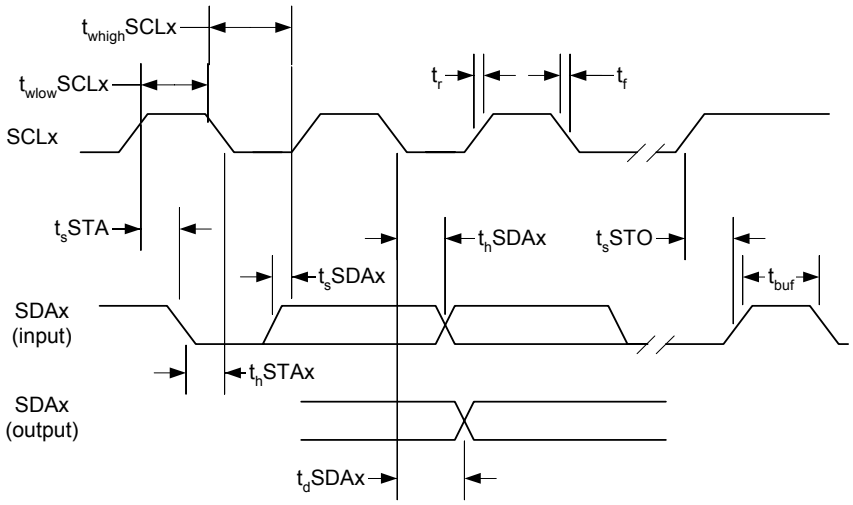


FIGURE 4: 2-Wire Interface Timing

PRELIMINARY

4 D2-814XX 128-PIN PACKAGE PINOUT

PRELIMINARY

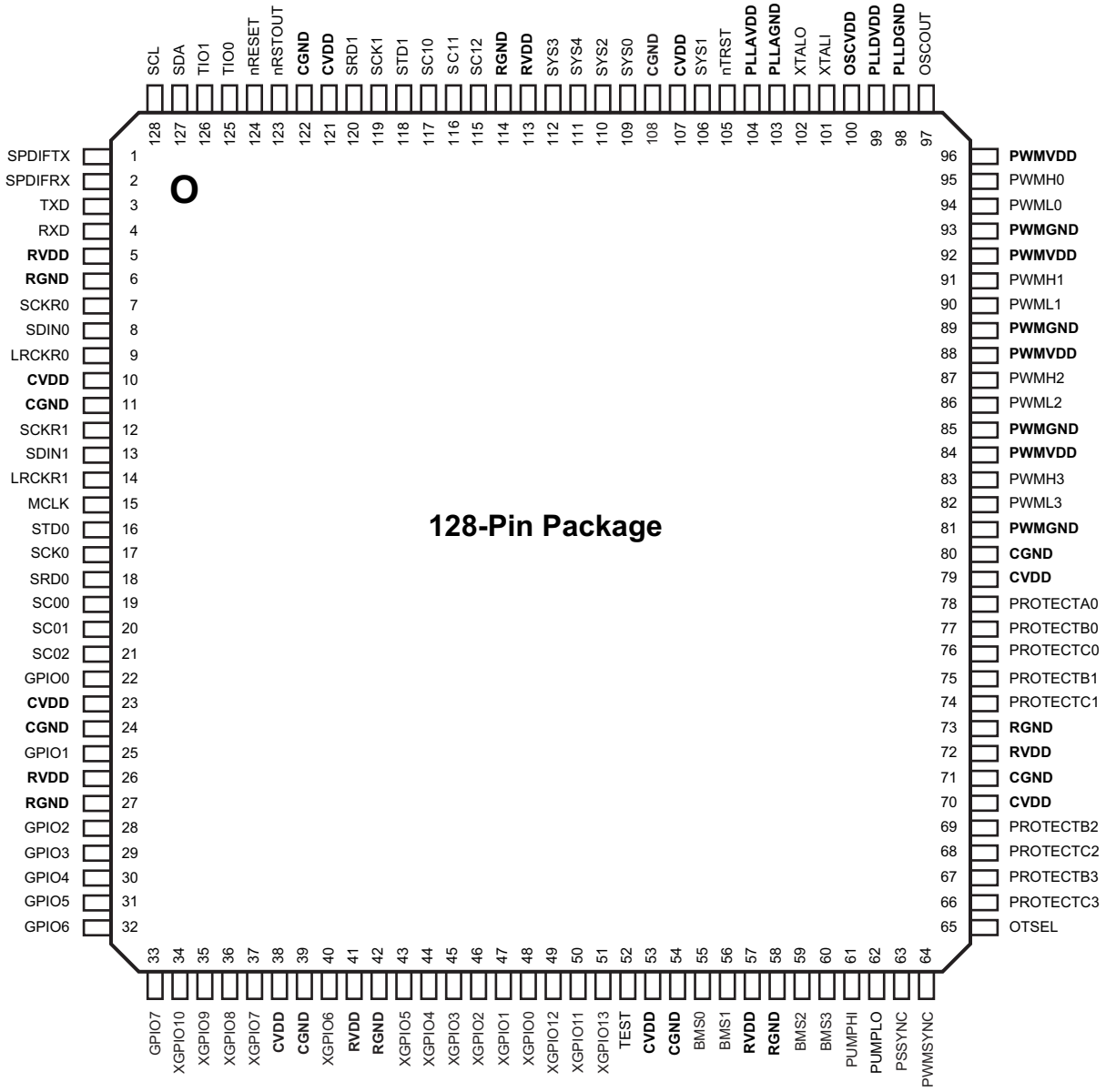
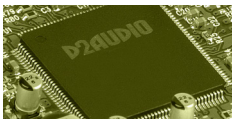


FIGURE 5: D2-814xx Pinout, 128-Pin LQFP Package

4.1 PIN DEFINITIONS, 128-PIN LQFP PACKAGE



PRELIMINARY

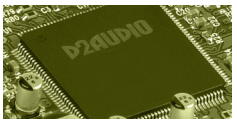
Serial Audio Interface (SAI) Pins			
Pin Number	**Port Name**	**Type**	**Description**
15	MCLK	Output	Master Clock
7	SCKR0	I/O	Serial Audio Bit Clock Receiver 0
9	LRCKR0	I/O	Serial Audio Left/Right Clock Receiver 0
8	SDIN0	Input	Serial Audio Data In 0
12	SCKR1	I/O	Serial Audio Bit Clock Receiver 1
14	LRCKR1	I/O	Serial Audio Left/Right Clock Receiver 1
13	SDIN1	Input	Serial Audio Data In 1
SPDIF Pins			
Pin Number	**Port Name**	**Type**	**Description**
1	SPDIFTX	Output	S/PDIF data output
2	SPDIFRX	Input	S/PDIF data input
PWM Pins			
Pin Number	**Port Name**	**Type**	**Description**
95	PWMH0	Output	Channel 0 PWM high side output
94	PWML0	Output	Channel 0 PWM low side output
91	PWMH1	Output	Channel 1 PWM high side output
90	PWML1	Output	Channel 1 PWM low side output
87	PWMH2	Output	Channel 2 PWM high side output
86	PWML2	Output	Channel 2 PWM low side output
83	PWMH3	Output	Channel 3 PWM high side output
82	PWML3	Output	Channel 3 PWM low side output
65	OTSEL	Input	Output topology select input
64	PWMSYNC	I/O	PWM Sync
2-Wire Serial Pins			
Pin Number	**Port Name**	**Type**	**Description**
128	SCL	I/O	Two wire serial clock
127	SDA	I/O	Two wire serial data
XGPIO Pins			
Pin Number	**Port Name**	**Type**	**Description**
34, 35, 36, 37, 40, 43, 44, 45, 46, 47, 48	XGPIO[10:0]	I/O	General purpose I/O
50	XGPIO[11]	I/O	
49	XGPIO[12]	I/O	
51	XGPIO[13]	I/O	
GPIO Pins			
Pin Number	**Port Name**	**Type**	**Description**
33, 32, 31, 30, 29, 28, 25, 22	GPIO[7:0]	I/O	General purpose I/O
Reset and Test Pins			
Pin Number	**Port Name**	**Type**	**Description**
124	nRESET	Input	Reset - active low
123	nRSTOUT	Output	Reset output- active low output
105	nTRST	Input	Test reset - active low
52	TEST	Input	Hardware test pin
Crystal Oscillator and PLL Pins			

TABLE 7: Pin Definitions Table, 128-Pin LQFP Package

PRELIMINARY

Pin Number	Port Name	Type	Description
97	OSCOUT	Output	Oscillator output to slave device
101	XTALI	Input	Crystal Oscillator input
102	XTALO	Output	Crystal Oscillator output
System Configuration Pins			
Pin Number	**Port Name**	**Type**	**Description**
109	SYS0	I/O	Reserved for factory test
106	SYS1	I/O	
110	SYS2	I/O	
112	SYS3	I/O	
111	SYS4	I/O	
Serial Communications Interface (SCI) Pins			
Pin Number	**Port Name**	**Type**	**Description**
4	RXD	I/O	SCI receive data
3	TXD	I/O	SCI transmit data
Reserved Serial Audio Interface Pins			
Pin Number	**Port Name**	**Type**	**Description**
16	STD0	I/O	Reserved Serial Audio Interface 0 Tx Data or GPIO
17	SCK0	I/O	Reserved Serial Audio Interface 0 Clock or GPIO
18	SRD0	I/O	Reserved Serial Audio Interface 0 Rx Data or GPIO
19	SC00	I/O	Reserved Serial Audio Interface 0 Control 0 or GPIO
20	SC01	I/O	Reserved Serial Audio Interface 0 Control 1 or GPIO
21	SC02	I/O	Reserved Serial Audio Interface 0 Control 2 or GPIO
118	STD1	I/O	Reserved Serial Audio Interface 1 Tx Data or GPIO
119	SCK1	I/O	Reserved Serial Audio Interface 1 Clock or GPIO
120	SRD1	I/O	Reserved Serial Audio Interface 1 Rx Data or GPIO
117	SC10	I/O	Reserved Serial Audio Interface 1 Control 0 or GPIO
116	SC11	I/O	Reserved Serial Audio Interface 1 Control 1 or GPIO
115	SC12	I/O	Reserved Serial Audio Interface 1 Control 2 or GPIO
Boot Mode Select Pins			
Pin Number	**Port Name**	**Type**	**Description**
55	BMS0	Input	Boot Mode Select 0
56	BMS1	Input	Boot Mode Select 1
59	BMS2	Input	Boot Mode Select 2
60	BMS3	Input	Boot Mode Select 3
Timer (TIO) Pins			
Pin Number	**Port Name**	**Type**	**Description**
126, 125	TIO[1:0]	I/O	Timer I/O ports
61	PUMPHI	I/O	Power supply pump control, high side or GPIO
62	PUMPLO	I/O	Power supply pump control, low side or GPIO
63	PSSYNC	I/O	Power supply synchronization or GPIO
PWM Protection Pins			
Pin Number	**Port Name**	**Type**	**Description**
78	PROTECTA0	I/O	PWM Temperature status input, or GPIO
67, 69, 75, 77	PROTECTB[3:0]	I/O	PWM Over Current Protection inputs, or GPIO
66, 68, 74, 76	PROTECTC[3:0]	I/O	PWM Shoot Through Current inputs or GPIO
Power Pins			

TABLE 7: Pin Definitions Table, 128-Pin LQFP Package (Continued)



Pin Number	Port Name	Type	Description
104	PLLAVDD	Power	PLL Analog power
103	PLLAGND	Ground	PLL Analog ground
99	PLLDVDD	Power	PLL Digital power
98	PLLDGND	Ground	PLL Digital ground
100	OSCVDD	Power	Oscillator power
121, 107, 79, 70, 53, 38, 23, 10,	CVDD	Power	Core power - 8 pins
122, 108, 80, 71, 54, 39, 24, 11	CGND	Ground	Core ground - 8 pins
96, 92, 88, 84	PWMVDD	Power	PWM output pin power - 4 pins
93, 89, 85, 81	PWMGND	Ground	PWM output pin ground - 4 pins
113, 72, 57, 41, 26, 5	RVDD	Power	Digital pad ring power - 6 pins
114, 73, 58, 42, 27, 6	RGND	Ground	Digital pad ring ground - 6 pins

TABLE 7: Pin Definitions Table, 128-Pin LQFP Package (Continued)

PRELIMINARY

4.2 PIN DESCRIPTIONS 128-PIN PACKAGE

Pins are 100% firmware and Reference Design Platform (RDP) Package dependent for their functionality. Output pins have one of 3 drive strengths - 4mA, 8mA, or 16mA. These strengths are characterized by the current that the pin will source or sink at the specified output voltage level.

PRELIMINARY

4.2.1 SERIAL AUDIO INTERFACE (SAI) PINS

MCLK — **Master Clock Output**
Master Clock output for external ADC/DAC components with 8mA drive strength. Pin drives low on reset. MCLK is also used by test hardware to monitor various internal clocks.

SCKR0 — **SAI Receiver Bit Clock 1**
SAI Receiver 0 bit clock is an output when D2-814xx is a master, or an input when D2-814xx is a slave. Defaults to an input on reset. Output has 4mA drive strength. Input has hysteresis.

LRCKR0 — **SAI Receiver Left/Right Clock 0**
SAI Receiver 0 left/right audio frame clock is an output when D2-814xx is a master or an input when D2-814xx is a slave. Defaults to an input on reset. Output has 4mA drive strength. Input has hysteresis.

SDIN0 — **SAI Receiver Serial Data Input 0**
SAI Receiver 0 data input.

SCKR1 — **SAI Receiver Bit Clock 1**
SAI Receiver 1 bit clock is an output when D2-814xx is a master, or an input when D2-814xx is a slave. Defaults to an input on reset. Output has 4mA drive strength. Input has hysteresis.

LRCKR1 — **SAI Receiver Left/Right Clock 1**
SAI Receiver 1 left/right audio frame clock is an output when D2-814xx is a master or an input when D2-814xx is a slave. Defaults to an input on reset. Output has 4mA drive strength. Input has hysteresis.

SDIN1 — **SAI Receiver Serial Data Input 1**
SAI Receiver 1 data input.

4.2.2 S/PDIF PINS

SPDIFRX — **S/PDIF Data Input**
This pin is the S/PDIF audio input and accepts a 3.3V stereo input up to 192kHz. To drive this pin, appropriate buffer and/or isolation circuits may be necessary to convert the S/PDIF cable input signal to clean logic levels.

SPDIFTX — **S/PDIF Data Output**
This pin is the S/PDIF audio output and drives a 3.3V stereo output up to 192kHz.

4.2.3 PWM PINS

PWMxH — **PWM High Side Driver Outputs**
PWM high side driver outputs, where x is 0 to 3, with 16mA drive strength. Pin drives to state determined by OTSEL on reset.

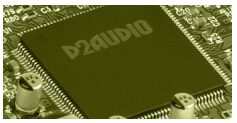
PWMxL — **PWM Low Side Driver Outputs**
PWM low side driver outputs, where x is 0 to 3, with 16mA drive strength. Pin drives low on reset.

OTSEL — **Output Topology Select Input**
Output topology select input. OTSEL pin state controls the PWMxH drive polarity. Typically, OTSEL will be tied either high for active-low PWMxH FET drivers, or tied low for active-high PWMxH FET drivers.

PWMSYNC — **PWM Synchronization**
PWM synchronization port with 4mA drive. Used in multi-D2-814xx configurations to synchronize the PWM controllers. The master D2-814xx will drive synchronization data to the slave D2-814xx(s), thus the pin will be an output on the master D2-814xx and an input on the slave D2-814xx(s). Pin floats on reset.

4.2.4 2-WIRE SERIAL PINS

SCL — **Serial Clock**
Two-Wire Serial clock port, open drain driver with 4mA drive strength. Bidirectional signal is used by both the master and slave controllers for clock signaling.



SDA — **Serial Data**
Two-Wire Serial data port, open drain driver with 4mA drive strength. Bidirectional signal used by both the master and slave controllers for data transport.

4.2.5 XGPIO PINS

XGPIO[10:0] — **General Purpose I/O**
Bidirectional GPIO port with 4mA driver. Resets to input port.

XGPIO[11] — **General Purpose I/O**
Bidirectional GPIO port with 4mA driver. Resets to input port.

XGPIO[12] — **General Purpose I/O**
Bidirectional GPIO port with 4mA driver. Resets to input port.

XGPIO[13] — **General Purpose I/O**
Bidirectional GPIO port with 4mA driver. Resets to input port.

4.2.6 RESET AND TEST PINS

nRESET — **System Reset Input**
Active low reset input with hysteresis. Low level activates system level reset, initializing all internal logic and program operations. System latches boot mode selection on the IRQ input pins on the rising edge.

nRSTOUT — **System Reset Output**
Active low reset output with 4mA driver. Pin drives low on any of POR output, 3.3V brown out detector, 1.8V brown out detector.

TEST — **Test Mode Input**
Hardware test mode control. For D2Audio usage only. Must be tied low.

nTRST — **Test Reset Input**
Active low test port reset. Low level activates test reset, initializing test hardware. Must be driven low with nRESET.

4.2.7 CRYSTAL OSCILLATOR AND PLL PINS

OSCOUT — **Oscillator Output**
Analog oscillator output to slave D2-814xx devices. On reset, OSCOUT drives a buffered version of the crystal oscillator signal from the XTALI pin. May be turned off by program control.

XTALI — **Crystal Oscillator Input**
Crystal oscillator analog input port. An external clock source would be driven into the this port. In multi-D2-814xx systems, the OSCOUT from the master D2-814xx would drive the XTALI pin.

XTALO — **Crystal Oscillator Output**
Crystal oscillator analog output port. When using an external clock source, this pin must be open.

4.2.8 GPIO PINS

GPIO[7:0] — **General Purpose I/O**
Bidirectional GPIO ports with 4mA driver. Resets to input ports.

4.2.9 SYSTEM CONFIGURATION PINS

SYS0 — **System Configuration Data 0**
Reserved for factory test. Tie low with 10k ohm resistor.

SYS1 — **System Configuration Data 1**
Reserved for factory test. Tie high with 10k ohm resistor.

SYS2 — **System Configuration Data 2**
Reserved for factory test. Tie high with 10k ohm resistor.

SYS3 — **System Configuration Data 3**
Reserved for factory test. Tie high with 10k ohm resistor.

SYS4 — **System Configuration Data 4**
Reserved for factory test. Tie high with 10k ohm resistor.

PRELIMINARY

PRELIMINARY

4.2.10 SERIAL COMMUNICATIONS INTERFACE (SCI) PINS

RXD — **Receive Data**
Serial communications receiver data with 4mA drive. Resets to input port. May be configured to GPIO.

TXD — **Transmit Data**
Serial communications transmitter data with 4mA drive. Resets to input port. May be configured to GPIO.

4.2.11 OPTIONAL/RESERVED FUNCTION PINS

SCK0 — **Reserved Serial Audio Interface 0 Serial Clock**
Serial Audio Interface 0 serial clock port with 4mA driver and hysteresis receiver. Resets to input port. May be configured as GPIO.

SC00-SC02 — **Reserved Serial Audio Interface 0 Serial Control**
0 serial control port with 4mA driver. Resets to input port. May be configured as GPIO.

STD0 — **Reserved Serial Audio Interface 0 Serial Transmit Data**
Serial Audio Interface 0 serial transmit data port with 4mA driver. Resets to input port. May be configured as GPIO.

SRD0 — **Reserved Serial Audio Interface 0 Serial Receive Data**
Serial Audio Interface 0 serial receive data port with 4mA driver. Resets to input port. May be configured as GPIO.

SCK1 — **Reserved Serial Audio Interface 1 Serial Clock**
Serial Audio Interface 1 serial clock port with 4mA driver and hysteresis receiver. Resets to input port. May be configured
as GPIO.

SC10-SC12 — **Reserved Serial Audio Interface 1 Serial Control**
Serial Audio Interface 1 serial control port with 4mA driver. Resets to input port. May be configured as GPIO.

STD1 — **Reserved Serial Audio Interface 1 Serial Transmit Data**
Serial Audio Interface 1 serial transmit data port with 4mA driver. Resets to input port. May be configured as GPIO.

SRD1 — **Reserved Serial Audio Interface 1 Serial Receive Data**
Serial Audio Interface 1 serial receive data port with 4mA driver. Resets to input port. May be configured as GPIO.

4.2.12 BOOT MODE SELECT PINS

BMS[3:0] — **Boot Mode Select Inputs**
External boot mode select inputs. On nRESET deassertion, these pins provide the boot mode selection.

4.2.13 TIMER (TIO) PINS

TIO[1:0] — **Timer**
Timer I/O ports with 4mA driver. May be configured as GPIO.

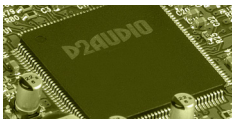
PUMPHI — **Power Supply Pump High**
High side power supply pump output with 16mA driver. May be configured as GPIO. Drives low on reset. Provides control means for operating an external switching power supply.

PUMPLO — **Power Supply Pump Low**
Low side power supply pump output with 16mA driver. May be configured as GPIO. Drives low on reset. Provides control means for operating an external switching power supply.

PSSYNC — **Power Supply Synchronization**
Switching power supply synchronization signal with 16mA driver. May be configured as GPIO. Resets to input port.

4.2.14 PWM PROTECTION PINS

PROTECTA0 — **PWM Temperature Protection Input**
PWM temperature protection input with hysteresis. May be configured as GPIO. In this instance, the GPIO pin has a 4mA driver.



PROTECTB[3:0] **PWM Over-Current Protection Inputs**

PWM over-current protection inputs with hysteresis. May be configured as GPIO. In this instance, the GPIO pins each have a 4mA driver. Each PWMOCP input is associated with the corresponding PWM driver channel.

PROTECTC[3:0] **PWM Shoot-Through Current Protection**

PWM shoot-through-current protection inputs with hysteresis. In this instance, the GPIO pins each have a 4mA driver. May be configured as GPIO. Each PWMSTC input is associated with the corresponding PWM driver channel.

4.2.15 POWER PINS

PLLAVDD/PLLAGND **PLL Analog power and ground**

PLL analog supply/return. This 1.8V supply is used for the jitter critical sections of the PLL.

PLLDVDD/PLLDGND **PLL Digital power and ground**

PLL digital supply/return. This 1.8V supply is used for the "dirty" sections of the PLL, and provides the pad supplies for all of the analog pads. Note that PLLDGND and CGND are connected through the substrate.

OSCVDD **Oscillator power**

Oscillator supply. This 1.8V supply is used for the crystal oscillator and oscillator bias circuits only.

CVDD/CGND **Core power and ground**

Core supply/return. This 1.8V supply is used in the chip interior logic and pad ring interfaces. There are 8 core supply pad pairs internally connected around the pad ring.

PWMVDD/PWMGND **PWM driver power and ground**

PWM I/O pad driver supply/return. This 3.3V supply is used for the PWM pad drivers only. There are 4 PWM internally connected supply pairs, one for each PWM data channel.

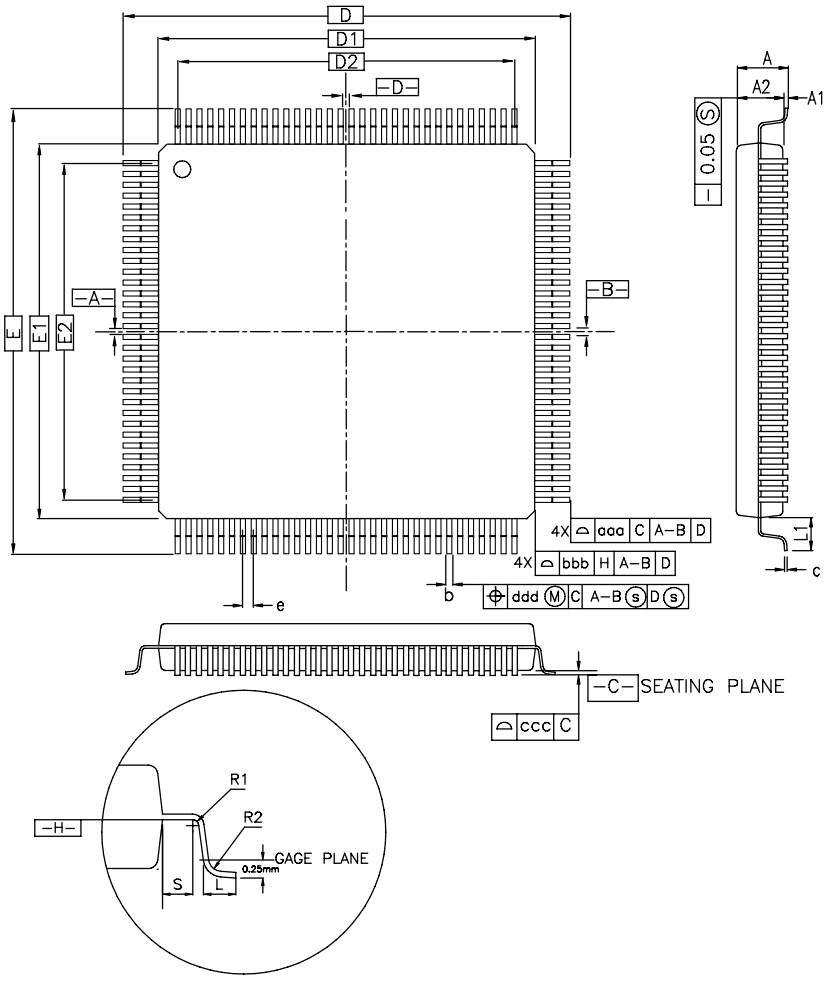
RVDD/RGND **Pad Ring power and ground**

Ring I/O pad driver supply/return. This 3.3V supply is used for all the digital I/O pad drivers and receivers except for the PWM and analog pads. There are 6 ring supply pairs internally connected around the pad ring.

PRELIMINARY

5 PHYSICAL DIMENSIONS 128-PIN PACKAGE

PRELIMINARY

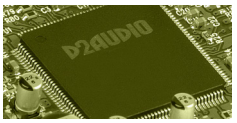


CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	16.00 BSC.			0.630 BSC.		
D1	14.00 BSC.			0.551 BSC.		
D2	12.40			0.488		
E	16.00 BSC.			0.630 BSC.		
E1	14.00 BSC.			0.551 BSC.		
E2	12.40			0.488		
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
b	0.13	0.16	0.23	0.005	0.006	0.009
c	0.09	—	0.20	0.004	—	0.008
e	0.40 BSC.			0.016 BSC.		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003		

FIGURE 6: D2-814xx Package Dimensions, 128-Pin Package

6 D2-814XX 144-PIN PACKAGE PINOUT



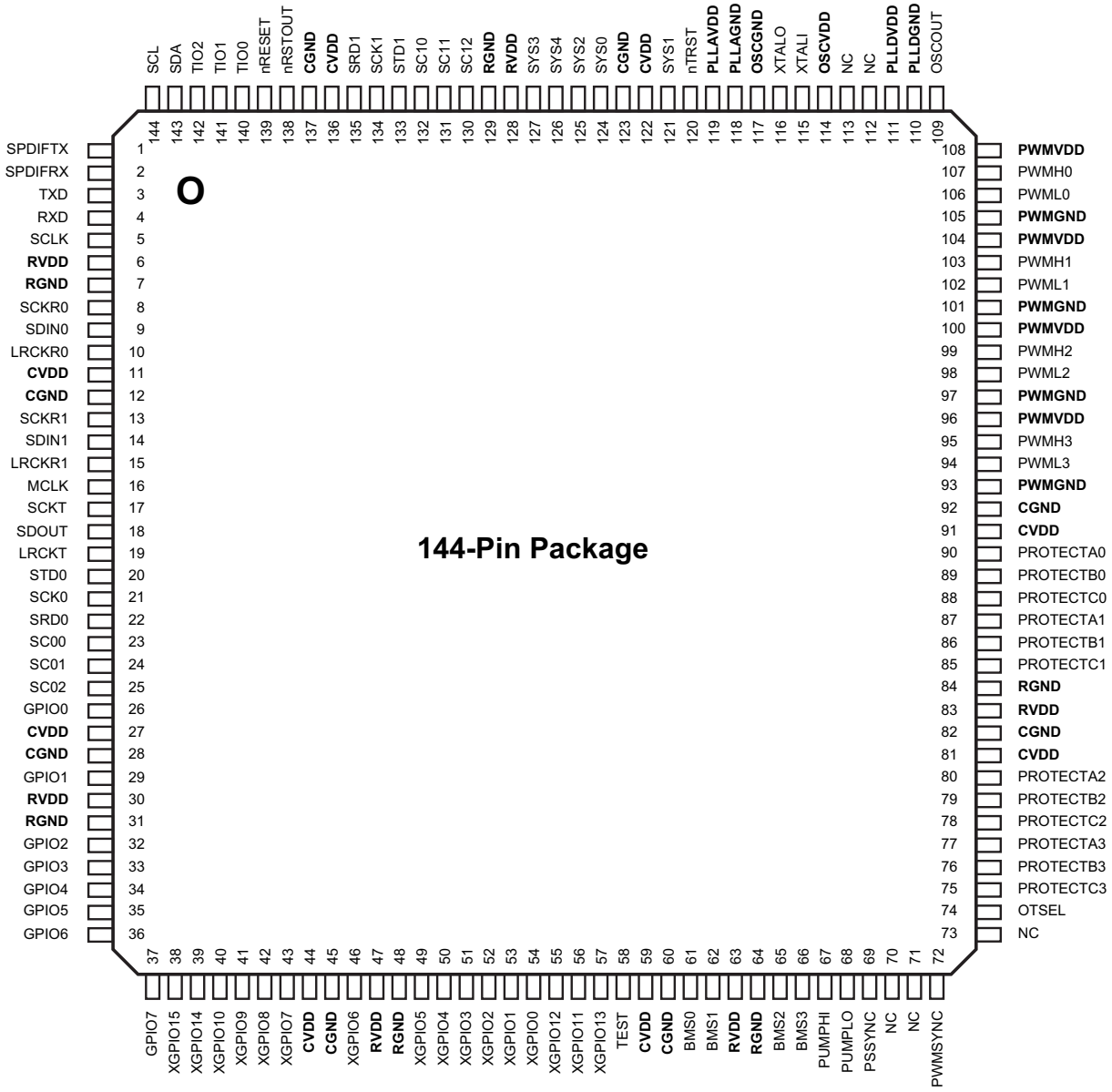


FIGURE 7: D2-814xx Pinout, 144-Pin LQFP Package

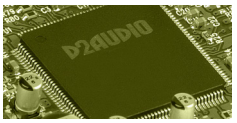
PRELIMINARY

PRELIMINARY

6.1 PIN DEFINITIONS 144-PIN LQFP PACKAGE

Serial Audio Interface (SAI) Pins			
Pin Number	**Port Name**	**Type**	**Description**
16	MCLK	Output	Master clock output
8	SCKR0	I/O	Serial Audio Input 0 clock receiver
10	LRCKR0	I/O	Serial Audio Input 0 left/right clock receiver
9	SDIN0	Input	Serial Audio Input 0 data
13	SCKR1	I/O	Serial Audio Input Clock 1 receiver
15	LRCKR1	I/O	Serial Audio Input 1 left/right clock receiver
14	SDIN1	Input	Serial Audio Input 1 data
17	SCKT	I/O	Serial Audio Output clock transmit
19	LRCKT	I/O	Serial Audio Output left/right clock transmit
18	SDOUT	Output	Serial Audio Output
S/PDIF			
Pin Number	**Port Name**	**Type**	**Description**
1	SPDIFTX	Output	S/PDIF data out
2	SPDIFRX	Input	S/PDIF data in
PWM Pins			
Pin Number	**Port Name**	**Type**	**Description**
107	PWMH0	Output	Channel 0 PWM high side output
106	PWML0	Output	Channel 0 PWM low side output
103	PWMH1	Output	Channel 1 PWM high side output
102	PWML1	Output	Channel 1 PWM low side output
99	PWMH2	Output	Channel 2 PWM high side output
98	PWML2	Output	Channel 2 PWM low side output
95	PWMH3	Output	Channel 3 PWM high side output
94	PWML3	Output	Channel 3 PWM low side output
74	OTSEL	Input	Output topology select input
72	PWMSYNC	I/O	PWM sync
2-Wire Serial Pins			
Pin Number	**Port Name**	**Type**	**Description**
144	SCL	I/O	Two wire serial clock
143	SDA	I/O	Two wire serial data
XGPIO Pins			
Pin Number	**Port Name**	**Type**	**Description**
43, 46, 49, 50, 51, 52, 53, 54	XGPIO[7:0]	I/O	General purpose I/O
38, 39, 57, 55, 56, 40, 41, 42	XGPIO[15:8]	I/O	
Reset and Test Pins			
Pin Number	**Port Name**	**Type**	**Description**
139	nRESET	Input	Reset - active low
138	nRSTOUT	Output	Reset output- active low output
120	nTRST	Input	Test reset - active low
58	TEST	Input	Hardware test pin

TABLE 8: Pin Definitions, 144-pin LQFP Package



PRELIMINARY

Crystal Oscillator and PLL Pins			
Pin Number	**Port Name**	**Type**	**Description**
109	OSCOUT	Output	Oscillator output to slave device
115	XTALI	Input	Crystal Oscillator input
116	XTALO	Output	Crystal Oscillator output
GPIO Pins			
Pin Number	**Port Name**	**Type**	**Description**
37, 36, 35, 34, 33, 32, 29, 26	GPIO[7:0]	I/O	General Purpose I/O
System Configuration Pins			
Pin Number	**Port Name**	**Type**	**Description**
124	SYS0	I/O	Reserved for factory test
121	SYS1	I/O	
125	SYS2	I/O	
127	SYS3	I/O	
126	SYS4	I/O	
Serial Communications Interface (SCI) Pins			
Pin Number	**Port Name**	**Type**	**Description**
5	SCLK	I/O	SCI clock
4	RXD	I/O	SCI receive data
3	TXD	I/O	SCI transmit data
Reserved Serial Audio Interface Pins			
Pin Number	**Port Name**	**Type**	**Description**
20	STD0	I/O	Reserved Serial Audio Interface 0 Tx Data or GPIO
21	SCK0	I/O	Reserved Serial Audio Interface 0 Clock or GPIO
22	SRD0	I/O	Reserved Serial Audio Interface 0 Rx Data or GPIO
23	SC00	I/O	Reserved Serial Audio Interface 0 Control 0 or GPIO
24	SC01	I/O	Reserved Serial Audio Interface 0 Control 1 or GPIO
25	SC02	I/O	Reserved Serial Audio Interface 0 Control 2 or GPIO
133	STD1	I/O	Reserved Serial Audio Interface 1 Tx Data or GPIO
134	SCK1	I/O	Reserved Serial Audio Interface 1 Clock or GPIO
135	SRD1	I/O	Reserved Serial Audio Interface 1 Rx Data or GPIO
132	SC10	I/O	Reserved Serial Audio Interface 1 Control 0 or GPIO
131	SC11	I/O	Reserved Serial Audio Interface 1 Control 1 or GPIO
130	SC12	I/O	Reserved Serial Audio Interface 1 Control 2 or GPIO
Boot Mode Select Pins			
Pin Number	**Port Name**	**Type**	**Description**
61	BMS0	Input	Boot Mode Select 0
62	BMS1	Input	Boot Mode Select 1
65	BMS2	Input	Boot Mode Select 2
66	BMS3	Input	Boot Mode Select 3
Timer (TIO) Pins			
Pin Number	**Port Name**	**Type**	**Description**
142, 141, 140	TIO[2:0]	I/O	Timer I/O ports
67	PUMPHI	I/O	Power supply pump control, high side or GPIO
68	PUMPLO	I/O	Power supply pump control, low side or GPIO
69	PSSYNC	I/O	Power supply synchronization or GPIO

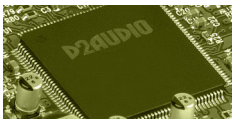
TABLE 8: Pin Definitions, 144-pin LQFP Package (Continued)

PRELIMINARY

PWM Protection Pins			
Pin Number	**Port Name**	**Type**	**Description**
77, 80, 87, 90	PROTECTA[3:0]	I/O	PWM Temperature status input, or GPIO
76, 79, 86, 89	PROTECTB[3:0]	I/O	PWM Over Current Protection inputs, or GPIO.
75, 78, 85, 88	PROTECTC[3:0]	I/O	PWM Shoot Through Current inputs or GPIO.
Power Pins			
Pin Number	**Port Name**	**Type**	**Description**
119	PLLAVDD	Power	PLL Analog power
118	PLLAGND	Ground	PLL Analog ground
111	PLLDVDD	Power	PLL Digital power
110	PLLDGND	Ground	PLL Digital ground
114	OSCVDD	Power	Oscillator power
117	OSCGND	Ground	Oscillator ground
11, 27, 44, 59, 81, 91, 122, 136	CVDD	Power	Core power - 8 pins
12, 28, 45, 60, 82, 92, 123, 137	CGND	Ground	Core ground - 8 pins
96, 100, 104, 108	PWMVDD	Power	PWM output pin power - 4 pins
93,97,101,105	PWMGND	Ground	PWM output pin ground.- 4 pins
6, 30, 47, 63, 83, 128	RVDD	Power	Digital pad ring power - 6 pins
7,31,48, 64,84,129	RGND	Ground	Digital pad ring ground- 6 pins
No Connect Pins			
Pin Number	**Port Name**	**Type**	**Description**
70, 71, 73, 112, 113	NC		No connect, leave pin floating

TABLE 8: Pin Definitions, 144-pin LQFP Package (Continued)

6.2 PIN DESCRIPTIONS 144-PIN PACKAGE



Pins are 100% firmware and Reference Design Platform (RDP) package dependent for their functionality. Output pins have one of 3 drive strengths - 4mA, 8mA, or 16mA. These strengths are characterized by the current that the pin will source or sink at the specified output voltage level.

6.2.1 SERIAL AUDIO INTERFACE (SAI) PINS

MCLK — **Master Clock Output**
Master Clock output for external ADC/DAC components with 8mA drive strength. Pin drives low on reset. MCLK is also used by test hardware to monitor various internal clocks.

SCKR0 — **SAI Receiver Bit Clock 1**
SAI Receiver 0 bit clock is an output when D2-814xx is a master, or an input when D2-814xx is a slave. Defaults to an input on reset. Output has 4mA drive strength. Input has hysteresis.

LRCKR0 — **SAI Receiver Left/Right Clock 0**
SAI Receiver 0 left/right audio frame clock is an output when D2-814xx is a master or an input when D2-814xx is a slave. Defaults to an input on reset. Output has 4mA drive strength. Input has hysteresis.

SDIN0 — **SAI Receiver Serial Data Input 0**
SAI Receiver 0 data input.

SCKR1 — **SAI Receiver Bit Clock 1**
SAI Receiver 1 bit clock is an output when D2-814xx is a master, or an input when D2-814xx is a slave. Defaults to an input on reset. Output has 4mA drive strength. Input has hysteresis.

LRCKR1 — **SAI Receiver Left/Right Clock 1**
SAI Receiver 1 left/right audio frame clock is an output when D2-814xx is a master or an input when D2-814xx is a slave. Defaults to an input on reset. Output has 4mA drive strength. Input has hysteresis.

SDIN1 — **SAI Receiver Serial Data Input 1**
SAI Receiver 1 data input.

SCKT — **SAI Transmitter Bit Clock**
SAI Transmitter bit clock is an output when D2-814xx is a master, or an input when D2-814xx is a slave. Defaults to an input on reset. Output has 4mA drive strength. SCKT is used to monitor the 3.3V brown out detector during the POR hardware test.

LRCKT — **SAI Transmitter Left/Right Clock**
SAI Transmitter left/right audio frame clock is an output when D2-814xx is a master, or an input when D2-814xx is a slave. Defaults to an input on reset. Output has 4mA drive strength. LRCKT is used to monitor the 1.8V brown out detector during the POR Hardware test. LRCKT is used to monitor PLL Lock during the PLL Hardware test.

SDOUT — **Serial Data Output**
SAI Transmitter data output with 4mA drive strength. Pin drives low on reset.

6.2.2 S/PDIF PINS

SPDIFRX — **S/PDIF Data Input**
This pin is the S/PDIF audio input and accepts a 3.3V stereo input up to 192kHz. To drive this pin, appropriate buffer and/or isolation circuits may be necessary to convert the S/PDIF cable input signal to clean logic levels.

SPDIFTX — **S/PDIF Data Output**
This pin is the S/PDIF audio output and drives a 3.3V stereo output up to 192kHz.

6.2.3 PWM PINS

PWMxH — **PWM High Side Driver Outputs**
PWM high side driver outputs, where x is 0 to 3, with 16mA drive strength. Pin drives to state determined by OTSEL on reset.

PWMxL — **PWM Low Side Driver Outputs**
PWM low side driver outputs, where x is 0 to 3, with 16mA drive strength. Pin drives low on reset.

OTSEL — **Output Topology Select Input**
Output topology select input. OTSEL pin state controls the PWMxH drive polarity. Typically, OTSEL will be tied either high for active-low PWMxH FET drivers, or tied low for active-high PWMxH FET drivers.

PRELIMINARY

PRELIMINARY

PWMSYNC **PWM Synchronization**
PWM synchronization port with 4mA drive. Used in multi-D2-814xx configurations to synchronize the PWM controllers. The master D2-814xx will drive synchronization data to the slave D2-814xx(s), thus the pin will be an output on the master D2-814xx and an input on the slave D2-814xx(s). Pin floats on reset.

6.2.4 2-WIRE SERIAL PINS

SCL **Serial Clock**
Two-Wire Serial clock port, open drain driver with 4mA drive strength. Bidirectional signal is used by both the master and slave controllers for clock signaling.

SDA **Serial Data**
Two-Wire Serial data port, open drain driver with 4mA drive strength. Bidirectional signal used by both the master and slave controllers for data transport.

6.2.5 XGPIO PINS

XGPIO[15:0] **Extended General Purpose I/O**
Bidirectional GPIO port with 4mA driver. Resets to input port.

6.2.6 RESET AND TEST PINS

nRESET **System Reset Input**
Active low reset input with hysteresis. Low level activates system level reset, initializing all internal logic and program operations. System latches boot mode selection on the IRQ input pins on the rising edge.

nRSTOUT **System Reset Output**
Active low reset output with 4mA driver. Pin drives low on any of POR output, 3.3V brown out detector, 1.8V brown out detector.

TEST **Test Mode Input**
Hardware test mode control. For D2Audio usage only. Must be tied low.

nTRST **Test Reset Input**
Active low test port reset. Low level activates test reset, initializing test hardware. Must be driven low with nRESET.

6.2.7 CRYSTAL OSCILLATOR AND PLL PINS

OSCOUT **Oscillator Output**
Analog oscillator output to slave D2-814xx devices. On reset, OSCOUT drives a buffered version of the crystal oscillator signal from the XTALI pin. May be turned off by program control.

XTALI **Crystal Oscillator Input**
Crystal oscillator analog input port. An external clock source would be driven into the this port. In multi-D2-814xx systems, the OSCOUT from the master D2-814xx would drive the XTALI pin.

XTALO **Crystal Oscillator Output**
Crystal oscillator analog output port. When using an external clock source, this pin must be open.

6.2.8 GPIO PINS

GPIO[7:0] **General Purpose I/O**
Bidirectional GPIO ports with 4mA driver. Resets to input ports.

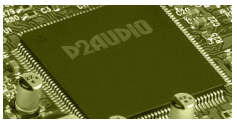
6.2.9 SYSTEM CONFIGURATION PINS

SYS0 **System Configuration Data 0**
Reserved for factory test. Tie low with 10k ohm resistor.

SYS1 **System Configuration Data 1**
Reserved for factory test. Tie high with 10k ohm resistor.

SYS2 **System Configuration Data 2**
Reserved for factory test. Tie high with 10k ohm resistor.

SYS3 **System Configuration Data 3**
Reserved for factory test. Tie high with 10k ohm resistor.



SYS4 — **System Configuration Data 4**
Reserved for factory test. Tie high with 10k ohm resistor.

6.2.10 SERIAL COMMUNICATIONS INTERFACE (SCI) PINS

SCLK — **Serial Clock**
Serial communications clock with 4mA drive and hysteresis on input. Resets to input port. May be configured to GPIO.

RXD — **Receive Data**
Serial communications receiver data with 4mA drive. Resets to input port. May be configured to GPIO.

TXD — **Transmit Data**
Serial communications transmitter data with 4mA drive. Resets to input port. May be configured to GPIO.

6.2.11 OPTIONAL/RESERVED FUNCTION PINS

SCK0 — **Reserved Serial Audio Interface 0 Serial Clock**
Serial Audio Interface 0 serial clock port with 4mA driver and hysteresis receiver. Resets to input port. May be configured as GPIO.

SC00-SC02 — **Reserved Serial Audio Interface 0 Serial Control**
Serial Audio Interface 0 serial control port with 4mA driver. Resets to input port. May be configured as GPIO.

STD0 — **Reserved Serial Audio Interface 0 Serial Transmit Data**
Serial Audio Interface 0 serial transmit data port with 4mA driver. Resets to input port. May be configured as GPIO.

SRD0 — **Reserved Serial Audio Interface 0 Serial Receive Data**
Serial Audio Interface 0 serial receive data port with 4mA driver. Resets to input port. May be configured as GPIO.

SCK1 — **Reserved Serial Audio Interface 1 Serial Clock**
Serial Audio Interface 1 serial clock port with 4mA driver and hysteresis receiver. Resets to input port. May be configured
as GPIO.

SC10-SC12 — **Reserved Serial Audio Interface 1 Serial Control**
Serial Audio Interface 1 serial control port with 4mA driver. Resets to input port. May be configured as GPIO.

STD1 — **Reserved Serial Audio Interface 1 Serial Transmit Data**
Serial Audio Interface 1 serial transmit data port with 4mA driver. Resets to input port. May be configured as GPIO.

SRD1 — **Reserved Serial Audio Interface 1 Serial Receive Data**
Serial Audio Interface 1 serial receive data port with 4mA driver. Resets to input port. May be configured as GPIO.

6.2.12 BOOT MODE SELECT PINS

BMS[3:0] — **Boot Mode Select Inputs**
External boot mode select inputs. On nRESET deassertion, these pins provide the boot mode selection.

6.2.13 TIMER (TIO) PINS

TIO[2:0] — **Timer**
Timer I/O ports with 4mA driver. May be configured as GPIO.

PUMPHI — **Power Supply Pump High**
High side power supply pump output with 16mA driver. May be configured as GPIO. Drives low on reset. Provides control means for operating an external switching power supply.

PUMPLO — **Power Supply Pump Low**
Low side power supply pump output with 16mA driver. May be configured as GPIO. Drives low on reset. Provides control means for operating an external switching power supply.

PRELIMINARY

PRELIMINARY

PSSYNC **Power Supply Synchronization**

Switching power supply synchronization signal with 16mA driver. May be configured as GPIO. Resets to input port.

6.2.14 PWM PROTECTION PINS

PROTECTA[3:0] **PWM Temperature Protection Inputs**

PWM temperature protection inputs with hysteresis. May be configured as GPIO. In this instance, the GPIO pins each have a 4mA driver. Each PWMTEMP input is associated with the corresponding PWM driver channel.

PROTECTB[3:0] **PWM Over-Current Protection Inputs**

PWM over-current protection inputs with hysteresis. May be configured as GPIO. In this instance, the GPIO pins each have a 4mA driver. Each PWMOCP input is associated with the corresponding PWM driver channel.

PROTECTC[3:0] **PWM Shoot-Through Current Protection**

PWM shoot-through-current protection inputs with hysteresis. May be configured as GPIO. In this instance, the GPIO pins each have a 4mA driver. Each PWMSTC input is associated with the corresponding PWM driver channel.

6.2.15 POWER PINS

PLLAVDD/PLLAGND **PLL Analog power and ground**

PLL analog supply/return. This 1.8V supply is used for the jitter critical sections of the PLL.

PLLDVDD/PLLDGND **PLL Digital power and ground**

PLL digital supply/return. This 1.8V supply is used for the "dirty" sections of the PLL, and provides the pad supplies for all of the analog pads. Note that PLLDGND and CGND are connected through the substrate.

OSCVDD/OSCGND **Oscillator power and ground**

Oscillator supply/return. This 1.8V supply is used for the crystal oscillator and oscillator bias circuits only.

CVDD/CGND **Core power and ground**

Core supply/return. This 1.8V supply is used in the chip interior logic and pad ring interfaces. There are 8 core supply pad pairs internally connected around the pad ring.

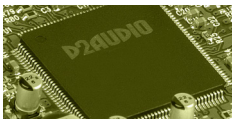
PWMVDD/PWMGND **PWM driver power and ground**

PWM I/O pad driver supply/return. This 3.3V supply is used for the PWM pad drivers only. There are 4 PWM internally connected supply pairs, one for each PWM data channel.

RVDD/RGND **Pad Ring power and ground**

Ring I/O pad driver supply/return. This 3.3V supply is used for all the digital I/O pad drivers and receivers except for the PWM and analog pads. There are 6 ring supply pairs internally connected around the pad ring.

7 D2-814XX RESET AND BOOT MODES



7.1 RESET

D2-814xx has a two reset inputs - the nRESET and nTRST input pins. The nRESET input pin is effectively a power-on system reset. All internal state logic, except internal test hardware, is initialized by nRESET. While reset is active the system is held in the reset condition. The reset condition is defined as all internal reset signals being active, the crystal oscillator is running, and the PLL disabled. The nTRST input resets internal factory test hardware only.

To assure proper system initialization, the nTRST input pin must be asserted along with nRESET.

7.2 BOOT MODES

The boot mode is determined by the BMS pin inputs. The BMS pin state is latched on the deassertion of system reset. It is expected that the application board will have pull-ups in the BMS pins, so that the desired boot mode is selected by default. The following table defines the boot modes.

Mode	BMS	M/S	Interface Speed	Description
2	0010	S	384Kb/s	Fast Asynchronous SCI slave boot (ex: D2-814xx to D2-814xx)
7	0111	M	385Kb/s	2-wire ROM on GPIO port (SCL=GPIO7, SDA=GPIO6)
C	1100	S	per Master	2-wire slave boot from micro, address = 1000100x

TABLE 9: Boot Modes

The Interface Speed specification is the speed at which the interface is configured to operate by the boot code. For the selection where the interface speed is "per Master", the interface must operate within the requirements of the selected interface specification.

PRELIMINARY

8 PHYSICAL DIMENSIONS 144-PIN PACKAGE

PRELIMINARY

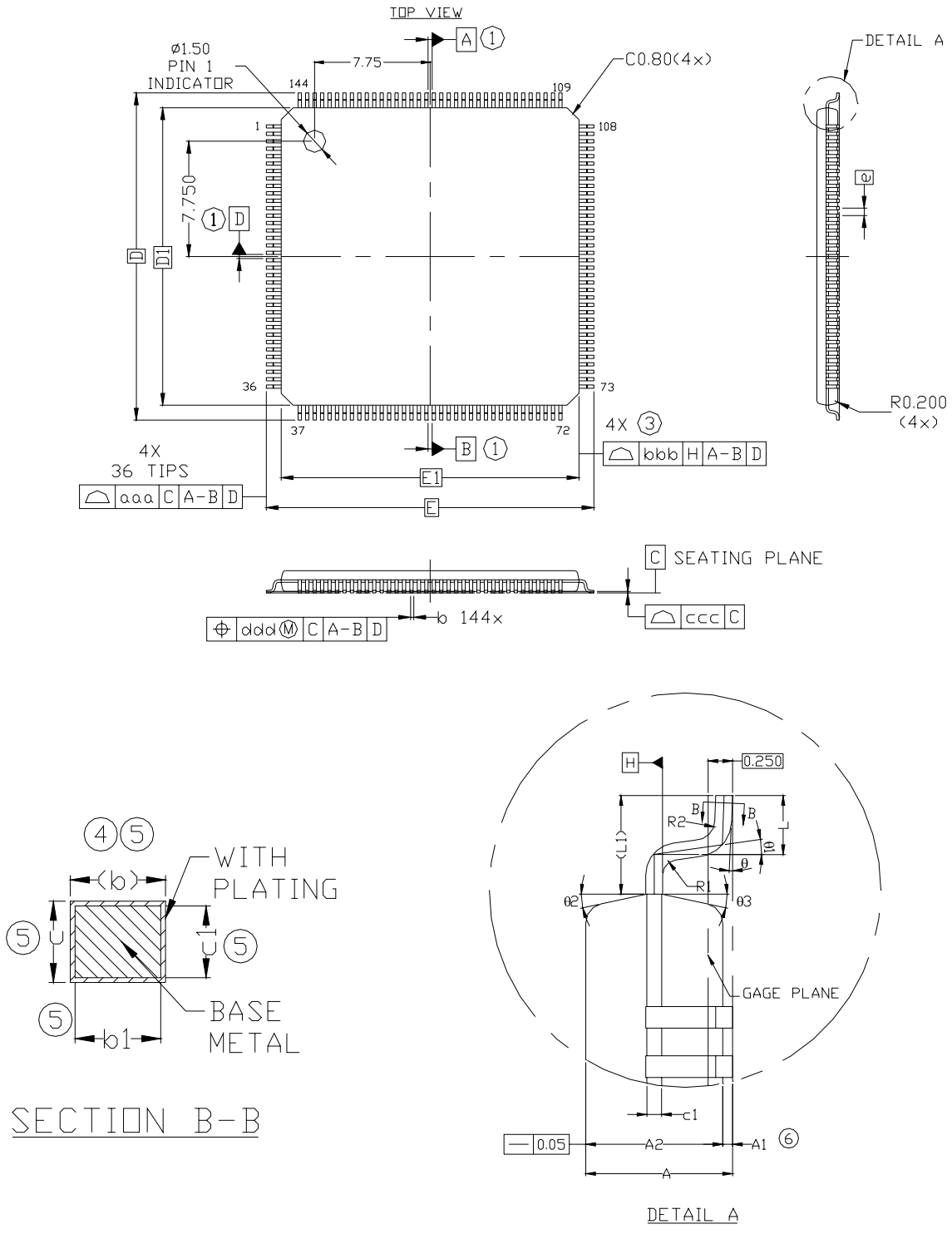
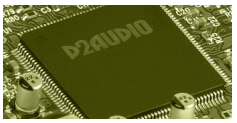


FIGURE 8: D2-814xx 144-Pin Package Dimensions



PRELIMINARY

SYMBOL	Min.	Nom.	Max.
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
D	22.00 BSC		
D1	20.00 BSC		
e	0.50 BSC		
E	22.00 BSC		
E1	20.00 BSC		
θ	0°	3.5°	7°
θ1	0°	–	–

SYMBOL	Min.	Nom.	Max.
θ2	11°	12°	13°
θ3	11°	12°	13°
c	0.09	–	0.20
c1	0.09	–	0.16
L	0.45	0.60	0.75
L1	1.00 REF.		
R1	0.08	–	–
R2	0.08	–	0.20
aaa	0.20		
bbb	0.20		
ccc	0.08		
ddd	0.08		

NOTE :
① DATUM A-B AND D TO DETERMINE AT DATUM PLANE H.
② TO BE DETERMINED AT SEATING DATUM PLANE C.
③ DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSIONS. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
④ DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07mm FOR 0.4mm AND 0.5mm PITCH PACKAGE.
⑤ THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
⑥ A1 IS THE DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
7 PACKAGE DIMENSIONS CONFORM TO JEDEC MS-026 Rev.D

FIGURE 9: D2-814xx 144-Pin Package Specifications

9 IC PART ORDERING

9.1 IC PART NUMBERING SCHEME

PRELIMINARY

Nomenclature

D2-[A][D][C][P][K]-[R][E]

A = Fundamental IC Architecture (single digit number)
"8" = 8-Series Advanced PWM Controller with Integrated Digital Audio Engine (4 Channel DSP + PWM Controller offered in 144-pin or 128-pin LQFP packages)

D = Chip Instantiation/Derivation Version (single digit hexadecimal number)
"1" = First Instantiation of IC Architecture

C = Number of PWM Outputs Channels (single digit hexadecimal number)
Channel count offerings:
"2" = 2 Channels
"4" = 4 Channels
(Note: The number of PWM output channels is not to be confused with the number of digital audio input channels that are available via Serial Audio Interface port.)

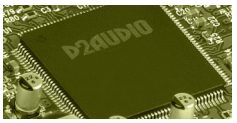
P = Performance (single digit hexadecimal number)
Performance Level offerings:
"0" = Customizable Functionality and Sonic Quality
"1" = THX® Ultra2™/Ultra-High-End Fixed-Level Performance
"2" = THX® Select™/High-End Fixed-Level Performance
"3" = Mid-End Performance

K = Pin Count (single digit hexadecimal number)
Current pin count offerings:
"1" = Undefined
"2" = 144-pin
"3" = 128-pin

R = Package Type (single character)
Current package Type offerings:
"E" = Engineering Prototype
"L" = LQFP
"P" = DIP
"S" = SOIC
"B" = BGA
"M" = Integrated Power Stage (Module IC) or Integrated Power Stage + Filter (Module IC)

E = Environment Category (single character)
Current Prohibited Material Usage Compliance Level:
"G" = D2Audio "Green Compliant"
"R" = RoHS Compliant (Pb-Free)
"P" = non-RoHS/non-Green Compliant

9.2 AVAILABLE PART NUMBERS



Part Number	Description
D2-81412-LR	X-Series Advanced PWM Controller with Integrated Digital Audio Engine, 4 channels, Full-Bridge or Half-Bridge Output Topology Support, Ultra High-End Performance Reference Design Support, 144-pin package, LQFP, RoHS Compliant (Pb-Free)
D2-81433-LR	X-Series Advanced PWM Controller with Integrated Digital Audio Engine, 4 channels, Full-Bridge or Half-Bridge Reference Output Topology Support, Mid-Performance Reference Design Support, 128-pin package, LQFP, RoHS Compliant (Pb-Free)

Table 10: Part Numbers and Feature Sets

PRELIMINARY

10 DOCUMENT REVISION HISTORY

07/25/05 Revision 0.0.1 - First Internal Release.
Created new data sheet template, updated product features, included new drawings of 128-pin package, included new 128-pin pinout and pin name descriptions.

08/12/05 Revision 0.0.2 - Second Internal Release.
Updated product features, included new drawings of 128-pin/144-pin package, included new 144-pin pinout and pin name descriptions.

08/15/05 Revision 0.0.3 - Third Internal Release.
Updated pins in 128-pin/144-pin package drawings, eliminated signal flow diagram, added 2 part numbers.

08/17/05 Revision 0.0.4 - Fourth Internal Release.
Updated IC image on master pages, added Section 8.1 "0" performance option, renamed document, updated cover page.

09/14/05 Revision 0.0.5 - Fifth Internal Release.
Updated all 128/144 package pinout tables and descriptions, removed waveforms, added block diagram, updated cover page.

10/20/05 Revision 1.0.0 - First External Release.
Updated cover page, updated block diagram Serial Audio Interface, updated OTSEL pin description, added 2-Wire interface and Serial Audio Port sections, added firmware and reference design disclaimers, updated part numbers.

12/6/05 Revision 1.0.1
Updated SYS0 pin from tie-high to tie-low.

12/22/05 Revision 1.0.2
Corrected cover page feature set descriptions, corrected Available Part Numbers in Table 10.

1/31/06 Revision 1.0.3
Changed 128-pin package pinouts in Figure 5, "D2-814xx Pinout, 128-Pin LQFP Package," on page 10, and Table 7 on page 11.

2/7/06 Revision 1.0.4
Changed text on cover page regarding valid boot modes. Updated Figure 1, "D2-814xx Block Diagram (144-pin package)," on page 5 to relable the Serial Audio block to Serial Audio Interface block. Renamed Serial Audio Interface block to be Reserved Serial Audio Interface block. Updated text in Section 2, "D2-814xx Signal Flow," on page 5. Changed "module" to "IC" in Section 3.5.1, "Serial Audio Interface (SAI ports)," on page 8. Updated text in Table 7 on page 11 to change "Serial Audio (SAI) Pins" to be "Serial Audio Interface (SAI) Pins". Updated text in Table 7 on the following page to change "Serial Audio Interface Pins" to be "Reserved Serial Audio Interface Pins" in both header and pin description sections. Changed title in Section 4.2.1, "Serial Audio Interface (SAI) Pins," on page 14 from "Serial Audio (SAI) Pins" to be "Serial Audio Interface (SAI) Pins". Changed SPDIF to S/PDIF in section Section 4.2.1, "Serial Audio Interface (SAI) Pins," on page 14. Deleted "or nRESET active low" from Section 4.2.6, "Reset and Test Pins," on page 15 and in Section 6.2.6, "Reset and Test Pins," on page 24 from the nRSTOUT pin description. Changed the title in Section 4.2.11, "Optional/Reserved Function Pins," on page 16 from "Optional Function Pins" to "Optional/Reserved Function Pins". Changed the pin descriptions in this section to now have a "Reserved" in front. Changed text in Section 4.2.14, "PWM Protection Pins," on page 16 on all pin descriptions. Relabled pin "SDO" to "SDOUT" in Figure 7, "D2-814xx Pinout, 144-Pin LQFP Package," on page 19, in Table 8 on page 20 as well as in Section 6.2.1, "Serial Audio Interface (SAI) Pins," on page 23.

2/8/06 Revision 1.0.5

Changed all related text, pin descriptions and pinout drawings for CTRL0, CTRL1, CTRL2, CTRL3. CTRL0 is now PUMPHI. CTRL1 is now PUMPLO. CTRL2 is now PSSYNC. CTRL3 is now PWMSYNC.

2/20/06 Revision 1.0.6

Added Junction Temperature to Table 1, "Absolute Maximum Ratings," on page 6 in addition to Note 1 on Operating Temperature, Storage Temperature and Storage Temperature. Added Table 4, "Thermal Characteristics," on page 7 which shows Theta J_A and J_C values for 128-pin and 144-pin LQFP packages.

3/27/06 Revision 1.1.1

Updated Theta J_A and J_C values for 128-pin and 144-pin LQFP packages in Table 4, "Thermal Characteristics," on page 7.

PRELIMINARY