D2AUDIO APPLICATION NOTE AN13

D2Audio X-Series Amplifier Digital Audio Inputs

1 Introduction

The self-contained X-series audio power amplifier modules from D2Audio™, with their high-efficiency and high-performance, provide the perfect solution for today's higher performance audio amplifiers, receivers, and powered speakers. These modules provide the customer with a complete drop-in class-D amplifier solution. Their flexibility and powerful digital processing features are only possible because of D2Audio's all digital audio path. To complement this, the D2Audio amplifier modules offer a variety of digital audio input methods. This application note describes the digital audio inputs found on the D2Audio XR, XM, XC and XS amplifier modules.

2 Digital Electrical Parameters

All amplifier module digital inputs and outputs are 3.3 volt compatible. All input signals should be driven by a 3.3 volt source. The input/output threshold characteristics are shown in Table 1.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input low voltage	V_{IL}	All inputs			0.8	V
Input high voltage	V_{IH}	All inputs	2.0			V
Output low voltage	V_{OL}	4 mA Load			0.4	V
Output high voltage	V_{OH}	4 mA Load	2.4			V
T_A = 25C, Nominal Voltage						

TABLE 1: Electrical Parameters

3 Available Digital Inputs

The X-series amplifier module is designed to interface with standard digital audio components via the Serial Audio Input (SAI) ports and will accept I^2S or Left Justified data formats. In either format, the SAI can receive 16 - 24 bit audio data at all standard sampling rates between 32 kHz and 192 kHz. At reset, the device is configured to receive I^2S formatted audio data.

The amplifier module may also optionally interface to incoming stereo PCM audio at sample rates between 32 kHz and 96 kHz via an optical (TOSLINK) or copper media (coaxial) S/PDIF digital input. The amplifier module does not support direct low-voltage S/PDIF signaling like that coming from a coaxial cable, which has a voltage swing of around 250 millivolts. An intermediary buffer is necessary to translate the incoming S/PDIF signal to the appropriate 3.3 volt digital signal needed by the amplifier module. Conversion from S/PDIF to linear PCM is performed by the module.

Additionally, a master clock is provided to drive external ADCs so that an external crystal is unnecessary.

A description of the amplifier module digital audio pins is shown in Table 2.

Pin	Description
SPDIFRX	S/PDIF Receiver Input These pins are S/PDIF audio inputs. They will accept a bi-phase encoded stereo input up to 96 kHz and are 3.3 volt inputs. An appropriate transformer or optical coupler is necessary for external interface.
LRCLK	Left/Right Clock This pin is the SAI framing clock or word clock. The LRCLK frequency determines the input sample rate (Fs). LRCLK is a 3.3 volt input.
SCLK	Serial Clock This pin is the SAI serial clock input. This serial clock is used to latch each input bit of the serial input data into the SAI port input buffer. The serial clock frequency is typically 64*Fs. SCLK is a 3.3 volt input.
SDIN	Serial Data Input This pin is the SAI serial data input. The SDIN pin is a 3.3 volt input.
MCLKT	MCLK Output This pin is the master clock (MCLK) output. The default master clock is 12.288 MHz, which corresponds to a 48 kHz sample rate (Fs) * 256.

TABLE 2: Digital Interface Pins

Amplifier modules with 2 to 3 output channels will have 1 SAI port and 1 optional S/PDIF receiver, modules with 4 channels will have 2 SAI ports and 1 optional S/PDIF receiver, modules with 5 to 6 output channels will have 3 SAI ports and 2 optional S/PDIF receivers, and modules with 7 to 8 output channel modules will have 4 SAI interfaces and 2 optional S/PDIF receivers. Each SAI uses a 3 pin interface containing the Serial Data Input (SDIN) pin, the Left/Right Clock (LRCLK) pin, and the Serial Clock (SCLK) pin. Each S/PDIF interface consists of a single pin, SPDIFRX.

Module Channels	SAI Inputs	SAI Pins	S/PDIF Inputs	S/PDIF Pins
2-3	1	LRCLK[0] SCLK[0] SDIN[0]	1*	SPDIFRX
4	2	LRCLK[1:0] SCLK[1:0] SDIN[1:0]	1*	SPDIFRX
5-6	3	LRCLK[2:0] SCLK[2:0] SDIN[2:0]	2*	SPDIFRX[1:0]
7-8	4	LRCLK[3:0] SCLK[3:0] SDIN[3:0]	2*	SPDIFRX[1:0]
* - S/PDIF Inputs are Optional				

TABLE 3: Input Availability

4 Selecting Input Source At Reset

XS, XM, and XC Modules

The XS, XM, and XC amplifier modules use several pins to determine the audio configuration at reset. Based on the state of the DIG/ANL and SPDIFEN pins, different audio inputs will be passed to the amplifier output. The availability and number of each of these pins varies depending on the module. The configurations available for a specific module can be found in the module documentation. For all audio configuration pins, these pins determine only determine the module state immediately after reset. After reset, any changes to the pin states will have no effect on module behavior. It is possible to alter the audio input configuration after reset, by using the Module Control Interface (MCI). The module behavior at reset is shown in Table 4.

SPDIFEN	DIG/ANL	XS/XM/XC Result
SPDIFEN[0] = 1	DIG/ANL[0] = 1	SAI 0 connected to SPKR_OUT1 and SPKR_OUT2 outputs
SPDIFEN[0] = 1	DIG/ANL[0] = 0	AIN 1/2 connected to SPKR_OUT1 and SPKR_OUT2 outputs
SPDIFEN[0] = 0	DIG/ANL[0] = X	SPDIFRX0 connected to SPKR_OUT1 and SPKR_OUT2 outputs
N/A	DIG/ANL[1] = 1	SAI 1 connected to SPKR_OUT3 and SPKR_OUT4 outputs
N/A	DIG/ANL[1] = 0	AIN3/4 connected to SPKR_OUT3 and SPKR_OUT4 outputs
SPDIFEN[1] = 1	DIG/ANL[2] = 1	SAI 2 connected to SPKR_OUT5 and SPKR_OUT6 outputs
SPDIFEN[1] = 1	DIG/ANL[2] = 0	AIN 5/6 connected to SPKR_OUT5 and SPKR_OUT6 outputs
SPDIFEN[1] = 0	DIG/ANL[2] = X	SPDIFRX1 connected to SPKR_OUT5 and SPKR_OUT6 outputs
N/A	DIG/ANL[3] = 1	SAI Input 3 connected to SPKR_OUT7 and SPKR_OUT8 outputs
N/A	DIG/ANL[3] = 0	AIN7/8 connected to SPKR_OUT7 and SPKR_OUT8 outputs

TABLE 4: XS, XM, and XC Reset Input Selection

If the SPDIFEN and DIG/ANL pins are all left unconnected, the module will come out of reset receiving audio via the SAI ports.

For more information on the optional analog inputs, refer to the amplifier module datasheet.

XR Modules

The XR amplifier modules use several pins to determine the audio configuration at reset. Based on the state of the ZONE2EN, ZONE3EN, and SPDIFEN pins, different audio inputs will be passed to the amplifier output. The availability and number of each of these pins varies depending on the module. The configurations available for a specific module can be found in the module documentation. For all audio configuration pins, these pins determine only determine the module state immediately after reset. After reset, any changes to the pin states will have no effect on module behavior. It is possible to alter the audio input configuration after reset, by using the Module Control Interface (MCI). The module behavior at reset is shown in Table 5.

SPDIFEN	ZONExEN	XR Result
SPDIFEN[0] = 1	ZONE3EN = 1	SAI 1 connected to SURL and SURR outputs
SPDIFEN[0] = 1	ZONE3EN = 0	Z3_AINx connected to SURL and SURR outputs
SPDIFEN[0] = 0	ZONE3EN = X	SPDIFRX0 connected to SURL and SURR outputs

TABLE 5: XR Reset Input Selection

SPDIFEN	ZONExEN	XR Result
SPDIFEN[0] = 1	ZONE2EN = 1	SAI 2 connected to SBL and SBR outputs
SPDIFEN[0] = 1	ZONE2EN = 0	Z2_AINx connected to SBL and SBR outputs
SPDIFEN[0] = 0	ZONE2EN = X	SPDIFRX1 connected to SBL and SBR outputs

TABLE 5: XR Reset Input Selection (Continued)

If the SPDIFEN and ZONExEN pins are all left unconnected, the module will come out of reset receiving audio via the SAI ports.

For more information on the optional analog zone inputs, refer to the amplifier module datasheet.

5 Selecting Input Source During Operation

XS, XM and XC Modules

After reset, the audio input selection can be altered via the Module Control Interface (MCI). These operations are performed by altering the InputSelectReg. The register bits for XS, XM, and XC modules are shown in Table 6.

InputSelectReg Bits	XS / XM / XC	XS / XM / XC Comment
23:8	Reserved	Set to F800h
7:5	Reserved	Set to 0
4	JUSTIFY	Selects SAI audio format 1: Use Left-Justified format 0: Use I^2S format
3	DIG_ANL_H	Select digital input or analog inputs 1: Digital input 0: Analog input
2	DIG_ANL_L	Selects digital or analog inputs
1	Reserved	Set to 0
0	SPDIFEN	Selects the SPDIF input

TABLE 6: XS / XM / XC InputSelectReg

For the XS, XM, and XC modules, the behavior of the DIG_ANL_X and SPDIFEN bits are shown in Table 7. The new operating modes become valid as soon as the MCI write operation is complete.

MCI Interface	SPDIFEN	DIG_ANL_L / DIG_ANL_H	XS / XM / XC Result
0	SPDIFEN0 = 0	DIG_ANL_L = 1	SAI 0 connected to SPKR_OUT1 and SPKR_OUT2 outputs
0	SPDIFEN0 = 0	DIG_ANL_L = 0	AIN 1/2 connected to SPKR_OUT1 and SPKR_OUT2 outputs
0	SPDIFEN0 = 1	DIG_ANL_L = X	SPDIFRX0 connected to SPKR_OUT1 and SPKR_OUT2 outputs
0	N/A	DIG_ANL_H = 1	SAI 1 connected to SPKR_OUT3 and SPKR_OUT4 outputs

TABLE 7: XS / XM / XC Input Selection Guide

MCI Interface	SPDIFEN	DIG_ANL_L / DIG_ANL_H	XS / XM / XC Result
0	N/A	DIG_ANL_H = 0	AIN3/4 connected to SPKR_OUT3 and SPKR_OUT4 outputs
1	SPDIFEN1 = 0	DIG_ANL_L = 1	SAI 2 connected to SPKR_OUT5 and SPKR_OUT6 outputs
1	SPDIFEN1 = 0	DIG_ANL_L = 0	AIN 5/6 connected to SPKR_OUT5 and SPKR_OUT6 outputs
1	SPDIFEN1 = 1	DIG_ANL_L = X	SPDIFRX1 connected to SPKR_OUT5 and SPKR_OUT6 outputs
1	N/A	DIG_ANL_H = 1	SAI Input 3 connected to SPKR_OUT7 and SPKR_OUT8 outputs
1	N/A	DIG_ANL_H = 0	AIN7/8 connected to SPKR_OUT7 and SPKR_OUT8 outputs

TABLE 7: XS / XM / XC Input Selection Guide (Continued)

Additionally, the SAI input format can be altered by the InputSelectReg. This action is performed by changing the JUSTIFY bit in the InputSelectReg register. For modules with multiple MCIs, the SAI format must be set the same on all interfaces.

The module attempts to gracefully transition between audio sources. To guarantee unwanted audio artifacts from being transmitted to the speaker, it is recommended that the output channels are muted during transition. Audio channels can be muted by setting the MasterVolumeParameter register to the minimum value.

Please refer to the “Input Selection Through Software” section of the amplifier module’s datasheet for more information.

XR Modules

After reset, the audio input selection can be altered via the Module Control Interface (MCI). These operations are performed by altering the InputSelectReg. The register bits for XR modules are shown in Table 8.

InputSelectReg Bits	XR	XR Comment
23:8	Reserved	Set to F800h
7:5	Reserved	Set to 0
4	JUSTIFY	Selects SAI audio format 1: Use Left-Justified format 0: Use I^2S format
3	Reserved	Always set to 1
2	ZONExEN	Select digital SAI or analog zone input 1: Digital SAI 0: Zone input
1	Reserved	Set to 0
0	SPDIFEN	Selects the SPDIF input

TABLE 8: XR InputSelectReg

For the XR modules, the behavior of the ZONExEN and SPDIFEN bits are shown in Table 9. The new operating modes become valid as soon as the MCI write operation is complete.

MCI Interface	SPDIFEN	ZONExEN	XR Result
0	SPDIFEN = 0	ZONExEN = 1	SAI 1 connected to SURL and SURR outputs
0	SPDIFEN = 0	ZONExEN = 0	Z3_AINx connected to SURL and SURR outputs
0	SPDIFEN = 1	ZONExEN = X	SPDIFRX0 connected to SURL and SURR outputs
1	SPDIFEN = 0	ZONExEN = 1	SAI 2 connected to SBL and SBR outputs
1	SPDIFEN = 0	ZONExEN = 0	Z2_AINx connected to SBL and SBR outputs
1	SPDIFEN = 1	ZONExEN = X	SPDIFRX1 connected to SBL and SBR outputs

TABLE 9: XR Input Selection Guide

Additionally, the SAI input format can be altered by the InputSelectReg. This action is performed by changing the JUSTIFY bit in the InputSelectReg register. For modules with multiple MCIs, the SAI format must be set the same on all interfaces.

The module attempts to gracefully transition between audio sources. To guarantee unwanted audio artifacts from being transmitted to the speaker, it is recommended that the output channels are muted during transition. Audio channels can be muted by setting the MasterVolumeParameter register to the minimum value.

Please refer to the “Input Selection Through Software” section of amplifier module’s datasheet for more information.

6 Digital Interface Layout Considerations

The signals of the digital audio interfaces are high speed digital and require careful considerations in a system design. All signals of this interface must be treated as high speed clock signals and given preferential routing on a PC board. Good engineering practices for line terminations, buffering, and trace lengths must be followed to ensure signal integrity.

D2Audio recommends adding 33 ohm series termination to all sources driving the digital audio input pins shown in Table 2. The series resistors should be placed with 0.5 inches of the driving pin. Additionally, board traces should be less than 12 inches (30 cm) and layer transitions should be minimized.

7 Connecting A Digital Audio Source To A Single SAI Port

For applications where there is a single digital audio source per SAI input, directly connect the SCLK, LRCK, and SDO pins on the audio source to the module. 33 ohm series resistance should

be added for each of the high-speed digital signals. Figure 1 illustrates this with an external ADC. Please verify that the audio source and the module are configured to compatible audio formats.

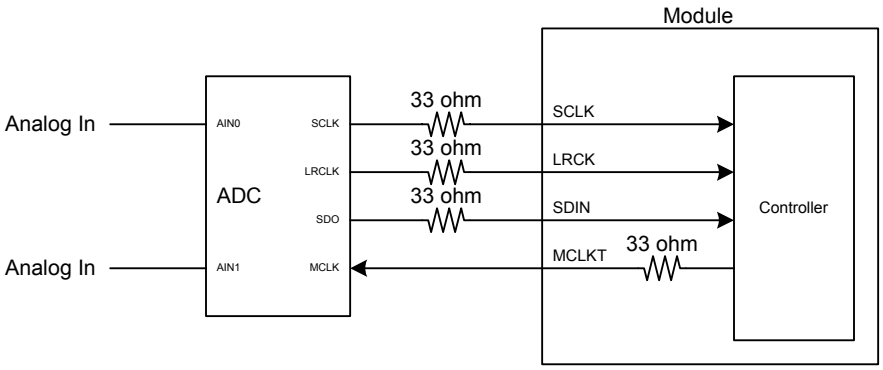

FIGURE 1: Direct Connect SAI Interface

8 Connecting A Digital Audio Source To Multiple SAI Ports

If multiple SAI inputs are fed from a single audio source, consider rebuffering the interface signals before connecting them to the module to help maintain signal integrity. This situation may apply in designs with multiple SAI inputs or with multiple modules. It is recommended to rebuffer with an LZ125 or equivalent buffer if more than 2 interfaces are tied together. The LZ125 should not be loaded with a fan-out greater than 4 module inputs. Please note that all buffers should be

driving 3.3 volts and that all buffer output legs have 33 ohm series termination. This topology is illustrated in Figure 2.

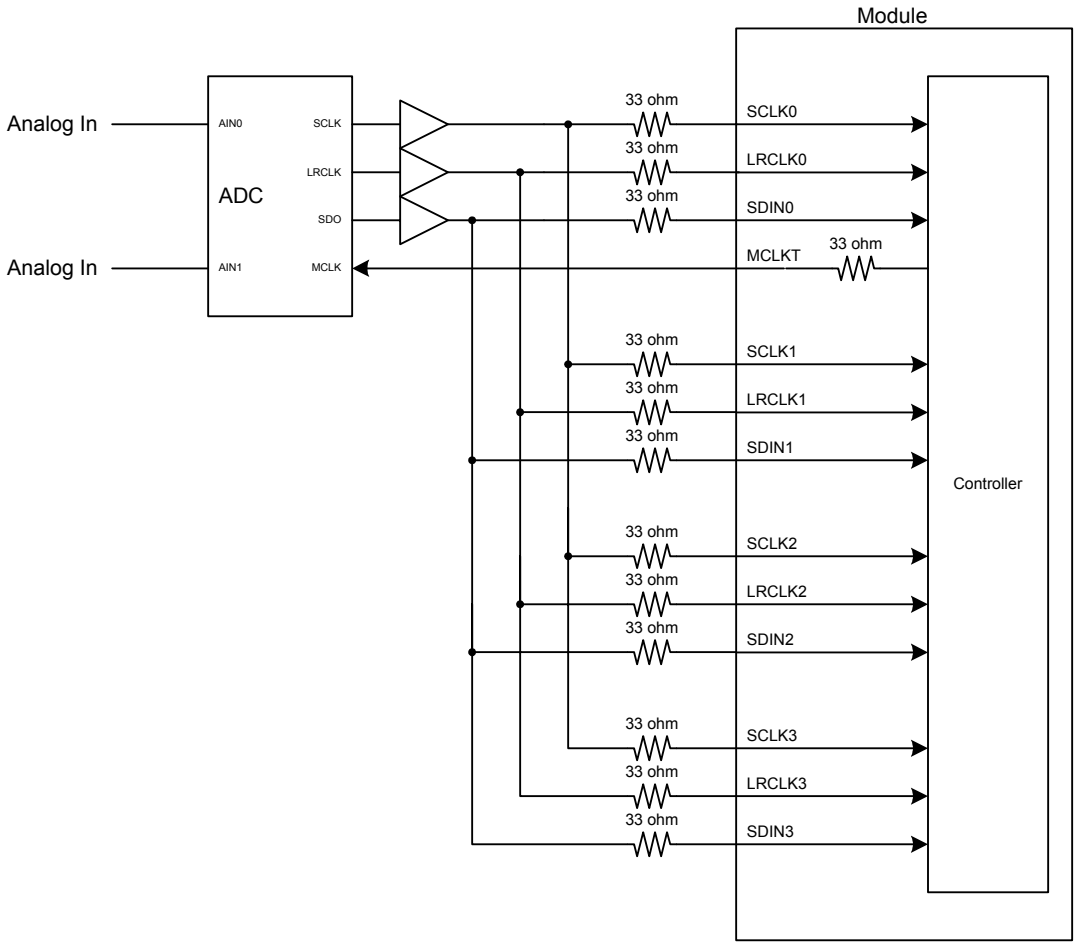

FIGURE 2: Rebuffered SAI Interface

9 Connecting To An Optical S/PDIF

To receive an optical S/PDIF input, an optical receiver translates the light signal to an electrical signal. The setup is shown in Figure 3. It should be noted that the 3.3 volt buffer is only necessary if the TOSLINK receiver does not operate at 3.3 volts

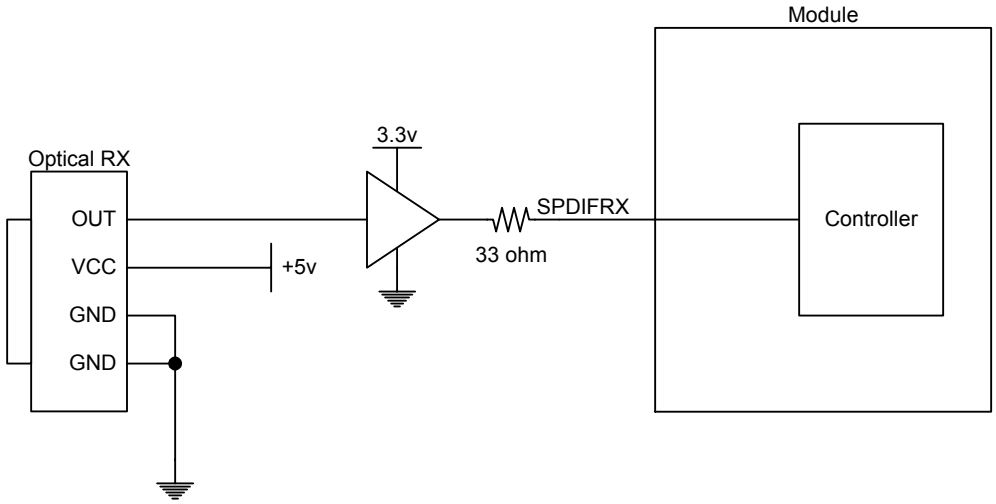

FIGURE 3: S/PDIF Optical Input

10 Connecting To A Coaxial S/PDIF Input

To receive a coaxial S/PDIF input, a transformer and buffer is used to recover the low-voltage signal. This configuration is shown in Figure 4.

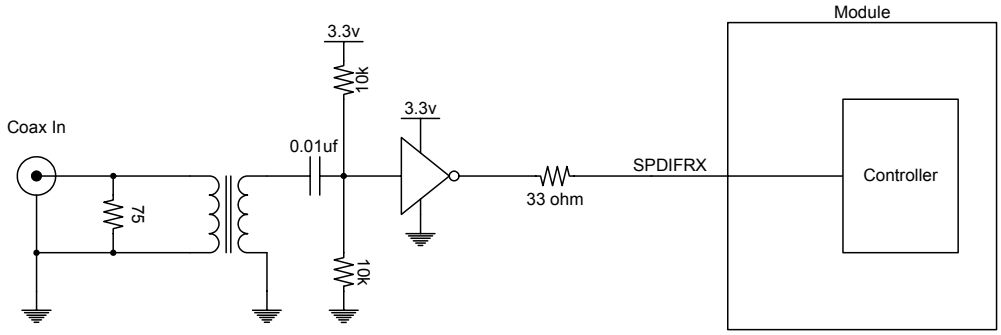

FIGURE 4: S/PDIF Coaxial Input

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