D2AUDIO MXS100 DATA SHEET

Intelligent digital amplifier module for manufacturers of consumer active speakers & in-wall audio distribution

PRELIMINARY

Complete Class-D Amplifier Solution

- D2Audio® Intelligent Digital Controller IC, PWM Driver, MOSFET Output Stage and Output Filter in one package
- Designed for compliance with UL and CSA

High-Performance Sound

- 100 Watts x 2 Channels, 8Ω Both Channels Driven Continuously (FTC, Alternative A) Capable[1]
- 105 Watts/Ch, 1kHz, 8Ω <.1% THD + N
- 100 Watts/Ch, 1kHz, 6Ω <.1% THD + N
- 95 Watts/Ch, 1kHz, 4Ω, <.1% THD + N
- > 105dB SNR/Dynamic Range (Unweighted, 20Hz-20kHz)
- +/-0.5dB frequency response (8Ω, 1W, 20Hz-20kHz)

High Peak-Wattage Stereo/Bi-Amp Capability

- 170 Watts/Channel, 8Ω[2]
- 220 Watts/Channel, 6Ω[2]
- 290 Watts/Channel, 4Ω[2]

Pure Digital Path

- 2 digital audio inputs which support I^2S and Left-Justified formats of Linear PCM (32kHz-192kHz, 16-24 bit)
- Sample Rate conversion performed on all audio outputs

Graceful Protection and Recovery

- Complete short-circuit, thermal, over-current fault protection
- Graceful handling of complex and lower impedance loads

Flexible Audio Configuration

- Complete Signal Processing: Tone Control, 8 Bands of Parametric EQ, Loudness Contour, Compression Limiting, Independent Channel Delay, Channel Attenuation
- Ease of adoption in systems (powered speakers), without a host microcontroller, via use of GPIO pins for controlling master volume, treble, and bass rotary encoders.
- Highly flexible programmable crossover capability across both channels for bi-amp designs with Butterworth, Bessel, Linkwitz-Riley filter types, and custom filter options.

Advanced Feature Options

- Optional S/PDIF Linear PCM Digital Audio Input
- Optional Internal ADC
- Optional Post-Processed I^2S/Left-Justified and S/PDIF outputs
- D2Audio Canvas™ GUI: an intuitive point-and-click audio configuration utility for OEMs, ODMs, and system designers

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The D2Audio® MXS100 is a self-contained 100 Watt per channel digital amplifier module for manufacturers of active loudspeaker systems and in-wall audio distribution applications. The MXS100 contains an D2Audio intelligent, high-performance digital switching controller IC, PWM driver MOSFET output stages, and high-performance output filters. The amplifier module is designed for compliance with UL and CSA requirements.

The MXS100 is capable of driving up to 2 output channels at 100 Watts into an 8Ω load continuously (with the appropriate amount of heat dissipation). The heat transfer plate has tabs for easy installation of OEM-supplied heat sink.

The MXS100 module provides configurable per channel audio processing including Parametric Equalization, Volume Control, Tone Control, Crossover, Adjustable Time Delay, and Dynamic Range Compression/Limiting.

The MXS100 amplifier module includes an advanced active programmable crossover for bi-amp, active loudspeaker designs including selectable Butterworth, Bessel, and Linkwitz-Riley crossover filter types.

Included are up to 2 channels of digital audio inputs supporting I^2S and Left-Justified Linear PCM (32kHz-192kHz, 16-24-bit).

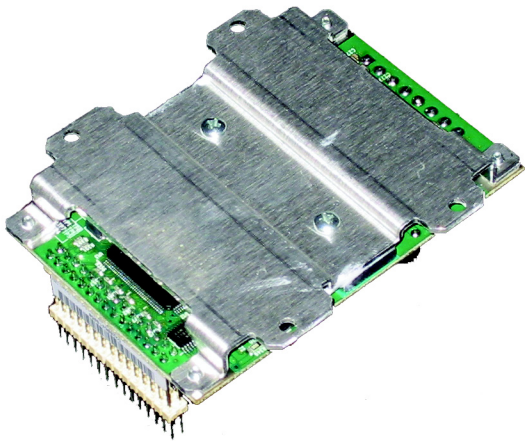
The MXS100 module features D2Audio Canvas, a Windows application with an intuitive graphical user interface (GUI). "Point-and-click" options simplify audio configuration and avoid complex programming. The user can activate the optional S/PDIF or ADC input, Loudness Contour, as well as adjust the 3/5-Band Parametric EQ filters, Tone Control, Crossover Point, or Channel Delay via D2Audio Canvas GUI.

The amplifier may be configured to start and run automatically without requiring an external controller. For more advanced configurations a simple controller interface is provided.

The MXS100 comes in a small (W 2.8 in. x L 3.5 in. x H 1.2 in.) footprint package that fits in a 2-gang electrical housings that are perfect for in-wall speaker applications or as individual amplifier module add-ons for a distributed audio system.

D2AUDIO MXS100

- **Complete digital amplifier for stereo mini systems, active bi-amplified loudspeakers & miniature powered subwoofer systems**
- **D2Audio Intelligent Controller IC**
- **Crossover, Time Alignment, EQ, Current Limiting, Power limiting**
- **I^2S, Left-Justified, or Optional S/PDIF Digital Audio Input**
- **93% Efficiency Reduces Heat and System Size**
- **Graceful protection & automatic fault recovery**



7600B Capital of TX Hwy 130 | Austin, TX 78731 | main: 512.343.9301 | fax: 512.343.9316 | www.d2audio.com

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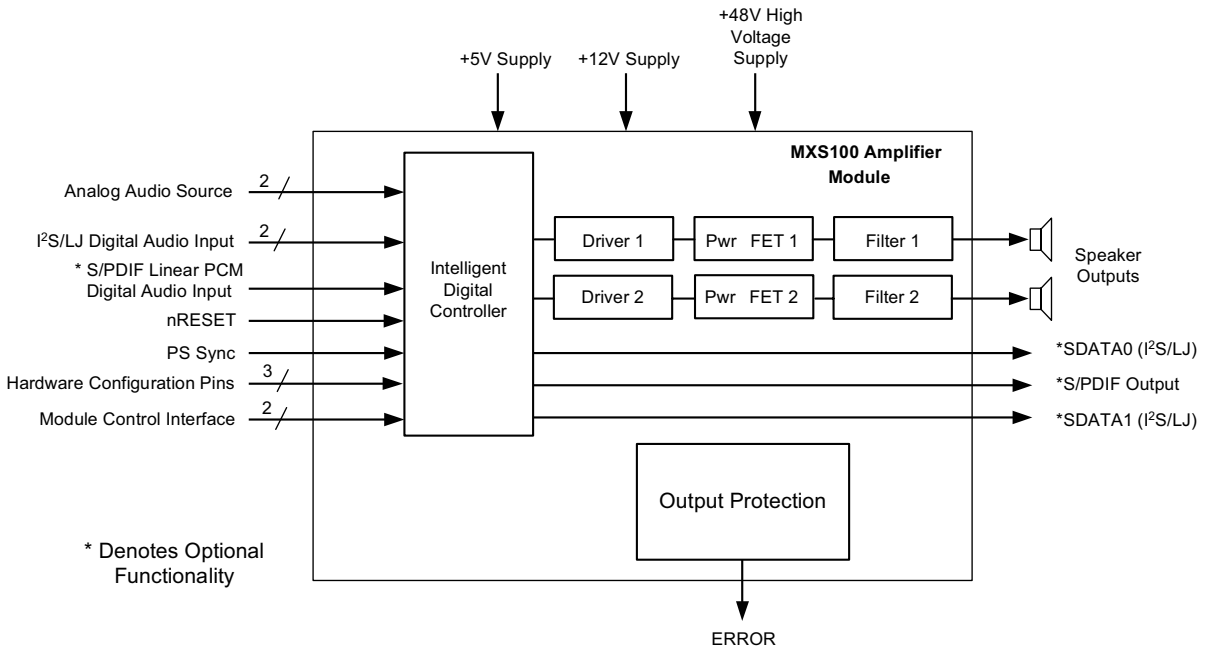

FIGURE 1: MXS100-2 Interface Block Diagram

[1] FTC Testing Method (footnote from Page 1)

This product is capable of meeting and exceeding the Alternative A, Alternative B or Alternative C end-product power rating method according to the FEDERAL TRADE COMMISSION 16 CFR Part 432 document which covers TRADE REGULATION RULE RELATING TO POWER OUTPUT CLAIMS FOR AMPLIFIERS UTILIZED IN HOME ENTERTAINMENT PRODUCTS, provided that adequate thermal management and an appropriate power supply has been designed into the end-system. This product must be provided with some method of thermal management (for example, addition of an external heat sink and/or fan-cooling system) before being powered up. For additional information about the FEDERAL TRADE COMMISSION 16 CFR Part 432 document, please go to the following link: http://www.ftc.gov/os/2000/12/amplifierrulenotice.pdf

[2] Peak Wattage Testing Methods (footnote from Page 1)

8, 6, and 4Ω peak power measurements were made using a 1kHz continuous sine wave, at 10% THD into resistive loads. For long periods of time, continuous sine wave high-wattage outputs may be limited by over-current or thermal protective algorithms.

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D2Audio products are not authorized for use as critical components in life support systems, equipment used in hazardous environments or nuclear control systems without the express written consent of D2Audio Corporation.

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1 SPECIFICATIONS

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1.1 ABSOLUTE MAXIMUM RATINGS

Parameter	Condition	Min	Typ	Max	Unit
High Voltage Supply	+48V DC Supply	0	48	50	V
Low Voltage Supply	+12V DC Supply	0	12	12.6	V
Signal Voltage Supply	+5V DC Supply	0	5	5.5	V
Digital Input Signal Level[1]	All digital inputs	-0.6	-	3.90	V
Analog Input Signal Level[2]	Peak to peak AC voltage	-	-	5	V
Analog Input DC Offset		-3.8	-	2.5	V
Input Current, any pin except supplies		-	-	+/-10	mA
Nominal Operating Temperature Range[3, 4]	Module ambient temperature Module heat sink temperature	-10 -10	- -	45 60	°C
Storage Temperature Range		-20	-	60	°C
Lead Temperature	Soldering 10 Seconds	-	-	300	°C

Note 1: -0.6V undershoots and 3.9V overshoots allowed for 4ns maximum
Note 2: Analog inputs are AC coupled internally
Note 3: Normal Operation refers to running the unit in accordance with FTC test methods.
Note 4: Refer to Figure 27, "Module Derating Curve," on page 46 for the operating range and derating curves.

TABLE 1: Absolute Maximum Ratings

1.2 ELECTRICAL CHARACTERISTICS

T_A = 25° C, Typical Power Supply, Ground = 0V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input low voltage	V_{IL}	All inputs	-	-	0.8	V
Input high voltage	V_{IH}	All inputs	2.0	-	-	V
Output low voltage	V_{OL}	4 mA Load	-	-	0.4	V
Output high voltage	V_{OH}	4 mA Load	2.4	-	-	V
Input leakage	I_L	Input Leakage - LRCK, SCLK, SDIN	-	-	+/-10	uA
Input current	I_C	All digital inputs with resistive pulls - BOOT_EE/I2C, RESET, BASS[2:1], TREBLE[2:1], VOLUME[2:1], STEREO/BIAMP, SCL, SDA, ANALOG/DIGITAL	-		+/-0.4	mA
Analog Input Resistance	R_I	Analog input resistance - all analog audio inputs	-	20	-	kΩ
Analog Input Source Impedance	Z_S	Recommended analog input source output impedance			<= 10	Ω
Analog Full Scale	V_{IFS}	Analog input voltage to get full scale from internal ADC	-	1.85	-	Vrms

TABLE 2: Electrical Characteristics

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1.3 PERFORMANCE CHARACTERISTICS

Resistance load = 8Ω (unless otherwise specified), T_A = 25°C, V_{+48V}=48V, V_{+12VDC}=12V, V_{+5VDC}=5V, Ground = 0V, at 48kHz input sample rate

Specification	Condition	Min	Typ	Max	Unit
Continuous Rated Output Power[1] - 4Ω load	Any single channel	150[2]	220[3]	290[4]	W
Continuous Rated Output Power[1] - 6Ω load	Any single channel	150[2]	170[3]	220[4]	W
Continuous Rated Output Power[1] - 8Ω load	Any single channel	125[2]	130[3]	170[4]	W
Frequency Response	20Hz to 20kHz	-0.5	-	0.5	dB
Dynamic Range	Digital Input	100	105	110	dB
Dynamic Range	Analog Input	-	100	-	dB
Output Distortion (THD+N)	Digital Input, 20Hz to 20kHz, 1W	-	0.05	-	%
Output Distortion (THD+N)	Analog* Input, 20Hz to 20kHz, 1W	-	0.05	-	%

Note 1: The output power of the amplifier module is limited by the thermal characteristics of the module, ambient air temperature, and airflow. The amplifier module will continue to operate up to its thermal limit and will limit output power gracefully until the amplifier has cooled. Full output power is restored once the amplifier has attained a safe operating temperature. Complete thermal shutdown will only occur under extreme conditions in which the amplifier is not able to maintain a safe operating temperature with reduced output power.
Note 2: <0.2% THD+N (1kHz)
Note 3: <1% THD+N (1kHz)
Note 4: <10% THD+N (1kHz)

TABLE 3: Performance Characteristics

1.4 DC POWER REQUIREMENTS

Resistance load = 8Ω, T_A = 25°C, V_{+48V}=48V, V_{+12VDC}=12V, V_{+5VDC}=5V, Ground = 0V

Symbol	Description	Min	Typ	Max	Unit
V_{+48V}	+48V High Voltage Supply[1]	0	48	50	V
V_{+12VDC}	+12V Low Voltage Supply	11.5	12	12.6	V
V_{+5VDC}	+5V Signal Voltage Supply	4.75	5	5.5	V
V_{logic}	Pin 9 is output voltage, but is logic reference only	NA	-	-	NA

Note 1: Amplifier operation with High Voltage supply less than the maximum will result in reduced output power. See Figure 11, “Full Scale Output vs. Power Supply Voltage (8W Load),” on page 20 for typical full scale outputs at reduced power supply voltages.

TABLE 4: DC Voltage Requirements

Symbol	Description	Min	Idle	Max	Unit
I_{+48V}	+48V High Voltage Supply Current, per channel[1]	0	0.03	3[3, 4]	A
I_{LV}	+12V Supply Current[1]	0	0.15[2]	0.2[3]	A
I_{+5V}	+5V Supply Current	0	0.45	0.5	A
I_{logic}	Pin 9 is output voltage, but is logic reference only	-	-	10	mA
I_{HCLTP}	Per-channel short-circuit hard current limit trip point[5]	-	-	20	A

Note 1: Minimum current measured with either the nRESET line asserted active-low, or the overload protection circuit activated for the particular channel

Note 2: Idle current measured with the amplifier in operation, but no input applied

Note 3: Maximum current measured with 1kHz sine wave output at rated power. The MXS100 amplifier module is designed for active crossover applications where each output channel is band limited to a range of frequencies. Under these conditions, and the applications that this amplifier is intended, all channels will not typically need to be driven at full power simultaneously. More typically, the power output requirement for most program material is 1/8 to 1/3 of the total amplifier output capability. However if the amplifier is allowed to be driven into high distortion ("clipping"), the power supply current may approach 20% more than required for a full scale output. It is therefore up to the system designer to determine how much power output will be allowed to produce, and hence determine the maximum and average power supply current requirements.

Note 4: Current specification based on 8Ω loads all channels driven.

Note 5: Hard current limit trip point triggers automatic short-circuit protection (see Section 3.6.1, "Short-Circuit/Over-Current Protection," on page 22).

TABLE 5: DC Current Requirements

1.5 SWITCHING CHARACTERISTICS - SERIAL AUDIO PORT

T_A = 25°C, V_{+48V}=48V, V_{+12VDC}=12V, V_{+5VDC}=5V, Ground = 0V, Sample Rate 32kHz-192kHz

Symbol	Description	Min	Typ	Max	Unit
t_cSCLK	SCLK frequency - SCLK	-	-	12.5	MHz
t_wSCLK	SCLKx pulse width (high and low) - SCLK	40	-	-	ns
t_sLRCLK	LRCLK setup to SCLK rising - LRCLK	20	-	-	ns
t_hLRCLK	LRCLK hold from SCLK rising - LRCLK	20	-	-	ns
t_sSDI	SDIN setup to SCLK rising - SDIN	20	-	-	ns
t_hSDI	SDIN hold from SCLK rising - SDIN	-	-	20	ns

TABLE 6: Serial Audio Port Timing

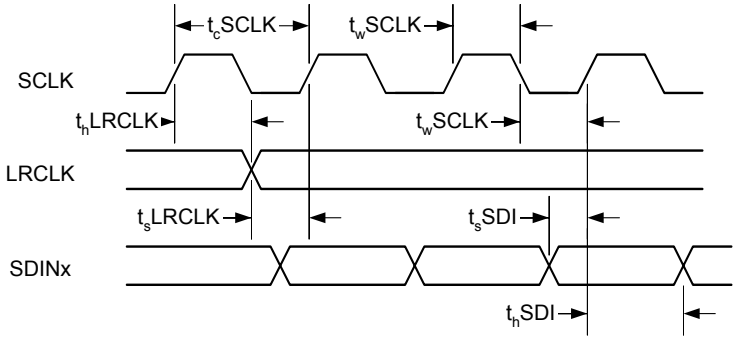

FIGURE 2: Serial Audio Port Timing

PRELIMINARY

1.6 SWITCHING CHARACTERISTICS - PSSYNC PIN

T_A = 25°C, V_{+48V}=48V, V_{+12VDC}=12V, V_{+5VDC}=5V, Ground = 0V

Description	Min	Typ	Max	Unit
PSSYNC Frequency	383	384	385	kHz
PSSYNC Duty Cycle	49	50	51	%

TABLE 7: PSSYNC Pin Characteristics

1.7 SWITCHING CHARACTERISTICS - CONTROL PORT

T_A = 25°C, V_{+48V}=48V, V_{+12VDC}=12V, V_{+5VDC}=5V, Ground = 0V

Symbol	Description	Min	Max	Unit
fSCL	SCL frequency	-	100	kHz
t_{buf}	Bus free time between transmissions	4.7	-	us
t_{wlow}SCL	SCL clock low	4.7	-	us
t_{whigh}SCL	SCL clock high	4.0	-	us
t_sSTA	Setup time for a (repeated) Start	4.7	-	us
t_hSTA	Start condition Hold time	4.0	-	us
t_hSDA	SDA hold from SCL falling (see note)	0	-	us
t_sSDA	SDA setup time to SCL rising	250	-	ns
t_dSDA	SDA delay time from SCL falling	-	3.5	us
t_r	Rise time of both SDA and SCL	-	1	us
t_f	Fall time of both SDA and SCL	-	300	ns
t_sSTO	Setup time for a Stop condition	4.7	-	us
Note: Data must be held sufficient time to bridge the 300ns transition time of SCL				

TABLE 8: Module Control Port Timing

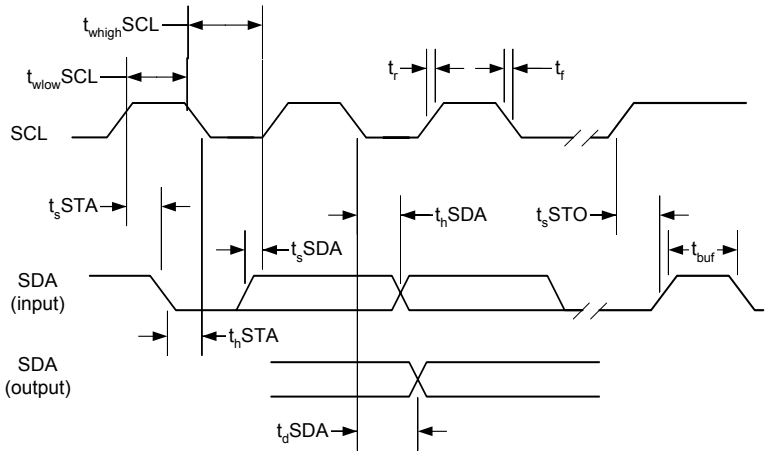

FIGURE 3: Module Control Interface Timing

1.8 PERFORMANCE PLOTS

The following graphs (Figure 4 - Figure 9) show the MXS100 amplifier performance. All inputs are driven with the same input signal, all inputs are mapped to their respective outputs with unity gain (0dBFS input, Master Volume control at 0dB, Channel Attenuation at -6dB). The output channels are tested one at a time and only the output channel being measured is terminated into its rated load. The other outputs are open.

1.8.1 FREQUENCY RESPONSE (1W, 8 OHM LOAD)

Conditions: Typical Supplies, Room Temperature, 24-bit I^2S Input Sampled at 48kHz, Referenced to 1W at 1kHz Sine Wave, 1W Output Power

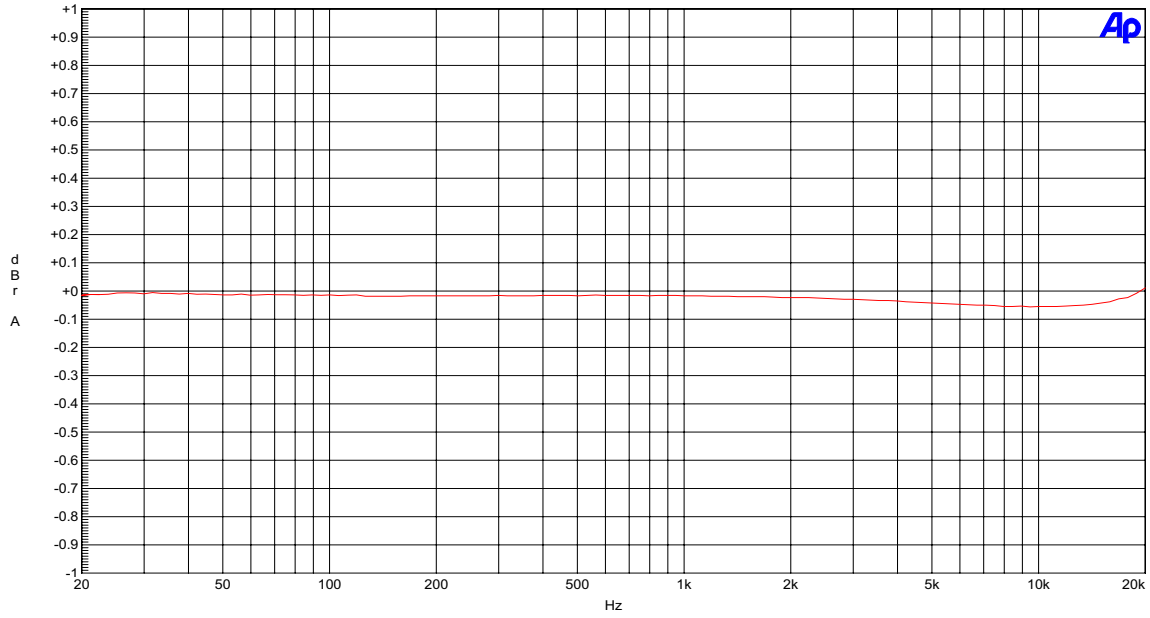

FIGURE 4: Frequency Response

1.8.2 THD+N VS. POWER (4 OHM LOAD)

Conditions: Typical Supplies, Room Temperature, 24-bit I^2S Input Sampled at 48kHz, 1kHz Sine Wave, 4Ω Load, 20kHz AES17 Filter Enabled, +48V

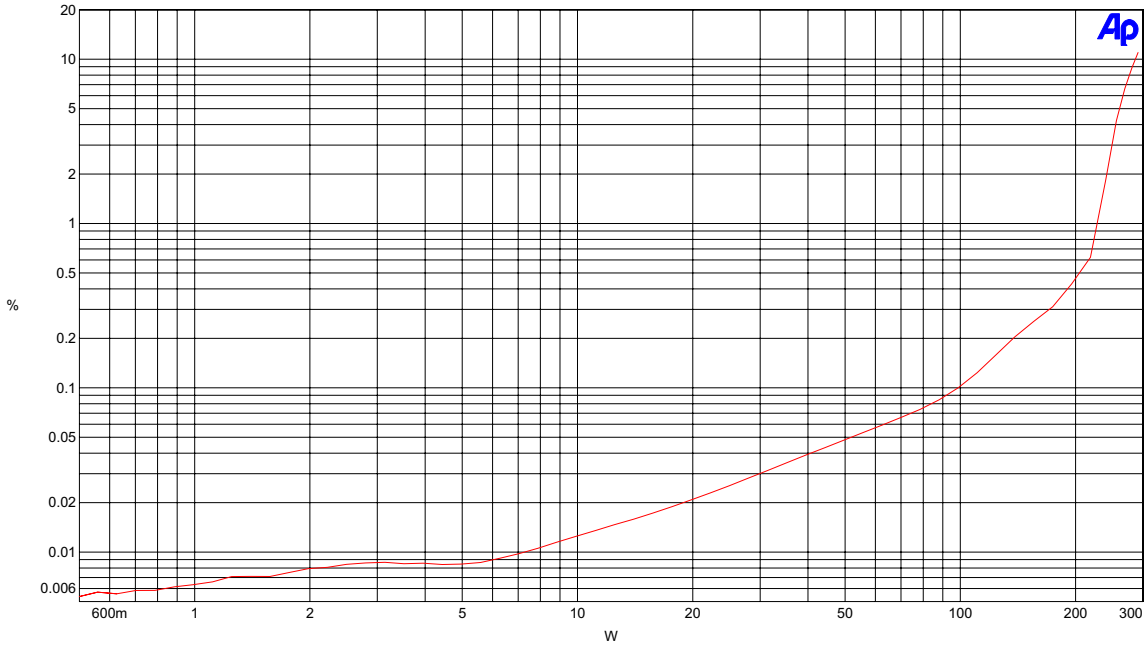

FIGURE 5: THD+N vs. Power (4Ω Load)

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1.8.3 THD+N VS. POWER (6 OHM LOAD)

Conditions: Typical Supplies, Room Temperature, 24-bit I^2S Input Sampled at 48kHz, 1kHz Sine Wave, 6Ω Load, 20kHz AES17 Filter Enabled, +48V

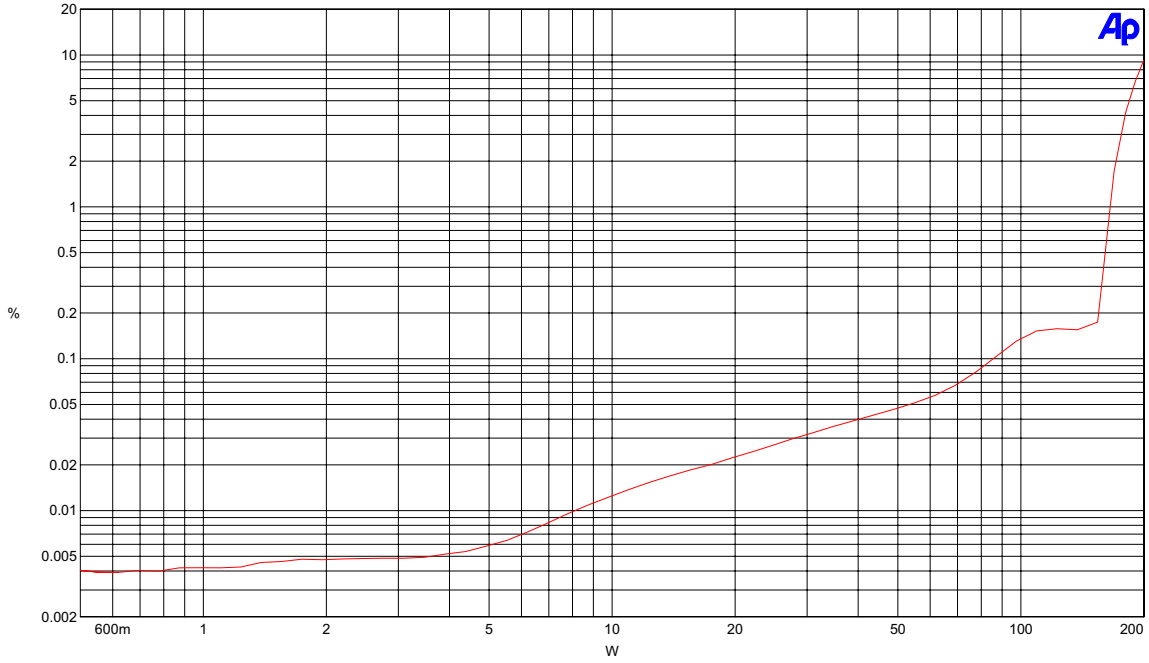

FIGURE 6: THD+N vs. Power (6Ω Load)

1.8.4 THD+N VS. POWER (8 OHM LOAD)

Conditions: Typical Supplies, Room Temperature, 24-bit I^2S Input Sampled at 48kHz, 1kHz Sine Wave, 8Ω Load, 20kHz AES17 Filter Enabled, +48V

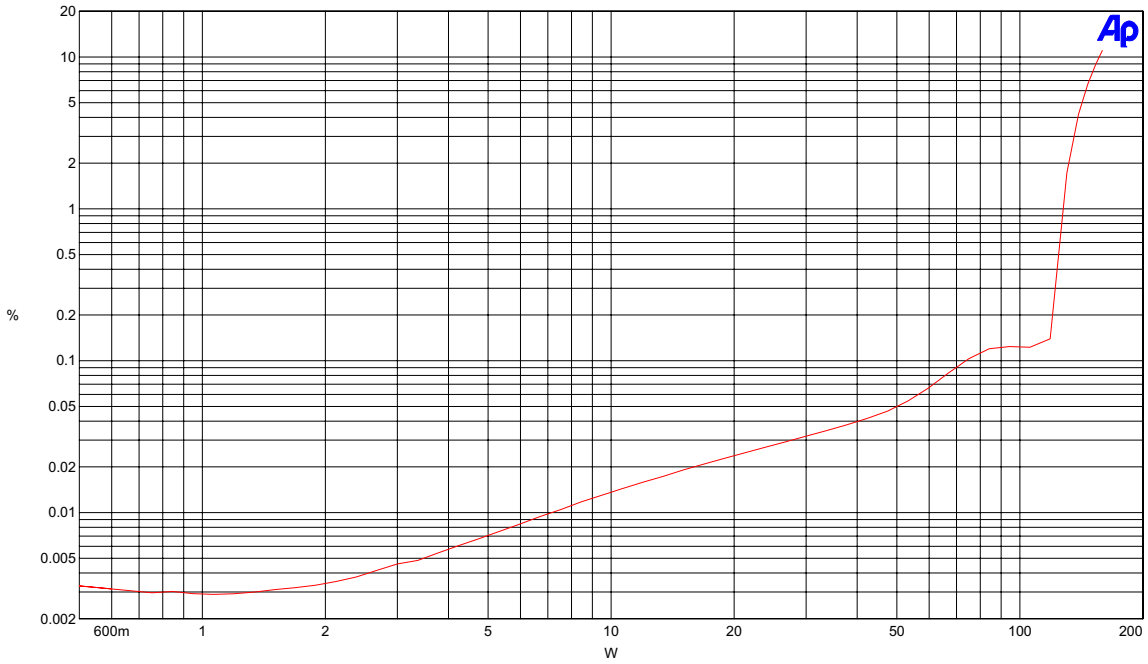

FIGURE 7: THD+N vs. Power (8Ω Load)

1.8.5 THD+N VS. INPUT LEVEL (NOISE FLOOR)

Conditions: Typical Supplies, Room Temperature, 24-bit I^2S Input Sampled at 48kHz, 1kHz Sine Wave, 8Ω Load, 20kHz AES17 Filter Enabled

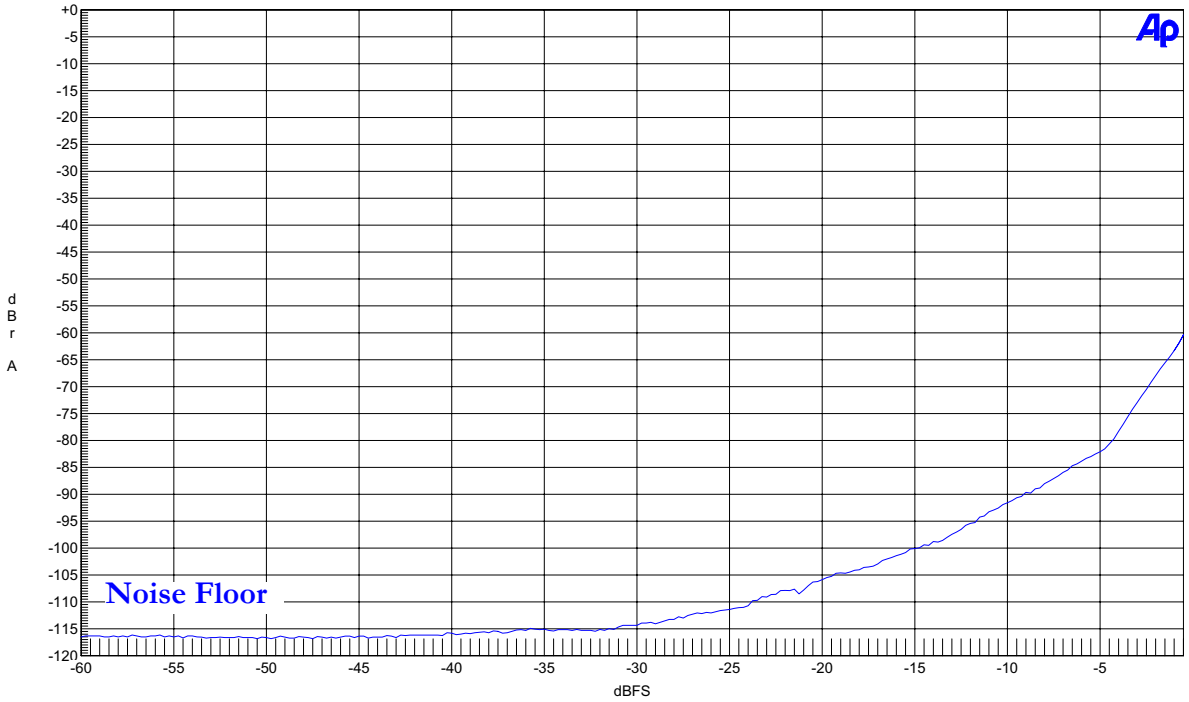

FIGURE 8: THD+N vs. Input Level (1kHz Sine Wave, 8Ω Load)

1.8.6 FFT NOISE FLOOR (8 OHM LOAD)

Conditions: Typical supplies, Room temperature, no input

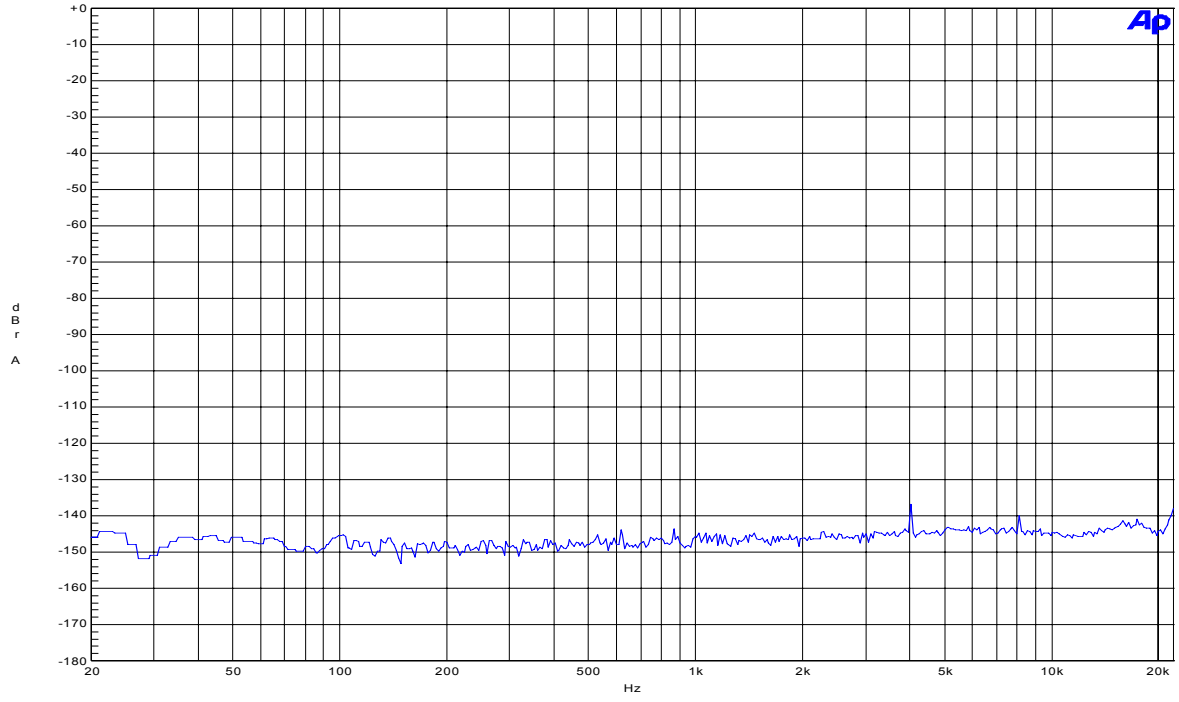

FIGURE 9: FFT Noise Floor

2 AMPLIFIER MODULE PINOUT

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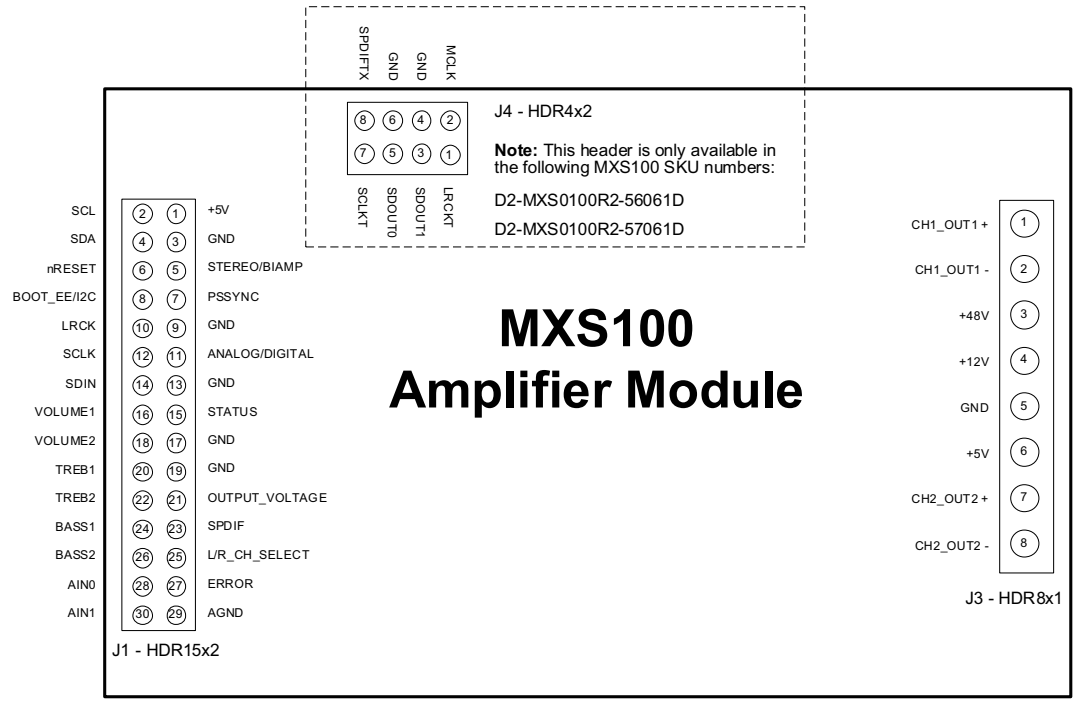

FIGURE 10: MXS100 Amplifier Module Pinout (Top View)

2.1 PIN DEFINITIONS

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Pin #	Pin Name	I/O	Description -
J1/23	SPDIF	I	Channel 1/2 S/PDIF input data
J1/14	SDIN	I	Channel 1/2 I^2S (or Left-Justified) input data
J1/12	SCLK	I	Channel 1/2 serial data bit clock
J1/10	LRCK	I	Channel 1/2 left/right clock
*J4/1	LRCKT	O	Serial Audio Output left/right clock
*J4/2	MCLK	O	Master clock output
*J4/3	SDOUT1	O	Serial Audio Output 1 data
*J4/5	SDOUT0	O	Serial Audio Output 0 data
*J4/7	SCLKT	O	Serial Audio Output clock
*J4/8	SPDIFTX	O	S/PDIF data output
*Note: Header only available in D2-MXS0100R2-56061D and D2-MXS0100R2-57061D			

TABLE 9: Digital Audio Signal Pins

Pin #	Pin Name	I/O	Description
J1/30	AIN1	I	Right Channel analog input
J1/28	AIN0	I	Left Channel analog input

TABLE 10: Analog Input Pins

Pin #	Pin Name	I/O	Description
J1/27	ERROR	O	Overall amplifier error indication, active high
J1/25	L/R_CH_SELECT	I	Hardware input select pin to select Left/Right Channels in Bi-amp mode ONLY!
J1/26	BASS2	I/O	GPIO pin controlling bass levels
J1/24	BASS1	I/O	GPIO pin controlling bass levels
J1/22	TREB2	I/O	GPIO pin controlling treble levels
J1/20	TREB1	I/O	GPIO pin controlling treble levels
J1/18	VOLUME2	I/O	GPIO pin controlling speaker master volume
J1/15	STATUS	O	Amplifier status
J1/16	VOLUME1	I/O	GPIO pin controlling speaker master volume
J1/11	ANALOG/DIGITAL	I	Hardware input select pin to select Analog or Digital input, Analog data input when held high, Digital data input when held low
J1/7	PSSYNC	O	Power supply sychronization clock
J1/8	BOOT_EE/I2C	I	Boot select control, interface to external controller
J1/5	STEREO/BIAMP	I	Hardware input select pin to select Stereo or Bi-Amp speaker mode
J1/6	nRESET	I	Amplifier reset, active low, open collector drive
J1/4	SDA	I/O	Module control interface data
J1/2	SCL	I/O	Module control interface clock

TABLE 11: Control Signal Pins

Pin #	Pin Name	I/O	Description
J3/1	CH1_OUT1+	O	Channel 1 Positive Loudspeaker Output
J3/2	CH1_OUT1-	O	Channel 1 Negative Loudspeaker Output
J3/7	CH2_OUT2+	O	Channel 2 Positive Loudspeaker Output
J3/8	CH2_OUT2-	O	Channel 2 Negative Loudspeaker Output

TABLE 12: Loudspeaker Output Pins

Pin #	Pin Name	I/O	Description
J1/29	AGND	-	Analog ground for analog inputs
J1/3, J1/9, J1/13, J1/17, J1/19, J3/5, *J4/4, *J4/6	GND	-	General purpose ground
J3/3	+48V	-	+48V DC High Voltage Supply
J3/4	+12V	-	+12V DC Supply
J1/1, J3/6	+5V	-	+5V DC Supply
J1/7	OUTPUT_VOLTAGE	O	Regulated +3.3V output, logic reference only
*Note: Header only available in D2-MXS0100R2-56061D and D2-MXS0100R2-57061D			

TABLE 13: Power Supply Pins

2.2 PIN DESCRIPTIONS - (*=OPTIONAL)

2.2.1 DIGITAL SERIAL AUDIO INPUTS (SAI PORTS)

LRCK — **Left/Right Clock**

This pin is the framing clock for the Serial Audio Input. The serial input data is transmitted as two channels every sample rate period. LRCK determines the start of each data pair. The LRCK frequency determines the input sample rate (Fs). The LRCK pin support a 3.3V input.

SCLK — **Shift Clock**

This pin is the shift clock for the Serial Audio Input. The shift clock is used to frame each input bit of the serial input data. The shift clock frequency is typically 64*Fs. The SCLK pin supports a 3.3V input.

SDIN — **Serial Data Input**

This pin is the serial data input. Input format options are I^2S or Left-Justified. 16, 18, 20, and 24 bit data lengths are supported. The SDIN pin supports a 3.3V input.

2.2.2 DIGITAL SERIAL AUDIO OUTPUTS (SAO PORTS)

MCLK — **Master System Clock Output**

This pin is the master clock output. The master clock is an integer multiple of the LRCK frequency. The default master clock is 12.288MHz, which corresponds to a 48kHz sample rate (Fs) * 256.

LRCKT — **Output Left/Right Clock**

This pin is the framing clock for the Serial Audio Output. The serial output data is transmitted as two channels every sample rate period. LRCKT determines the start of each data pair. The LRCKT frequency determines the output sample rate (Fs). LRCKT is a 3.3V output.

SCLKT — **Output Shift Clock**

This pin is the shift clock for the Serial Audio Output and is used to frame each bit of the serial output data. The shift clock frequency is typically 64*Fs. SCLKT is a 3.3V output.

SDOUT[1:0] — **Serial Data Outputs**

These pins provides one Serial Data Output. Serial Data is arranged as one left/right pair. SDOUT is a 3.3V output.

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2.2.3 DIGITAL S/PDIF AUDIO

***SPDIF** — **S/PDIF Data Input**

This pin is the S/PDIF audio input and accepts 3.3V stereo linear PCM audio data up to 192kHz. An appropriate transformer or optical coupler is necessary for the external interface. To drive this pin, appropriate buffer and isolation circuits are necessary to convert the S/PDIF cable input signal into a clean logic level.

SPDIFTX — **S/PDIF Data Output**

This pin contains an identical audio output as SDOUT[1]. SPDIFTX enables a COMPLETELY INDEPENDENT Post-Processed PCM data path routed from one or more of the inputs to the MXS100. SDIFTX can be connected to a consumer electronic product such as a DVD-Recorder, CD-Recorder, MD-Recorder, DAT-Recorder, or other digital audio recording device that accepts a S/PDIF input. The output of this pin has a fixed Fs of 48kHz, regardless of the Fs of the digital audio input. SPDIFTX is a 3.3V output.

2.2.4 ANALOG INPUTS

***AIN[0:1]** — **Analog Inputs**

Each pair of AIN pins is an unbuffered analog input. Each input is terminated with 20kΩ, then AC-coupled to the internal input. The analog inputs are selected by pulling the ANALOG/DIGITAL pin high while valid data is not present on the SAI (I^2S) input.

2.2.5 CONTROL SIGNAL PINS

BOOT_EE/I2C — **Boot Selection - Input, Internal Pull-up**

This pin is the boot selection input. The boot selection picks the source location for the DSP boot code and is used for firmware upgrades. This pin is pulled high internally to +3.3V via a 10kΩ resistor.

ERROR — **Amplifier Error - Output**

When high (3.3V), ERROR either indicates that a fault condition has occurred in the amplifier, or that the amplifier has not been initialized. Fault conditions include over-temperature, over-current, short circuit, and output power stage disabled. See Section 3.6, “Amplifier Overload Protection,” on page 22 for further details. The pin sources up to 5mA and may be used to directly drive an external LED with appropriate current limiting resistance.

nRESET — **Reset - Input, Internal Pull-up**

This pin is the active-low reset input to the amplifier module. Driving the nRESET low for 10 ms brings all internal devices to their default state. During the power on sequence, nRESET must be active (low) during the high voltage supply ramp period. The reset pin must be held for a minimum of 100ms after the high voltage supply reaches 95% of its nominal value. The reset pin must be driven with an open collector or open drain driver. This pin is pulled high internally to 3.3V via a a 10kΩ resistor.

PSSYNC — **Power Supply Synchronization - Output**

This pin is a power supply synchronization output. It may be used to synchronize an external switching power supply to the 384kHz PWM output switch rate.

STATUS — **Amplifier Status - Output**

This pin indicates the internal status of the amplifier. STATUS switches to 3.3V when the amplifier has completed internal initialization and is active. The pin will source up to 5mA and may be used to directly drive an external LED with appropriate current limiting resistance.

ANALOG/DIGITAL — **Analog/Digital Input Selection - Input, Internal Pull-up**

When tied low, ANALOG/DIGITAL selects the SPDIF pin as the input source for channels 1 and 2. When tied high or left unconnected, ANALOG/DIGITAL enables the analog input source AIN0 and AIN1 or the SAI(I^2S) digital input as the input source to channels 1 and 2. If valid data is not present on the I^2S digital inputs, the amplifier defaults to the analog inputs. Changes on the ANALOG/DIGITAL input or the I^2S digital input will result in an immediate change to the input source to channel 1 and 2. This pin is pulled high internally to 3.3V via a 10kΩ resistor.

SCL — **SCL - Input, Internal Pull-up**

The SCL pin is the serial clock line of the 2-wire serial control interface. This pin is pulled high internally to 3.3V via a 10kΩ resistor.

SDA — **Serial Data - Input, Internal Pull-Up**

The SDA pin is the bidirectional serial data line of the 2-wire serial control interface. This pin is pulled high internally to 3.3V via a 10kΩ resistor.

PRELIMINARY

BASS [2:1] **BASS Level Control - Input, Internal Pull-up**

The BASS1 and BASS2 pins are general purpose input pins that may be used to control bass levels on channels 1 and 2. The designer should take into consideration that these input pins have no sense of the bass level control knob absolute position. Turning the knob clockwise increases the bass level, turning the knob counter-clockwise decreases the level. Adjustments to these input pins are relative only. For designs requiring sensing of the absolute position of the bass knob position, this may be accomplished using an external microcontroller. These pins are internally pulled up to +3.3V via a 10kΩ resistor.

TREBLE [2:1] **TREBLE Level Control - Input, Internal Pull-up**

The TREBLE1 and TREBLE2 pins are general purpose input pins that may be used to control treble levels on channels 1 and 2. The designer should take into consideration that these input pins have no sense of the treble level control knob absolute position. Turning the knob clockwise increases the treble level, turning the knob counter-clockwise decreases the level. Adjustments to these inputs are relative only. For designs requiring sensing of the absolute position of the treble knob position, this may be accomplished using an external microcontroller. These pins are internally pulled up to +3.3V via a 10kΩ resistor.

VOLUME [2:1] **Volume Level Control - Input, Internal Pull-up**

The VOLUME1 and VOLUME2 pins are general purpose input pins that may be used to control the master volume on channels 1 and 2. The designer should take into consideration that these pins have no sense of the master volume control knob absolute position. Turning the knob clockwise increases the volume level, turning the knob counter-clockwise decreases the level. Adjustments to this input are relative only. For designs requiring sensing of the absolute position of the master volume knob position, this may be accomplished using an external microcontroller. These pins are internally pulled up to +3.3V via a 10kΩ resistor.

L/R_CH_SELECT **Left/Right Channel Selection - Input**

The L/R_CH_SELECT pin is a selector pin that is used to select Left or Right Channels for Input. When the L/R_CH_SELECT pin is high, the Left Channel input is selected, and when this pin is Low the Right Channel input is selected. The setting of this pin is only applicable when the module is in Bi-Amp mode. This pin **must** be tied high or low if not connected to mode switching logic, this pin is a pure input that cannot be left unconnected

STEREO/BIAMP **Stereo/Bi-Amp Output Selection - Input**

The STEREO/BIAMP pin is a selector pin used to configure the speakers for Bi-Amp or Stereo audio distribution and is used primarily for product demonstration. When the STEREO/BIAMP pin is high, the module is configured for stereo mode, and when the pin is low, the module is configured for bi-amplification mode. This pin **must** be tied high or low if not connected to mode switching logic, this pin is a pure input that cannot be left unconnected.

2.2.6 LOUDSPEAKER OUTPUTS

CH[2:1]_OUT **Loudspeaker Channel Outputs 1 and 2**

These pins provide the power amplifier outputs 1 and 2. Each amplifier channel is a full-bridge output configuration consisting of a positive (+) and negative (-) output. The outputs must remain floating and must not be connected to ground.

3 AMPLIFIER OPERATION

The amplifier module may be operated with any combination of analog or digital inputs. The amplifier has one digital serial audio input, one optional stereo analog input, and one optional S/PDIF digital audio input. The ANALOG/DIGITAL pin provides a means to select between the optional S/PDIF digital audio input and the optional analog audio input. The digital Serial Audio Input port allows for driving I^2S or Left-Justified digital audio to the module at any time when the state of the ANALOG/DIGITAL pin is high. The amplifier system processor monitors the ANALOG/DIGITAL, L/R_CH_SELECT, and STEREO/BIAMP pins. Any change of state with these input pins are processed immediately.

3.1 HARDWARE CONFIGURATION

The ANALOG/DIGITAL pin provides a means to select between the optional analog inputs for channels 1 and 2 vs. the optional S/PDIF digital audio input through hardware. The SAI port, when I^2S or Left-Justified digital audio input is active, is available when the ANALOG/DIGITAL pin is active high. Hardware source selection pins are monitored by the system processor and any change of state is processed immediately. Alternatively, the input selection can be made through the register interface via software commands, which override the hardware settings - see Section 5, “Module Control Interface (MCI) Specification,” on page 23.

The following table illustrates the functionality of the hardware configuration pins on the module. Note that when tied low, the setting of the SPDIF pin overrides the setting of the ANALOG/DIGITAL pin.

ANALOG/DIGITAL Setting	Input Source Selection
ANALOG/DIGITAL = 0	S/PDIF input connected to channels 1/2.
ANALOG/DIGITAL = 1 (SAI Inactive)	Stereo Analog Inputs connected to channels 1/2.
ANALOG/DIGITAL = 1 (SAI Active)	SAI port connected to channels 1/2.

TABLE 14: Audio Source Selection using Hardware Pins

3.2 ACTIVATING THE AMPLIFIER

After reset the MXS100 amplifier module DSP boots from internal EEPROM. The two boot mode selections are defined in the following table.

BOOT_EE/I2C	Description
1	Module boots from internal EEPROM - default setting since the pin is pulled high internally
0	Module boots from external MCI at address 0xB2

TABLE 15: Boot Selection

When BOOT_EE/I2C is high, the amplifier will boot from the internal EEPROM. When BOOT_EE/I2C is low, the amplifier gets the boot code from an external device via the Module Control Interface. An external controller is expected to load the boot code. The BOOT_MCI/I2C pin is used primarily for field firmware upgrades.

3.3 POWER SUPPLY AND POWER ON RESET

An internal reset circuit generates the nRESET signal for the amplifier. On power-up any externally applied nRESET must be greater than 200ms in duration, after the 5V supply is stable. The nRESET input has an internal 10kΩ, pullup to 3.3V.

3.3.1 POWER SUPPLY VOLTAGE VS. OUTPUT POWER

The MXS100 amplifier may be operated at any high voltage supply between 0 and +48V. The typical full scale output power is a function of the high voltage power supply. Figure 11 below shows a typical full scale output with respect to the power supply voltage. The data is derived from the following parameters:

- Input Signal: 1kHz, -0.5dBFS, 24-bit data, 48kHz Sampling Frequency
- Input Signal Delivery Format: I^2S Audio
- Bandwidth: 20Hz to 20kHz
- Filters Used: 20kHz AES17 Filter

FIGURE 11: Full Scale Output vs. Power Supply Voltage (8Ω Load)

3.3.2 POWER SUPPLY SEQUENCING AND RESET

When powering up the MXS100 module, the parameters below **must** be followed (see also the flowchart in Figure 12 and the waveform diagram in Figure 13, below):

Low-Voltage Supplies (+12V, +5V):
- 10% to 90% voltage ramp rate >= 1.5V/mS

High-Voltage Supply (+48V):
- 10% to 90% voltage ramp rate <= 1.5V/mS

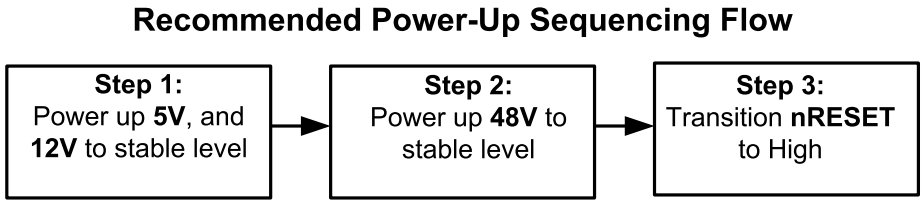


FIGURE 12: Power-Up Sequencing Flow Diagram

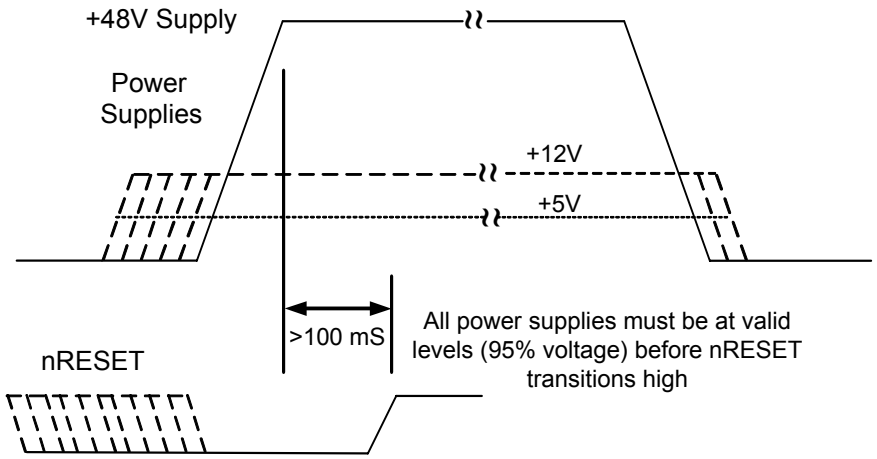


FIGURE 13: Power Supply Sequencing

When powering down the MXS100 module, the amplifier must have nRESET asserted active-low prior to transitioning the power supplies. The +12V and +5V supplies must not drop below their respective minimum values until the +48V supply falls below +12V.

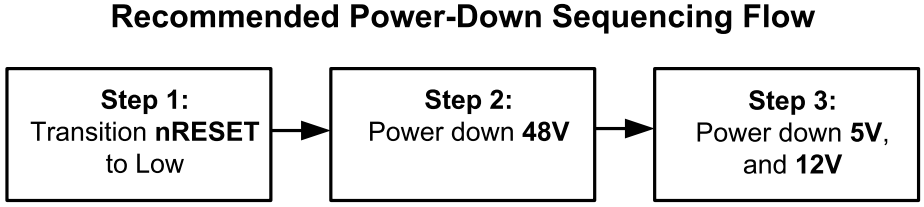


FIGURE 14: Power-Down Sequencing Flow Diagram

It is acceptable to use voltage regulators to derive the +12V and +5V from the +48V supply if only a single +48V supply is available in the system. The +12V and +5V supplies must not drop below minimum specified operating values at any time if the +48V supply exceeds +12V.

3.4 ADJUSTING CONTROL SETTINGS

All control settings for the amplifier are adjusted by writing to configuration registers through the module control interface (see Section 4, "Digital Audio Interface," on page 23). The DSP within the module will automatically provide a smooth transition between changes to control settings in order to avoid pops. It is recommended that input selection be changed with the amplifier muted.

3.5 OPERATIONAL LIMITATIONS

Do not operate the module at audio frequencies greater than 20kHz with no load. Peaking in the output filter can cause the output voltages to exceed the filter capacitor voltage rating. Avoid using continuous test tones above 20kHz.

3.6 AMPLIFIER OVERLOAD PROTECTION

The amplifier monitors output current in each loudspeaker channel and the heat sink temperature. The current sensors protect the loudspeaker channels from over-current and short-circuit faults. The temperature sensor protects the amplifier from excessive operating temperature. Configuration and register settings are not altered by amplifier protection actions.

3.6.1 SHORT-CIRCUIT/OVER-CURRENT PROTECTION

If a short-circuit or over-current event is detected, the affected loudspeaker output channel will be disabled, and the module will drive the nERROR output to active low. Recovery from a short-circuit or over-current shutdown is automatic.

Automatic Short Circuit Protection – Prevents amplifier damage against shorts between the amplifier loudspeaker output terminals and shorts to system ground. Short-circuit protection acts on a per output basis, and is module dependent (see Table 5 on page 9). If a loudspeaker channel experiences a short-circuit, then only that channel is disabled, while the other channels are unaffected. If a short-circuit is detected after the 10th attempt to recover, then the channel that caused the short is permanently disabled, and will not produce output until module power is cycled. The nERROR signal stays active while the channel is disabled.

Automatic Current Limit Protection – Limits the maximum output current that is available for each loudspeaker output channel. The over-current protection will soft current limit to a module-dependant maximum.

For example, in Figure 15 below, a short-circuit resulting in an over-current is detected, which triggers an immediate disabling of the shorted loudspeaker channel and assertion of nERROR. After 5 seconds, the channel is reactivated, and nERROR is deasserted. Then another short-circuit/over-current is detected, resulting in another shutdown and assertion of nERROR. If the amplifier resumes normal operation, the shutdown sequence stops. However, if the short-circuit/over-current event continues, the output channel will permanently shutdown after the 11th event. If a permanent shutdown occurs, the amplifier module must be power-cycled to re-enable the affected channel.

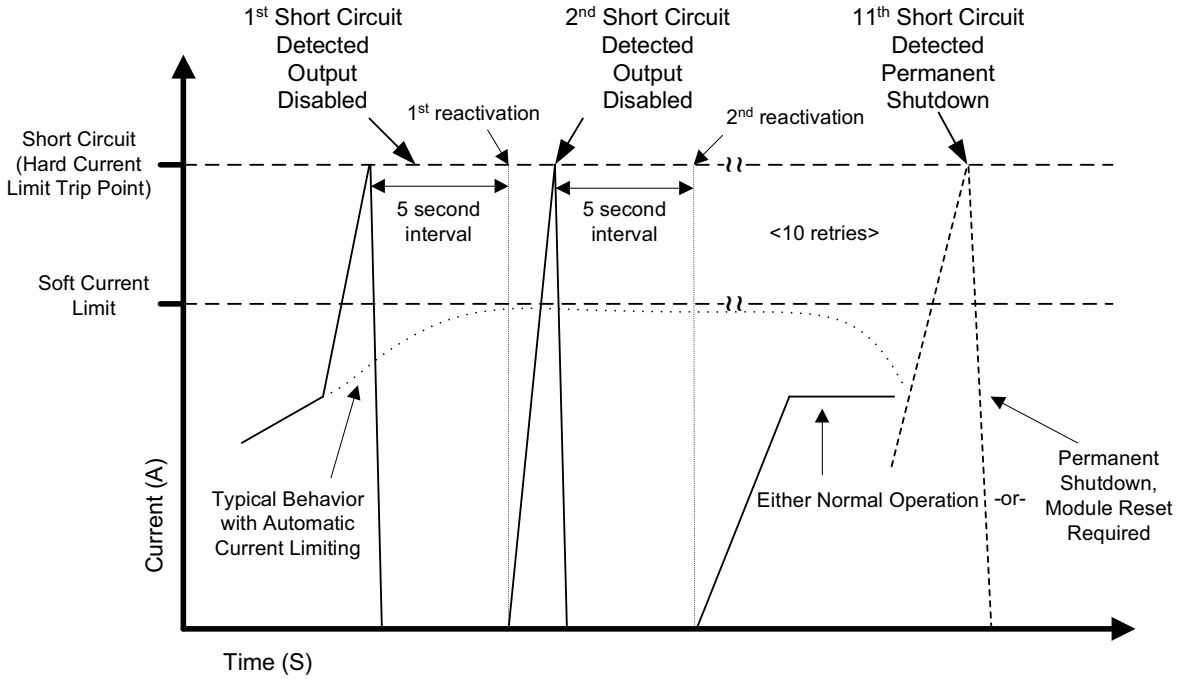


FIGURE 15: Automatic Current Protection Example

3.6.2 OVER-TEMPERATURE PROTECTION

An temperature sensor monitors the amplifier's temperature. As the internal temperature begins to reach critical levels, the controller will begin to limit the output power. If the temperature exceeds the critical level, the amplifier will shut down all output channels and the nERROR output will be driven low indicating an over-temperature fault. Recovery from an over-temperature shut down is automatic and includes an amount of hysteresis to allow for proper cooling before reactivation. See Section 7.3, "Ambient Operating Conditions," on page 46 for normal operating temperature ranges.

4 DIGITAL AUDIO INTERFACE

The MXS100 amplifier module has one digital Serial Audio Input (SAI) port as well as one optional S/PDIF digital audio input.

4.1 SERIAL AUDIO INPUTS (SAI PORTS)

The MXS100 module contains one SAI port. The SAI port Each input can support a sample rate from 32kHz to 192kHz. All digital audio inputs are +3.3V CMOS logic. The SAI port is designed to interface with standard digital audio components and to accept I^2S or Left-Justified data formats.

For I^2S format, the left channel data is read when LRCK is low. For the Left-Justified (LJ) format, the left channel data is read when LRCK is high. The I^2S format requires that the MSB of the SDIN data word start after one SCLK delay after the transition of the LRCK, while the Left-Justified (LJ) format requires that the MSB of the SDIN data word start immediately after the transition of the LRCK. Either format requires data to be valid on the rising edge of SCLK and sent MSB-first on SDIN with 32 bits of data per channel. Each set of digital inputs may run asynchronously to the others and may accept different sample rates and formats.

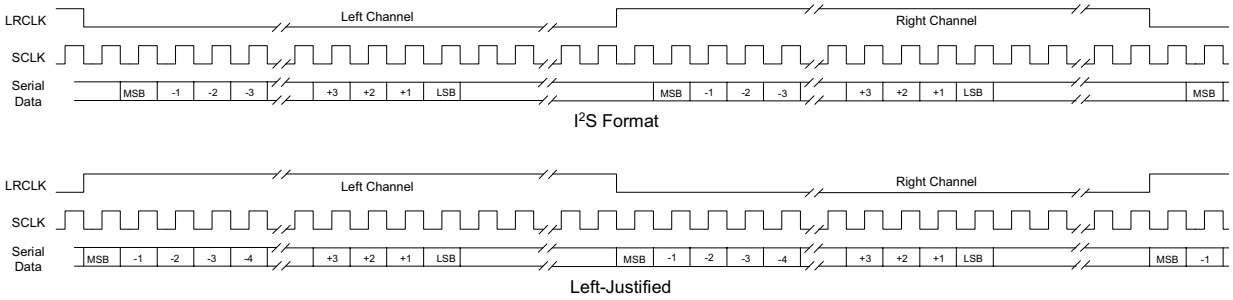


FIGURE 16: Digital Audio Data Formats

5 MODULE CONTROL INTERFACE (MCI) SPECIFICATION

The controller inside the MXS100 amplifier module provides a number of registers used to control operation. The Module Control Interface (MCI) is used to set and query these registers through the SDA and SCL pins. This protocol defines any device that sends data on to the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. For this interface, the definition of the master is an external microcontroller or control logic. All modules in the system are logically slaves to the external microcontroller. The master always starts the transfer and provides the serial clock for synchronization. The MXS100 module controller only functions as a slave device in all of its communications and will not function with multiple masters.

5.1 HARDWARE CONTROL INTERFACE STATES

5.1.1 DATA TRANSITION OR CHANGE

During a data transfer, changes on the SDA line must only occur while SCL is in the low state. An SDA transition while SCL is high is used to identify a START or STOP condition.

5.1.2 START CONDITION

START is identified by a high to low transition of SDA while SCL is stable in the high state. A START condition must precede any command for data transfer.

5.1.3 STOP CONDITION

STOP is identified by low to high transition of SDA while SCL is stable in the high state. A STOP condition terminates communication between the MXS100 module and the bus master.

5.1.4 DATA INPUT

During the data input, the MXS100 module samples the SDA signal on the rising edge of SCL. For correct device operation the SDA signal must be stable during the rising edge of SCL and SDA can change only when SCL is low.

5.1.5 ACKNOWLEDGE

All data transfers across the module control interface must be acknowledged. Each byte transferred is followed by an acknowledge bit (ACK). When data is being written to the module, it will generate the ACK; when being read, the bus master generates the ACK. ACK refers to a true-acknowledge and NACK refers to a not-acknowledge. In general, ACK means continue or ready and NACK means terminate or not ready. The bus master is responsible for correctly interpreting the acknowledge response.

5.2 AMPLIFIER MODULE ADDRESSING

To start communication between the master and the MXS100 amplifier module, the master must initiate with a start condition. Following this, the master sends onto the SDA line 8-bits (MSB first) corresponding to the device select address and read or write mode. If the device address matches that of the MXS100 amplifier module, the module will acknowledge the address during the 9th bit. The 7 most significant bits are the device address identifiers. The 8th bit (LSB) identifies read or write operation, R/W. This bit is set to 1 in read mode and 0 for write mode.

One hardware device address (B2h) is used to identify the MXS100 amplifier module.

5.3 CONTROLLER I/O PROCEDURES

5.3.1 CONTROLLER WRITE PROCEDURE

All writes to the MXS100 amplifier module controller registers must begin with the Start Condition, followed by the Device Address byte (with read/write bit cleared), three Register Address bytes, three Data bytes and a Stop Condition (see Figure 17). The MXS100 amplifier module slave controller acknowledges each byte by pulling SDA low on the bit immediately following each byte. These bytes are described below:

Byte	Read/Write	Name	Description
0	W	Device Address + Read/Write Bit	Device Address of channel group, with R/W bit cleared
1	W	Register Address [23:16]	Upper 8 bits of register address
2	W	Register Address [15:8]	Middle 8 bits of register address
3	W	Register Address [7:0]	Lower 8 bits of register address
4	W	Data[23:16]	Upper 8 bits of register data to write
5	W	Data[15:8]	Middle 8 bits of register data to write
6	W	Data[7:0]	Lower 8 bits of register data to write

Table 16: Controller Write Byte Description

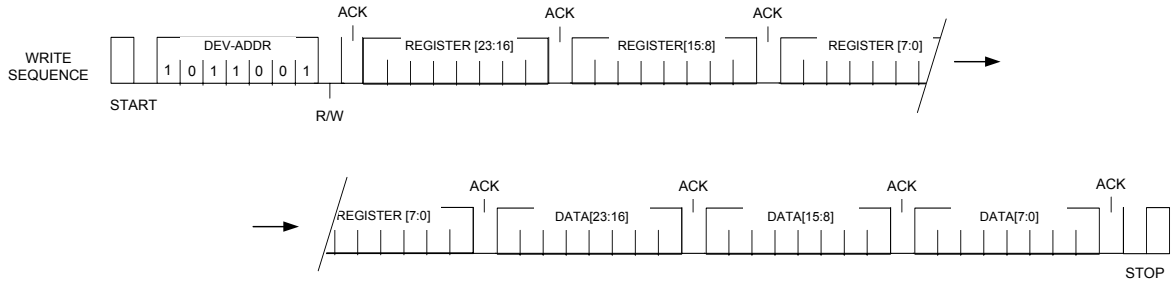


FIGURE 17: Controller Write Sequence Diagram

5.3.2 CONTROLLER READ PROCEDURE

All reads from the MXS100 amplifier module controller registers require two steps. During the first step, the master must send the Start Condition, followed by the Device Address byte (with read/write bit cleared), Initialization byte and two Register Address bytes (see Figure 18). The MXS100 amplifier slave controller acknowledges each byte in the first step by pulling SDA low on the bit immediately following each byte.

Immediately following the first step, the master must send another Start Condition, followed by the Device Address byte (with read/write bit set). The MXS100 amplifier slave controller will acknowledge the Device Address byte by pulling SDA low on the bit immediately following the Device Address. The next 3 bytes are sent by the MXS100 amplifier slave controller to the master, and contain the three Data bytes to be read. The master must acknowledge the first two Data bytes by pulling SDA low on the bit immediately following the Device Address. After the third Data byte, the master should not send an acknowledgement to the slave. At the end of the second step, the master must send the Stop Condition.

Step	Byte	Master Read/Write	Name	Description
1	0	W	Device Address + Read/Write Bit	Device Address of channel group, with R/W bit cleared
	1	W	Register Address [23:16]	Upper 8 bits of register address
	2	W	Register Address [15:8]	Middle 8 bits of register address
	3	W	Register Address [7:0]	Lower 8 bits of register address
2	Repeat Start Condition			
	4	W	Second Device Address + Read/Write Bit	Device Address of channel group, with R/W bit set
	5	R	Data[23:16]	Upper 8 bits of register data to read
	6	R	Data[15:8]	Middle 8 bits of register data to read
	7	R	Data[7:0]	Lower 8 bits of register data to read

Table 17: Controller Read Byte Description

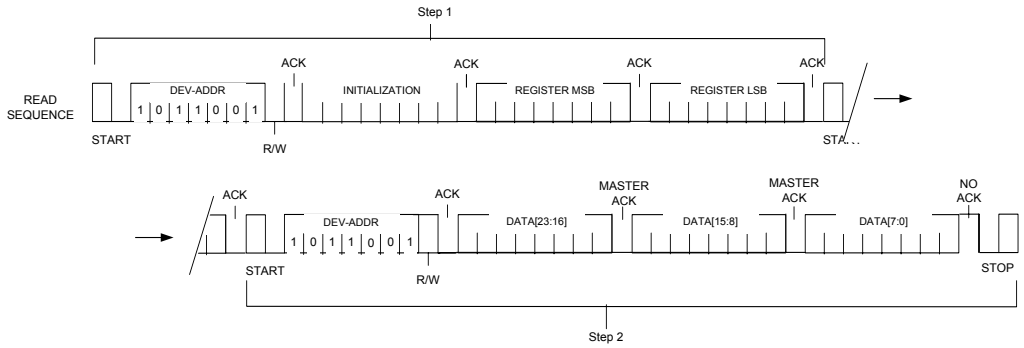


FIGURE 18: Controller Read Sequence Diagram

PRELIMINARY

5.3.3 STORE TO EEPROM COMMAND

A EEPROM within the amplifier module stores the default values of each register for recall on reset or power up. The default values in the EEPROM when shipped from the factory set all software settings to flat or disabled, with each Channel Attenuation at -12dB and the Master Volume at 0dB. Note that the default values for input selection are determined by the Hardware Configuration Pins and not by the EEPROM. The amplifier has the capability to update the EEPROM contents at any time.

The following module control interface command will cause all of the current software settings to become the default settings by storing them into the EEPROM. Note: The input source selection is not stored in the EEPROM. The input source is selected at power up or module reset. If an input source is changed via software control, its configuration will be lost at power down or during reset.

Byte	Read/Write	Name	Description
0	W	Device Address + Read/Write Bit	Device Address of channel group, with R/W bit cleared
1	W	Register Address [23:16]	Set to 0x80 for EEPROM write
2	W	Register Address [15:8]	Set to 0x00 for EEPROM write
3	W	Register Address [7:0]	Set to 0x00 for EEPROM write
4	W	Data[23:16]	Set to 0x00 for EEPROM write
5	W	Data[15:8]	Set to 0x00 for EEPROM write
6	W	Data[7:0]	Set to 0x00 for EEPROM write

TABLE 18: Store to EEPROM Command Byte Description

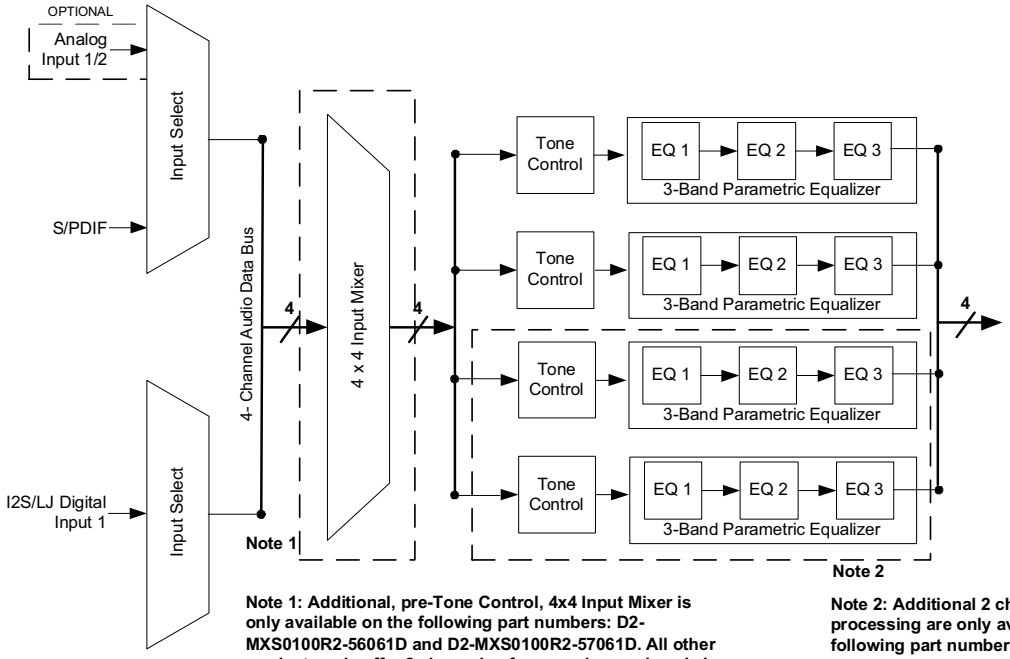
6 SOFTWARE CONTROL SETTINGS

All control settings for the amplifier are adjusted by writing to configuration registers through the Module Control Interface (see Section 5, “Module Control Interface (MCI) Specification,” on page 23).

6.1 DSP PROCESSING ORGANIZATION

The MXS100 amplifier module controller contains a powerful DSP engine, which provides a wide range of audio processing functions through each channel of the amplifier module. Each channel contains a group of input processing blocks, a mixer, and a group of output processing blocks. The input blocks include Input Select, Tone Control and 3-band Parametric EQ for each channel. The mixer block can mix/route any amplifier inputs to any amplifier output. The output processing blocks include Programmable Filters, 5-band Parametric EQ, Adjustable Time Delay, Compression, and Level Control for each channel. A Master Volume setting controls the level of all channels within the amplifier module.

The signal-flow through the DSP processing blocks is organized as shown in Figure 19 and Figure 20 below:



Note 1: Additional, pre-Tone Control, 4x4 Input Mixer is only available on the following part numbers: D2-MXS0100R2-56061D and D2-MXS0100R2-57061D. All other products only offer 2 channels of processing, and no 4x4 Input Mixer is located here. The default routing is Channel 1 in, Channel 1 out; Channel 2 in, Channel 2 out, etc. to maintain backwards compatibility.

Note 2: Additional 2 channels of processing are only available on the following part numbers: D2-MXS0100R2-56061D and D2-MXS0100R2-57061D. All other products only offer 2 channels of audio processing.

FIGURE 19: DSP Input Processing Blocks

PRELIMINARY

PRELIMINARY

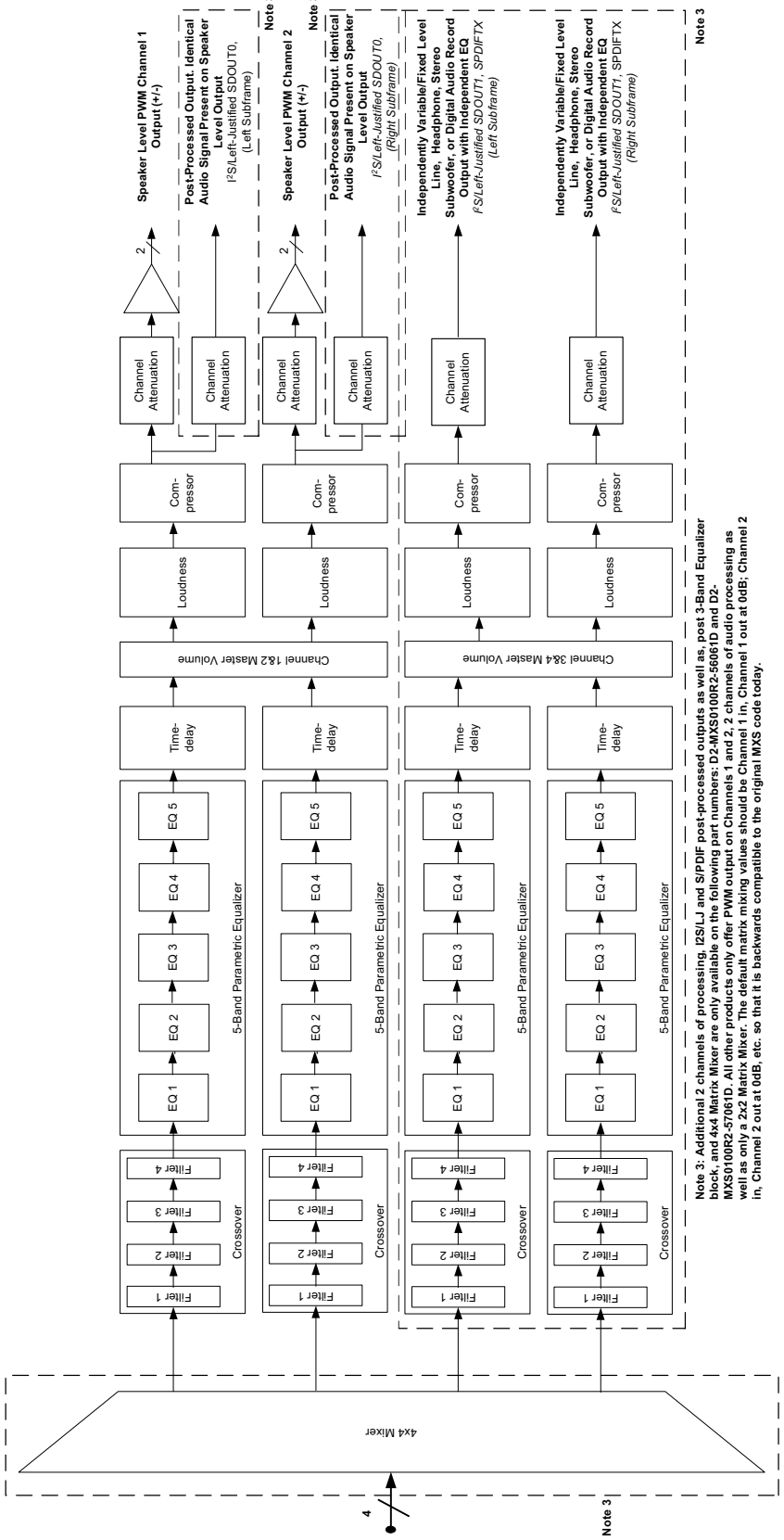


FIGURE 20: DSP Output Processing Blocks

6.2 GAIN MANAGEMENT

Careful attention must be paid to the signal level at the input and at each stage through the DSP in order to prevent clipping. Changes to DSP parameters must be made only after thorough consideration of the effects on signal level throughout the entire signal path from input to output. **Though reducing the gain of the input signal will result in additional DSP headroom, this action will cause a corresponding reduction in the signal-to-noise ratio of the amplifier.**

6.2.1 DSP GAIN STRUCTURE

At the input to the DSP, an attenuation of -6dB is applied to allow for headroom within the DSP processing blocks. At the DSP output, +18dB of gain is applied prior to driving the PWM amplifier outputs. This organization is shown in the following figure:

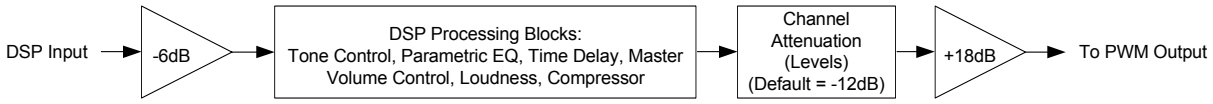


FIGURE 21: DSP Gain Stages

Once a signal is input, 6dB of headroom is provided for all of the DSP processing blocks and volume controls. Clipping will occur if any of the DSP processing blocks cause the signal level to exceed 0dBFS. At the DSP processing final stage, a maximum of 18dB of gain is added prior to the PWM amplifier outputs. The module is designed to output full power (assuming the high-voltage supply is at the correct voltage) with a -0.5dBFS input signal, all other DSP processing functions and individual channel volume controls at unity gain, and the output master volume control set to +6dB.

6.2.2 GAIN CALCULATIONS

Proper gain management begins with determining the maximum amplifier input level that is expected for the system design. If the S/PDIF or I^2S inputs are used, the maximum level can be as high as 0dBFS if connected directly to source material. If the analog inputs are used, a 2Vrms signal is required to produce an input of 0dBFS to the DSP.

6.3 SOFTWARE REGISTER ADDRESSING

Changes to each of the DSP Processing Blocks are made by writing to a software register set within the module. Each software register is accessed using a Module Control Device address and an internal register address.

Register locations are defined as a Module Control Device address followed by a 24-bit register location. The Register Address Table syntax list the register location as $AA:xxxxxx where AA is the Module Control Device address followed by the "xxxxxx" register offset. An example of muting all channels in the amplifier would be a write to $B2:000000.

6.4 INPUT SELECTION THROUGH SOFTWARE

Analog, digital SAI port, or optional digital S/PDIF inputs are available. The Input Select Register specifies which source is active, and the data format of the SAI port. The default value for Input Selection is read on reset through the hardware pin ANALOG_DIGITAL and optional S/PDIF. At any time, the Input Selection may be changed in software through the Input Select register. The amplifier outputs must be muted during changes to Input Selection to avoid pops. For the SAI port, the left channel data is assigned to the odd-numbered input (channel 1). Right channel data is then assigned to the even-numbered input.(channel 2).

Register $B2:020001h is the Input Select register write address. The Input Select register read address is $B2:020002. The bit functions of the Input Select register are as follows:

Input Select Bits	4	3	2	1	0
Value	JUSTIFY	Reserved Always set to 0	ANALOG/DIGITAL	Reserved Always set to 0	*S/PDIF

Table 19: Input Select Register Bits [4:0]

Input Select Bits	[23:14]	13	12	[11:5]
Value	Reserved Always set to 1100 0000 11	STEREO/BIAMP	LEFT/RIGHT	Reserved Always set to 0

Table 20: Input Select Register Bits [23:5]

PRELIMINARY

Bits [23:14] **RESERVED**

Set these bits to '1100 0000 11' when writing to the Input Select register.

Bit 13 **STEREO/BIAMP**

Writing a 1 to STEREO/BIAMP configures the module for stereo audio distribution mode. Writing a 0 to STEREO/BIAMP configures the module for bi-amplification mode.

Bit 12 **LEFT/RIGHT**

Writing a 1 to LEFT/RIGHT configures the module for left channel input. Writing a 0 to LEFT/RIGHT configures the module for right channel input.

Bits [11:5] **RESERVED**

Set these bits to 0 when writing to the Input Select register.

Bit 4 **JUSTIFY**

When a 1 is written to JUSTIFY, both pairs of SAI ports will accept digital audio data in Left-Justified format. When a 0 is written to JUSTIFY, both pairs of SAI inputs will accept digital audio data in I^2S format. The default value for JUSTIFY is 0.

Bit 3 **RESERVED**

Set this bit to 0 when writing to the Input Select register.

Bit 2 **ANALOG/DIGITAL**

When a 1 is written to ANALOG/DIGITAL, the SAI port is selected for Channels 1 and 2. When a 0 is written to ANALOG/DIGITAL, the analog input is selected. When a 1 is written to ANALOG/DIGITAL, the I^2S/Left-Justified (or S/PDIF) input is selected. ANALOG/DIGITAL is only valid when S/PDIF is 0 (S/PDIF input is not selected). Upon reset, the value of ANALOG/DIGITAL is equal to the state of the ANALOG/DIGITAL pin.

Bit 1 **RESERVED**

Set this bit to 0 when writing to the Input Select register.

Bit 0 ***S/PDIF (Optional)**

When the optional S/PDIF is 1, the optional S/PDIF input is selected for channels 1 and 2. When a 0 is written to S/PDIF, the input selection for these channels is determined by ANALOG/DIGITAL. Upon reset, the value of S/PDIF is equal to the state of the SPDIF hardware pin.

*S/PDIF Setting	ANALOG/DIGITAL Setting	Input Source Selection
S/PDIF = 0	ANALOG/DIGITAL = 1	SAI port 0 connected to channels 1/2
S/PDIF = 0	ANALOG/DIGITAL = 0	*AIN0/1 connected to channels 1/2
S/PDIF = 1	ANALOG/DIGITAL = x	*S/PDIF connected to channels 1/2

TABLE 21: Audio Source Selection through Input Selection Register, * denotes optional

6.5 4X4 INPUT MIXER

Any inputs of the MXS100 amplifier module (only available in D2-MXS0100R2-56061D and D2-MXS0100R2-57061D) can be mixed and/or routed to any Tone Control inputs through the Mixer. A configuration of up to 4-inputs/4-outputs is supported using one module. The DSP within the module will automatically provide a smooth transition between changes to the Mixer.

6.5.1 MIXER GAIN CALCULATION

For each Tone Control channel, the Mixer contains 4 registers; one corresponding to each input channel. Each mixer register specifies the gain of a specific input channel that is mixed into a specific output channel.

For a given Gain in dB, the appropriate parameter is a signed, 24-bit number calculated using the following equation. Valid range for Gain is -100dB to 0dB. Note that the value for Gain is always negative and the resulting parameter is also always negative.

$$MixerGainParameter = -\left[2^{23} \times 10^{\left(\frac{Gain}{20}\right)}\right]$$

The following figure illustrates the organization of MixerGainParameter (MGP) registers. The first number in each entry is the input channel, and the second number is the output channel.

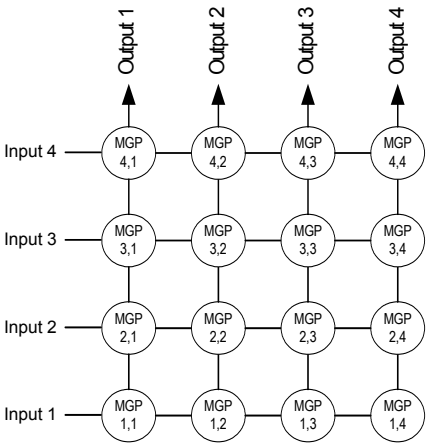


FIGURE 22: Input Mixer Gain Parameter (MGP) Channel Organization

PRELIMINARY

6.5.2 INPUT MIXER REGISTER SUMMARY

Register Name	Minimum Value	Maximum Value	Description
MixerGainParameter	FFFFFFh	800001h	Mixer gain for a given input channel that is mixed into a given Tone Control input channel

Table 22: Mixer Register Summary

6.5.3 INPUT MIXER REGISTER TABLE

Register Name	*Channel 1 Register Address (MGP x,1)	*Channel 2 Register Address (MGP x,2)	*Channel 3 Digital Out Register Address (MGP x,3)	*Channel 4 Digital Out Register Address (MGP x,4)
MixerGainParameter, Input Channel 1 (MGP 1,x)	B2:000127h	B2:00012Bh	B2:00012Fh	B2:000133h
MixerGainParameter, Input Channel 2 (MGP 2,x)	B2:000128h	B2:00012Ch	B2:000130h	B2:000134h
MixerGainParameter, Input Channel 3 (MGP 3,x)	B2:000129h	B2:00012Dh	B2:000131h	B2:000135h
MixerGainParameter, Input Channel 4 (MGP 4,x)	B2:00012Ah	B2:00012Eh	B2:000132h	B2:000136h
* Denotes feature only available in D2-MXS0100R2-56061D and D2-MXS0100R2-57061D.				

Table 23: Input Mixer Register Address Table

6.6 TONE CONTROL

The MXS100 amplifier provides individual software-controlled Tone Controls for each channel. These are implemented as low-pass and high-pass shelving filters for bass and treble control, respectively, which are added back into the signal flow. Each filter contains a first-order (6dB/octave) rolloff, with programmable corner frequency and gain. The amplifier will automatically provide a smooth transition between Tone Control changes.

6.6.1 TONE CONTROL CORNER FREQUENCY CALCULATION

The Corner Frequency of the Tone Control is defined as the frequency at which the gain of the filter is -3dB. For a given Corner Frequency, the appropriate parameter is a signed, 24-bit number calculated using the following equations.

First, determine the intermediate value Θ, then use Θ to calculate the frequency corner parameter value. Valid range for Corner Frequency is 20Hz to 24,000Hz.

$$\Theta = Frequency \times 9.817477 \times 10^{-5}$$

$$ToneControlCornerFrequencyParameter = 2^{23} \times \left(\frac{\sin(\Theta) - 1}{\cos(\Theta)} \right)$$

6.6.2 TONE CONTROL GAIN CALCULATION

For a given Gain in dB, the appropriate parameter is a signed, 24-bit number calculated using the following equation. Valid range for Tone Control Gain is -100dB to +9.542dB.

$$ToneControlGainParameter = 2^{23} \times \left[\frac{10^{\left(\frac{Gain}{20}\right)} - 1}{4} \right]$$

6.6.3 TONE CONTROL REGISTER SUMMARY

Register Name	Minimum Value	Maximum Value	Description
BassToneControlCorner FrequencyParameter	804047h	3504F3h	Per-channel corner frequency parameter for bass tone control shelving filter.
BassToneControlGain Parameter	C0002Ah	7FFFFFh	Per-channel gain for bass tone control shelving filter
TrebleToneControlCornerFrequencyParameter	804047h	3504F3h	Per-channel corner frequency parameter for treble tone control shelving filter.
TrebleToneControlGain Parameter	C0002Ah	7FFFFFh	Per-channel gain for treble tone control shelving filter

Table 24: Tone Control Register Summary

6.6.4 TONE CONTROL REGISTER ADDRESS TABLE

Register Name	Channel 1 Register Address	Channel 2 Register Address	*Channel 3 Digital Out Register Address	*Channel 4 Digital Out Register Address
BassToneControlCorner FrequencyParameter	B2:000015h	B2:000019h	B2:00001Dh	B2:000021h
BassToneControlGain Parameter	B2:000016h	B2:00001Ah	B2:00001Eh	B2:000022h
TrebleToneControlCorner FrequencyParameter	B2:000017h	B2:00001Bh	B2:00001Fh	B2:000023h
TrebleToneControlGain Parameter	B2:000018h	B2:00001Ch	B2:000020h	B2:000024h
* Denotes feature only available in D2-MXS0100R2-56061D and D2-MXS0100R2-57061D.				

Table 25: Tone Control Register Address Table

6.7 3-BAND PRE-MIXER PARAMETRIC EQUALIZER

Eight parametric equalizer bands are available on each channel - 3 prior to mixing and 5 post-mixing. Each band contains adjustable Frequency, Gain and Bandwidth. Setting the Gain to 0 disables a band. The amplifier will automatically provide a smooth transition between changes to the Parametric EQ.

6.7.1 3-BAND PRE-MIXER PARAMETRIC EQ CENTER FREQUENCY CALCULATION

For a given center frequency, the appropriate parameter is a signed, 24-bit number calculated using the following equation. Valid range for center frequency is 20Hz to 24,000Hz.

$$EQCenterFrequencyParameter = 2^{23} \times Frequency \times 31.25 \times 10^{-6}$$

6.7.2 3-BAND PRE-MIXER PARAMETRIC EQ QUALITY FACTOR CALCULATION

For a given Q, the appropriate parameter is a signed, 24-bit number calculated using the following equation. Valid range for Q is 0.5 < Q <= 10. (Note that a value of 0.5 for Q results in an EQQParameter value of 800000h, which in invalid)

$$EQQParameter = 2^{23} \times \left(\frac{1}{2 \times Q}\right)$$

6.7.3 3-BAND PRE-MIXER PARAMETRIC EQ GAIN CALCULATION

For a given Gain in dB, the appropriate parameter is a signed, 24-bit number calculated using the following equation. Valid range for gain is -60 to +6.

$$EQGainParameter = -\left\{2^{23} \times \left[1 - 10^{\left(\frac{Gain}{20}\right)}\right]\right\}$$

6.7.4 3-BAND PRE-MIXER PARAMETRIC EQ REGISTER SUMMARY

Register Name	Minimum Value	Maximum Value	Description
EQCenterFrequency Parameter	00147Ah	600000h	Center frequency for Parametric EQ, 3 bands per channel
EQQParameter	066666h	7FFFFFh	Quality factor for Input Parametric EQ, 5 blocks per channel
EQGainParameter	8020C5h	7F64C1h	Gain for Parametric EQ, 5 blocks per channel

Table 26: 3-Band Pre-Mixer Parametric EQ Register Summary

6.7.5 3-BAND PRE-MIXER PARAMETRIC EQ REGISTER ADDRESS TABLE

Register Name	Channel 1 Register Address	Channel 2 Register Address	*Channel 3 Digital Out Register Address	*Channel 4 Digital Out Register Address
EQCenterFrequency Parameter, band 1	B2:000061h	B2:00006Ah	B2:000073h	B2:00007Ch
EQQParameter, band 1	B2:000062h	B2:00006Bh	B2:000074h	B2:00007Dh
EQGainParameter, band 1	B2:000063h	B2:00006Ch	B2:000075h	B2:00007Eh
EQCenterFrequency Parameter, band 2	B2:000064h	B2:00006Dh	B2:000076h	B2:00007Fh
EQQParameter, band 2	B2:000065h	B2:00006Eh	B2:000077h	B2:000080h
EQGainParameter, band 2	B2:000066h	B2:00006Fh	B2:000078h	B2:000081h
EQCenterFrequency Parameter, band 3	B2:000067h	B2:000070h	B2:000079h	B2:000082h
EQQParameter, band 3	B2:000068h	B2:000071h	B2:00007Ah	B2:000083h
EQGainParameter, band 3	B2:000069h	B2:000072h	B2:00007Bh	B2:000084h
* Denotes feature only available in D2-MXS0100R2-56061D and D2-MXS0100R2-57061D.				

Table 27: 3-Band Pre-Mixer Parametric EQ Register Address Table

6.8 MIXER

Any inputs of the MXS100 amplifier module can be mixed and/or routed to any outputs through the Mixer. A configuration of up to 2-inputs/2-outputs is supported using one module. The DSP within the module will automatically provide a smooth transition between changes to the Mixer.

6.8.1 MIXER GAIN CALCULATION

For each output channel, the Mixer contains 4 registers; one corresponding to each input channel. Each mixer register specifies the gain of a specific input channel that is mixed into a specific output channel.

For a given Gain in dB, the appropriate parameter is a signed, 24-bit number calculated using the following equation. Valid range for Gain is -100dB to 0dB. Note that the value for Gain is always negative and the resulting parameter is also always negative.

$$MixerGainParameter = -\left[2^{23} \times 10^{\left(\frac{Gain}{20}\right)}\right]$$

The following figure illustrates the organization of MixerGainParameter (MGP) registers. The first number in each entry is the input channel, and the second number is the output channel.

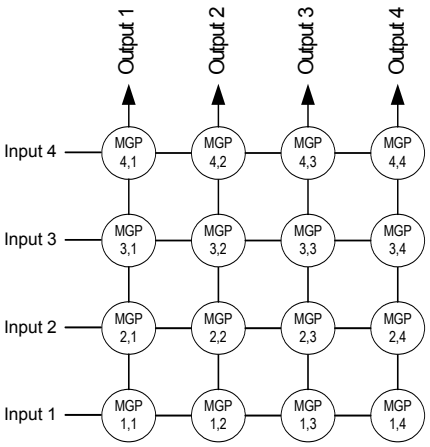


FIGURE 23: Mixer Gain Parameter (MGP) Channel Organization

PRELIMINARY

6.8.2 MIXER REGISTER SUMMARY

Register Name	Minimum Value	Maximum Value	Description
MixerGainParameter	FFFFFFh	800001h	Mixer gain for a given input channel that is mixed into a given output channel

Table 28: Mixer Register Summary

6.8.3 MIXER REGISTER TABLE

Register Name	Channel 1 Register Address (MGP x,1)	Channel 2 Register Address (MGP x,2)	*Channel 3 Digital Out Register Address (MGP x,3)	*Channel 4 Digital Out Register Address (MGP x,4)
MixerGainParameter, Input Channel 1 (MGP 1,x)	B2:000005h	B2:000009h	B2:00000Dh	B2:000011h
MixerGainParameter, Input Channel 2 (MGP 2,x)	B2:000006h	B2:00000Ah	B2:00000Eh	B2:000012h
MixerGainParameter, Input Channel 3 (MGP 3,x)	B2:000007h	B2:00000Bh	B2:00000Fh	B2:000013h
MixerGainParameter, Input Channel 4 (MGP 4,x)	B2:000008h	B2:00000Ch	B2:000010h	B2:000014h
* Denotes feature only available in D2-MXS0100R2-56061D and D2-MXS0100R2-57061D.				

Table 29: Mixer Register Address Table

6.9 5-BAND POST-MIXER PARAMETRIC EQUALIZER

Five Parametric Equalizer blocks are available on each input channel.

Register Name	Minimum Value	Maximum Value	Description
EQCenterFrequency Parameter	00147Ah	600000h	Center frequency for Parametric EQ, 5 bands per channel
EQQParameter	066666h	7FFFFFh	Quality factor for output Parametric EQ, 5 blocks per channel
EQGainParameter	8020C5h	7F64C1h	Gain for Parametric EQ, 5 blocks per channel

Table 30: 5-Band Post-Mixer Parametric EQ Register Summary

6.9.1 5-BAND POST-MIXER PARAMETRIC EQ REGISTER ADDRESS TABLE

Register Name	Channel 1 Register Address	Channel 2 Register Address	*Channel 3 Digital Out Register Address	*Channel 4 Digital Out Register Address
EQCenterFrequency Parameter, band 1	B2:000025h	B2:000034h	B2:000043h	B2:000052h
EQQParameter, band 1	B2:000026h	B2:000035h	B2:000044h	B2:000053h
EQGainParameter, band 1	B2:000027h	B2:000036h	B2:000045h	B2:000054h
EQCenterFrequency Parameter, band 2	B2:000028h	B2:000037h	B2:000046h	B2:000055h
EQQParameter, band 2	B2:000029h	B2:000038h	B2:000047h	B2:000056h
EQGainParameter, band 2	B2:00002Ah	B2:000039h	B2:000048h	B2:000057h
EQCenterFrequency Parameter, band 3	B2:00002Bh	B2:00003Ah	B2:000049h	B2:000058h
EQQParameter, band 3	B2:00002Ch	B2:00003Bh	B2:00004Ah	B2:000059h
EQGainParameter, band 3	B2:00002Dh	B2:00003Ch	B2:00004Bh	B2:00005Ah
EQCenterFrequency Parameter, band 4	B2:00002Eh	B2:00003Dh	B2:00004Ch	B2:00005Bh
EQQParameter, band 4	B2:00002Fh	B2:00003Eh	B2:00004Dh	B2:00005Ch
EQGainParameter, band 4	B2:000030h	B2:00003Fh	B2:00004Eh	B2:00005Dh
EQCenterFrequency Parameter, band 5	B2:000031h	B2:000040h	B2:00004Fh	B2:00005Eh
EQQParameter, band 5	B2:000032h	B2:000041h	B2:000050h	B2:00005Fh
EQGainParameter, band 5	B2:000033h	B2:000042h	B2:000051h	B2:000060h
* Denotes feature only available in D2-MXS0100R2-56061D and D2-MXS0100R2-57061D.				

Table 31: 5-Band Post-Mixer Parametric EQ Register Address Table

6.10 LOW/HIGH-PASS FILTERS (CROSSOVER)

Four cascaded filter blocks are available for each channel. Each filter may be configured for low-pass or high-pass operation with adjustable slope and Q. Higher order slopes and bandpass functions can be achieved by using multiple low or high pass filters.

6.10.1 CROSSOVER FILTER CORNER FREQUENCY CALCULATION

For a given Corner Frequency, the appropriate parameter is a signed, 24-bit number calculated using the following equation. Valid range for the filter Corner Frequency is 20Hz to 24,000Hz.

$$FilterCornerFrequencyParameter = 2^{23} \times Frequency \times 31.25 \times 10^{-6}$$

6.10.2 CROSSOVER QUALITY FACTOR CALCULATION

For a given filter Q, the appropriate parameter is a signed, 24-bit number calculated using the following equation.
Valid range for filter Q is 0.5 < Q <= 10. (Note that a value of 0.5 for Q results in an FilterQParameter value of 800000h, which is invalid)

$$FilterQParameter = 2^{23} \times \left[\frac{1}{(2 \times Q)}\right]$$

6.10.3 CROSSOVER REGISTER SUMMARY

Register Name	Minimum Value	Maximum Value	Description
FilterMode	-	-	Filter mode for each block 000000h = Lowpass, 12dB/octave slope 000001h = Lowpass, 6dB/octave slope 000002h = Highpass, 12dB/octave slope 000003h = Highpass, 6dB/octave slope 8XXXXXh = Bypass
FilterCornerFrequency Parameter	00147Ah	600000h	Corner frequency for each block
FilterQParameter	066666h	7FFFFFh	Quality factor for each block

Table 32: Crossover/Filter Register Summary

6.10.4 CROSSOVER REGISTER TABLE

Register Name	Channel 1 Register Address	Channel 2 Register Address	*Channel 3 Digital Out Register Address	*Channel 4 Digital Out Register Address
FilterMode, Block 1	B2:000085h	B2:000091h	B2:00009Dh	B2:0000A9h
FilterCornerFrequency Parameter, Block 1	B2:000086h	B2:000092h	B2:00009Eh	B2:0000AAh
FilterQParameter, Block 1	B2:000087h	B2:000093h	B2:00009Fh	B2:0000ABh
FilterMode, Block 2	B2:000088h	B2:000094h	B2:0000A0h	B2:0000ACh
FilterCornerFrequency Parameter, Block 2	B2:000089h	B2:000095h	B2:0000A1h	B2:0000ADh
FilterQParameter, Block 2	B2:00008Ah	B2:000096h	B2:0000A2h	B2:0000AEh
FilterMode, Block 3	B2:00008Bh	B2:000097h	B2:0000A3h	B2:0000AFh
FilterCornerFrequency Parameter, Block 3	B2:00008Ch	B2:000098h	B2:0000A4h	B2:0000B0h
FilterQParameter, Block 3	B2:00008Dh	B2:000099h	B2:0000A5h	B2:0000B1h
FilterMode, Block 4	B2:00008Eh	B2:00009Ah	B2:0000A6h	B2:0000B2h
FilterCornerFrequency Parameter, Block 4	B2:00008Fh	B2:00009Bh	B2:0000A7h	B2:0000B3h
FilterQParameter, Block 4	B2:000090h	B2:00009Ch	B2:0000A8h	B2:0000B4h
* Denotes feature only available in D2-MXS0100R2-56061D and D2-MXS0100R2-57061D.				

Table 33: Filter/Crossover Register Address Table

PRELIMINARY

6.11 ADJUSTABLE TIME DELAY

Each channel of the MXS100 amplifier module contains an Adjustable Time Delay for each channel.

6.11.1 TIME DELAY CALCULATION

For a given Delay in milliseconds, the appropriate parameter is an unsigned, 24-bit integer calculated using the following equation. Valid range for Delay is 0 to 3.984375ms in steps of 0.015625ms, which is based on a range of 0 to 255 for TimeDelayParameter.

$$TimeDelayParameter = Delay \times 64$$

6.11.2 TIME DELAY REGISTER SUMMARY

Register Name	Minimum Value	Maximum Value	Description
TimeDelayParameter	000000h	0000FFh	Per-channel Time Delay

6.11.3 TIME DELAY REGISTER TABLE COMPRESSOR

Register Name	Channel 1 Register Address	Channel 2 Register Address	*Channel 3 Digital Out Register Address	*Channel 4 Digital Out Register Address
TimeDelayParameter	B2:0000B5h	B2:0000B6h	B2:0000B7h	B2:0000B8h
* Denotes feature only available in D2-MXS0100R2-56061D and D2-MXS0100R2-57061D.				

Table 34: Adjustable Time Delay Control Registers

The MXS100 amplifier provides individual software-controlled Compressors for each channel. Each Compressor has configurable Compression Ratio, Threshold, Attack and Release Time, as well as Makeup Gain. The amplifier will automatically provide a smooth transition between changes to the Compressor.

6.12 LOUDNESS CONTOUR

The MXS100 module provides individual software-controlled Loudness Contour for each channel. Each Loudness Contour curve is implemented as low-pass and high-pass shelving filter that is dynamically and automatically adjusted for the correct amount of bass and treble boost based on the Master Volume level, which are added back into the signal flow. The Loudness Contour precisely models the Fletcher and Munson Curve. The DSP within the module will automatically provide a smooth transition between changes to the Loudness Contour setting in addition to changes to the Master Volume level when the Loudness Contour is enabled. Please refer to the D2Audio Loudness Contour White Paper for additional information.

6.12.1 LOUDNESS CONTOUR REGISTER SUMMARY

Register Name	Minimum Value	Maximum Value	Description
LoudnessContourParameter	000000h	000001h	Enables the Loudness Contour per channel when the LoudnessContourParameter is equal to 1. The Loudness Contour is disabled by default.

Table 35: Tone Control Register Summary

6.12.2 LOUDNESS CONTOUR REGISTER ADDRESS TABLE

Register Name	Channel 1 Register Address	Channel 2 Register Address	*Channel 3 Digital Out Register Address	*Channel 4 Digital Out Register Address
LoudnessContourParameter	B2:000101h	B2:000104h	B2:000107h	B2:00010Ah
* Denotes feature only available in D2-MXS0100R2-56061D and D2-MXS0100R2-57061D.				

Table 36: Loudness Contour Register Address Table

PRELIMINARY

6.13 COMPRESSOR

The Compressor reduces the gain of signals which exceed a given threshold.

6.13.1 COMPRESSOR THRESHOLD CALCULATION

For a given Threshold in dB, the appropriate parameter is a signed, 24-bit number calculated using the following equation. Valid range for Threshold is -90dB to 0dB.

$$CompressorThresholdParameter = 2^{23} \times [(0.010381025 \times Threshold) + 0.96875]$$

6.13.2 COMPRESSOR ATTACK TIME CALCULATION

The Attack Time is the rate at which the gain is reduced when the input exceeds the Threshold. For a given Attack Time in milliseconds, the appropriate parameter is a signed, 24-bit number. Valid range for attack time is 1ms to 100ms. Below is a table of values for Attack Time. Other values can be calculated by interpolating between these.

Attack Time	CompressorAttackTime Parameter
1ms	1C2F43h
10ms	032900h
100ms	0051D1h

Table 37: Compressor Values for Attack Time

6.13.3 COMPRESSOR RELEASE TIME CALCULATION

The Release Time is the rate at which the gain is increased when the input falls below the Threshold. For a given Release Time in milliseconds, the appropriate parameter is a signed, 24-bit number. Valid range for Release Time is 1ms to 100ms. Below is a table of values for Release Time. Other values can be calculated by interpolating between these.

Release Time	CompressorReleaseTime Parameter
1ms	1C2F43h
10ms	032900h
100ms	0051D1h

Table 38: Compressor Values for Release Time

6.13.4 COMPRESSOR RATIO CALCULATION

The Compressor Ratio is the number of dB above the Threshold that the input level must increase in order to increase the output level by 1dB. For a given Compressor Ratio in dB, the appropriate parameter is a signed, 24-bit number calculated using the following equation. Valid range for Compressor Ratio is 1 to 100. Note that a ratio of 1 results in no change and a ratio of 10 or greater results in a limiter.

$$CompressorRatioParameter = 2^{23} \times \left(1 - \left(\frac{1}{Ratio}\right)\right)$$

6.13.5 COMPRESSOR MAKEUP GAIN CALCULATION

Depending on the settings for Threshold and Compressor Ratio, additional Makeup Gain may be necessary to reach a full-scale output. For a given Makeup Gain in dB, the appropriate parameter is a signed, 24-bit number calculated using the following equation. Valid range for Makeup Gain is 0dB to +18.06dB.

$$CompressorMakeupGainParameter = 2^{23} \times 10^{[(Gain \times 0.05) - 0.90309]}$$

6.13.6 COMPRESSOR REGISTER SUMMARY

Register Name	Minimum Value	Maximum Value	Description
CompressorThreshold Parameter	04691Ch	7C0000h	Per-channel Compressor threshold
CompressorAttackTime Parameter	0051D1h	1C2F43h	Per-channel Compressor attack time
CompressorReleaseTime Parameter	0051D1h	1C2F43h	Per-channel Compressor release time
CompressorRatioParameter	000000h	7EB851h	Per-channel Compressor ratio
CompressorMakeupGain Parameter	0FFFFFh	7FFFFFh	Per-channel Compressor makeup gain

Table 39: Compressor Register Summary

6.13.7 COMPRESSOR REGISTER ADDRESS TABLE

Register Name	Channel 1 Register Address	Channel 2 Register Address	*Channel 3 Digital Out Register Address	*Channel 4 Digital Out Register Address
CompressorThreshold Parameter	B2:0000BAh	B2:0000C0h	B2:0000C6h	B2:0000CCh
CompressorAttackTime Parameter	B2:0000BCh	B2:0000C2h	B2:0000C7h	B2:0000CDh
CompressorReleaseTime Parameter	B2:0000BDh	B2:0000C3h	B2:0000C8h	B2:0000CEh
CompressorRatioParameter	B2:0000BBh	B2:0000C1h	B2:0000C9h	B2:0000CFh
CompressorMakeupGain Parameter	B2:0000BEh	B2:0000C4h	B2:0000CAh	B2:0000D0h
* Denotes feature only available in D2-MXS0100R2-56061D and D2-MXS0100R2-57061D.				

TABLE 40: Compressor Register Address Table

6.14 VOLUME CONTROL

Software-controlled Master Volume Control is provided, which controls the final gain for all output channels. Individual attenuators are also provided for each channel.

6.14.1 MASTER VOLUME CALCULATION

For a given Master Volume in dB, the appropriate parameter is a signed, 24-bit number calculated using the following equation. Valid range for Master Volume is -100dB to +18.06dB.

$$MasterVolumeParameter = 1 - 2^{23} \times 10^{\left[\frac{(MasterVolume - 18.06)}{20}\right]}$$

6.14.2 CHANNEL ATTENUATION CALCULATION

For a given Channel Attenuation in dB, the appropriate parameter is a signed, 24-bit negative number calculated using the following equation. Valid range for Channel Attenuation is 0dB to 120dB. Note that channel attenuation is positive, such that a value of 0dB results in no attenuation. Also changing the polarity of the calculation will invert the polarity of the output channel.

$$ChannelAttenuationParameter = -\left[2^{23} \times 10^{\left(\frac{-Attenuation}{20}\right)}\right]$$

The Channel Attenuation Parameter can also be used to invert the polarity of a channel. To do this, remove the negative sign from the formula above and recalculate the ChannelAttenuationParameter:

$$InvertedChannelAttenuationParameter = 2^{23} \times 10^{\left(\frac{-Attenuation}{20}\right)}$$

6.14.3 VOLUME CONTROL REGISTER SUMMARY

Register Name	Minimum Value	Maximum Value	Description
MasterVolumeParameter	FFFFFFh (minimum volume)	800000h (maximum volume)	Master Volume for all channels
ChannelAttenuationParameter	800000h (minimum attenuation)	FFFFFFh (maximum attenuation)	Per-channel attenuation setting
ChannelAttenuationParameter (with polarity inversion)	7FFFFFh (minimum attenuation)	000000h (maximum attenuation)	Per-channel attenuation setting (with polarity inversion)

TABLE 41: Volume Control Register Summary

6.14.4 VOLUME CONTROL REGISTER ADDRESS TABLE

Register Name	Channel 1 Register Address	Channel 2 Register Address	*Channel 1 Digital Out Register Address (SDOUT0)	*Channel 2 Digital Out Register Address (SDOUT0)
MasterVolume Parameter	B2:000000h			
ChannelAttenuation Parameter	B2:000001h	B2:000002h	B2:000123h	B2:000124h
* Denotes feature only available in D2-MXS0100R2-56061D and D2-MXS0100R2-57061D.				

Table 42: Volume Control Register Address Table (Output Channels 1 - 2)

Register Name	*Channel 3 Digital Out Register Address (SDOUT1)	*Channel 4 Digital Out Register Address (SDOUT1)	*Channel 3 Digital Out Register Address (SPDIFTX)	*Channel 4 Digital Out Register Address (SPDIFTX)
MasterVolume Parameter	B2:00011Fh			
ChannelAttenuation Parameter	B2:000125h	B2:000126h	B2:000121h	B2:000122h
* Denotes feature only available in D2-MXS0100R2-56061D and D2-MXS0100R2-57061D.				

Table 43: Volume Control Register Address Table (Output Channels 3 - 4)

7 PHYSICAL DIMENSIONS

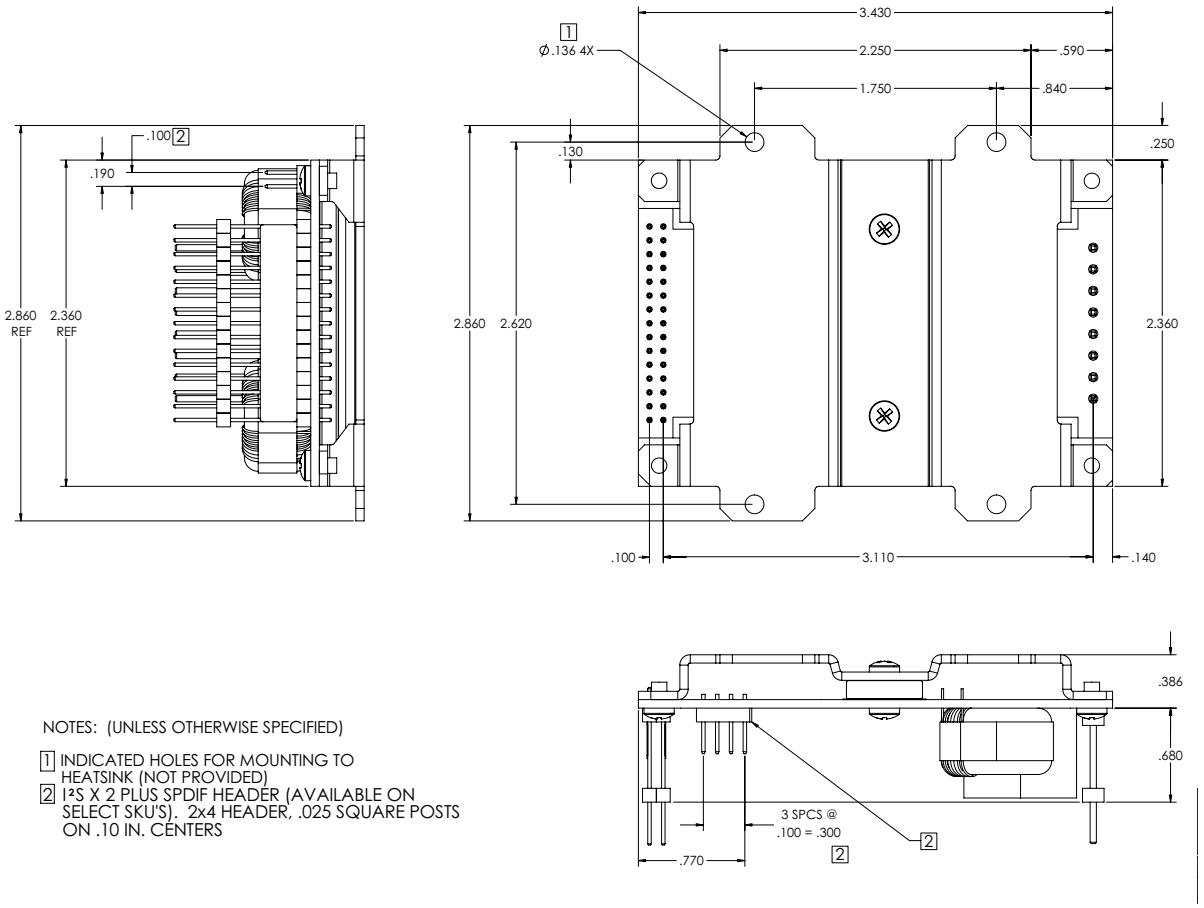


FIGURE 24: Physical Dimensions

7.1 HEAT SINK MOUNTING DETAILS

EXAMPLE OF INSTALLATION

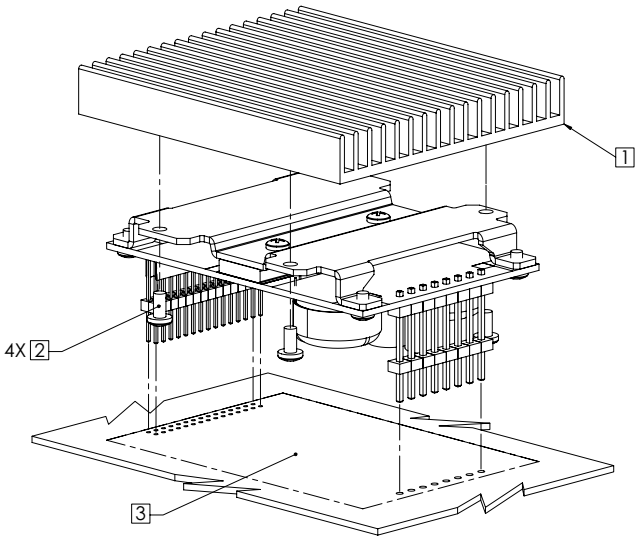


FIGURE 25: Mounting the Heat Sink

Figure Notes: (See call-out numbers in drawing)

Call-out 1: Heat sink (not supplied)

Call-out 2: Screws (not supplied). Recommended size: M3 or 4-40

Call-out 3: Application shown using a system board (not supplied), but the use of connectors mating directly to the headers is also possible.

7.2 PIN LOCATIONS AND PCB DIMENSIONS

TOP VIEW BOARD MOUNT

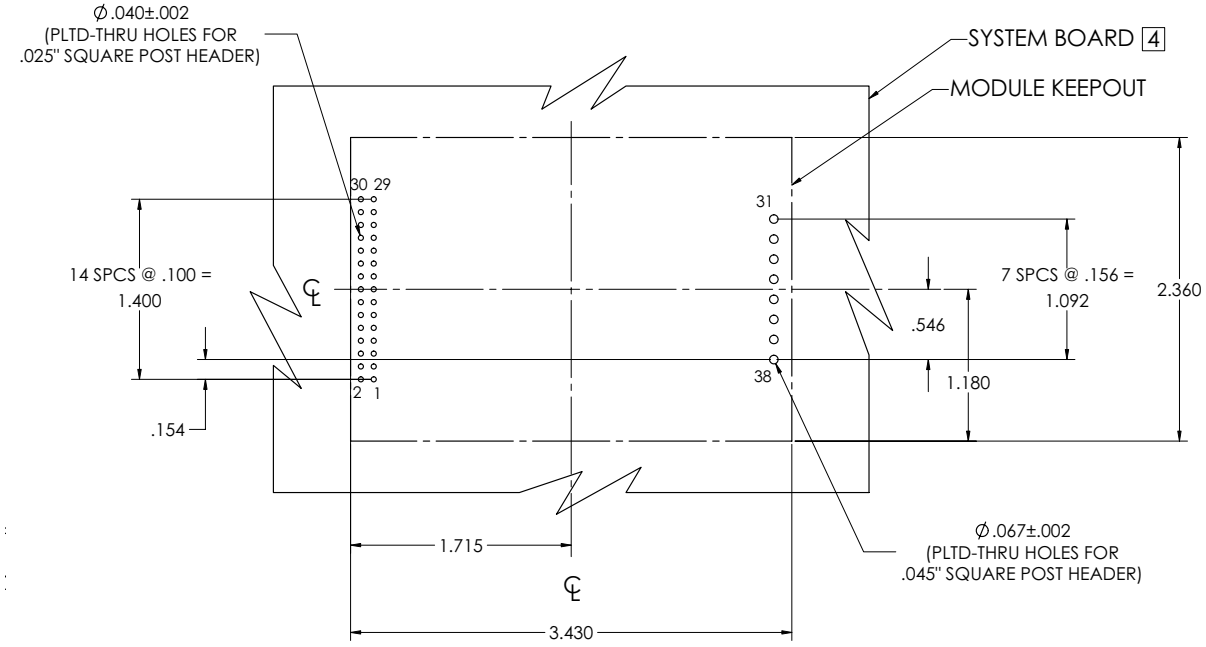


FIGURE 26: Pin Locations (View from top, not to scale)

Figure Notes: (See call-out numbers in drawing)

Call-out 4: Module mounting diagram for OEM'S system board (not supplied)

PRELIMINARY

7.3 AMBIENT OPERATING CONDITIONS

The MXS100 amplifier generates modest heat and is designed to dissipate that heat to the ambient environment. An internal temperature sensor detects if the temperature at the power output FET rail hits 80°C. At 80°C, the amplifier will linearly reduce output power proportional to the delta difference above 80°C to 100°C. This allows the amplifier to run at reduced capability rather than experience an abrupt power down. At 100°C, a "fail-safe" mode disables the amplifier. The amplifier will return to normal operation when the operating temperatures fall below the "fail-safe" or reduced power temperature thresholds. The internal temperature sensor is accessible through a temperature register (see "Temperature Register" on page 46).

Figure 27 shows the recommended operating range and power derating temperatures:

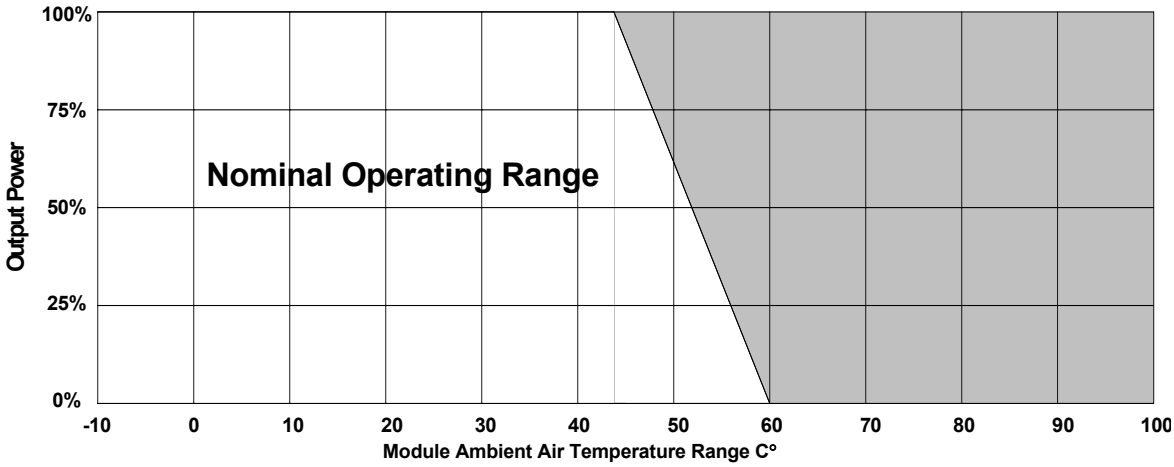


FIGURE 27: Module Derating Curve

7.3.1 TEMPERATURE REGISTER

The MXS100 contains a temperature sensor located at the power output FET rail. The register below stores the user-accessible temperature value:

Register Name	Address
Temperature	B2:020010h

Table 44: Temperature Sensor Register Address Table

To compute the temperature in degrees C:
°C (decimal) = (value_from_temp_register_hex/256)

8 PART NUMBERS AND FEATURE SETS

PRELIMINARY

SKU	Watts/Channel into 8Ω, (< 0.1% THD+N, Typical Supplies)	Channels of Amplification	Audio Input Method(s)	Firmware Functionality Beyond Baseline	RoHS Compliant
D2-MXS010002-04061D	100W	2	I^2S/LJ Digital Input, S/PDIF Input	Loudness	No
D2-MXS010002-05061D			I^2S/LJ Digital Input, S/PDIF Input & Internal ADC		
D2-MXS0100R2-04061D			I^2S/LJ Digital Input, S/PDIF Input		Yes
D2-MXS0100R2-05061D			I^2S/LJ Digital Input, S/PDIF Input & Internal ADC		
D2-MXS0100R2-56061D		4	I^2S/LJ Digital Input, S/PDIF Input, 2x I^2S/LJ Digital Outputs, S/PDIF Output		
D2-MXS0100R2-57061D			I^2S/LJ Digital Input, S/PDIF Input & Internal ADC 2x I^2S/LJ Digital Outputs, S/PDIF Output		

Table 45: Part Numbers and Feature Sets

PRELIMINARY

9 DOCUMENT REVISION HISTORY

10/21/04 Revision 0.1.0 - First Internal Release. Based on Revision v1.0.0 of the XS125 Data Sheet.
Imported new source material specific to the MXS100. Created drawings with custom file names to match product name. Made sure all drawings can be edited.

10/28/04 Revision 1.0.0 - Second Internal Release
Entered new mechanical drawings ver. 2. Entered review comments from the subject matter experts.

11/04/04 Revision 1.0.1 - Third Internal Release
Entered new performance plots, deleted old performance plots except for Figures 3 and 10. Added additional review comments from the subject matter experts.

11/09/04 Revision 1.0.2 - First Public Release
Updated front page to include high peak power numbers. Added paralleled output operation high peak power numbers. Finalized part numbers and feature set table.

01/12/05 Revision 2.0.0 - Second Public Release
Changed definition of nERROR pin to ERROR. Original definition of nERROR pin was open collector with 10K pullup. Actual function of pin is totem-pole output. Polarity of pin is active high. Added definition of STATUS pin. Corrected pinout drawing to correctly reflect ERROR in place of nERROR. Added SAI interface pin description. Corrected description of ANALOG_SPDIF pin. Updated Amplifier Operation

03/01/05 Revision 2.1.0 - Third Public Release
Correct verbiage on page 17 in the ANALOG_SPDIF section. Corrected verbiage on page 18 in the Bass [2:1], Treble [2:1] and Volume [2:1] sections.

05/27/05 Revision 2.1.1 - Fourth Public Release
Document style and pinout fixes. Added new power derating curve and thermal protection section, fixed Loudness Contour base address, added new photo on cover page.

07/27/05 Revision 2.1.2 - Fifth Public Release
Added new Short-Circuit/Over-Current Protection section, fixed Volume Control Register Summary, added RoHS compliant part numbers.

09/26/05 Revision 2.1.3 - Sixth Public Release
Changed STEREO_BIAMP/LR_CH_SEL pin description to floating (must be tied high or low) in Section 2.2, “Pin Descriptions - (*=Optional),” on page 16. Removed Absolute Operating Temperature values (Table 1 on page 7). Removed non-RoHS compliant part numbers from Table 45.

10/26/05 Revision 2.1.4
Changed ANALOG/S/PDIF pin/bit name to ANALOG/DIGITAL and updated description, fixed polarity of S/PDIF bits in Table 21 on page 30, updated API and Signal Flow Diagrams with new GENII register definitions, updated mechanical drawings in Section 7, “Physical Dimensions,” on page 43.

11/9/05 Revision 2.1.5
Updated pinout diagram (Section 2, “Amplifier module pinout,” on page 14) and pinout listings for GENII headers and layout, added new SAO and S/PDIF pins and descriptions, updated cover page with post-processed I^2S/Left-Justified and S/PDIF outputs text.

03/17/06 Revision 2.1.6
- Removed FCC and CE compliance text from Cover Page
- Updated pinout diagram (Figure 10, “MXS100 Amplifier Module Pinout (Top View),” on page 14) and header pinout listings (Table 9 on page 15, Table 10 on page 15, Table 11 on page 15, Table 13 on page 16).