D2AUDIO VR100-7 DATA SHEET

Intelligent digital amplifier reference designs for manufacturers of high-volume home theater components

CONSUMER

PRELIMINARY

Complete Class-D Amplifier Solution

- D2Audio® Intelligent Digital Controller IC, PWM Driver, MOSFET Output Stage and Output Filter in one package
- Designed for compliance with FCC[4], UL, CSA, CE[4]

High-Performance Quality Sound

- Reference Design is scalable from 50 Watts x 5 Channels up to 100 Watts x 7 Channels, 8Ω, From 1 Channel Driven to All Channels Driven Continuously (FTC, Alternative A) Capable[1]
- <0.32% THD+N (Typical, 8Ω, 75W, 20Hz-20kHz, FB + DPSC)[2]
- <0.08% THD+N (Typical, 8Ω, 1W, 20Hz-20kHz, FB + DPSC)[2]
- 103 dB SNR/Dynamic Range (Typical, Unweighted, 20Hz-20kHz, FB + DPSC)[2]
- ± 0.5 dB Frequency Response (Typical, 8Ω, Unweighted, 20Hz-40kHz, FB + DPSC)[2]

High Peak-Wattage Capability

- 210 Watts/Channel, 3Ω[3]

93% Efficiency Reduces Heat and System Size

- Output pin available for controlling customer-provided fan

Pure Digital Path

- 4 digital audio inputs which support I²S and Left-Justified formats of Linear PCM (32kHz-192kHz, 16-24 bit).
- 2 digital audio inputs which support S/PDIF format with Linear PCM (32kHz-192kHz, 16-24 bit) for Zone 2/3
- Independent Sample Rate Conversion (SRC) on digital inputs removes the need to load complicated coefficient sets
- Simple 2-wire controller interface for external controllers

Graceful Protection and Auto Recovery

- Complete short-circuit, thermal, over-current fault protection
- Graceful handling of complex and lower impedance loads

Flexible Audio Configuration

- Audio Control Source processing: Tone Control, Channel Attenuation, and 5-bands of Parametric EQ per channel
- Programmable compression per channel
- Master Volume Control

Advanced Audio Options

- D2Audio SoundSuite® LEO™ Listening Environment Optimization (Firmware Available Q306)
- D2Audio Canvas™ GUI, an intuitive point-and-click audio configuration utility for OEMs, ODMs, and system designers

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The D2Audio VR100-7 is a self-contained 100 Watts per channel digital amplifier digital amplifier reference design for manufacturers of high-volume home theater components. The VR100-7 contains two DAE-2 Digital Audio Engine-2 ICs (D2-914xx-LR), PWM driver, MOSFET output stages and high-quality output filter stages.

It is designed for compliance with FCC[4], UL, CSA, and CE[4] requirements and is capable of driving up to 5, 6 or 7 channels from 50 Watts per channel up to 100 Watts per channel into 8Ω per FTC, Alternative A, B or C implementation, depending on the size and type of power supply used[1].

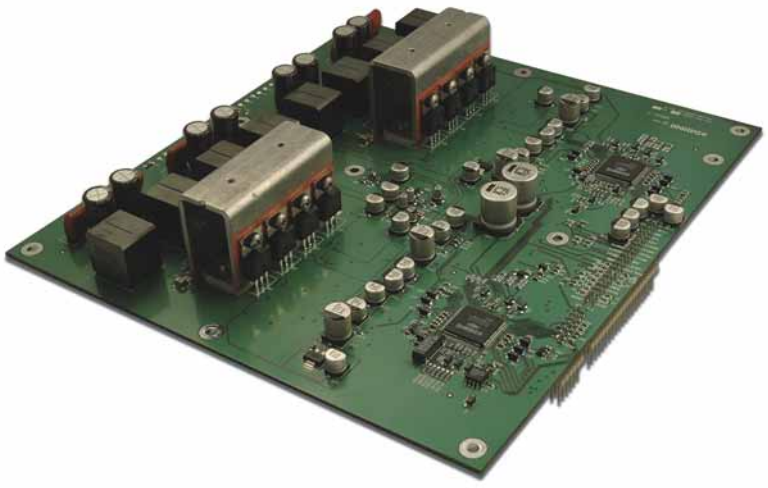
The size of the heat sink used in the end-design is entirely up to the customer allowing them to taylor the reference design to their needs. Optionally, customers may choose to add a fan to cool the amplifier inside their end-system by way of using the PWM fan control output pin. When connected to a fan, the amplifier automatically turns the fan on/off and increases/decreases fan speed when temperature levels around the amplifier require it.

Advanced audio options include D2Audio SoundSuite LEO (Listening Environment Optimization) and are available as a firmware enhancement to the VR100-7 reference design. The VR100-7 provides configurable per channel audio processing including Tone Control, Channel Attenuation, 5-band Parametric Equalization, Master Volume Control, and Dynamic Range Compression/Limiting. Included are up to 8-channels of digital audio inputs supporting I²S or Left-Justified (16-24-bit, 32-192kHz) formats.

All D2Audio reference designs feature D2Audio Canvas, a Windows application with an intuitive graphical user interface (GUI). "Point-and-click" options simplify audio configuration and avoid complex programming during initial evaluation, generating the system default settings, or even writing microcontroller code.

D2AUDIO VR100-7

- **Uses two DAE-2 (D291413-LR) which support Digital Feedback and DPSC**
- **Up to 100 Watts/Channel[1]**
- **<.08% THD+N (1W, 8 Ohm, 20Hz - 20kHz)[2]**
- **>103dB SNR (20Hz - 20kHz)[2]**
- **Up to 7 Output Channels**
- **PWM Filtered Subwoofer Line Output on Channel 8**
- **Pure digital audio signal path**
- **93% efficient**
- **Graceful protection and automatic fault recovery**



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PRELIMINARY

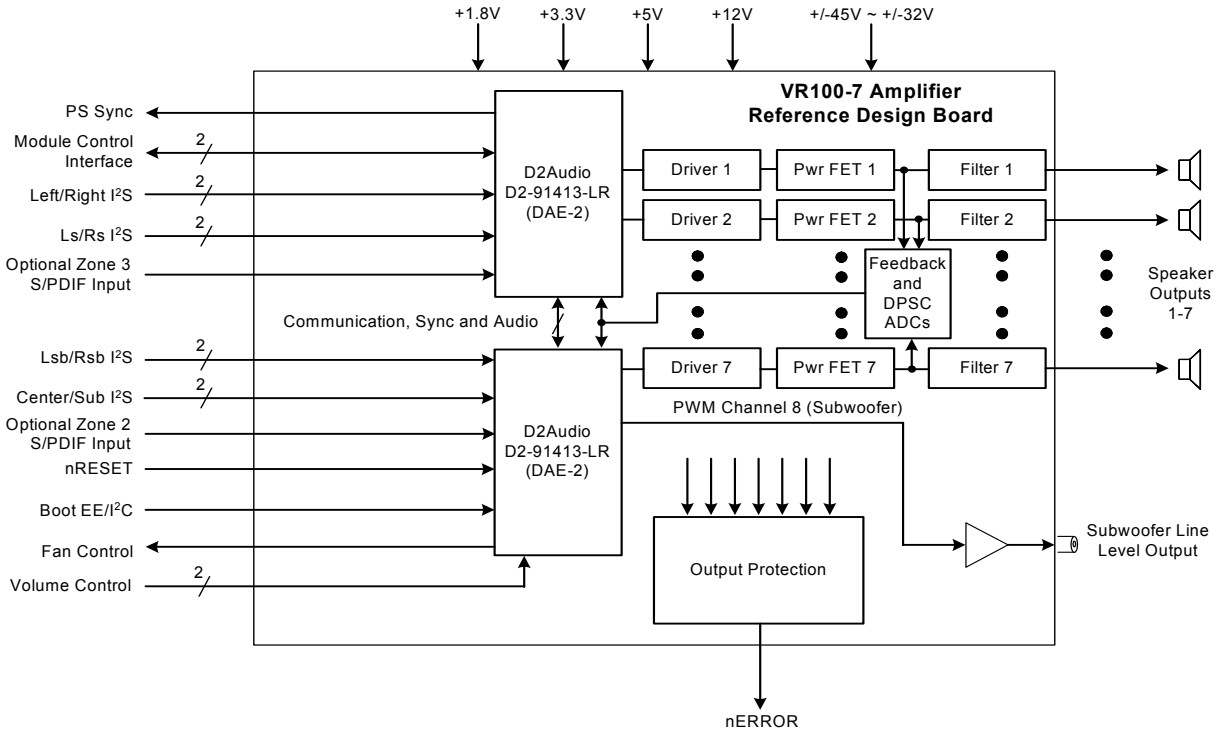

FIGURE 1: VR100/75/50-5/7 Block Diagram (Shown with D2-91413-LR ICs which support Feedback and DPSC)

[1] FTC Testing Method (footnote from Page 1)
This product is capable of meeting and exceeding the Alternative A, Alternative B or Alternative C end-product power rating method according to the FEDERAL TRADE COMMISSION 16 CFR Part 432 document which covers TRADE REGULATION RULE RELATING TO POWER OUTPUT CLAIMS FOR AMPLIFIERS UTILIZED IN HOME ENTERTAINMENT PRODUCTS, provided that adequate thermal management and an appropriate power supply has been designed into the end-system. This product must be provided with some method of thermal management (for example, addition of an external heat sink and/or fan-cooling system) before being powered up. The Linear Power Supply included in the VR100-7 Evaluation Kit is only for evaluation purposes and may not achieve 100W of output. Depending on the end-system requirements (maximum continuous output power and the number of channels driven), use a different linear or switch-mode power supply may be desireable.

For additional information about the FEDERAL TRADE COMMISSION 16 CFR Part 432 document, please go to the following link: http://www.ftc.gov/os/2000/12/amplifierrulenotice.pdf

[2] The performance numbers stated on page 1 were measured on 3/21/2006 on a variety of VR100-7 Evaluation Kits using the following firmware: VR100 RC2 128k 512k_14 PsDecimator 130.cld. These performance numbers are subject to change at any time with newer releases of firmware and/or component changes. All measurements were taken with an unregulated linear power supply provided with the VR100-7 Evaluation Kit, a digital audio input (Optical TOSLINK S/PDIF input with an Fs of 96kHz). With the exception of the Frequency Response measurement, all performance test were made with an AES17 20kHz filter and no A-Weighting filter. The Frequency Response measurement was made with an AES17 40kHz filter and again no A-Weighting filter.

[3] Peak Wattage Testing Methods (footnote from Page 1)
3Ω peak power measurements were calculated using a Linear PS that has a 35V Peak Voltage (losses and sag taken into account), 12A Per Channel Hard Current Limit. For long periods of time, continuous sine wave high-wattage outputs may be limited by over-current or thermal protective algorithms running inside the D2-914xx-LR ICs.

[4] Designed for compliance with FCC and CE (footnote from Page 1)
The VR100/75/50-5/7 Digital Amplifier (with/without Digital Feedback and/or DPSC) Reference Design has been designed with the need for an end-product to pass an FCC Class B or CE EMI/EMC test. The best engineering practices for reduction of EMI/EMC have been followed in the component selection, component usage, and signal routing in the board layout. D2Audio is willing to work with their customers in helping to ensure that the amplifier portion of their design will pass these particular EMI/EMC tests, however D2Audio can not assume responsibility that the entire end-product will pass these EMI/EMC tests.

CONSUMER

PRELIMINARY

Trademarks

Nuclear and Medical Applications

D2Audio products are not authorized for use as critical components in life support systems, equipment used in hazardous environments or nuclear control systems without the express written consent of D2Audio Corporation.

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CONSUMER

PRELIMINARY

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CONSUMER

PRELIMINARY

CONSUMER

PRELIMINARY

CONSUMER

PRELIMINARY

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1 SPECIFICATIONS

CONSUMER

PRELIMINARY

1.1 ABSOLUTE MAXIMUM RATINGS

Parameter	Condition	Min	Typ	Max	Unit
High Voltage Supply for 100W Output, 8 Ohm	+45V DC Supply	0	45	48	V
High Voltage Supply for 100W Output, 8 Ohm	-45V DC Supply	0	-45	-48	V
High Voltage Supply for 75W Output, 8 Ohm	+39V DC Supply	0	39	42	V
High Voltage Supply for 75W Output, 8 Ohm	-39V DC Supply	0	-39	-42	V
High Voltage Supply for 50W Output, 8 Ohm	+32V DC Supply	0	32	35	V
High Voltage Supply for 50W Output, 8 Ohm	-32V DC Supply	0	-32	-35	V
Low Voltage Supply	+12V DC Supply	0	12	12.6	V
Signal Voltage Supply	+5V DC Supply	0	5.0	5.5	V
Digital Voltage Supply (RVDD)	+3.3V DC Supply	3.0	3.3	3.6	V
Digital Voltage Supply	+1.8V DC Supply	1.7	1.8	2.0	V
Digital Input Signal Level[1]	All inputs	-0.6	-	3.9	V
Input Current, any pin but supplies		-	-	+/-10	mA
Nominal Operating Temperature Range[2, 5]	Amplifier board ambient temperature[3] Amplifier board heat sink temperature[4]	-10 -10	- -	45 65	°C
Storage Temperature Range	Ambient temperature	-	-	105	°C
Lead Temperature	Soldering 10 Seconds	-	-	300	°C

Note 1: -0.6V undershoots and 3.9V overshoots allowed for 4ns maximum
Note 2: Normal Operation refers to running the unit in accordance with FTC test methods.
Note 3: Temperature surrounding the VR100-7.
Note 4: Temperature at heat sink (see "Heat Sink Thermal Performance After Installation" on page 52).
Note 5: Please refer to Section 7.6, "Ambient Operating Conditions," on page 53 for the operating range and derating curves.

TABLE 1: Absolute Maximum Ratings

1.2 ELECTRICAL CHARACTERISTICS

T_A = 25° C, Typical Power Supply for VR100-7, Ground = 0V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input low voltage[1]	V_{IL}	All inputs	-	-	0.8	V
Input high voltage[1]	V_{IH}	All inputs	2.0	-	-	V
Output low voltage[1]	V_{OL}	4mA Load	-	-	0.4	V
Output high voltage[1]	V_{OH}	4mA Load	RVDD-0.4	-	-	V
Input current	I_C	All inputs with resistive pulls - BOOT_EE/I2C, nRESET, SDA, SCL, LRCLK[3:0], SCLK[3:0], SDIN[3:0], GPIO[1:0]	-	-	+/-0.4	mA

Note 1: Voltage levels refer to digital signals only, not PWM outputs or power supplies.

TABLE 2: Electrical Characteristics

CONSUMER

PRELIMINARY

1.3 PERFORMANCE CHARACTERISTICS

Resistance load = 8Ω, T_A = 25°C, (V_{+45V}=45V ~32V, V_{-45V}=-45V ~ -32V for VR100-7), V_{+12VDC}=12V, V_{+5VDC}=5V, $V_{+3.3VDC}$=3.3V, $V_{+1.8VDC}$=1.8V, Ground = 0V, 24-bit I^2S Input Sampled at 48kHz

Specification	Condition	Min	Typ	Max	Unit
Output Power for VR100-7 when V_{+45V}=45V, V_{-45V}=-45V	FTC, Alternative A, B, C or EIA/CEA-490-A test method[1]	0	100	110[2]	W
Output Power for VR100-7 when V_{+45V}=39V, V_{-45V}=-39V	FTC, Alternative A, B, C or EIA/CEA-490-A test method[1]	0	75	85[2]	W
Output Power for VR100-7 when V_{+45V}=32V, V_{-45V}=-32V	FTC, Alternative A, B, C or EIA/CEA-490-A test method[1]	0	50	60[2]	W
Frequency Response	20Hz to 40kHz, 1W	-0.5		+0.5	dB
SNR/Dynamic Range		100	101	103[3]	dB
Output Distortion (THD+N)	20Hz to 20kHz, 1W		0.1		%

Note 1: With the appropriate amount of heat distribution via external heat sink and power supply. Heat sink size (and addition of optional fan) and power supply size ultimately determines which of the above mentioned tests the end-product is capable of passing.

Note 2: The max power numbers shown may be limited in duration due a number of factors including: Current Limiting algorithms running inside the D2-914xx-LR ICs, the type of power supply used (unregulated linear or regulated SMPS), the size of the transformer or SMPS used, the amount of bulk capacitance used, variations in the voltage applied to the power stage, etc.

Note 3: The SNR/Dynamic Range, using the current VR100-7 (Rev 3) Evaluation Kit and latest firmware at the time of this writing was found to be 103dB. Performance is subject to change in the future due to changes in the firmware running on the DAE-2 ICs, surrounding components or changes in the board layout.

TABLE 3: Performance Characteristics

1.4 DC POWER REQUIREMENTS

CONSUMER

PRELIMINARY

Resistance load = 8Ω, T_A = 25°C, (V_{+45V}=45V ~ 32V, V_{-45V}=-45V ~ -32V for VR100-7), V_{+12VDC}=12V, V_{+5VDC}=5V, $V_{+3.3VDC}$=3.3V, $V_{+1.8VDC}$=1.8V, Ground = 0V

Symbol	Description	Min	Typ	Max	Unit
V_{+45V}	+45V High Voltage Supply for VR100-7 (100W Designs)	0	45	48	V
V_{-45V}	-45V High Voltage Supply for VR100-7 (100W Designs)	0	-45	-48	V
V_{+45V}	+39V High Voltage Supply for VR100-7 (75W Designs)	0	39	42	V
V_{-45V}	-39V High Voltage Supply for VR100-7 (75W Designs)	0	-39	-42	V
V_{+45V}	+32V High Voltage Supply for VR100-7 (50W Designs)	0	32	35	V
V_{-45V}	-32V High Voltage Supply for VR100-7 (50W Designs)	0	-32	-35	V
V_{+12VDC}	+12V Low Voltage Supply	11.5	12	12.6	V
V_{+5VDC}	+5V Signal Voltage Supply	4.75	5	5.5	V
$V_{+3.3VDC}$	+3.3V Digital Voltage Supply	3.0	3.3	3.6	V
$V_{+1.8VDC}$	+1.8V Digital Voltage Supply	1.7	1.8	1.9	V

TABLE 4: DC Voltage Requirements

Symbol	Description	Min	Idle	Max	Unit
$I_{+/-45V}$	+/-45V High Voltage Supply Current, per channel[1]	0	0.02	-	A
I_{+12V}	+12V Supply Current[1]	0	0.35[2]	0.40[3]	A
I_{+5V}	+5V Supply Current	0	0.850	-	A
$I_{3.3V}$	+3.3V Digital Voltage Supply	0	0.15	0.16	A
$I_{1.8V}$	+1.8V Digital Voltage Supply	0	2.00	2.50	A
I_{HCLTP}	Per-channel short-circuit hard current limit trip point[5]	-	-	12	A

Note 1: Minimum current measured with either the nRESET line asserted active-low, or the overload protection circuit activated for the particular channel

Note 2: Idle current measured with the amplifier in operation, but no input applied

Note 3: Maximum current measured with 1kHz sine wave output at rated power. The VR100-7 is designed to meet FTC Alternative A (all associated channels driven), Alternative B (front or surround channels driven), Alternative C (two associated channels driven) test method or the EIA/CEA-490-A test method, provided that the designer has provided enough heat-sinking and cooling to the digital amplifier reference design and/or end-system. Under normal conditions for most applications, all channels may not need to be driven at full power simultaneously. More typically, the power output requirement is 1/8 to 1/3 of the total amplifier output. However if the amplifier is allowed to be driven into high distortion ("clipping"), the power supply current may approach 20% more than required for a full scale output. It is therefore up to the system designer to determine how much power output will be allowed to be produced, and hence determine the maximum and average power supply current requirements.

Note 4: Current specification based on 8Ω loads under FTC all channels driven specification.

Note 5: Hard current limit trip point triggers automatic short-circuit protection (see Section 3.4.1, "Short-Circuit/Over-Current Protection," on page 27).

TABLE 5: DC Current Requirements

CONSUMER

PRELIMINARY

1.5 SWITCHING CHARACTERISTICS - SERIAL AUDIO PORT

T_A = 25°C, (V_{+45V}=45V ~ 32V, V_{-45V}=-45V ~ -32V for VR100-7), V_{+12VDC}=12V, V_{+5VDC}=5V, $V_{+3.3VDC}$=3.3V, $V_{+1.8VDC}$=1.8V, Ground = 0V, Sample Rate 32kHz-192kHz

Symbol	Description	Min	Typ	Max	Unit
t_cSCLK	SCLKx frequency - SCLK0, SCLK1, SCLK2, SCLK3, SCLKT	-	-	12.5	MHz
t_wSCLK	SCLKx pulse width (high and low) - SCLK0, SCLK1, SCLK2, SCLK3, SCLKT	40	-	-	ns
t_sLRCLK	LRCLKx setup to SCLK rising - LRCLK0, LRCLK1, LRCLK2, LRCLK3, LRCLKT	20	-	-	ns
t_hLRCLK	LRCLKx hold from SCLK rising - LRCLK0, LRCLK1, LRCLK2, LRCLK3, LRCLKT	20	-	-	ns
t_sSDI	SDINx setup to SCLKx rising - SDIN0, SDIN1	20	-	-	ns
t_hSDI	SDINx hold from SCLKx rising - SDIN0, SDIN1	20	-	-	ns

TABLE 6: Serial Audio Port Timing

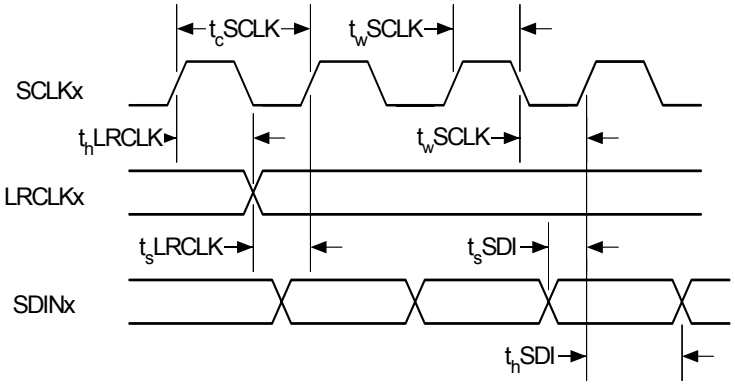


FIGURE 1: Serial Audio Port Timing

1.6 SWITCHING CHARACTERISTICS - PSSYNC PIN

T_A = 25°C, (V_{+45V}=45V ~ 32V, V_{-45V}=-45V ~ -32V for VR100-7), V_{+12VDC}=12V, V_{+5VDC}=5V, $V_{+3.3VDC}$=3.3V, $V_{+1.8VDC}$=1.8V, Ground = 0V

Description	Min	Typ	Max	Unit
PSSYNC Frequency	511	512	513	kHz
PSSYNC Duty Cycle	49	50	51	%

TABLE 7: PSSYNC Pin Characteristics

1.7 SWITCHING CHARACTERISTICS - FAN_CONTROL PIN

T_A = 0° - 65°C, (V_{+45V}=45V ~ 32V, V_{-45V}=-45V ~ -32V for VR100-7), V_{+12VDC}=12V, V_{+5VDC}=5V, $V_{+3.3VDC}$=3.3V, $V_{+1.8VDC}$=1.8V, Ground = 0V

Description	Min	Typ	Max	Unit
FAN_CONTROL Frequency	511	512	513	kHz
FAN_CONTROL Duty Cycle	30	Note 1	95	%
Note 1: There is a relationship between temperature and pulse width. At temperatures below 35 degrees C, the duty cycle is 30%. At 65 degrees C, the duty cycle is maximum. Between 35 and 65 degrees, the duty cycle increases linearly with increasing temperature.				

TABLE 8: FAN_CONTROL Pin Characteristics

1.8 SWITCHING CHARACTERISTICS - CONTROL INTERFACE

CONSUMER

T_A = 25°C, (V_{+45V}=45V ~ 32V, V_{-45V}=-45V ~ -32V for VR100-7), V_{+12VDC}=12V, V_{+5VDC}=5V, $V_{+3.3VDC}$=3.3V, $V_{+1.8VDC}$=1.8V, Ground = 0V

Symbol	Description	Min	Max	Unit
fSCL	SCL frequency - SCL	-	100	kHz
t_{buf}	Bus free time between transmissions	4.7	-	us
t_{wlow}SCL	SCLx clock low - SCL	4.7	-	us
t_{whigh}SCL	SCLx clock high - SCL	4.0	-	us
t_sSTA	Setup time for a (repeated) Start	4.7	-	us
t_hSTA	Start condition Hold time	4.0	-	us
t_hSDA	SDA hold from SCL falling (see note) - SDA	0	-	us
t_sSDA	SDA setup time to SCL rising - SDA	250	-	ns
t_dSDA	SDA output delay time from SCL falling - SDA	-	3.5	us
t_r	Rise time of both SDA and SCL	-	1	us
t_f	Fall time of both SDA and SCL	-	300	ns
t_sSTO	Setup time for a Stop condition	4.7	-	us
Note: Data must be held sufficient time to bridge the 300ns transition time of SCL				

TABLE 9: Control Interface Port Timing

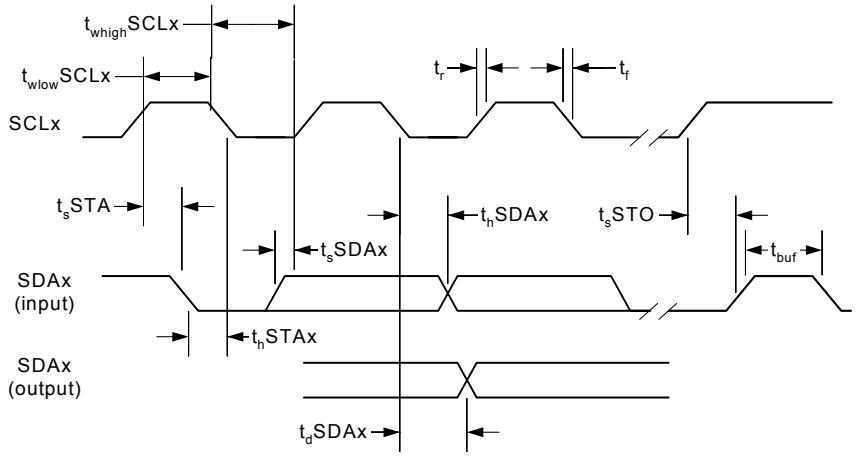


FIGURE 2: Control Interface Timing

PRELIMINARY

1.9 PERFORMANCE PLOTS

The following graphs (Figure 3 - Figure 8) show the VR100-7 amplifier performance taken from VR100-7 (Rev 3) Evaluation Kits on 3/21/2006 with the following firmware code load: VR100 RC2 128k 512k_14 PsDecimator 130.cld. In all plots, both Digital Feedback and DPSC are enabled. The DAE-2 ICs used in these Evaluation Kits were the D2-91413-LR which enable both Digital Feedback and DPSC. The power supply used was unregulated and implemented a 650VA Basler Electronics Transformer, Slow-Start Power Supply Circuit board, full-bridge rectifier, and a total of 37,700uF of bulk capacitance per high voltage rail (+/-45V). The transformer also delivered +15V to the VR100-7 MoM board which derived the remaining voltages needed by the VR100-7. These voltages were regulated by the MoM board or on the VR100-7 itself. All inputs are driven with the same input signal. All inputs are mapped to their respective outputs. The output channels are tested one at a time and only the output channel being measured is terminated with an ideal 8Ω load, unless otherwise noted. The other outputs are open.

1.9.1 FREQUENCY RESPONSE AT 1W, 10W, 75W (20HZ - 20KHZ)

Conditions: Typical Supplies, Room Temperature, Optical TOSLINK S/PDIF Input Sampled at 96kHz with a Bit Resolution of 24-bit, 20Hz to 20kHz, 1kHz Sine Wave, 1W (Red Colored Line), 10W (Aqua Colored Line) and 75W (Blue Colored Line) Output Power, 0dBr Referenced to 100W, 20kHz AES17 Filter Enabled, Unweighted

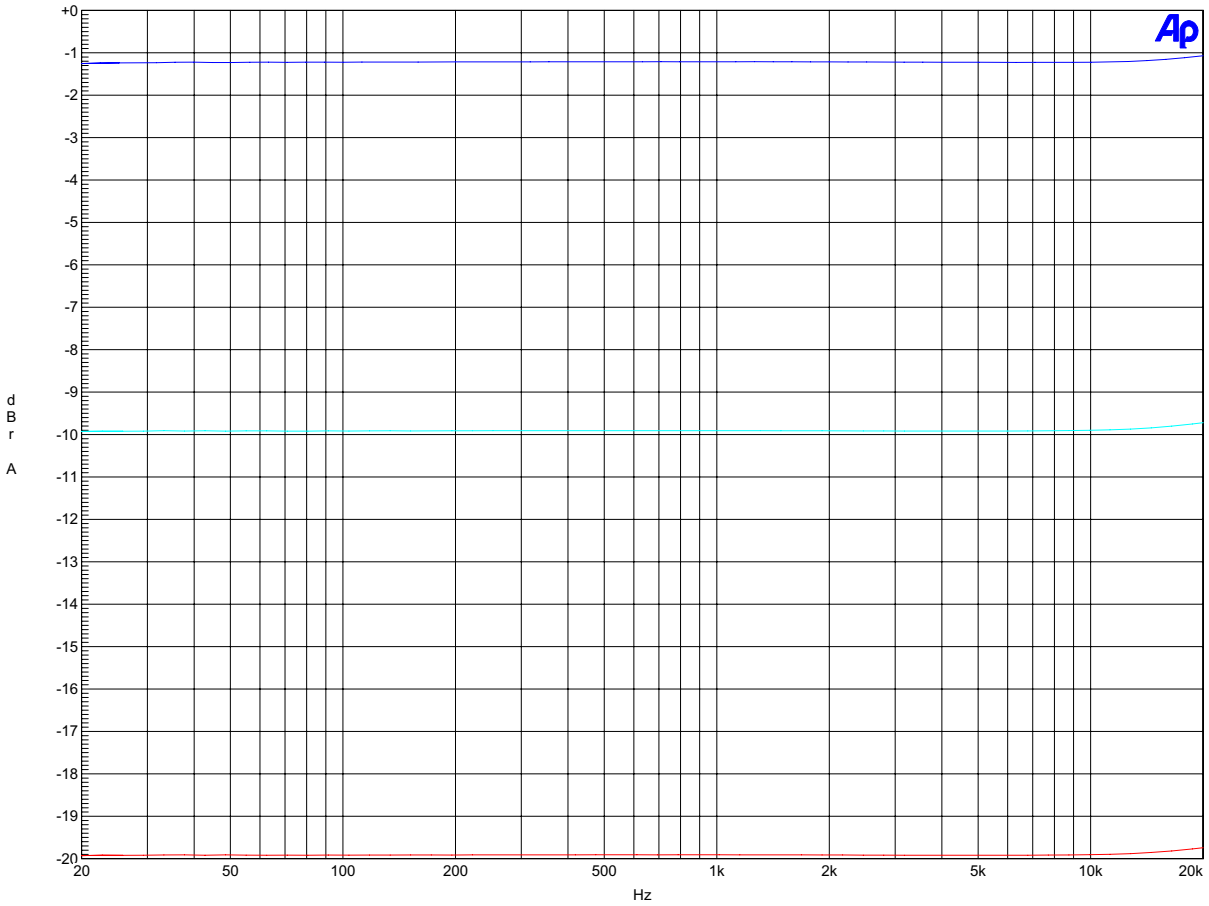


FIGURE 3: Frequency Response at 1W, 10W, 75W (20Hz - 20kHz)

1.9.2 FREQUENCY RESPONSE AT 1W, 10W (20HZ - 40KHZ)

CONSUMER

Conditions: Typical Supplies, Room Temperature, Optical TOSLINK S/PDIF Input Sampled at 96kHz with a Bit Resolution of 24-bit, 20Hz to 40kHz, 1kHz Sine Wave, 1W (Red Colored Line) and 10W (Aqua Colored Line) Output Power, 0dBr Referenced to 100W, 40kHz AES17 Filter Enabled, Unweighted

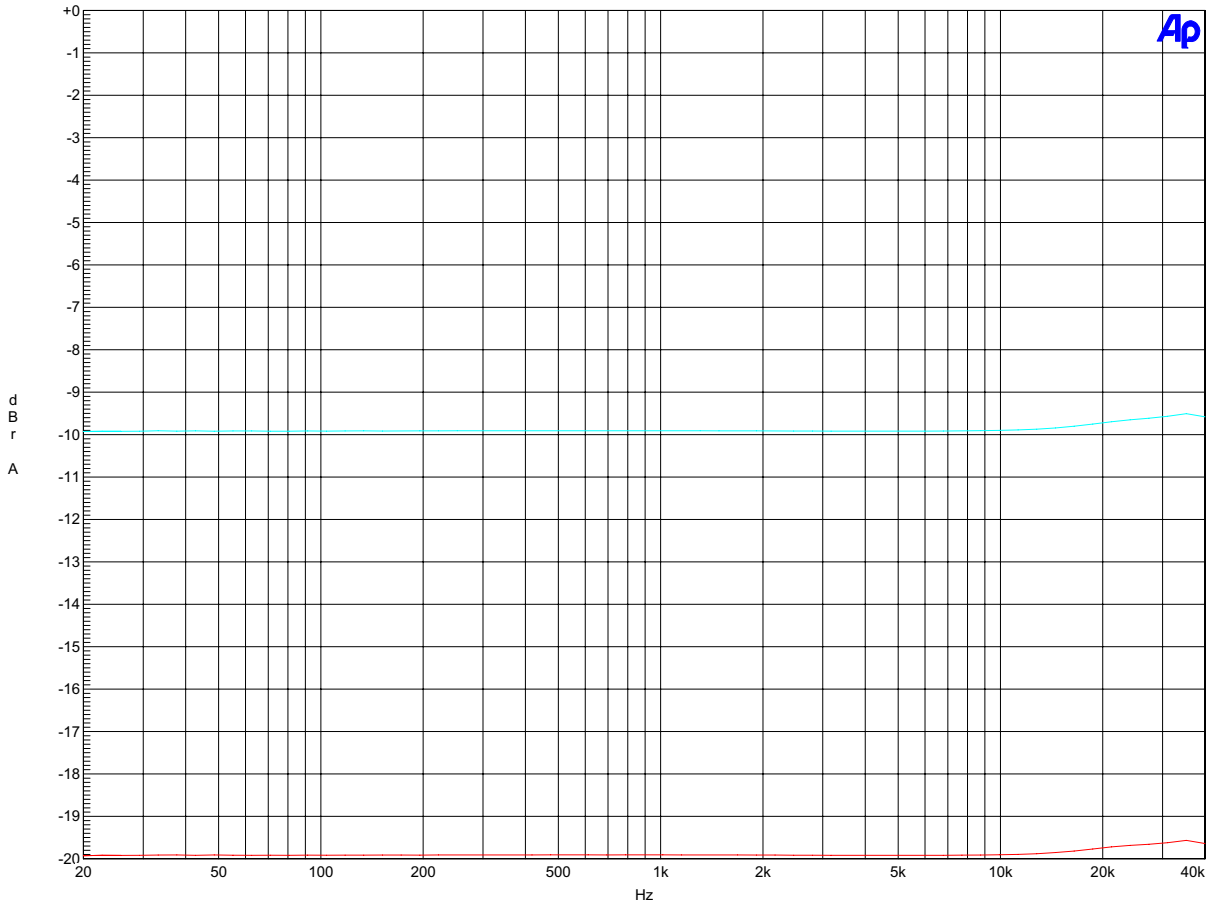


FIGURE 4: Frequency Response at 1W, 10W (20Hz - 40kHz)

PRELIMINARY

CONSUMER

PRELIMINARY

1.9.3 THD+N VS. FREQUENCY

Conditions: Typical Supplies, Room Temperature, Optical TOSLINK S/PDIF Input Sampled at 96kHz with a Bit Resolution of 24-bit, 20Hz to 20kHz, -20.6dBFS Input, 1W Output Power, 20kHz AES17 Filter Enabled, Unweighted

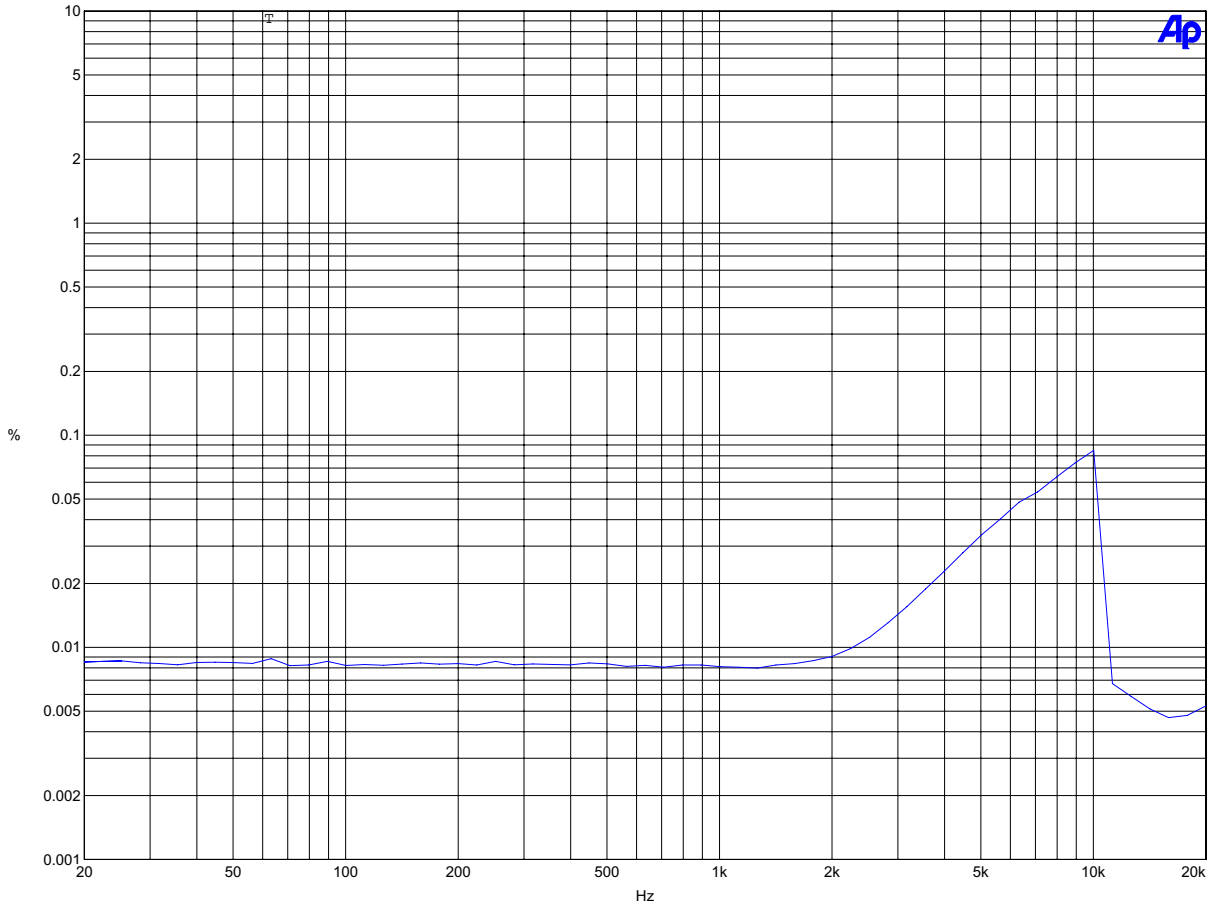


FIGURE 5: THD+N vs. Frequency (1W, 8Ω Load)

1.9.4 THD+N VS. POWER (1W TO 100W, 8Ω LOAD)

Conditions: Typical Supplies, Room Temperature, Optical TOSLINK S/PDIF Input Sampled at 96kHz with a Bit Resolution of 24-bit, 1kHz Sine Wave Input, 20kHz AES17 Filter Enabled, Unweighted

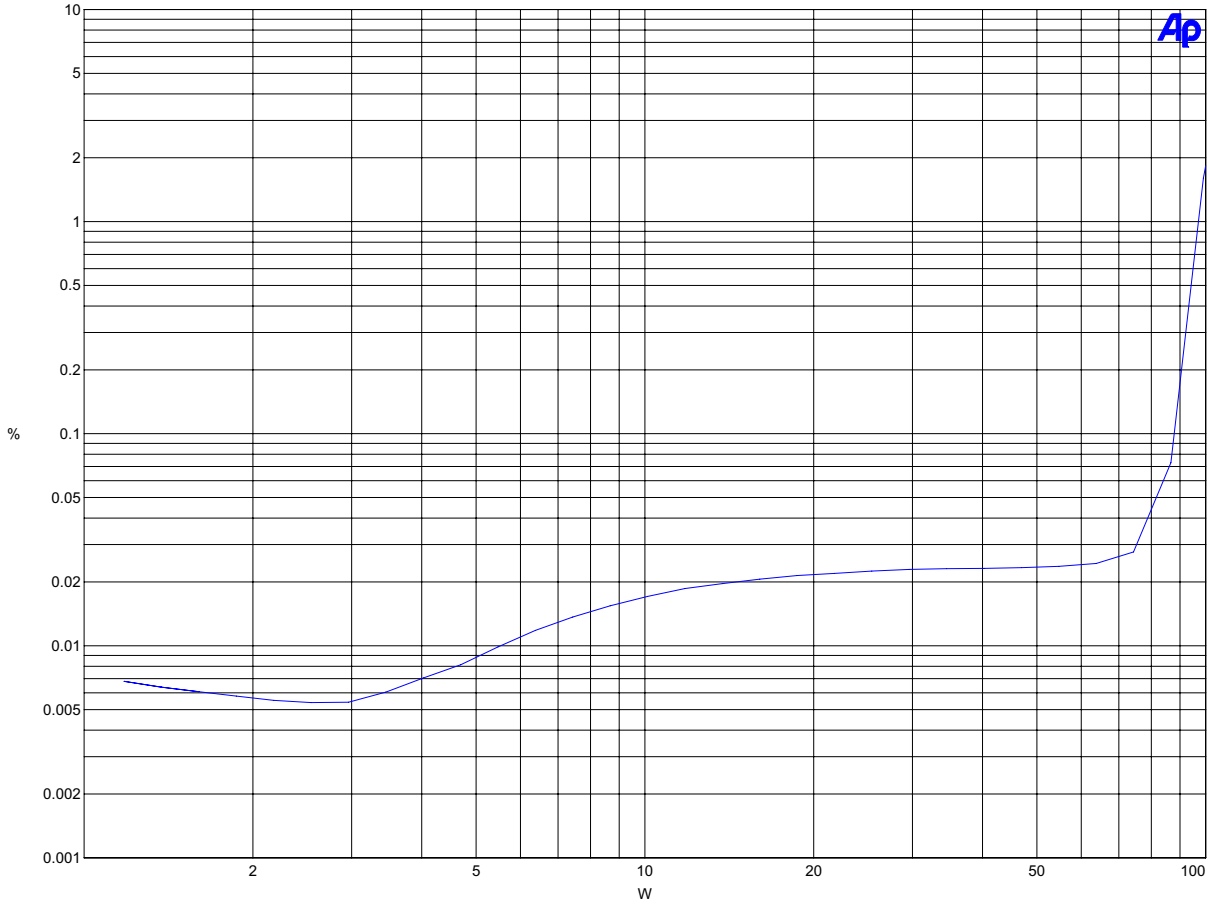


FIGURE 6: THD+N vs. Power (From 1W to 100W, 8Ω Load)

CONSUMER

PRELIMINARY

CONSUMER

PRELIMINARY

1.9.5 CROSSTALK (CHANNEL 1 TO 2, 8Ω LOAD)

Conditions: Typical Supplies, Room Temperature, Optical TOSLINK S/PDIF Input Sampled at 96kHz with a Bit Resolution of 24-bit, Input -3.0 dBFS into Channel 1, measure THD+N Amplitude on Channel 2, 20Hz - 20kHz, 20kHz AES17 Filter Enabled, Unweighted

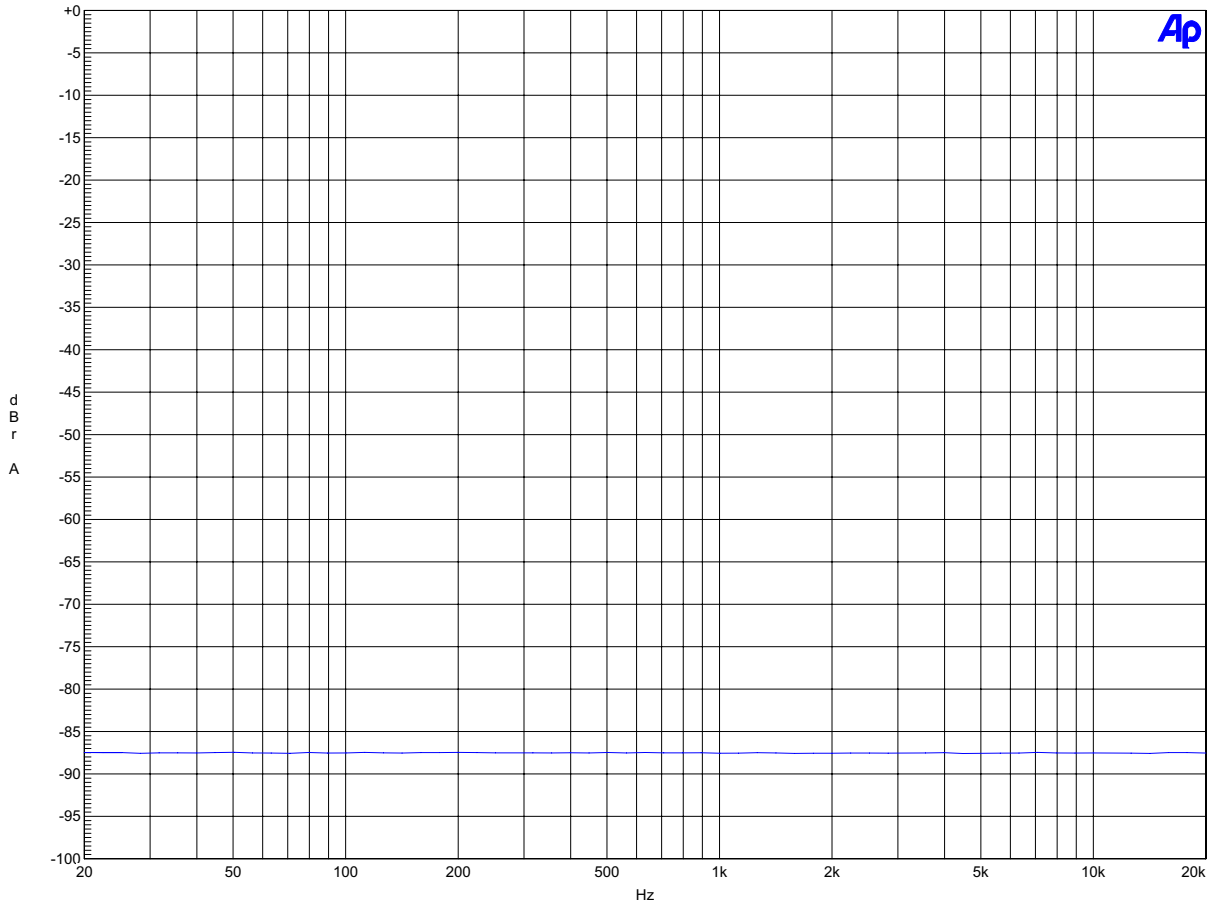


FIGURE 7: Crosstalk (20Hz - 20kHz, 8Ω Load)

1.9.6 FFT - NOISE FLOOR (1W, 1KHZ, 8OHM, 20HZ - 40KHZ)

Conditions: Power Supplies, Room Temperature, Optical TOSLINK S/PDIF Input Sampled at 96kHz with a Bit Resolution of 24-bit, -20.6dBFS Input Level, 1kHz Sine Wave, 8Ω Load, 40kHz AES17 Filter Enabled, Unweighted

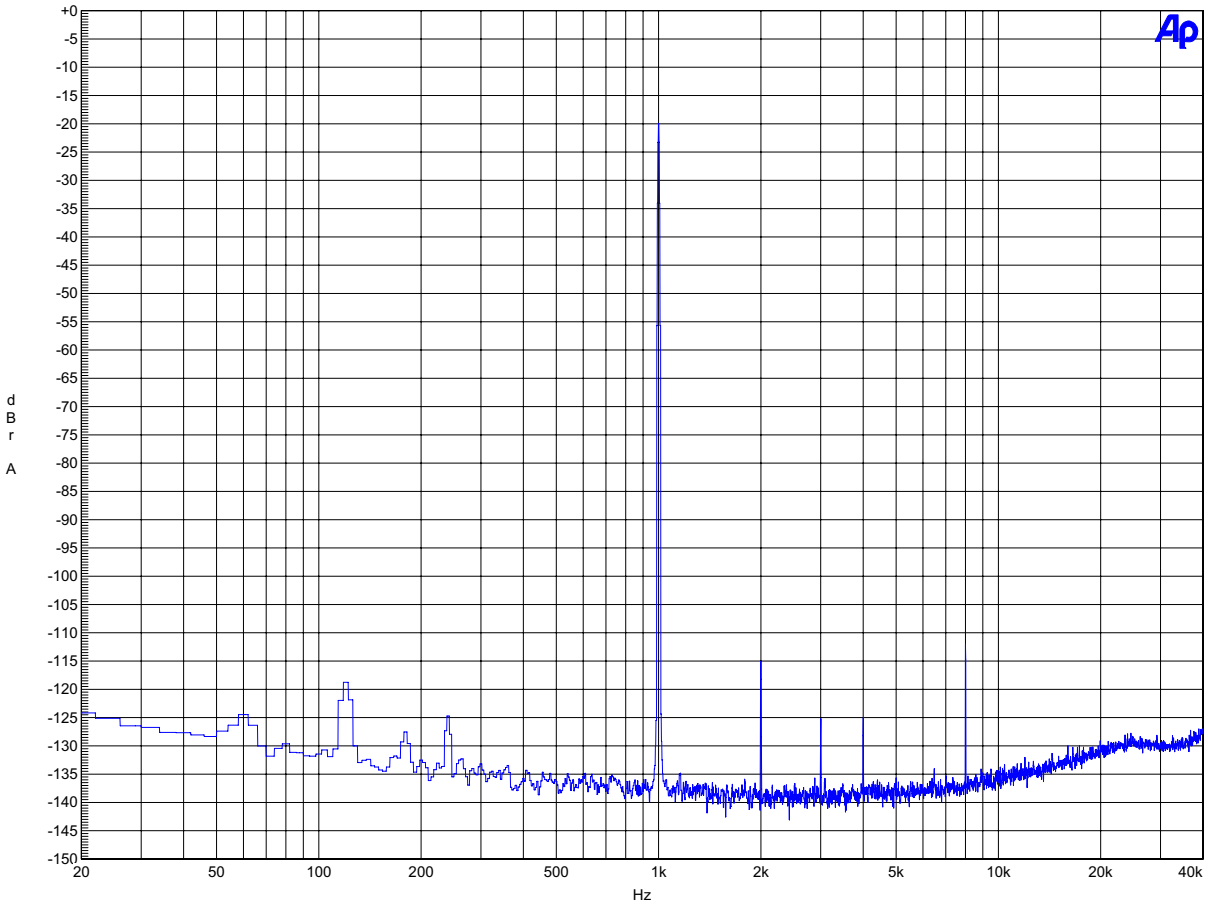


FIGURE 8: FFT - Noise Floor (1W, 1kHz Sine Wave, 8Ω Load, 20Hz - 40kHz)

CONSUMER

PRELIMINARY

2 AMPLIFIER PINOUT

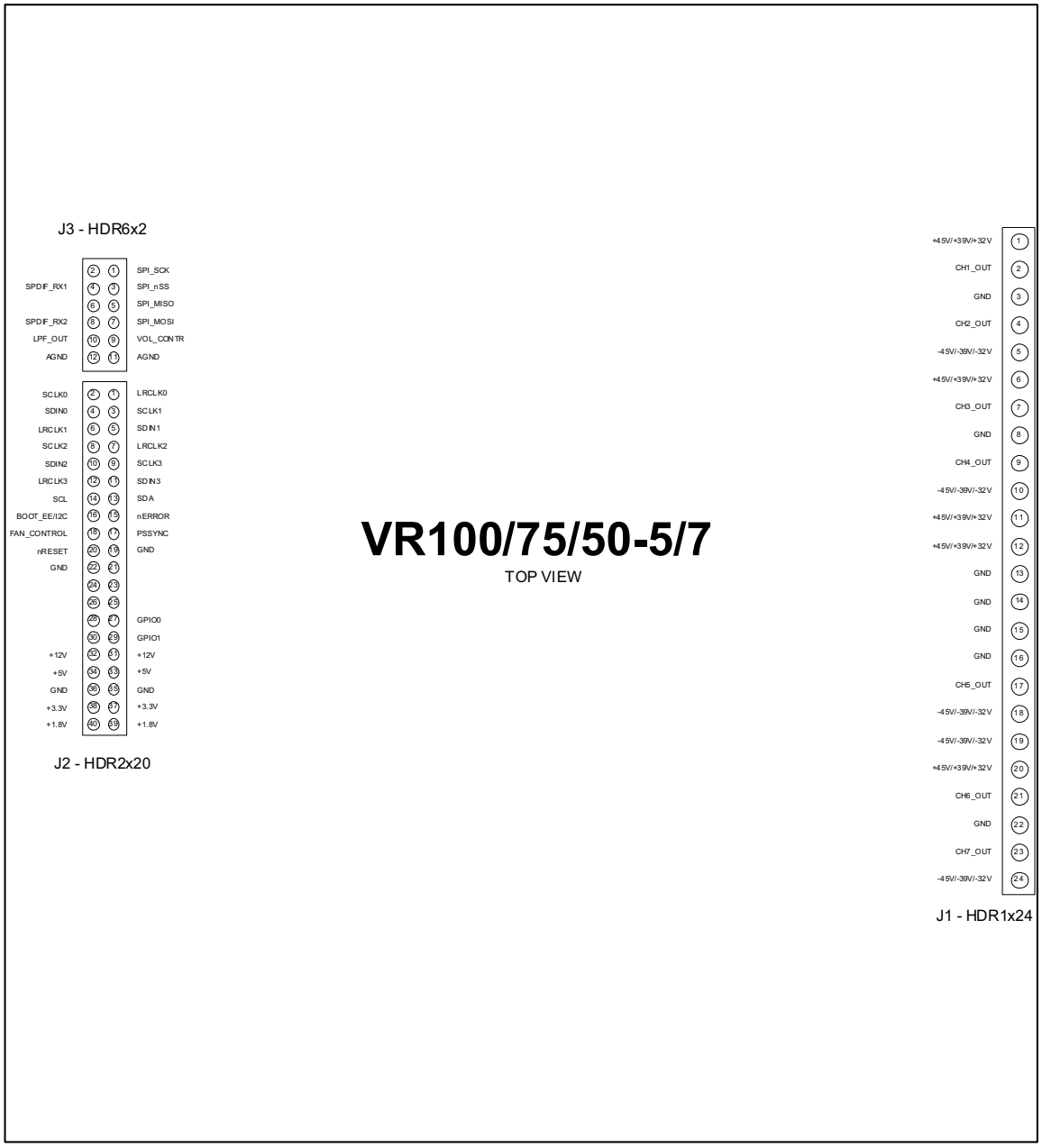


FIGURE 9: VR100-7 Amplifier Pinout (Not to Scale)

2.1 PIN DEFINITIONS

CONSUMER

PRELIMINARY

Pin #	Pin Name	I/O	Description
J2-1	LRCLK0	I	SAI 0 left/right clock
J2-2	SCLK0	I	SAI 0 serial data bit clock
J2-3	SCLK1	I	SAI 1 serial data bit clock
J2-4	SDIN0	I	SAI 0 input data
J2-5	SDIN1	I	SAI 1 input data
J2-6	LRCLK1	I	SAI 1 left/right clock
J2-7	LRCLK2	I	SAI 2 left/right clock
J2-8	SCLK2	I	SAI 2 serial data bit clock
J2-9	SCLK3	I	SAI 3 serial data bit clock
J2-10	SDIN2	I	SAI 2 input data
J2-11	SDIN3	I	SAI 3 input data
J2-12	LRCLK3	I	SAI 3 left/right clock
J3-4	SPDIF_RX1	I	S/PDIF1 data input
J3-8	SPDIF_RX2	I	S/PDIF2 data input

TABLE 10: Digital Audio Signal Pins

Pin #	Pin Name	I/O	Description
J3-10	LPF_OUT	O	This is a filtered PWM output from Channel 8 which is intended to be used as a Subwoofer Line-Level Analog Output.

TABLE 11: Analog Audio Signal Pin

Pin #	Pin Name	I/O	Description
J2-13	SDA	I/O	Digital amplifier reference design control interface data- channels Left, Right, Left Surround, Right Surround, Surround Back Left, Surround Back Right, Center, Subwoofer
J2-14	SCL	I/O	Digital amplifier reference design control interface clock- channels Left, Right, Left Surround, Right Surround, Surround Back Left, Surround Back Right, Center, Subwoofer
J2-15	nERROR	O	Overall amplifier error indication, active low
J2-16	BOOT_EE/I2C	I	Boot select control
J2-17	PSSYNC	O	Power supply sychronization clock
J2-18	FAN_CONTROL	O	Optional external cooling fan control signal
J2-20	nRESET	I	Amplifier reset, active low, Open Collector Drive
J2-27	GPIO0	I/O	GPIO pin
J2-29	GPIO1	I/O	GPIO pin
J3-9	VOL_CONTR	O	Power Supply Volume Control.

TABLE 12: Control Interface Signal Pins

Pin #	Pin Name	I/O	Description
J1-1	SPI_SCK	I/O	SPI clock IO
J1-3	SPI_nSS	I/O	SPI slave select IO
J1-5	SPI_MISO	I	SPI master input
J1-7	SPI_MOSI	O	SPI master output

TABLE 13: SPI Pins

Pin #	Pin Name	I/O	Description
J1-2	CH1_OUT	O	Channel 1 Loudspeaker Output
J1-4	CH2_OUT	O	Channel 2 Loudspeaker Output
J1-7	CH3_OUT	O	Channel 3 Loudspeaker Output
J1-9	CH4_OUT	O	Channel 4 Loudspeaker Output
J1-17	CH5_OUT	O	Channel 5 Loudspeaker Output
J1-21	CH6_OUT	O	Channel 6 Loudspeaker Output
J1-23	CH7_OUT	O	Channel 7 Loudspeaker Output

TABLE 14: Loudspeaker Output Pins

Pin #	Pin Name	I/O	Description
J2-19, J2-22, J2-35, J2-36, J1-3, J1-8, J1-13, J1-14, J1-15, J1-16, J1-22	GND	-	General purpose ground
J3-11, J3-12	AGND	-	Analog ground
J1-1, J1-6, J1-11, J1-12, J1-20	45V ~ 32V	-	VR100-7 (+45V ~ 32V) DC High Voltage Positive Supply
J1-5, J1-10, J1-18, J1-19, J1-24	-45V ~ -32V	-	VR100-7 (-45V ~ -32V) DC High Voltage Negative Supply
J2-31, J2-32	+12V	-	+12V DC Low Voltage Supply
J2-33, J2-34	+5V	-	+5V DC Signal Voltage Supply
J2-37, J2-38	+3.3V	-	+3.3V DC Digital Voltage Supply
J2-39, J2-40	+1.8V	-	+1.8V DC Digital Voltage Supply

TABLE 15: Power Supply Pins

2.2 PIN DESCRIPTIONS

2.2.1 DIGITAL S/PDIF AUDIO INPUTS

SPDIF_RX[2:1] **S/PDIF Data Inputs**

These pins are the S/PDIF audio inputs and accept a 3.3V stereo input up to 192kHz. To drive these pins, appropriate buffer and/or isolation circuits may be necessary to convert the S/PDIF cable input signal to clean logic levels. These inputs can serve a 2nd or 3rd Zone S/PDIF inputs where the audio format is IEC60958 compliant. These S/PDIF inputs can not handle IEC61937-packed audio data streams.

2.2.2 DIGITAL SERIAL AUDIO INPUTS (SAI PORTS)

LRCLK[3:0] **Left/Right Clock**

These pins are the framing clocks for the respective Serial Audio Inputs. The serial input data is transmitted as two channels every sample rate period. LRCLK determines the start of each data pair. The LRCLK frequency determines the input sample rate (Fs). LRCLK is a 3.3V input.

SCLK[3:0] **Shift Clock**

These pins are the shift clocks for the respective independent Serial Audio Inputs and are used to frame each input bit of the serial input data. The shift clock frequency is typically 128*Fs. SCLK is a 3.3V input.

SDIN[3:0] **Serial Data Input**

These pins are the serial data inputs and are arranged as four left/right input pairs. Input format options are I^2S or Left-Justified. 16, 18, 20, and 24 bit data lengths are supported. SDIN is a 3.3V input.

2.2.3 CONTROL SIGNAL PINS

BOOT_EE/I2C **Boot Selection**

This pin is the boot selection input. The boot selection picks the source location for the DSP boot code and is predominantly used for firmware upgrade. See Section 3.1, "Activating the amplifier," on page 25 for further information. This pin is pulled high internally to 3.3V via a 10kΩ resistor.

FAN_CONTROL **Fan Control**

This output pin controls an **optional** external cooling fan and operates at a 512kHz PWM output switch rate.

nERROR **Amplifier Error**

The error signal is an open-drain output with 10kΩ internal pullup to 3.3V that, when low, indicates a fault condition has occurred in the amplifier, or that the amplifier has not been initialized. Fault conditions include over-temperature, over-current, short circuit, and output power stage disabled. See Section 3.4, "Amplifier Protection," on page 27 for further details.

nRESET **Reset**

This pin is the active-low reset input to the digital amplifier reference design. Driving the reset to active low for 10mS will bring all internal devices to their default state. During the power on sequence, the reset line must be active low during the high voltage supply ramp period and held for a minimum of 100 mS after the high voltage supply reaches 95% of its nominal value. The nReset is a bidirectional pin and is used to issue a reset between digital amplifier reference designs in a master/slave configuration. The reset pin must be driven with an open collector or open drain driver.

PSSYNC **Power Supply Synchronization**

This pin is a power supply synchronization output and may be used to synchronize any external switching power supply to the 512kHz PWM output switch rate.

SCL **Digital Amplifier Reference Design Control Interface Clock**

This pin is the serial clock input line of the digital amplifier reference design control interface and is pulled high internally to 3.3V via a 10 kΩ resistor.

SDA **Serial Data**

This pin is the bidirectional serial data line of the digital amplifier reference design control interface. This pin is pulled high internally to 3.3V via a 10kΩ resistor.

GPIO[1:0] **General Purpose**

These pins are general purpose input pins and are pulled high internally to 3.3V via a 10kΩ resistor.

LPF_OUT **General Purpose**

This pin is a 3.3V level output and operates at a 512kHz PWM output switch rated. It is connected to Channel 8 of the D2-914xx-LR and is intended to be sent to an active filter circuit (opamp) which then filters and amplifies the signal to become a line-level subwoofer line out. This additional active filter circuitry is included in the VR100-7 for the designer's reference. The subwoofer line output has approximately 5.3Vrms output capability.

VOL_CONTR **General Purpose**

This output pin can be optionally connected to the power supply to adjust the +/- high-voltage rails with additional circuitry. This has the effect of having "analog-like" volume control. This pin operates at a 512kHz PWM output switch rate.

2.2.4 DIGITAL SERIAL AUDIO INPUTS (SAI PORTS)

SPI_nSS **Slave Select**

SPI slave select IO. This pin is pulled high internally to 3.3V via a 10kΩ resistor.

SPI_SCK **SPI Clock**

SPI clock IO with hysteresis input. This pin is pulled high internally to 3.3V via a 10kΩ resistor.

SPI_MISO **Master In Slave Out**

SPI master input, slave output data signal. This pin is pulled high internally to 3.3V via a 10kΩ resistor.

SPI_MOSI **Master Out Slave In**

SPI master output, slave input data signal. This pin is pulled high internally to 3.3V via a 10kΩ resistor.

2.2.5 LOUDSPEAKER OUTPUTS

CH[7:1]_OUT **Loudspeaker Outputs**

These pins provide the power amplifier outputs. Each channel of the amplifier is a half-bridge output configuration consisting of a single output. The outputs must remain floating and must not be connected to ground.

2.3 MULTICHANNEL INPUT MAPPING

The definition for the serial data inputs to the amplifiers are fixed in order to accommodate the Zone_2 and Zone_3 functionality. The following table defines the SAI inputs to their respective speaker output channels. Note: For those who may have designed with D2Audio's module-based products before in an AVR design, please note that the VR100-7 signal flow does not swap SAI0 and SAI1 inputs with respect to the outputs like the XR, XRT, MXR signal flows.

Speaker Output	SAI Interface	I^2S/LJ Channel
Left	0	Left
Right	0	Right
Left Surround	1	Left
Right Surround	1	Right
Surround Back Left	2	Left
Surround Back Right	2	Right
Center	3	Left
Subwoofer (Line Level Output Only)	3	Right

TABLE 16: 7.1 Multichannel Input Mapping

Speaker Output	SAI Interface	I^2S/LJ Channel
Left	0	Left
Right	0	Right
Left Surround	1	Left
Right Surround	1	Right
Zone 2 Left	2	Left
Zone 2 Right	2	Right
Center	3	Left
Subwoofer (Line Level Output Only)	3	Right

TABLE 17: 5.1 Multichannel Input with Second Zone Mapping

Speaker Output	SAI Interface	I^2S/LJ Channel
Left	0	Left
Right	0	Right
Zone 3 Left	1	Left
Zone 3 Right	1	Right
Zone 2 Left	2	Left
Zone 2 Right	2	Right
Center	3	Left
Subwoofer (Line Level Output Only)	3	Right

TABLE 18: 3.1 Multichannel with Zone 2 and Zone 3 Input Mapping

3 AMPLIFIER OPERATION

CONSUMER

The input to each pair of amplifier channels is a digital SAI port. The input sources may be configured through hardware or software settings.

3.1 ACTIVATING THE AMPLIFIER

After reset, the VR100-7 digital amplifier reference design DSP typically boots from the I2C EEPROM. There are two boot mode selections as defined in the following table:

BOOT_EE/I2C	Description
1	Boot from internal EEPROM (Default mode)
0	Boot through the Control Interface (a.k.a. Module Control Interface or MCI)

Table 19: Boot Selection

When BOOT_EE/I2C is high, the amplifier will boot from the I2C EEPROM. When BOOT_EE/I2C is low, the amplifier gets the boot code from an external device via the control interface. An external controller is expected to load the boot code. The BOOT_EE/I2C pin is used primarily for field firmware upgrades using the SCAMP III dongle.

3.1.1 POWER SUPPLY REQUIREMENTS VS. OUTPUT POWER

The VR100-7 must be operated at the specified typical high voltage supplies documented in sectionSection 1.4, "DC Power Requirements," on page 11 between 0 and 49V. The typical full scale output is a function of the high voltage power supply, when the digital amplifier reference design has Digital Feedback and DSPC disabled (running "open loop"). However, when Digital Feedback and DSPC is enabled, the output power of the amplifier will try to hold the same level of output power, even if the voltage rail dips slightly below the nominal operating level.

3.1.2 POWER SUPPLY SEQUENCING AND RESET

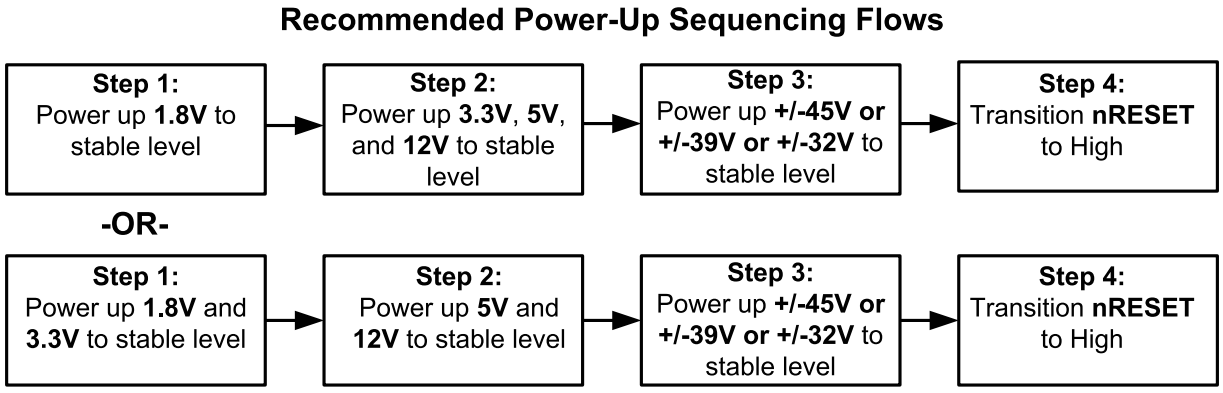
When powering up the VR100-7, the parameters below **must** be followed (see also the flowchart in Figure 10 and the waveform diagram in Figure 11, below):

Low-Voltage Supplies (+12V, +5V, +3.3V, +1.8V):

- 10% to 90% voltage ramp time >= 1.5V/mS

High-Voltage Supply (+/-45V ~ +/-32V):

- 10% to 90% voltage ramp time <= 1.5V/mS



PRELIMINARY

FIGURE 10: Power Supply Sequencing Flow Diagram

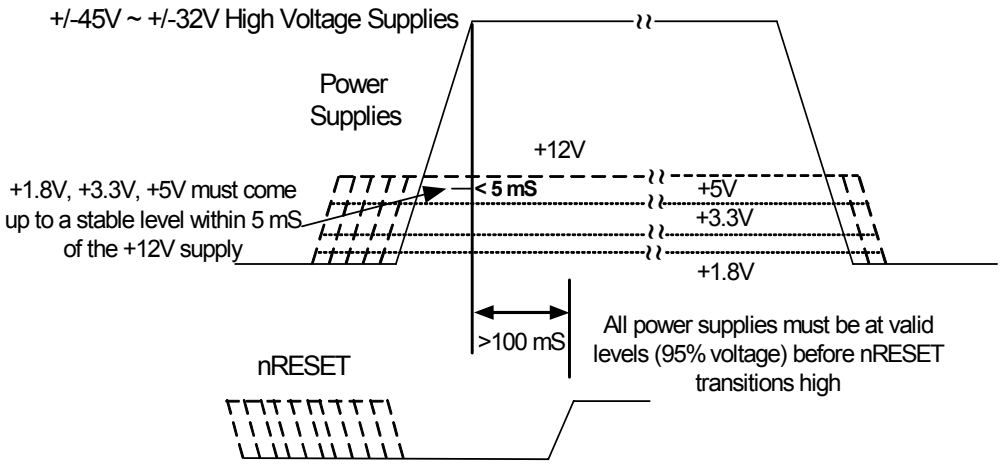


FIGURE 11: Power Supply Sequencing

When powering down the VR100-7, nRESET must be asserted active-low prior to transitioning the power supplies. The +12V, +5V, +3.3V, and +1.8V supplies must not drop below their respective minimum values until the +/-45V ~ +/-32V supply falls below +12V. The +1.8V line should drop at the same time (or later) than the +3.3V line.

Recommended Power-Down Sequencing Flows

Step 1:	Step 2:	Step 3:	Step 4:
Transition **nRESET** to Low	Power down **+/-45V or +/-39V or +/-32V**	Power down **3.3V**, **5V**, and **12V**	Power down **1.8V**

-OR-

Step 1:	Step 2:	Step 3:	Step 4:
Transition **nRESET** to Low	Power down **+/-45V or +/-39V or +/-32V**	Power down **5V**, and **12V**	Power down **3.3V** and **1.8V**

FIGURE 12: Power-Down Sequencing Flow Diagram

It is acceptable to use voltage regulators to derive the +12V, +5V, +3.3V, and +1.8V supplies from the +48V supply if only a single +48V supply is available in the system. In the case where multiple supplies are used to power the VR100-7, the +1.8V MUST NOT be derived from the +3.3V supply (see Figure 13) due to the requirement that the +1.8V supply must come up to a stable level before (or at the same time) as the +3.3V supply does. However, it is acceptable to have both the +1.8V and the +3.3V derived from a +5V rail (see Figure 14). Furthermore, the +12V, +5V, +3.3V, and +1.8V supplies must not drop below minimum specified operating values at any time if the +/-45V or +/-39V or +/-32V supply exceeds 12V.

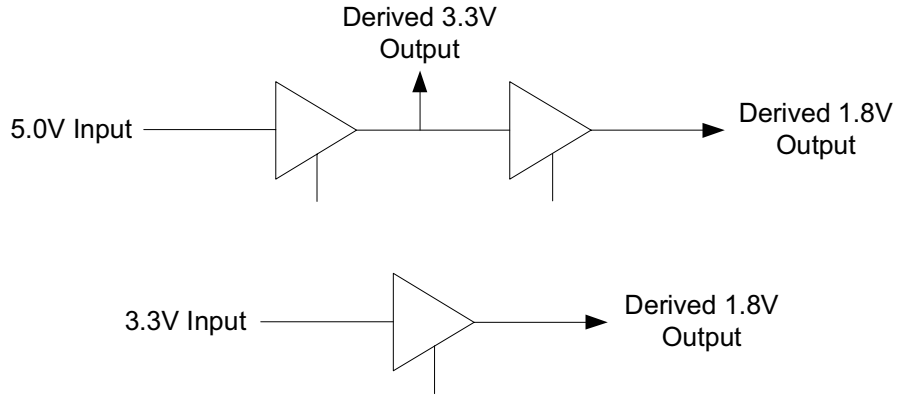


FIGURE 13: Prohibited Regulator Configurations

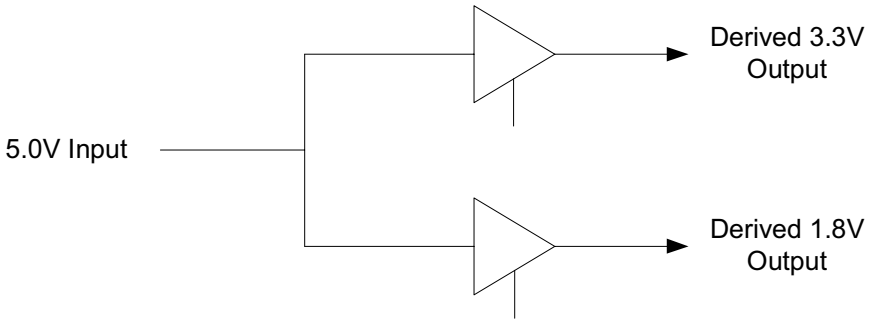


FIGURE 14: Recommended Regulator Configuration

3.2 ADJUSTING CONTROL SETTINGS

All control settings for the amplifier are adjusted by writing to configuration registers through the VR100-7 control interface (see Section 4, "Digital Audio Interface," on page 28). While changing input source settings, the amplifier should be muted to avoid pops. For all other settings, the amplifier will automatically provide a smooth transition between changes in order to avoid pops.

3.3 OPERATIONAL LIMITATIONS

Do not operate the VR100-7 with signals with frequency content higher than 20kHz under no-load conditions. Peaking in the output filter can cause the output voltages to exceed the filter capacitor voltage rating. Avoid test tones above 20kHz.

3.4 AMPLIFIER PROTECTION

The amplifier monitors output current in each loudspeaker channel and the heat sink temperature. The current sensors protect the loudspeaker channels from over-current and short-circuit faults. The temperature sensor protects the amplifier from excessive operating temperature. Configuration and register settings are not altered by amplifier protection actions.

3.4.1 SHORT-CIRCUIT/OVER-CURRENT PROTECTION

If a short-circuit or over-current event is detected, the affected loudspeaker output channel will be disabled, and the VR100-7 will drive the nERROR output to active low. Recovery from a short-circuit or over-current shutdown is automatic.

Automatic Short Circuit Protection – Prevents amplifier damage against shorts between the amplifier loudspeaker output terminals and shorts to system ground. Short-circuit protection acts on a per output basis, and is reference design dependent (see Table 5 on page 11). If a loudspeaker channel experiences a short-circuit, then only that channel is disabled, while the other channels are unaffected. If a short-circuit is detected after the 10th attempt to recover, then the channel that caused the short is permanently

disabled, and will not produce output until the VR100-7 power is cycled. The nERROR signal stays active while the channel is disabled.

Automatic Current Limit Protection – Limits the maximum output current that is available for each loudspeaker output channel. The over-current protection will soft current limit to a reference design power level-dependant maximum.

For example, in Figure 15 below, a short-circuit resulting in an over-current is detected, which triggers an immediate disabling of the shorted loudspeaker channel and assertion of nERROR. After 5 seconds, the channel is reactivated, and nERROR is deasserted. Then another short-circuit/over-current is detected, resulting in another shutdown and assertion of nERROR. If the amplifier resumes normal operation, the shutdown sequence stops. However, if the short-circuit/over-current event continues, the output channel will permanently shutdown after the 11th event. If a permanent shutdown occurs, the amplifier digital amplifier reference design must be power-cycled to re-enable the affected channel.

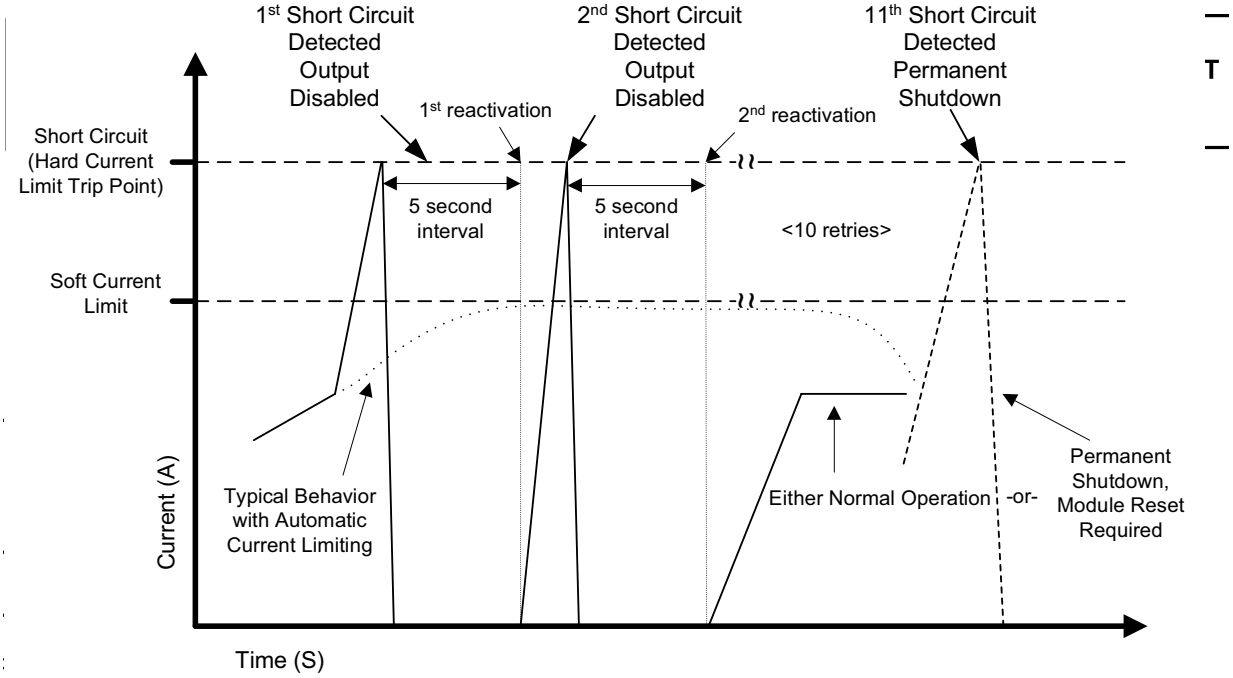


FIGURE 15: Automatic Current Protection Example

3.4.2 OVER-TEMPERATURE PROTECTION

A temperature sensor monitors the amplifier's temperature. As the internal temperature begins to reach critical levels, the controller will begin to limit the output power. If the temperature exceeds the critical level, the amplifier will shut down all output channels and the nERROR output will be driven active low indicating an over-temperature fault. Recovery from an over-temperature shut down is automatic and includes an amount of hysteresis to allow for proper cooling before reactivation. See Section 7.6, "Ambient Operating Conditions," on page 53 for normal operating temperature ranges.

4 DIGITAL AUDIO INTERFACE

The VR100-7 has one digital SAI port for each pair of channels.

4.1 SERIAL AUDIO INPUTS (SAI PORTS)

The VR100-7 contains one SAI port for each pair of channels. Each input can support an individually selectable sample rate from 32kHz to 192kHz. All digital audio inputs are 3.3V CMOS logic. The SAI port is designed to interface with standard digital audio components and to accept I^2S or Left-Justified data formats.

For I^2S format, the left channel data is read when LRCK is low. For the Left-Justified format, the left channel data is read when LRCK is high. Either format requires data to be valid on the rising edge of SCLK and sent MSB-first on SDIN with 32 bits of data per channel. Each set of digital inputs runs asynchronously to the others and may accept different sample rates and formats.

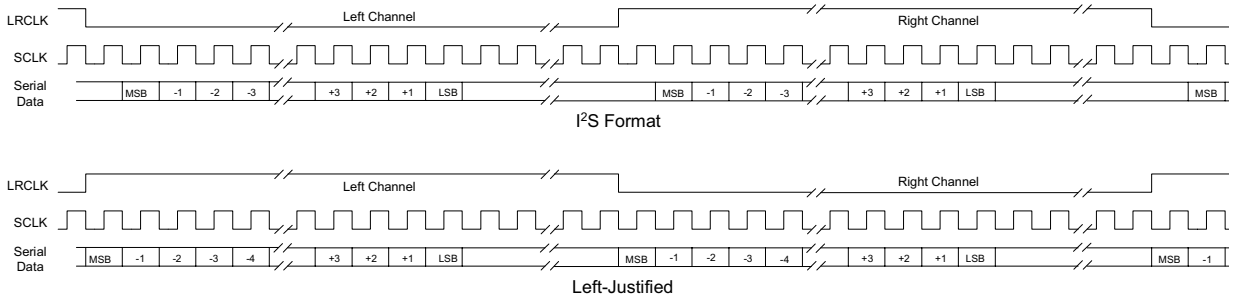


FIGURE 16: SAI port Data Formats

5 CONTROL INTERFACE (CI) SPECIFICATION

The two DAE-2 controllers inside the VR100-7 reference design provide a number of registers that are used to control its behavior. The Control Interface (previously referred to as the MCI, or Module Control Interface in D2Audio's module-based solution Datasheets) is used to set and query these registers through the SDA and SCL pins. This protocol defines any device that sends data on to the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. For this interface, the definition of the master is an external microcontroller or control logic. All digital amplifier reference designs in the system are logically slaves to the external microcontroller. The master always starts the transfer and provides the serial clock for synchronization. The DAE-2 controllers only functions as a slave device in all of its communications and will not function with multiple masters.

5.1 DIGITAL AMPLIFIER REFERENCE DESIGN CONTROL INTERFACE STATES

5.1.1 DATA TRANSITION OR CHANGE

During a data transfer, changes on the SDAx line must only occur while SCLx is in the low state. An SDAx transition while SCLx is high is used to identify a START or STOP condition.

5.1.2 START CONDITION

START is identified by a high to low transition of SDAx while SCLx is stable in the high state. A START condition must precede any command for data transfer.

5.1.3 STOP CONDITION

STOP is identified by low to high transition of SDAx while SCLx is stable in the high state. A STOP condition terminates communication between the VR100-7 and the bus master.

5.1.4 DATA INPUT

During data input, the VR100-7 samples the SDAx signal on the rising edge of SCLx. For correct device operation the SDAx signal must be stable during the rising edge of SCLx and SDAx can change only when SCLx is low.

5.1.5 ACKNOWLEDGE

All data transfers across the control interface bus must be acknowledged. Each byte transfer is followed by an acknowledge bit (ACK). When data is being written to the VR100-7, it will generate the ACK; when being read, the bus master generates the ACK. ACK refers to a true-acknowledge and NACK refers to a not-acknowledge. In general, ACK means continue or ready and NACK means terminate or not ready. The bus master is responsible for correctly interpreting the acknowledge response.

5.2 DEVICE ADDRESS CHANNEL GROUPINGS

To start communication between the master and the VR100-7, the master must initiate with a start condition. Following this, the master sends onto the SDA line 8-bits (MSB first) corresponding to the device select address and read or write mode. If the device address matches that of the DAE-2 controller, the DAE-2 controller will acknowledge the address during the 9th bit time. The 7 most significant bits are the device address identifiers. The 8th bit (LSB) identifies read or write operation R/W. This bit is set to 1 in read mode and 0 for write mode.

Two hardware device addresses are used to identify each of the two DAE-2 controllers are located in the VR100-7 design. Each DAE-2 controller is capable of handling 4 channels of audio each.

Left, Right, Left Surround, Right Surround Channels for the VR100-7 Control Device Address (DAE-2 Controller, D2-914xx-LR #1)	Surround Back Left, Surround Back Right, Center, Subwoofer for the VR100-7 Control Device Address (DAE-2 Controller, D2-914xx-LR #2)
C2h	C4h

Table 20: DAE-2 Device Address Channel Groupings

5.3 DAE-2 CONTROLLER I/O PROCEDURES

5.3.1 DAE-2 CONTROLLER WRITE PROCEDURE

All writes to the DAE-2 controller registers must begin with the Start Condition, followed by the Device Address byte (with read/write bit cleared), three Register Address bytes, three Data bytes and a Stop Condition (see Figure 17). The DAE-2 controller acknowledges each byte by pulling SDA low on the bit immediately following each byte. These bytes are described below:

Byte	Read/Write	Name	Description
0	W	Device Address + Read/Write Bit	Device Address of channel group, with R/W bit cleared
1	W	Register Address [23:16]	Upper 8 bits of register address
2	W	Register Address [15:8]	Middle 8 bits of register address
3	W	Register Address [7:0]	Lower 8 bits of register address
4	W	Data[23:16]	Upper 8 bits of register data to write
5	W	Data[15:8]	Middle 8 bits of register data to write
6	W	Data[7:0]	Lower 8 bits of register data to write

Table 21: DAE-2 Controller Write Byte Sequence Description

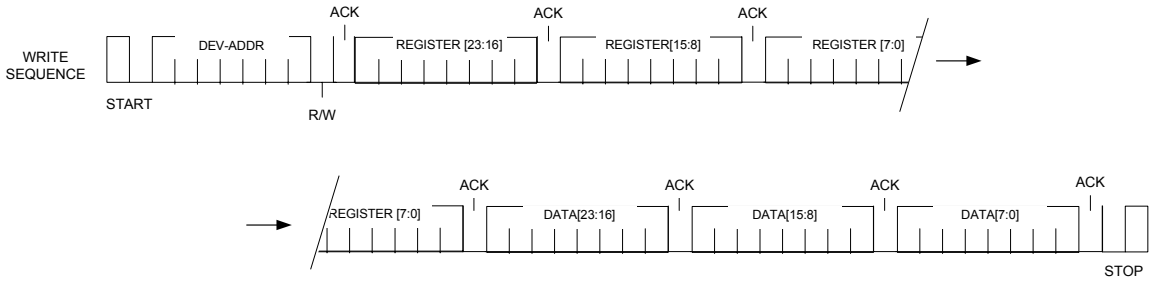


FIGURE 17: DAE-2 Controller Write Sequence Diagram

5.3.2 DAE-2 CONTROLLER READ PROCEDURE

All reads from the DAE-2 controller registers require two steps. During the first step, the master must send the Start Condition, followed by the Device Address byte (with read/write bit low), and three Register Address bytes (see Figure 18). The DAE-2 controller acknowledges each byte in the first step by pulling SDA low on the bit immediately following each byte.

Immediately following the first step, the master must send another Start Condition, followed by the Device Address byte (with read/write bit high). The DAE-2 controller will acknowledge the Device Address byte by pulling SDA low on the bit immediately following the Device Address. The next 3 bytes are sent by the DAE-2 controller to the master, and contain the three Data bytes to be read. The master must acknowledge the first two Data bytes by pulling SDA low on the bit immediately following the Device

Address. After the third Data byte, the master should not send an acknowledgement to the digital amplifier reference design. At the end of the second step, the master must send the Stop Condition.

Step	Byte	Master Read/Write	Name	Description
1	0	W	First Device Address + Read/Write Bit	Device Address of channel group, with R/W bit low
	1	W	Register Address [23:16]	Upper 8 bits of register address
	2	W	Register Address [15:8]	Middle 8 bits of register address
	3	W	Register Address [7:0]	Lower 8 bits of register address
2	Repeat Start Condition			
	4	W	Second Device Address + Read/Write Bit	Device Address of channel group, with R/W bit set
	5	R	Data[23:16]	Upper 8 bits of register data to read
	6	R	Data[15:8]	Middle 8 bits of register data to read
	7	R	Data[7:0]	Lower 8 bits of register data to read

Table 22: DAE-2 Controller Read Byte Sequence Description

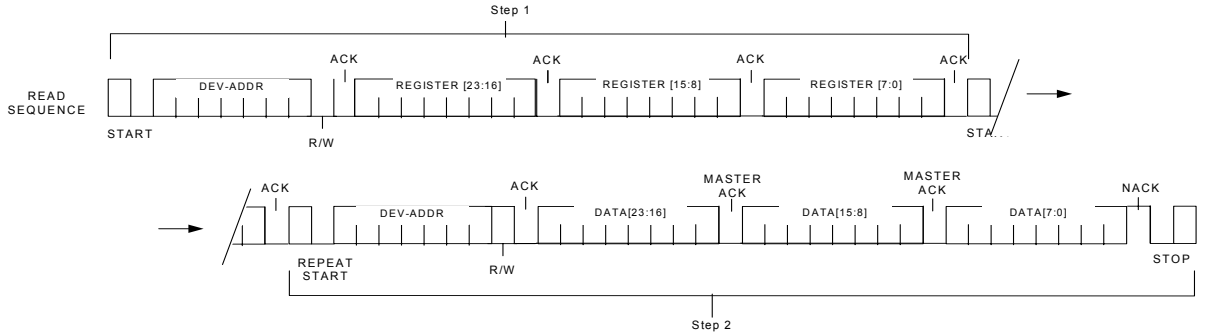


FIGURE 18: DAE-2 Controller Read Sequence Diagram

5.4 STORE TO I2C EEPROM COMMAND

The I2C EEPROM in the VR100-7 design stores the default values of each register for recall on reset or power up. Note that the all default values, from input selection to master volume control levels, are determined by the settings stored in the EEPROM. The amplifier has the capability to update the EEPROM contents at any time from a command from the system microcontroller.

The following control interface command will cause all of the current software settings to become the default settings by storing them into the I2C EEPROM. This command will update the I2C EEPROM values for a group of channels identified by the Device Address. In order to update the I2C EEPROM for all channels within a digital amplifier reference design, the command must be issued twice- once for each Device Address within the digital amplifier reference design.

Byte	Read/Write	Name	Description
0	W	Device Address + Read/Write Bit	Device Address of channel group, with R/W bit cleared
1	W	Register Address [23:16]	Set to 0x80 for EEPROM write
2	W	Register Address [15:8]	Set to 0x00 for EEPROM write
3	W	Register Address [7:0]	Set to 0x00 for EEPROM write
4	W	Data[23:16]	Set to 0x00 for EEPROM write
5	W	Data[15:8]	Set to 0x00 for EEPROM write
6	W	Data[7:0]	Set to 0x00 for EEPROM write

Table 23: Store to I2C EEPROM Command Byte Description

CONSUMER

PRELIMINARY

6 SOFTWARE CONTROL SETTINGS

All control settings for the amplifier are adjusted by writing to configuration registers through the Control Interface (see Section 6, "Software Control Settings," on page 32). While changing input source settings, the amplifier should be muted to avoid pops. For all other settings, the amplifier will automatically provide a smooth transition between changes in order to avoid pops.

6.1 DSP PROCESSING ORGANIZATION

The VR100-7 digital amplifier reference design controller contains a powerful DSP engine which provides a group of processing blocks, including Input Select, Tone Control, 5-band Parametric EQ, Crossover, Master Volume Control, Compression, and Level Control (Channel Attenuation). Master Volume control is available for each controller and its corresponding 2 audio input pairs. Figure 19 illustrates the DSP functions of the VR100-7 firmware intended for AVR system designs.

PRELIMINARY

AVR Design Firmware

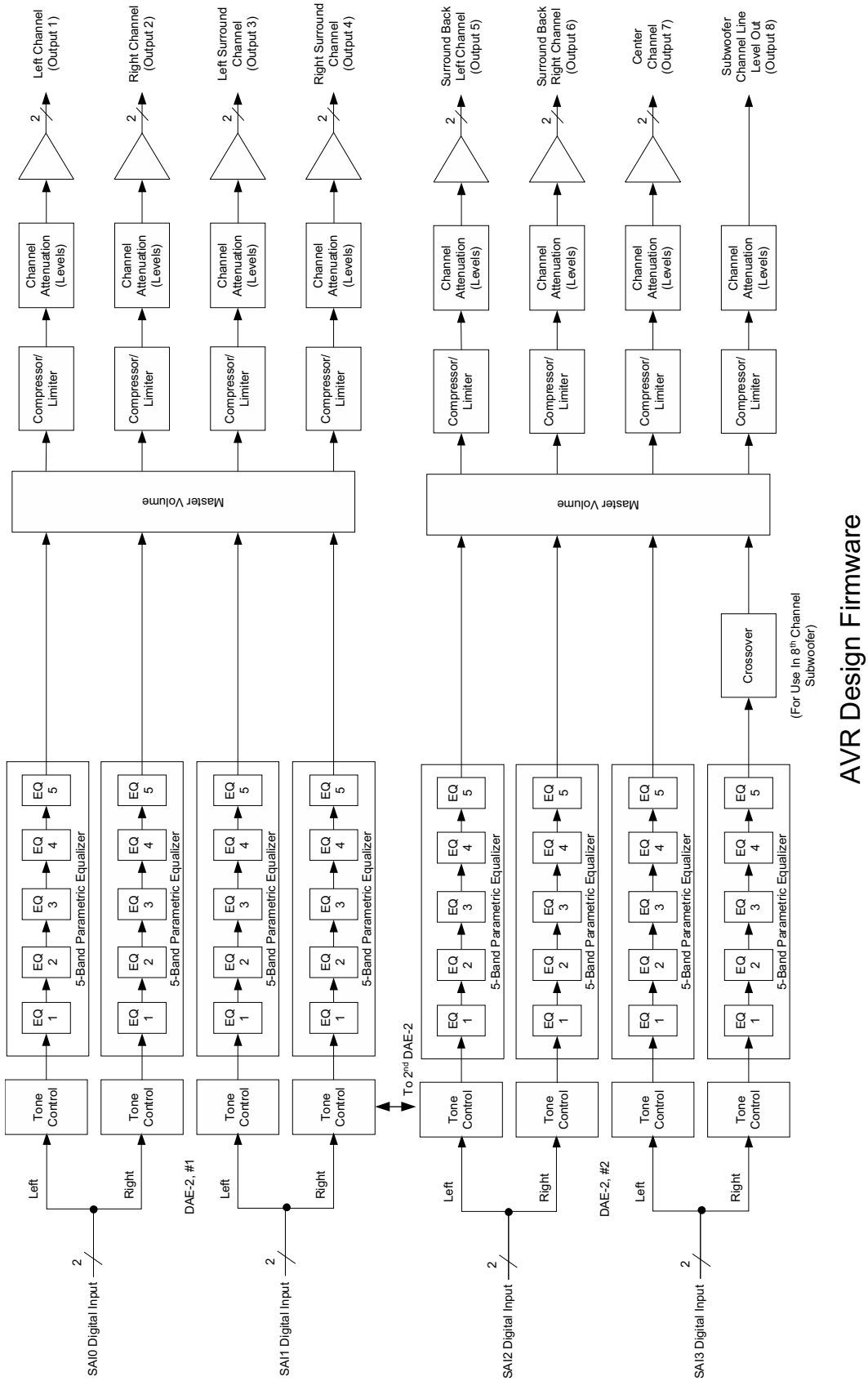


FIGURE 19: DSP Processing Blocks - AVR Configuration

6.2 GAIN MANAGEMENT

Careful attention must be paid to the signal level at the input and at each stage through the DSP in order to prevent clipping. Changes to DSP parameters must be made only after thorough consideration of the effects on signal level throughout the entire signal path from input to output. **Though reducing the gain of the input signal will result in additional DSP headroom, this action will cause a corresponding reduction in the signal-to-noise ratio of the amplifier.**

6.2.1 DSP GAIN STRUCTURE

At the input to the DSP, an attenuation of -6dB is applied to allow for headroom within the DSP processing blocks. At the DSP output, +18dB of gain is applied prior to driving the PWM amplifier outputs. This organization is shown in the following figure:

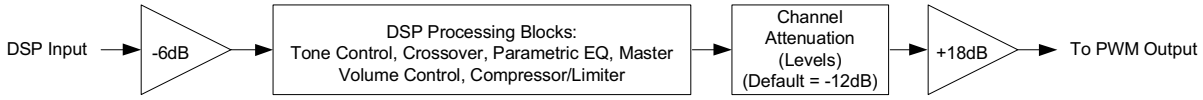


FIGURE 20: DSP Gain Stages

Once a signal is input, 6dB of headroom is provided for all of the DSP processing blocks and volume controls. Clipping will occur if any of the DSP processing blocks cause the signal level to exceed 0dBFS. At the DSP processing final stage, a maximum of 18dB of gain is added prior to the PWM amplifier outputs. The digital amplifier reference design is designed to output full power (assuming the high-voltage supply is at the correct voltage) with a -0.5dBFS input signal, all other DSP processing functions and individual channel volume controls at unity gain, and the output master volume control set to +6dB.

6.2.2 GAIN CALCULATIONS

Proper gain management begins with determining the maximum digital amplifier reference design input level that is expected for the system design. When the I^2S inputs are used, the maximum level can be as high as 0dBFS if connected directly to source material.

6.3 SOFTWARE REGISTER ADDRESSING

Changes to each of the DSP Processing Blocks are made by writing to a software register set within the digital amplifier reference design. Each software register is accessed using a digital amplifier reference design control device address and an internal register address. The internal register addresses are repeated for each group of four channels. The digital amplifier reference design control device address is used to identify the appropriate set of four.

Register locations are defined as a Control Device Address, as defined in Table 20, followed by a 24-bit register location. The Register Address Table syntax lists the register location as $AA:xxxxxx, where AA is the Control Device Address followed by the "xxxxxx"register offset. An example of muting all channels in the amplifier would be a write to $C2:000000 and a write to $C4:000000 to mute all 8 master channels.

6.4 INPUT SOURCE CONFIGURATION

All channels have digital SAI ports as the primary inputs. The optional Zone 2 and Zone 3 inputs are also available for Left Surround and Right Surround, and the Surround Back Left and Surround Back Right. At any time, the Input Selection may be changed in software through the following registers. The amplifier outputs must be muted during changes to the Input Select Register to avoid pops.

There is one Input Select Register for each input pair. Table 24 defines the input mapping to Digital Amplifier Reference Design Control Device Addresses. The following table summarizes the Input Select Register addresses.

Register Name	Left, Right, Left Surround, Right Surround, Zone 3	Surround Back Left, Surround Back Right, Center, Subwoofer, Zone 2
Input Select	C2:020001h	C4:020001h

Table 24: Input Select Register Address Table

The functions of the bits in each Input Select Register are as follows:

Input/Output Select Bits	[23:8]	[7:5]	4	3	2	1	0
Value	Reserved Always set to F800h	Reserved Always set to 0	JUSTIFY	Reserved Always set to 0	Reserved Always set to 0	Reserved Always set to 0	SPDIFEN

Table 25: Input/Output Select Register Bit Definitions

Bits [23:8] **RESERVED**

These bits should always be set to F800h when writing to the Input Select Register.

Bits [7:0] **RESERVED**

These bits should always be set to '0' when writing to the Input Select Register.

Bit 4 **JUSTIFY**

When a '1' is written to JUSTIFY, both SAI ports will accept digital audio data in Left-Justified format. Additionally, both SAO ports will transmit digital audio data in Left-Justified format. When a '0' is written to JUSTIFY, both SAI ports will accept digital audio data in I^2S format. Additionally, both SAO ports will transmit digital audio data in I^2S format. The default value for JUSTIFY is 0.

Bit 3 **RESERVED**

This bit should always be set to '1' when writing to InputSelectReg.

Bit 2 **RESERVED**

This bit should always be set to a '0' when writing to InputSelectReg.

Bit 1 **RESERVED**

This bit should always be set to a '0' when writing to InputSelectReg.

Bit 0 **SPDIFEN**

When SPDIFEN is set to a '1', the SPDIF input is selected for the pair of channels corresponding to the module control device address. For example, if SPDIFEN is set on the second device, the Sbl and Sbr I2S/LJ input data channels will be replaced with input data from the SPDIFRX_1.

Note: The audio sources selected via software through the Input Select Registers are not stored in EEPROM. The input source is determined by a set of hardware pins at power up or digital amplifier reference design reset. Changes made through a software command will be lost on power off or system reset.

6.5 TONE CONTROL

The DAE-2 ICs provide individual software-controlled Tone Controls for each channel. These are implemented as low-pass and high-pass shelving filters for bass and treble control, respectively, which are added back into the signal flow. Each filter contains a first-order (6dB/octave) rolloff, with programmable corner frequency and gain. The DAE-2 ICs will automatically provide a smooth transition between changes to the Tone Control.

6.5.1 CORNER FREQUENCY CALCULATION

The Corner Frequency of the Tone Control is defined as the frequency at which the gain of the filter is +-3dB. For a given Corner Frequency, the appropriate parameter is a signed, 24-bit number calculated using the following equations. First, determine the intermediate value Θ, then use Θ to calculate the frequency corner parameter value (note that Θ is in radians). Valid range for Corner Frequency is 20Hz to 24,000Hz.

$$\Theta(radians) = Frequency \times 9.817477 \times 10^{-5}$$

$$ToneControlCornerFrequencyParameter = 2^{23} \times \left(\frac{\sin(\Theta) - 1}{\cos(\Theta)}\right)$$

6.5.2 GAIN CALCULATION

For a given Gain in dB, the appropriate parameter is a signed, 24-bit number calculated using the following equation. Valid range for Tone Control Gain is -10dB to +9.542dB.

$$ToneControlGainParameter = 2^{23} \times \left[\frac{10^{\left(\frac{Gain}{20}\right)} - 1}{4}\right]$$

6.5.3 TONE REGISTER SUMMARY

Register Name	Minimum Value	Maximum Value	Description
BassToneControlCorner FrequencyParameter	804047h	3504F3h	Per-channel corner frequency parameter for bass tone control shelving filter.
BassToneControlGain Parameter	C0002Ah	7FFFFFh	Per-channel gain for bass tone control shelving filter
TrebleToneControlCornerFrequencyParameter	804047h	3504F3h	Per-channel corner frequency parameter for treble tone control shelving filter.
TrebleToneControlGain Parameter	C0002Ah	7FFFFFh	Per-channel gain for treble tone control shelving filter

Table 26: Tone Control Register Summary

6.5.4 TONE REGISTER ADDRESS TABLE

Register Name	Surround Left Register Address	Surround Right Register Address	Left Register Address	Right Register Address
BassToneControlCorner FrequencyParameter	C2:000015h	C2:000019h	C2:00001Dh	C2:000021h
BassToneControlGain Parameter	C2:000016h	C2:00001Ah	C2:00001Eh	C2:000022h
TrebleToneControlCorner FrequencyParameter	C2:000017h	C2:00001Bh	C2:00001Fh	C2:000023h
TrebleToneControlGain Parameter	C2:000018h	C2:00001Ch	C2:000020h	C2:000024h

Table 27: Tone Control Register Address Table

Register Name	Rear Surround Left Register Address	Rear Surround Right Register Address	Center Register Address	Subwoofer Register Address
BassToneControlCorner FrequencyParameter	C4:000015h	C4:000019h	C4:00001Dh	C4:000021h
BassToneControlGain Parameter	C4:000016h	C4:00001Ah	C4:00001Eh	C4:000022h
TrebleToneControlCorner FrequencyParameter	C4:000017h	C4:00001Bh	C4:00001Fh	C4:000023h
TrebleToneControlGain Parameter	C4:000018h	C4:00001Ch	C4:000020h	C4:000024h

Table 28: Tone Control Register Address Table

6.6 PARAMETRIC EQUALIZER

There is a 5-band equalizer available on each channel. Each band contains adjustable Frequency, Gain and Q. Setting the Gain to 0 disables a band. The DSP within the digital amplifier reference design will automatically provide a smooth transition between changes to the Parametric EQ.

6.6.1 EQ CENTER FREQUENCY CALCULATION

For a given center frequency, the appropriate parameter is a signed, 24-bit number calculated using the following equation. Valid range for center frequency is 20Hz to 24,000Hz.

$$EQCenterFrequencyParameter = 2^{23} \times Frequency \times 31.25 \times 10^{-6}$$

6.6.2 EQ QUALITY FACTOR CALCULATION

For a given Q, the appropriate parameter is a signed, 24-bit number calculated using the following equation.
Valid range for Q is 0.5 < Q <= 10. (Note that a value of 0.5 for Q results in an EQQParameter value of 800000h, which is invalid)

$$EQQParameter = 2^{23} \times \left(\frac{1}{2 \times Q}\right)$$

6.6.3 EQ GAIN CALCULATION

For a given Gain in dB, the appropriate parameter is a signed, 24-bit number calculated using the following equation. Valid range for gain is -60dB to +6dB.

$$EQGainParameter = -2^{23} \times \left[1 - 10^{\left(\frac{Gain}{20}\right)}\right]$$

6.6.4 EQ REGISTER SUMMARY

Register Name	Minimum Value	Maximum Value	Description
EQCenterFrequency Parameter	00147Ah	600000h	Center frequency for Parametric EQ, 8 bands per channel
EQQParameter	066666h	7FFFFFh	Quality factor for Parametric EQ, 8 bands per channel
EQGainParameter	8020C5h	7F64C1h	Gain for Parametric EQ, 8 bands per channel

Table 29: Parametric EQ Register Summary

6.6.5 5-BAND EQ REGISTER ADDRESS TABLE

Register Name	Surround Left Register Address	Surround Right Register Address	Left Register Address	Right Register Address
EQCenterFrequency Parameter, band 1	C2:000025h	C2:000034h	C2:000043h	C2:000052h
EQQParameter, band 1	C2:000026h	C2:000035h	C2:000044h	C2:000053h
EQGainParameter, band 1	C2:000027h	C2:000036h	C2:000045h	C2:000054h
EQCenterFrequency Parameter, band 2	C2:000028h	C2:000037h	C2:000046h	C2:000055h
EQQParameter, band 2	C2:000029h	C2:000038h	C2:000047h	C2:000056h
EQGainParameter, band 2	C2:00002Ah	C2:000039h	C2:000048h	C2:000057h
EQCenterFrequency Parameter, band 3	C2:00002Bh	C2:00003Ah	C2:000049h	C2:000058h
EQQParameter, band 3	C2:00002Ch	C2:00003Bh	C2:00004Ah	C2:000059h
EQGainParameter, band 3	C2:00002Dh	C2:00003Ch	C2:00004Bh	C2:00005Ah
EQCenterFrequency Parameter, band 4	C2:00002Eh	C2:00003Dh	C2:00004Ch	C2:00005Bh
EQQParameter, band 4	C2:00002Fh	C2:00003Eh	C2:00004Dh	C2:00005Ch
EQGainParameter, band 4	C2:000030h	C2:00003Fh	C2:00004Eh	C2:00005Dh
EQCenterFrequency Parameter, band 5	C2:000031h	C2:000040h	C2:00004Fh	C2:00005Eh
EQQParameter, band 5	C2:000032h	C2:000041h	C2:000050h	C2:00005Fh
EQGainParameter, band 5	C2:000033h	C2:000042h	C2:000051h	C2:000060h

Table 30: 5-Band EQ Register Address Table

Register Name	Rear Surround Left Register Address	Rear Surround Right Register Address	Center Register Address	Subwoofer Register Address
EQCenterFrequency Parameter, band 1	C4:000025h	C4:000034h	C4:000043h	C4:000052h
EQQParameter, band 1	C4:000026h	C4:000035h	C4:000044h	C4:000053h
EQGainParameter, band 1	C4:000027h	C4:000036h	C4:000045h	C4:000054h
EQCenterFrequency Parameter, band 2	C4:000028h	C4:000037h	C4:000046h	C4:000055h
EQQParameter, band 2	C4:000029h	C4:000038h	C4:000047h	C4:000056h
EQGainParameter, band 2	C4:00002Ah	C4:000039h	C4:000048h	C4:000057h
EQCenterFrequency Parameter, band 3	C4:00002Bh	C4:00003Ah	C4:000049h	C4:000058h
EQQParameter, band 3	C4:00002Ch	C4:00003Bh	C4:00004Ah	C4:000059h
EQGainParameter, band 3	C4:00002Dh	C4:00003Ch	C4:00004Bh	C4:00005Ah
EQCenterFrequency Parameter, band 4	C4:00002Eh	C4:00003Dh	C4:00004Ch	C4:00005Bh
EQQParameter, band 4	C4:00002Fh	C4:00003Eh	C4:00004Dh	C4:00005Ch
EQGainParameter, band 4	C4:000030h	C4:00003Fh	C4:00004Eh	C4:00005Dh
EQCenterFrequency Parameter, band 5	C4:000031h	C4:000040h	C4:00004Fh	C4:00005Eh
EQQParameter, band 5	C4:000032h	C4:000041h	C4:000050h	C4:00005Fh
EQGainParameter, band 5	C4:000033h	C4:000042h	C4:000051h	C4:000060h

Table 31: 5-Band EQ Register Address Table

6.7 SUBWOOFER LOW-PASS FILTER

2 cascaded, 2nd-order filter blocks are available for the Subwoofer channel. Different order slopes can therefore be achieved.

6.7.1 CORNER FREQUENCY CALCULATION

For a given Corner Frequency, the appropriate parameter is a signed, 24-bit number calculated using the following equation. Valid range for the filter Corner Frequency is 20Hz to 24,000Hz.

$$FilterCornerFrequencyParameter = 2^{23} \times Frequency \times 31.25 \times 10^{-6}$$

6.7.2 FILTER QUALITY FACTOR CALCULATION

For a given filter Q, the appropriate parameter is a signed, 24-bit number calculated using the following equation.
Valid range for filter Q is 0.5 < Q <= 10. (Note that a value of 0.5 for Q results in an FilterQParameter value of 800000h, which is invalid)

$$FilterQParameter = 2^{23} \times \left[\frac{1}{(2 \times Q)}\right]$$

6.7.3 SUBWOOFER LOW-PASS FILTER REGISTER SUMMARY

Register Name	Minimum Value	Maximum Value	Description
FilterMode	-	-	Filter mode for each block 000000h = Lowpass, 12dB/octave slope 000001h = Lowpass, 6dB/octave slope 8XXXXXh = Bypass
FilterCornerFrequency Parameter	00147Ah	600000h	Corner frequency for each block
FilterQParameter	066666h	7FFFFFh	Quality factor for each block

Table 32: Subwoofer Low-Pass Filter Register Summary

6.7.4 SUBWOOFER LOW-PASS FILTER REGISTER TABLE

Register Name	Subwoofer Channel Register Address
FilterMode, Block 1	C2:000117h
FilterCornerFrequency Parameter, Block 1	C2:000118h
FilterQParameter, Block 1	C2:000119h
FilterMode, Block 2	C2:00011Ah
FilterCornerFrequency Parameter, Block 2	C2:00011Bh
FilterQParameter, Block 2	C2:00011Ch

Table 33: Subwoofer Low-Pass Filter Register Address Table

6.8 COMPRESSOR

CONSUMER

The VR100-7 digital amplifier reference design provides individual software-controlled Compressors for each channel. Each Compressor has configurable Compression Ratio, Threshold, Attack and Release Time, as well as Makeup Gain. The DSP within the digital amplifier reference design will automatically provide a smooth transition between changes are written to the Compressor settings.

6.8.1 THRESHOLD CALCULATION

The Compressor reduces the gain of signals which exceed a given threshold. For a given Threshold in dB, the appropriate parameter is a signed, 24-bit number calculated using the following equation. Valid range for Threshold is -90dB to 0dB.

$$CompressorThresholdParameter = 2^{23} \times [(0.010381025 \times Threshold) + 0.96875]$$

6.8.2 ATTACK TIME CALCULATION

The Attack Time is the rate at which the gain is reduced when the input exceeds the Threshold. For a given Attack Time in milliseconds, the appropriate parameter is a signed, 24-bit number. Valid range for attack time is 1 mS to 100 mS. Below is a table of values for Attack Time. Other values can be calculated by linearly interpolating between these sample values.

Attack Time	CompressorAttackTime Parameter
1 mS	1C2F43h
10 mS	032900h
100 mS	0051D1h

Table 34: Values for Attack Time

6.8.3 RELEASE TIME CALCULATION

The Release Time is the rate at which the gain is increased when the input falls below the Threshold. For a given Release Time in milliseconds, the appropriate parameter is a signed, 24-bit number. Valid range for Release Time is 1 mS to 100 mS. Below is a table of values for Release Time. Other values can be calculated by linearly interpolating between these sample values.

Release Time	CompressorReleaseTime Parameter
1 mS	1C2F43h
10 mS	032900h
100 mS	0051D1h

Table 35: Values for Release Time

6.8.4 COMPRESSOR RATIO CALCULATION

The Compressor Ratio is the number of dB above the Threshold that the input level must increase in order to increase the output level by 1dB. For a given Compressor Ratio in dB, the appropriate parameter is a signed, 24-bit number calculated using the following equation. Valid range for Compressor Ratio is 1 to 100. Note that a ratio of 1 disables the compressor, while a ratio of above 10 causes the Compressor to behave as a Limiter.

$$CompressorRatioParameter = 2^{23} \times \left(1 - \left(\frac{1}{Ratio}\right)\right)$$

6.8.5 MAKEUP GAIN CALCULATION

Depending on the settings for Threshold and Compressor Ratio, additional Makeup Gain may be necessary to reach a full-scale output. For a given Makeup Gain in dB, the appropriate parameter is a signed, 24-bit number calculated using the following equation. Valid range for Makeup Gain is 0dB to +18.06dB.

$$CompressorMakeupGainParameter = 2^{23} \times 10^{[(Gain \times 0.05) - 0.90309]}$$

PRELIMINARY

6.8.6 COMPRESSOR REGISTER SUMMARY

Register Name	Minimum Value	Maximum Value	Description
CompressorThreshold Parameter	04691Ch	7C0000h	Per-channel Compressor threshold
CompressorAttackTime Parameter	0051D1h	1C2F43h	Per-channel Compressor attack time
CompressorReleaseTime Parameter	0051D1h	1C2F43h	Per-channel Compressor release time
CompressorRatioParameter	000000h	7EB851h	Per-channel Compressor ratio
CompressorMakeupGain Parameter	0FFFFFh	7FFFFFh	Per-channel Compressor makeup gain

Table 36: Compressor Register Summary

6.8.7 COMPRESSOR REGISTER ADDRESS TABLE

Register Name	Surround Left Register Address	Surround Right Register Address	Left Register Address	Right Register Address
CompressorThreshold Parameter	C2:0000C6h	C2:0000CCh	C2:0000BAh	C2:0000C0h
CompressorRatioParameter	C2:0000C7h	C2:0000CDh	C2:0000BBh	C2:0000C1h
CompressorAttackTime Parameter	C2:0000C8h	C2:0000CEh	C2:0000BCh	C2:0000C2h
CompressorReleaseTime Parameter	C2:0000C9h	C2:0000CFh	C2:0000BDh	C2:0000C3h
CompressorMakeupGain Parameter	C2:0000CAh	C2:0000D0h	C2:0000BEh	C2:0000C4h

Table 37: Compressor Register Address Table

Register Name	Rear Surround Left Register Address	Rear Surround Right Register Address	Center Register Address	Subwoofer Register Address
CompressorThreshold Parameter	C4:0000BAh	C4:0000C0h	C4:0000C6h	C4:0000CCh
CompressorRatioParameter	C4:0000BBh	C4:0000C1h	C4:0000C7h	C4:0000CDh
CompressorAttackTime Parameter	C4:0000BCh	C4:0000C2h	C4:0000C8h	C4:0000CEh
CompressorReleaseTime Parameter	C4:0000BDh	C4:0000C3h	C4:0000C9h	C4:0000CFh
CompressorMakeupGain Parameter	C4:0000BEh	C4:0000C4h	C4:0000CAh	C4:0000D0h

Table 38: Compressor Register Address Table

6.9 VOLUME CONTROL

CONSUMER

Software-controlled Master Volume Control is provided, which controls the final gain for all output channels. Individual attenuators are also provided for each channel. The DSP within the digital amplifier reference design will automatically provide a smooth transition between changes to the Volume Control.

6.9.1 MASTER VOLUME CALCULATION

For a given Master Volume in dB, the appropriate parameter is a signed, 24-bit number calculated using the following equation. Valid range for Master Volume is -100dB to +18.06dB.

$$MasterVolumeParameter = 1 - (2^{23}) \times 10^{\left[\frac{[Mainvolume - 18.06]}{20}\right]}$$

6.9.2 CHANNEL ATTENUATION CALCULATION

For a given Channel Attenuation in dB, the appropriate parameter is a signed, 24-bit negative number calculated using the following equation. Valid range for Channel Attenuation is 0dB to 120dB. Note that channel attenuation is positive, such that a value of 0dB results in no attenuation.

$$ChannelAttenuationParameter = -\left[2^{23} \times 10^{\left(\frac{-Attenuation}{20}\right)}\right]$$

The Channel Attenuation Parameter can also be used to invert the polarity of a channel. To do this, remove the negative sign from the formula above and recalculate the ChannelAttenuationParameter:

$$InvertedChannelAttenuationParameter = 2^{23} \times 10^{\left(\frac{-Attenuation}{20}\right)}$$

6.9.3 VOLUME CONTROL REGISTER SUMMARY

Register Name	Minimum Value	Maximum Value	Description
MasterVolumeParameter	FFFFFFh (minimum volume)	800000h (maximum volume)	Master Volume for all channels
ChannelAttenuationParameter	800000h (minimum attenuation)	FFFFFFh (maximum attenuation)	Per-channel attenuation setting
ChannelAttenuationParameter (with polarity inversion)	7FFFFFh (minimum attenuation)	000000h (maximum attenuation)	Per-channel attenuation setting (with polarity inversion)

Table 39: Volume Control Register Summary

PRELIMINARY

6.9.4 VOLUME CONTROL REGISTER ADDRESS TABLE

Register Name	Left Channel Register Address	Right Channel Register Address	Left Surround Channel Register Address	Right Surround Channel Register Address
MasterVolumeParameter	C2:000000h			
ChannelAttenuation Parameter	C2:000001h	C2:000002h	C2:000003h	C2:000004h

Table 40: Volume Control Register Address Table

Register Name	Surround Back Left Channel Register Address	Surround Back Right Channel Register Address	Center Channel Register Address	Subwoofer Channel Register Address
MasterVolumeParameter	C4:000000h			
ChannelAttenuation Parameter	C4:000001h	C4:000002h	C4:000003h	C4:000004h

Table 41: Volume Control Register Address Table

6.10 SOUNDSUITE - LEO (LISTENING ENVIRONMENT OPTIMIZATION)

The SoundSuite LEO (Listening Environment Optimization) feature in VR100-7 adjusts and refines the amplifier's sound, taking into consideration the audience's location in the room and the audio components and speakers to which it is connected. LEO also recognizes and optimizes for acoustic imperfections, such as tonal imbalances and impedance inconsistencies from different speakers, non-ideal speaker placement, and auditory challenges such as glass and tile expanses, hardwood floors, rugs, low or vaulted ceilings, textured walls, even furniture. LEO obtains acoustic feedback via an omnidirectional microphone in the room.

6.10.1 LEO REGISTER AND MEMORY ADDRESS TABLE

The following table summarizes the LEO Control Register and address pointer locations:

Name	Address
LEO Control/Status Register	C2:020011h
Address Pointer	C2:020012h

Table 42: LEO Control Register

The functions of the bits in the LEO Control Register are as follows:

LEO Control Register Bits	5	4	3	2	1	0
Value	LEO Channel Four Enable	LEO Channel Three Enable	LEO Channel Two Enable	LEO Channel One Enable	RESERVED	LEO Main Enable

Table 43: LEO Control Register Bit Definitions [5:0]

LEO Control Register Bits	[23:12]	11	10	9	8	7	6
Value	Reserved Always set to 000h	LEO Correlate	LEO ARMC SPL and Speaker Size Enable	LEO Channel Eight Enable	LEO Channel Seven Enable	LEO Channel Six Enable	LEO Channel Five Enable

Table 44: LEO Control Register Bit Definitions [23:6]

Bits [23:12] **RESERVED**
These bits should always be set to 000h when writing to the LEO Control Register.

Bit 11 **LEO_CORRELATE**
Correlate bit. When set to a "1", this bit enables testing for **Acoustic Speaker Detection**, **Speaker Polarity**, and **Distance Measurement** testing.

Bit 10 **LEO_ARMC_SPL_AND_SPEAKER_SIZE_ENABLE**
ARMC bit. When set to a "1", this bit enables testing for **Automatic Room Mode Correction**, **Speaker Level Normalization**, and **Speaker Size Detection**.

Bit 9 **LEO_CHANNEL_EIGHT_ENABLE**
When set to a "1", this bit enables LEO compensation for the Subwoofer Channel.

Bit 8 **LEO_CHANNEL_SEVEN_ENABLE**
When set to a "1", this bit enables LEO compensation for the Center Channel.

Bit 7 **LEO_CHANNEL_SIX_ENABLE**
When set to a "1", this bit enables LEO compensation for the Surround Back Right Channel.

Bit 6 **LEO_CHANNEL_FIVE_ENABLE**
When set to a "1", this bit enables LEO compensation for the Surround Back Left Channel.

Bit 5 **LEO_CHANNEL_FOUR_ENABLE**
When set to a "1", this bit enables LEO compensation for the Right Surround Channel.

Bit 4 **LEO_CHANNEL_THREE_ENABLE**
When set to a "1", this bit enables LEO compensation for the Left Surround Channel.

Bit 3 **LEO_CHANNEL_TWO_ENABLE**
When set to a "1", this bit enables LEO compensation for the Right Channel.

Bit 2 **LEO_CHANNEL_ONE_ENABLE**
When set to a "1", this bit enables LEO compensation for the Left Channel.

Bit 1 **RESERVED**
The microcontroller should set this bit to a '0'.

Bit 0 **LEO_MAIN_ENABLE**
Main enable bit.

6.10.2 ENABLING LEO

After the microcontroller sets the appropriate channel enable bits (9-2), either of the configuration bits (LEO_CORRELATE, LEO_ARMC_SPL_AND_SPEAKER_SIZE_ENABLE), the main enable is set to a "1". This activates either ARMC or LEO (in addition to Speaker Level Normalization and Speaker Size Detection). Test signals are sent out in succession through all enabled speakers. After the acoustic tests complete, LEO resets LEO_MAIN_ENABLE to a "0". The microcontroller must poll this bit to determine when LEO finishes.

6.10.3 LEO MEMORY LOCATIONS

LEO functions either change equalizer settings (ARMC), or generate a set of results such as speaker distance measurements (LEO_CORRELATE). To operate properly, LEO is provided a microphone calibration curve and a desired response as detailed in Section 6.10.7, "LEO Microphone Response," on page 48, below. These curves and other measurement results are stored in memory arrays specified by an address pointer. The address to these memory arrays are stored at C2:020012h. The value read from this location provides an address which points to the calibration curves, the desired response, and the results generated by the LEO_CORRELATE set of functions. The array offsets are shown below:

LEO Memory Location	Size	Array Offset Mnemonic	Array Offset Address
ARMC/Room EQ Calibration Curve[1]	31	LEO_CALIBRATION_CURVE_OFFSET	00h - 1Eh
Microphone Response Curve[2]	31	LEO_MICROPHONE_CURVE_OFFSET	1Fh - 3Dh
Acoustic Speaker Detection[3]	4	LEO_ ACOUSTIC_SPEAKER_DETECT_OFFSET	3Eh - 41h
Speaker Distance[4]	4	LEO_DISTANCE_OFFSET	42h - 45h
Speaker Polarity[5]	4	LEO_POLARITY_OFFSET	46h - 49h

Table 45: LEO Data and Memory Offset Values

LEO Memory Location	Size	Array Offset Mnemonic	Array Offset Address
Speaker Level Normalization[6]	4	LEO_SPL_OFFSET	4Ah - 4Dh
Speaker Size[7]	4	LEO_SPEAKER_SIZE_OFFSET	4Eh - 51h
Microphone Calibration Lower Limit[8]	1	MCL	52h
LEO Kill Bit[9]	1	LEO_KILL	53h
Note 1: see Section 6.10.6, "LEO ARMC," on page 47 Note 2: see Section 6.10.7, "LEO Microphone Response," on page 48 Note 3: see Section 6.10.8, "LEO Acoustic Speaker Detection," on page 49 Note 4: see Section 6.10.9, "LEO Speaker Distance," on page 50 Note 5: see Section 6.10.10, "LEO Speaker Polarity," on page 50 Note 6: see Section 6.10.11, "LEO SPL Normalization," on page 50 Note 7: see Section 6.10.12, "LEO Speaker Size," on page 51 Note 8: see Section 6.10.13, "LEO Microphone Calibration Lower Limit," on page 51 Note 9: see Section 6.10.14, "LEO_KILL," on page 52			

Table 45: LEO Data and Memory Offset Values (Continued)

6.10.4 TO READ/WRITE A LEO MEMORY LOCATION:

- Read the **address pointer value** stored at C2:020012h
- Determine the **base address** by adding the **DSP address** to the **address pointer value**
- Determine the array address by adding the **base address** to the **array offset address**

Note: Read the address pointer value each time the LEO process executes.

6.10.5 AN EXAMPLE FOR DETERMINING THE SPEAKER SIZE ARRAY ADDRESSES:

Step 1: Read the address pointer value stored at memory location: C2:020012h (this address applies to both DSP's):
For example, assume the pointer value = 001000h

Step 2: Add the DSP address (C2:040000h/C4:040000h) to the pointer value address (001000h):
For example, now the base address = C2:041000h/C4:041000h

Step 3: Add the Speaker Size Array Offset Address (4Eh) from Table 45 to the base addresses obtained in Step 2:
For example, now the array address = C2:04104Eh/C4:04104Eh

The table below show the result addresses for each entry in the Speaker Size array:

Base Address (DSP address + pointer value)	Offset Address	Table Address	Speaker
C2:041000h	4Eh	C2:04104Eh	Left
C2:041000h	4Fh	C2:04104Fh	Right
C2:041000h	50h	C2:041050h	Left Surround
C2:041000h	51h	C2:041051h	Right Surround
C4:041000h	4Eh	C4:04104Eh	Surround Back Left
C4:041000h	4Fh	C4:04104Fh	Surround Back Right
C4:041000h	50h	C4:041050h	Center
C4:041000h	51h	C4:041051h	Subwoofer

Table 46: Array Address Example

6.10.6 LEO ARMC

CONSUMER

When LEO executes acoustic tests, the calibration curve which compensates for the microphone frequency response is stored in an array at offset LEO_CALIBRATION_CURVE_OFFSET in memory. The desired response is also incorporated into this curve. The format of the array is a Q7.16 format - 1 sign bit, 7 integer bits and 16 fractional bits. The equation below shows how to convert a dB value into a microphone response value for storage in the LEO Calibration Curve Array:

$$CalibrationCurveValue = dB \times 2^{16}$$

The table below uses the CalibrationCurveValue equation above to convert -0.25 dB into Q7.16 format, then the result is converted into 24-bit sign extended hexadecimal format for storage in the LEO Calibration Curve array**:**

dB To Convert	2^{16}	Calibration Curve Value	Conversion to hexadecimal (24-bit sign extended)
-0.25	65536	-16384	FFC000h

Table 47: LEO Calibration Curve Conversion Example

See the D2Audio Application Note AN09 for detailed LEO Calibration Curve scaling examples.

PRELIMINARY

The LEO Calibration curve consists of 31 points. Each point corresponds to the frequency points tabulated below:

Base Address (DSP address + pointer value)	Offset Address	Value (Hz)
C2:04xxxxh	00h	15.625
	01h	19.686
	02h	24.803
	03h	31.250
	04h	39.373
	05h	49.606
	06h	62.500
	07h	78.745
	08h	99.213
	09h	125.000
	0Ah	157.490
	0Bh	198.425
	0Ch	250.000
	0Dh	314.980
	0Eh	396.850
	0Fh	500.000
	10h	629.961
	11h	793.701
	12h	1000.000
	13h	1259.921
	14h	1587.401
	15h	2000.000
	16h	2519.842
	17h	3174.802
	18h	4000.000
	19h	5039.684
	1Ah	6349.604
	1Bh	8000.000
	1Ch	10079.368
	1Dh	12699.208
	1Eh	16000.000

Table 48: LEO Calibration Curve Array

6.10.7 LEO MICROPHONE RESPONSE

When LEO executes acoustic tests, the microphone frequency response is stored in an array at offset LEO_MICROPHONE_CURVE_OFFSET in memory. The format of the array is Q7.16 format - 1 sign bit, 7 integer bits and 16 fractional bits. The dB values need to be scaled by (log(10) base 2)/20 before being converted to Q7.16 format. The equation below shows how to convert a dB value into a microphone response value for storage in the LEO Microphone Response Array:

$$MicrophoneResponseCurveValue = dB \times \left[\frac{(\log(10)base2)}{20}\right] \times 2^{16}$$

The table below uses the MicrophoneResponseCurveValue equation above to convert -0.25 dB into Q7.16 format, then the result is converted into 24-bit sign extended hexadecimal format for storage in the LEO Microphone Response array:

CONSUMER

dB To Convert	$\log_2 10/20$	2^{16}	Microphone Response Curve Value	Conversion to hexadecimal (24-bit sign extended)
-0.25	0.166096	65536	-2721	FFF55Fh

Table 49: LEO Microphone Response Curve Conversion Example

PRELIMINARY

See the D2Audio Application Note AN09 for detailed LEO Microphone Response Curve scaling examples.

The LEO Microphone Response curve consists of 31 points.

Base Address (DSP address + pointer value)	Offset Address	Value
C2:04xxxxh	1Fh - 3Dh	LEO_MICROPHONE_CURVE

Table 50: LEO Microphone Response Array

6.10.8 LEO ACOUSTIC SPEAKER DETECTION

The results of the Acoustic Speaker Detect portion of LEO_CORRELATE measurement are stored in an array at offset LEO_ACOUSTIC_SPEAKER_DETECT_OFFSET in memory. This array contains four entries. Each array index is a placeholder for a channel on the addressed DSP. A "1" indicates that a speaker is present, a "0" indicates that no speaker is present at the particular channel.

Base Address (DSP address + pointer value)	Offset Address	Speaker
C2:04xxxxh	3Eh	Left
C2:04xxxxh	3Fh	Right
C2:04xxxxh	40h	Left Surround
C2:04xxxxh	41h	Right Surround
C4:04xxxxh	3Eh	Surround Back Left
C4:04xxxxh	3Fh	Surround Back Right
C4:04xxxxh	40h	Center
C4:04xxxxh	41h	Subwoofer

Table 51: LEO Speaker Detection Array

6.10.9 LEO SPEAKER DISTANCE

The output of the Distance Measurement portion of LEO_CORRELATE is stored in an array at offset LEO_DISTANCE_OFFSET in memory. The array contains four entries. Each array index is a placeholder for a channel on the addressed DSP. The format of the distance is given in terms of the time taken for the microphone to detect a test pulse from the speaker. The actual units of the time used are the time period for the sampling frequency used within the DSP. This is (1/64000) seconds for the D2Audio DSP. For example, "4" would correspond to an actual time of 4 * (1/64000) seconds.

Base Address (DSP address + pointer value)	Offset Address	Speaker
C2:04xxxxh	42h	Left
C2:04xxxxh	43h	Right
C2:04xxxxh	44h	Left Surround
C2:04xxxxh	45h	Right Surround
C4:04xxxxh	42h	Surround Back Left
C4:04xxxxh	43h	Surround Back Right
C4:04xxxxh	44h	Center
C4:04xxxxh	45h	Subwoofer

Table 52: LEO Speaker Distance Array

6.10.10 LEO SPEAKER POLARITY

The output of the Polarity Measurement portion of the LEO_CORRELATE is stored in an array at offset LEO_POLARITY_OFFSET in memory. The array contains four entries. Each array index is a placeholder for a channel on the addressed DSP. If the entry contains a positive value, then the corresponding channel did not reverse polarity. If the entry contains a negative value, then the speaker connections required a polarity reversal. If the entry contains "0", no speaker was detected.

Base Address (DSP address + pointer value)	Offset Address	Speaker
C2:04xxxxh	46h	Left
C2:04xxxxh	47h	Right
C2:04xxxxh	48h	Left Surround
C2:04xxxxh	49h	Right Surround
C4:04xxxxh	46h	Surround Back Left
C4:04xxxxh	47h	Surround Back Right
C4:04xxxxh	48h	Center
C4:04xxxxh	49h	Subwoofer

Table 53: LEO Speaker Polarity Array

6.10.11 LEO SPL NORMALIZATION

The output of the Speaker Level Normalization portion of the LEO_ARMC_SPL_AND_SPEAKER_SIZE_ENABLE test is stored in an array at offset LEO_SPL_OFFSET in memory. The array contains four entries. Each array index is a placeholder for the channel on the addressed DSP. The array entries are recommendations on how many dBs a particular channel deviates from a reference level (Left front speaker). Thus a value of -3 dB for a certain channel would indicate that channel is 3 dB less than the reference level. The array entries are in Q7.16 format - 1 sign bit, 7 integer bits and 16 fractional bits. The dB values need to be scaled by 20/(log(10) base 2) before being converted to Q7.16 format.

The equation below shows how to convert a dB value into a speaker level normalization value for storage in the LEO Speaker Level Normalization Array:

$$SpeakerLevelNormalizationValue = dB \times \left[\frac{20}{(\log(10)base2)}\right] \times 2^{16}$$

The table below uses the SpeakerLevelNormalizationValue equation above to convert -0.25 dB into Q7.16 format, then the result is converted into 24-bit sign extended hexadecimal format for storage in the LEO Speaker Level Normalization array:

dB To Convert	$20/\log_2 10$	2^{16}	Speaker Level Normalization Value	Conversion to hexadecimal (24-bit sign extended)
-0.25	6.0206	65536	-98641	FE7EAFh

Table 54: LEO Microphone Response Curve Conversion Example

See the D2Audio Application Note AN09 for detailed LEO Speaker Level Normalization scaling examples.

Base Address (DSP address + pointer value)	Offset Address	Speaker
C2:04xxxxh	4Ah	Left
C2:04xxxxh	4Bh	Right
C2:04xxxxh	4Ch	Left Surround
C2:04xxxxh	4Dh	Right Surround
C4:04xxxxh	4Ah	Surround Back Left
C4:04xxxxh	4Bh	Surround Back Right
C4:04xxxxh	4Ch	Center
C4:04xxxxh	4Dh	Subwoofer

Table 55: LEO Speaker Level Normalization Array

6.10.12 LEO SPEAKER SIZE

The output of the Speaker Size Detection portion of the LEO_ARMC_SPL_AND_SPEAKER_SIZE_ENABLE test is stored in an array at offset LEO_SPEAKER_SIZE_OFFSET in memory. The array contains four entries. Each array index is a placeholder for a channel on the addressed DSP. Each entry is presented in the format of an index. This index can be used in conjunction with Table 48 to determine the frequency at which significant rolloff occurs for a speaker attached to a specific output.

Base Address (DSP address + pointer value)	Offset Address	Speaker
C2:04xxxxh	4Eh	Left
C2:04xxxxh	4Fh	Right
C2:04xxxxh	50h	Left Surround
C2:04xxxxh	51h	Right Surround
C4:04xxxxh	4Eh	Surround Back Left
C4:04xxxxh	4Fh	Surround Back Right
C4:04xxxxh	50h	Center
C4:04xxxxh	51h	Subwoofer

Table 56: LEO Speaker Size Array

6.10.13 LEO MICROPHONE CALIBRATION LOWER LIMIT

Most microphones may not be calibrated down to DC level. To compensate for this, the user indicates to LEO the lower limit of the frequency range below which measurements are not taken into account. This frequency is the Microphone Calibration Limit (MCL) and is derived from the LEO Calibration Curve values in Table 48. If an exact frequency is not found in the LUT, use the next higher

frequency value from the LEO Calibration Curve. The Microphone Calibration Limit value is stored in an array at offset MCL in memory.

Base Address (DSP address + pointer value)	Offset Address	Value
C2:04xxxxh	52h	MCL

Table 57: LEO Speaker Microphone Calibration Lower Limit

6.10.14 LEO_KILL

LEO kill bit. When set to a "1", this bit prematurely terminates LEO processing. The LEO_KILL bit is stored in an array at offset LEO_KILL in memory.

Base Address (DSP address + pointer value)	Offset Address	Value
C2:04xxxxh	53h	LEO_KILL

Table 58: LEO_KILL

7 PHYSICAL DIMENSIONS

This section is still under development.

7.1 HEAT SINK MOUNTING DETAILS

This section is still under development.

7.2 HEAT SINK MOUNTING SURFACE

This section is still under development.

7.3 THERMAL HEAT SINK REQUIREMENTS

This section is still under development.

7.3.1 HEAT SINK THERMAL PERFORMANCE AFTER INSTALLATION

This section is still under development.

7.4 PIN LOCATIONS AND PCB DIMENSIONS

This section is still under development.

7.5 MOUNTING HARDWARE

This section is still under development.

7.6 AMBIENT OPERATING CONDITIONS

CONSUMER

The VR100-7 amplifier generates modest heat and is designed to dissipate that heat to the ambient environment. An internal temperature sensor detects if the temperature at the power output FET rail hits 80°C. At 80°C, the amplifier will linearly reduce output power proportional to the delta difference above 80°C to 100°C. This allows the amplifier to run at reduced capability rather than experience an abrupt power down. At 100°C, a "fail-safe" mode disables the amplifier. The amplifier will return to normal operation when the operating temperatures fall below the "fail-safe" or reduced power temperature thresholds. The internal temperature sensor is accessible through a temperature register (see Section 7.6.1, "Temperature Register," on page 53).

PRELIMINARY

Figure 21 shows the recommended operating range and power derating temperatures:

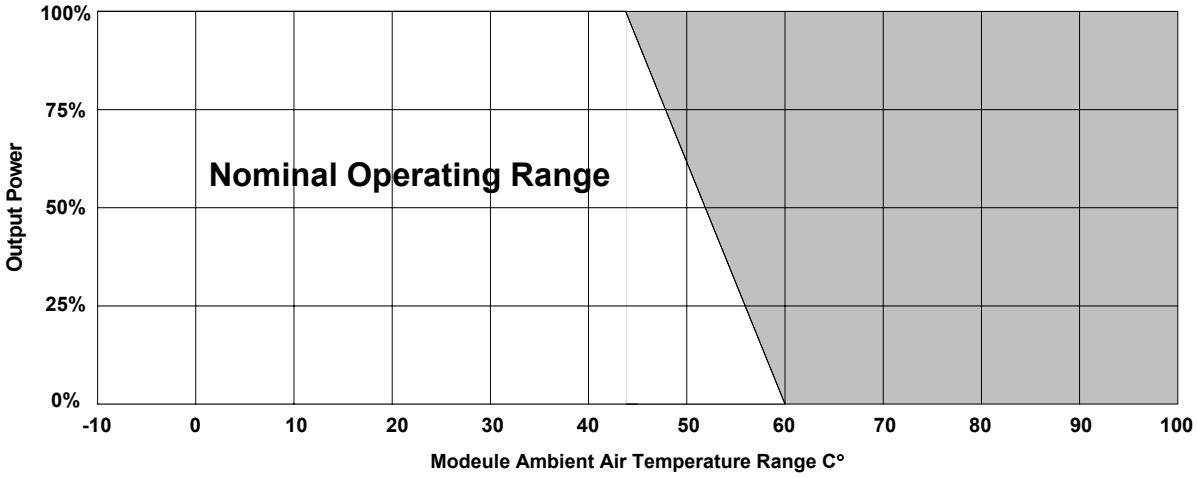


FIGURE 21: Power Derating Curve

7.6.1 TEMPERATURE REGISTER

The VR100-7 contains a temperature sensor located at the power output FET rail. The register below stores the user-accessible temperature value:

Register Name	Address
Temperature	C2:020010h

Table 59: Temperature Sensor Register Address Table

To compute the temperature in degrees C:
°C (decimal) = (value_from_temp_register_hex/256)

8 REFERENCE DESIGN PLATFORM PACKAGE PART NUMBERS AND FEATURE SETS

SKU	Watts/Channel into 8Ω, (< 0.1% THD+N, Typical Supplies)	Channels of Amplification	Audio Input Method(s)	Firmware Functionality Beyond Baseline	RoHS Compliant
D2-0VR0100R7-00061F	100W, 75W, or 50W	5 ~ 7	I^2S/LJ Digital + 2 S/PDIF Inputs		Yes
D2-0VR0100R7-00076F	100W, 75W, or 50W	5 ~ 7	I^2S/LJ Digital + 2 S/PDIF Inputs	LEO	Yes

Table 60: VR-Series Reference Design Platform Package Part Numbers and Feature Sets

CONSUMER

PRELIMINARY

9 DOCUMENT REVISION HISTORY

11/8/05 Revision 0.0.1 - First Internal Release.

- Based on Revision v1.0.8 of the MXR125 Data Sheet.

12/10/05 Revision 0.0.2 - Second Internal Release.

- Updated RVR100 to be VR100/75/50-5/7 to represent the fact that this reference design platform package covers all possible design combinations (3 Power Levels for 5, 6 and 7 Channel applications with and without DPSC). Updated DC Electrical requirements. Updated Pinout Drawing.

12/12/05 Revision 0.0.3 - Third Internal Release.

- Updated "RVR100 Data Sheet" to be "VR100/75/50-5/7 Data Sheet" on both left/right master pages in the body .FM file.

12/21/05 Revision 0.0.4 - Fourth Internal Release.

- Replaced cover page image with hi-res professional image, replaced Frequency Response and THD+N vs. Frequency plots with TBD note.

2/10/06 Revision 0.0.5 - Fifth Internal Release.

- Increased bandwidth to 40kHz
- Increased Fs to 128kHz
- Increased PWM switch rate to 512kHz
- Removed digital audio outputs from Cover Page, Figure 9, "VR100-7 Amplifier Pinout (Not to Scale)," on page 20, Section 1.5, "Switching Characteristics - Serial Audio Port," on page 12, and Section 2.1, "Pin Definitions," on page 21
- Removed Time Delay, 8-band EQ, and Loudness Contour from Cover Page, Section 6, "Software Control Settings," on page 32, Section 6.2, "Gain Management," on page 34, and Figure 60, "VR-Series Reference Design Platform Package Part Numbers and Feature Sets," on page 53
- Added Section 6.6.5, "5-Band EQ Register Address Table," on page 39

2/20/06 Revision 0.0.6

- Updated AVR signal flow, removed 8-band parametric EQ and 4x4 Matrix Mixer.

2/22/06 Revision 0.0.7

- Unreleased version. Minor changes.

3/30/06 Revision 0.0.8

- Incorporated suggested changes from JK.
- Replaced all mentions of VR100/75/50-5/7 with VR100-7.
- Removed mentions of "digital amplifier reference design" in place of only VR100-7.
- Added mentions of DAE-2 Controller.