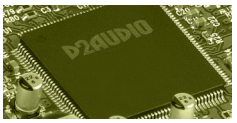
D2AUDIO D2-914xx DATA SHEET

Intelligent digital amplifier controller for manufacturers of class D audio amplifiers



PRELIMINARY

Complete Class-D Amplifier Controller SOC

- Advanced 4 Channel Digital Switching Controller with Integrated Digital Audio Engine™
- Flexible Audio Input Sources
- Multiple Controller Synchronization
- Support for both Bridge and Non-Bridged Output Topologies
- Stand-Alone or Microcontroller Boot Options (Two-Wire and SPI™)

High-Performance Sound

- Unique performance for each part number
- Superior Dynamic Range
- Up to >115 dB SNR (Open Loop)*
- Up to >118 dB SNR (Closed Loop using CS5381 ADCs)*
- Less than 0.01% THD+N (1W, 1kHz, 8 Ohm, Open Loop)*
- Less than 0.001% (1W, 1kHz, Load Independent, Closed Loop)*
- +/-0.5dB Frequency Response (1W, 20Hz ~ 20kHz, 8 Ohm, Open Loop)
- +/-0.25dB Frequency Response (1W, 20Hz ~ 20kHz, 8 Ohm, DF Enabled)

Graceful Protection and Recovery

- Complete short-circuit, over-current, and over-voltage fault protection

Pure Digital Path

- Multiple Digital Audio Inputs which support I²S and Left-Justified Formats with Linear PCM (32-192 kHz, 16-24-bit)
- Digital Audio Input which supports S/PDIF format with Linear PCM (32kHz-192kHz, 16-24 bit, IEC60958 Compliant)

Multiple Part Offerings

- **D2-91413-LR**: Ultra-High-End Performance Solution. 4 Channel PWM Controller with Integrated Digital Audio Engine™ with Digital Feedback (DF) and Digital Power Supply Correction (DPSC), 128-Pin LQFP, RoHS Compliant
- **D2-91423-LR**: High-End Performance Solution. 4 Channel PWM Controller with Integrated Digital Audio Engine™ with DF Only, 128-Pin LQFP, RoHS Compliant
- **D2-91433-LR**: Mid-End Performance Solution. 4 Channel PWM Controller with Integrated Digital Audio Engine™ with Digital Power Supply Correction (DPSC), 128-Pin LQFP, RoHS Compliant

System Control Support

- Reference Design Dependant

The D2Audio™ D2-914xx is a fully self-contained 4 channel digital amplifier controller System-On-Chip (SOC). The D2-914xx enables rapid system design for manufacturers of home theater receivers, multi-room distributed audio systems, OEM and Aftermarket Automotive Amplifiers, Powered Subwoofers and Powered Speakers.

The D2-914xx contains a high-performance digital switching controller to play any input source on any output channel.

A configurable audio signal processor provides equalization, volume control, tone control, and compression for each channel, also crossover and power limiting for powered speaker applications

The D2-914xx includes 4-channels I²S/Left-Justified inputs (16-24-bit, 16-192 kHz), optional SPDIF receiver (16-24-bit).

Boot options include external serial ROM, asynchronous serial, and asynchronous SRC.

D2AUDIO D2-914xx

- **Powerful Digital Audio Management - Reference Design Dependant SRC, Routing, Mixing, Multiple Digital Audio I/O, Tone Control, Parametric EQ, Compression**
- **Reduced Audio System Cost for manufacturers of Class D Audio amplifiers**
- **Audio Processing features enable optimized speaker performance and delivers dramatically improved sound quality.**
- **Minimum Development Cost/Risk/Time-to-Market**
- **Pure Digital Path**
- **Superior Dynamic Range**
- **>110dB SNR, <0.1% THD+N**
- **+/-0.5dB Frequency Response (20Hz - 40kHz)**

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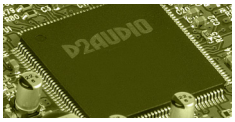
Nuclear and Medical Applications

D2Audio products are not authorized for use as critical components in life support systems, equipment used in hazardous environments or nuclear control systems without the express written consent of D2Audio Corporation.

TABLE OF CONTENTS



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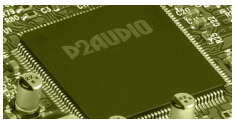
1 D2-914XX ARCHITECTURE



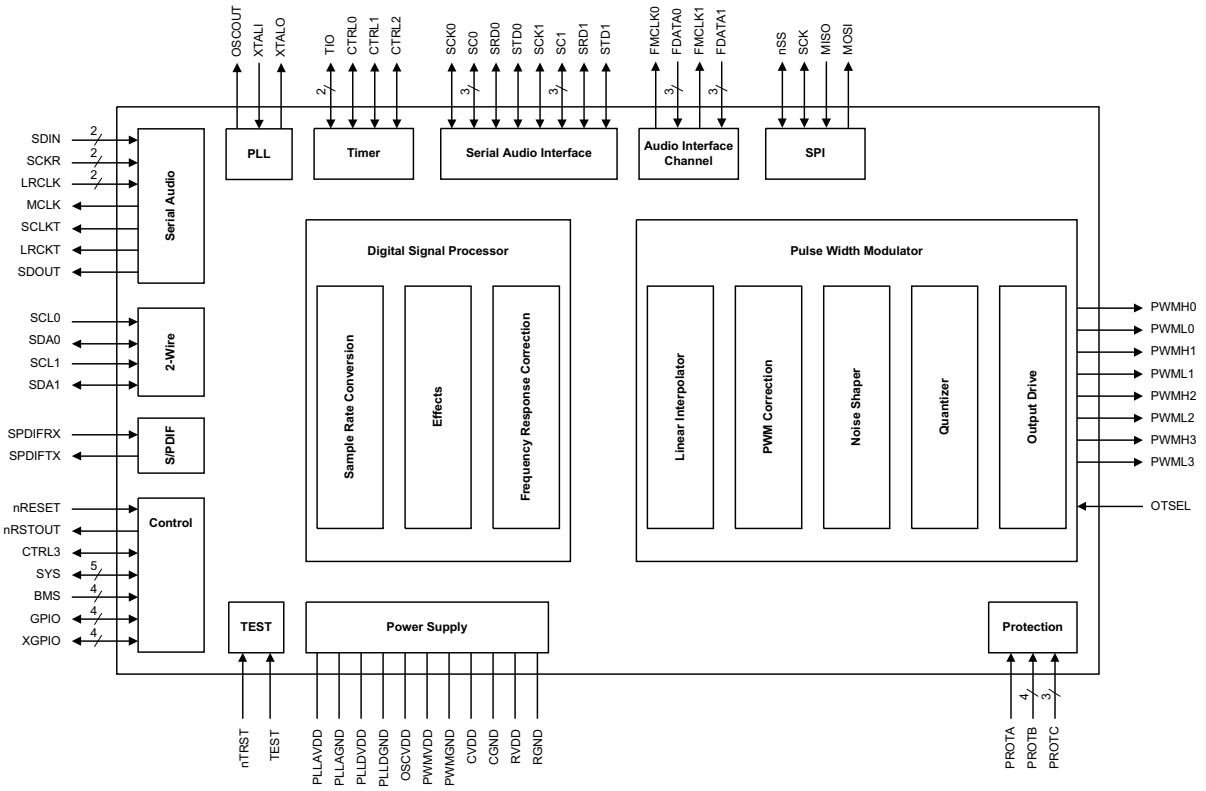


FIGURE 1: D2-914xx Block Diagram

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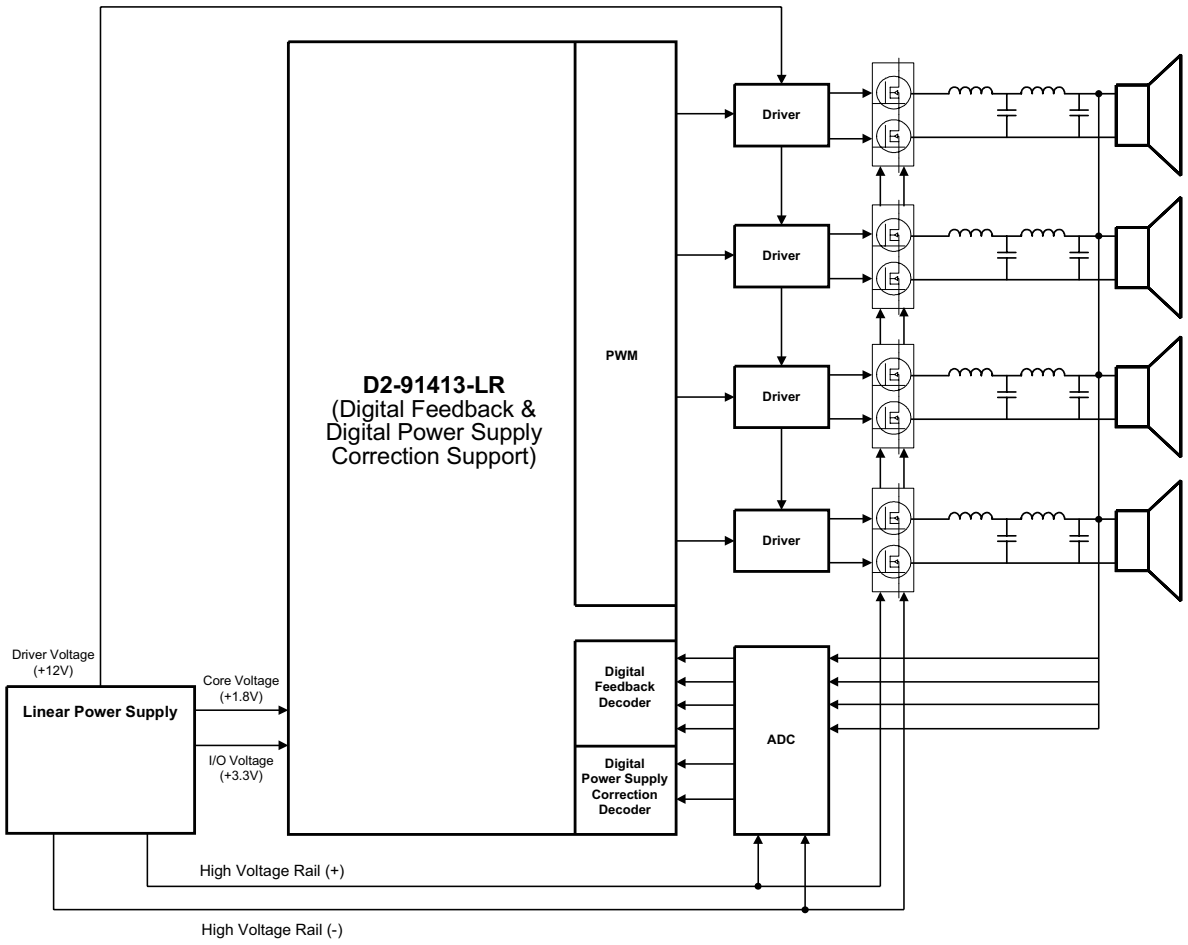
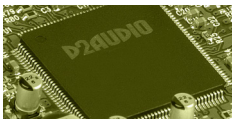


FIGURE 2: D2-91413-LR Block Diagram



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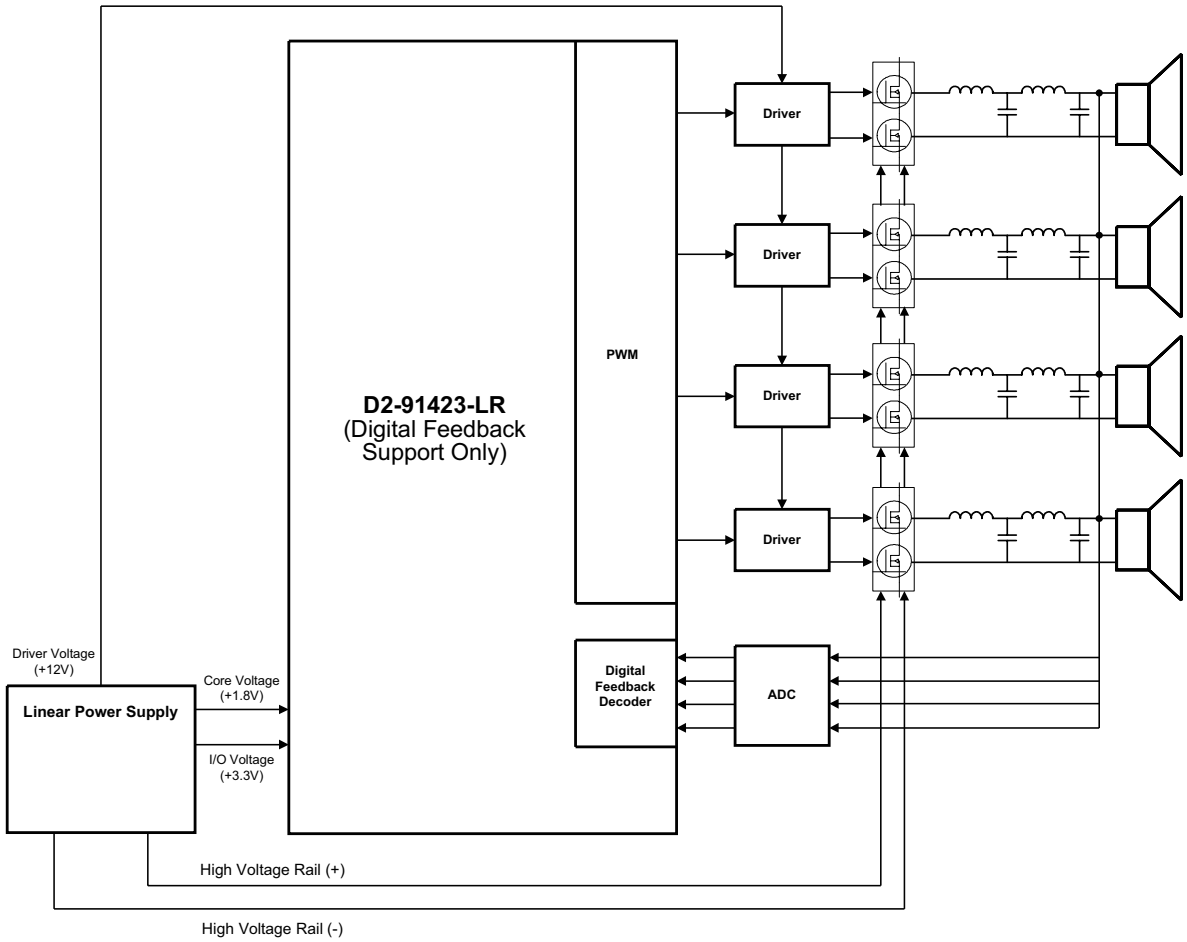

FIGURE 3: D2-91423-LR Block Diagram

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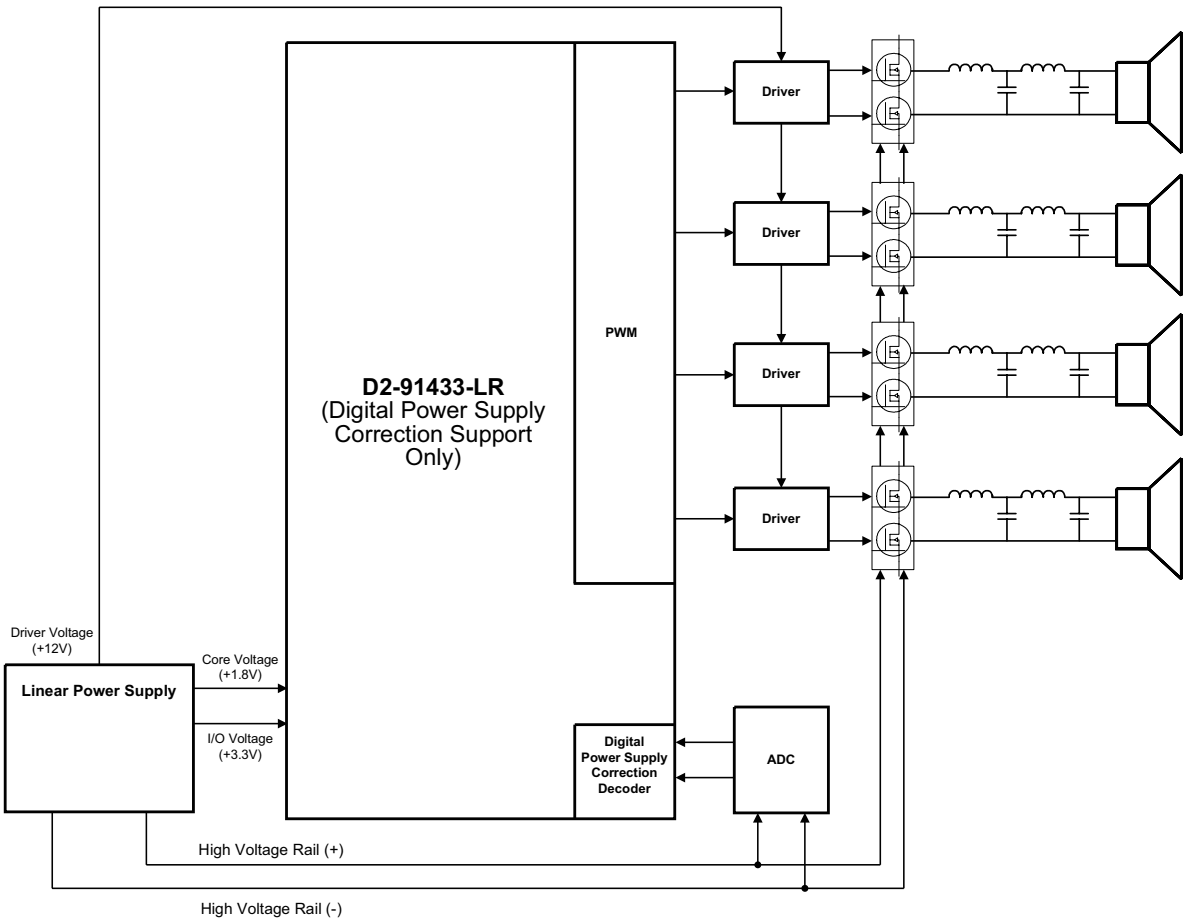
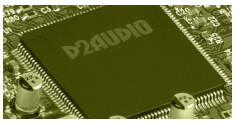


FIGURE 4: D2-91433-LR Block Diagram

1.1 D2-914XX SIGNAL FLOW

The D2-914xx supports a wide variety of signal flows that are fully programmable and are reference design dependant. D2-914xx use is to only be used as part of a licensed reference design from D2Audio corporation, and furthermore, each reference design has a set signal flow and associated performance level. See corresponding D2Audio Digital Amplifier datasheets for design-specific signal flows.

2 SPECIFICATIONS



2.1 ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Supply Voltage RVDD, PWMVDD		-0.3	4.0	V
Supply Voltage CVDD, PLLAVDD, PLLDVDD, OSCVDD		-0.3	2.4	V
Input Voltage, any input but XTALI		-0.3	RVDD+0.3	V
Input Voltage XTALI		-0.3	OSCVDD+0.3	V
Input Current, any pin but supplies		-	+/-10	mA
Operating Temperature	T_{MAX}	-10	+85	°C
Junction Temperature	T_{JNC}	-	+125	°C
Storage Temperature	T_{STG}	-55	+150	°C

TABLE 1: Absolute Maximum Ratings

2.2 PIN CHARACTERISTICS

TA=25 degrees C, CVDD=PLLAVDD=PLLDVDD=OSCVDD=1.8V +/-5%, RVDD=PWMVDD=3.3V +/-10%. All grounds at 0.0V. All voltages referenced to ground.

Parameter	Symbol	Min	Typ	Max	Unit
High Level Input Drive Voltage, note 1	V_{IH}	2.0	-	-	V
Low Level Input Drive Voltage, note 1	V_{IL}	-	-	0.8	V
High Level Output Drive Voltage, note 2 Iout = -Pad Drive	V_{OH}	RVDD - 0.3	-	-	V
Low Level Output Drive Voltage, note 2 Iout = +Pad drive	V_{OL}	-	-	0.3	V
High Level Input Drive Voltage, note 3	V_{IHX}	0.7	-	OSCVDD	V
Low Level Input Drive Voltage, note 3	V_{ILX}	-	-	0.3	V
High Level Output Drive Voltage OSCOUT pin	V_{OHO}	PLLDVDD - 0.3	-	-	V
Low Level Output Drive Voltage OSCOUT pin	V_{OLO}	-	-	0.3	V
Input Leakage Current	I_{IN}	-		+/- 10	uA
Input Capacitance	Cin	-	9	-	pF
Output Capacitance	Cout	-	9	-	pF
Note 1: All input pins except XTALI Note 2: All digital output pins Note 3: For XTALI input overdrive operation only					

TABLE 2: Pin Characteristics

PRELIMINARY

PRELIMINARY

2.3 POWER REQUIREMENTS

Typical supply currents measured at TA=25 degrees C, PLL at 300MHz, OSC at 27MHz, core running at 150MHz with typical audio data traffic. Minimum supply currents are measured in full power down configuration.

Parameter	Symbol	Min	Typ	Max	Unit
Core Supply Pins	CVDD	1.7	1.8	1.9	V
		0.01	300		mA
Digital I/O Pad Ring Supply Pins	RVDD	3.0	3.3	3.6	V
		0.01	10		mA
PWM I/O Pad Ring Supply Pins	PWMVDD	3.0	3.3	3.6	V
		0.01	5		mA
Analog Supply Pins (PLL)	PLLAVDD	1.7	1.8	1.9	V
		0.01	10		mA
	PLLDVDD	1.7	1.8	1.9	V
		0.01	2		mA
	OSCVDD	1.7	1.8	1.9	V
		0.01	4		mA

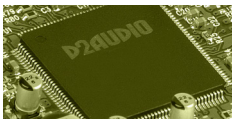
TABLE 3: Power Requirements

2.4 THERMAL CHARACTERISTICS

Package Type	Airflow	Theta J_a	Theta J_c	Unit
128-Pin LQFP	0	25.5	14.7	°C/W
	1 m/s	19.5		
	2 m/s	17.9		

TABLE 4: Thermal Characteristics

2.5 SWITCHING CHARACTERISTICS - SERIAL AUDIO PORT



T_A = 25°C, CVDD=PLLAVDD=PLLDVDD=OSCVDD=1.8V +/-5%, RVDD=PWMVDD=3.3V +/-10%. All grounds at 0.0V. All voltages referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
t_cSCLK	SCKRx frequency - SCKR0, SCKR1			12.5	MHz
t_wSCLK	SCKRx pulse width (high and low) - SCKR0, SCKR1	40			ns
t_sLRCLK	LRCKRx setup to SCLK rising - LRCKR0, LRCKR1	20			ns
t_hLRCLK	LRCKRx hold from SCLK rising - LRCKR0, LRCKR1	20			ns
t_sSDI	SDINx setup to SCLK rising - SDIN0, SDIN1	20			ns
t_hSDI	SDINx hold from SCLK rising - SDIN0, SDIN1	20			ns
t_dSDO	SDOUTx delay from SCLK falling			20	ns

TABLE 5: Serial Audio Port Timing

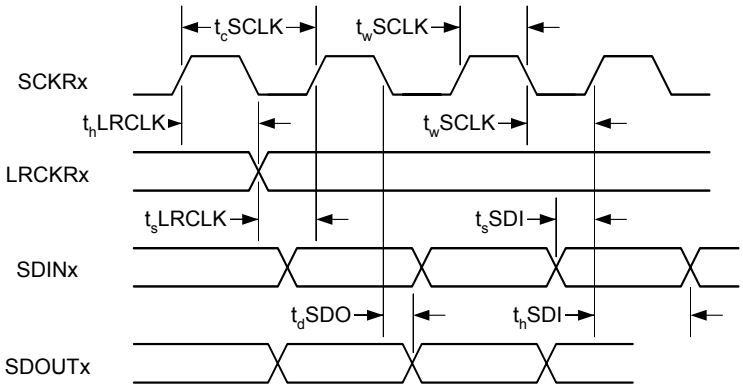


FIGURE 5: Serial Audio Port Timing

2.5.1 SERIAL AUDIO INPUTS (SAI PORTS)

The D2-914xx module contains one SAI port for each pair of channels. Each input can support an individually selectable sample rate from 32kHz to 192kHz. All digital audio inputs are 3.3V CMOS logic. The SAI port is designed to interface with standard digital audio components and to accept I^2S or Left-Justified data formats.

For I^2S format, the left channel data is read when LRCK is low. For the Left-Justified format, the left channel data is read when LRCK is high. Either format requires data to be valid on the rising edge of SCLK and sent MSB-first on SDIN with 32 bits of data per channel. Each set of digital inputs runs asynchronously to the others and may accept different sample rates and formats.

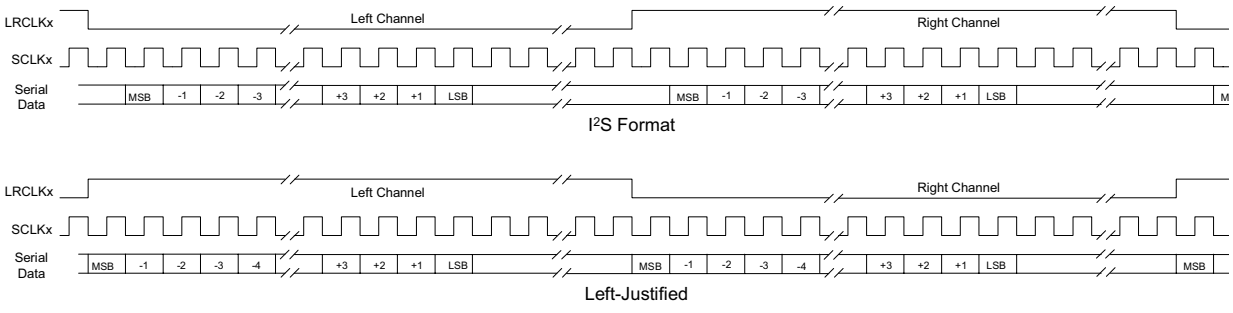


FIGURE 6: SAI port Data Formats

PRELIMINARY

2.6 SWITCHING CHARACTERISTICS - 2-WIRE INTERFACE

T_A = 25°C, CVDD=PLLAVDD=PLLDVDD=OSCVDD=1.8V +/-5%, RVDD=PWMVDD=3.3V +/-10%. All grounds at 0.0V. All voltages referenced to ground.

Symbol	Description	Min	Max	Unit
fSCL	SCL frequency		100	kHz
t_{buf}	Bus free time between transmissions	4.7		us
t_{wlow}SCLx	SCL clock low	4.7		us
t_{whigh}SCLx	SCL clock high	4.0		us
t_sSTA	Setup time for a (repeated) Start	4.7		us
t_hSTA	Start condition Hold time	4.0		us
t_hSDAx	SDA hold from SCL falling (see note)	0		us
t_sSDAx	SDA setup time to SCL rising	250		ns
t_dSDAx	SDA output delay time from SCL falling		3.5	us
t_r	Rise time of both SDA and SCL		1	us
t_f	Fall time of both SDA and SCL		300	ns
t_sSTO	Setup time for a Stop condition	4.7		us
Note: Data must be held sufficient time to bridge the 300ns transition time of SCL				

TABLE 6: 2-Wire Interface Port Timing

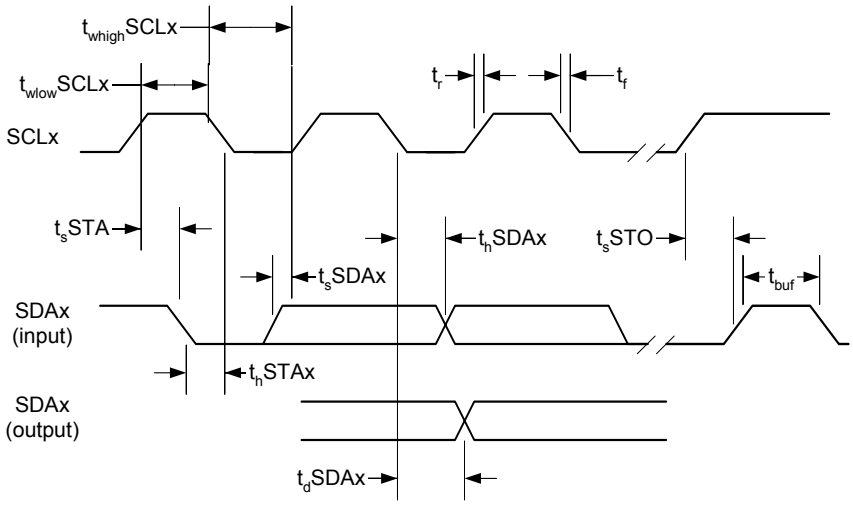


FIGURE 7: 2-Wire Interface Timing

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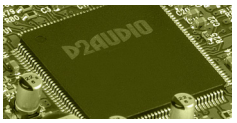
2.7 SWITCHING CHARACTERISTICS - SPI™ INTERFACE



T_A = 25°C, CVDD=PLLAVDD=PLLDVDD=OSCVDD=1.8V +/-5%, RVDD=PWMVDD=3.3V +/-10%. All grounds at 0.0V. All voltages referenced to ground.

Symbol	Description	Min	Max	Unit
fSCL	SCK frequency		TBD	MHz
t_V	MOSI valid from clock edge		TBD	ns
t_S	MISO setup to clock edge	TBD		ns
t_H	MISO hold from clock edge	TBD		ns
t_{WI}	nSS minimum width	3		3 system clocks + 2ns

TABLE 7: SPI Port Timing

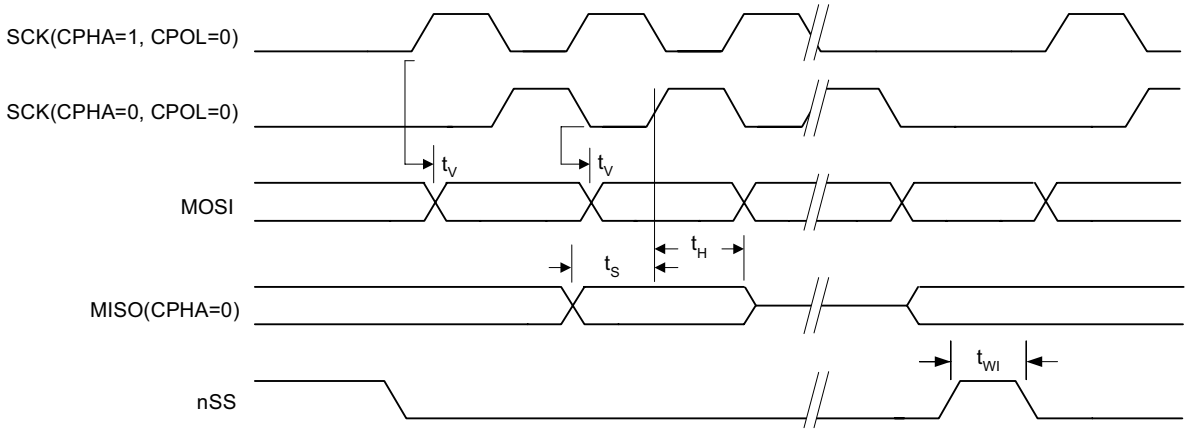


FIGURE 8: SPI Timing

PRELIMINARY

3 D2-91413-LR PACKAGE PINOUT

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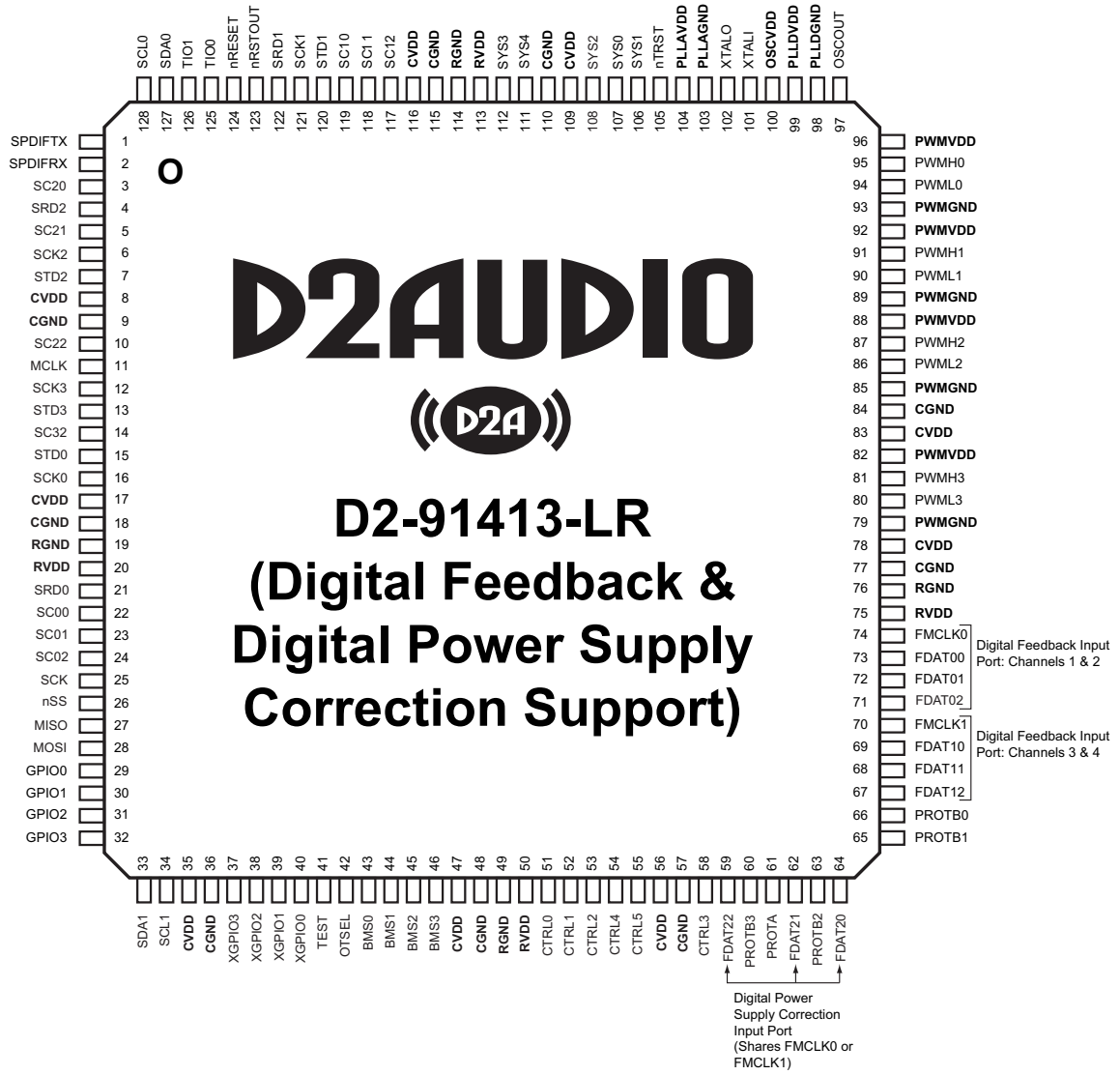
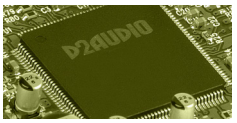


FIGURE 9: D2-91413-LR Pinout

4 D2-91423-LR PACKAGE PINOUT



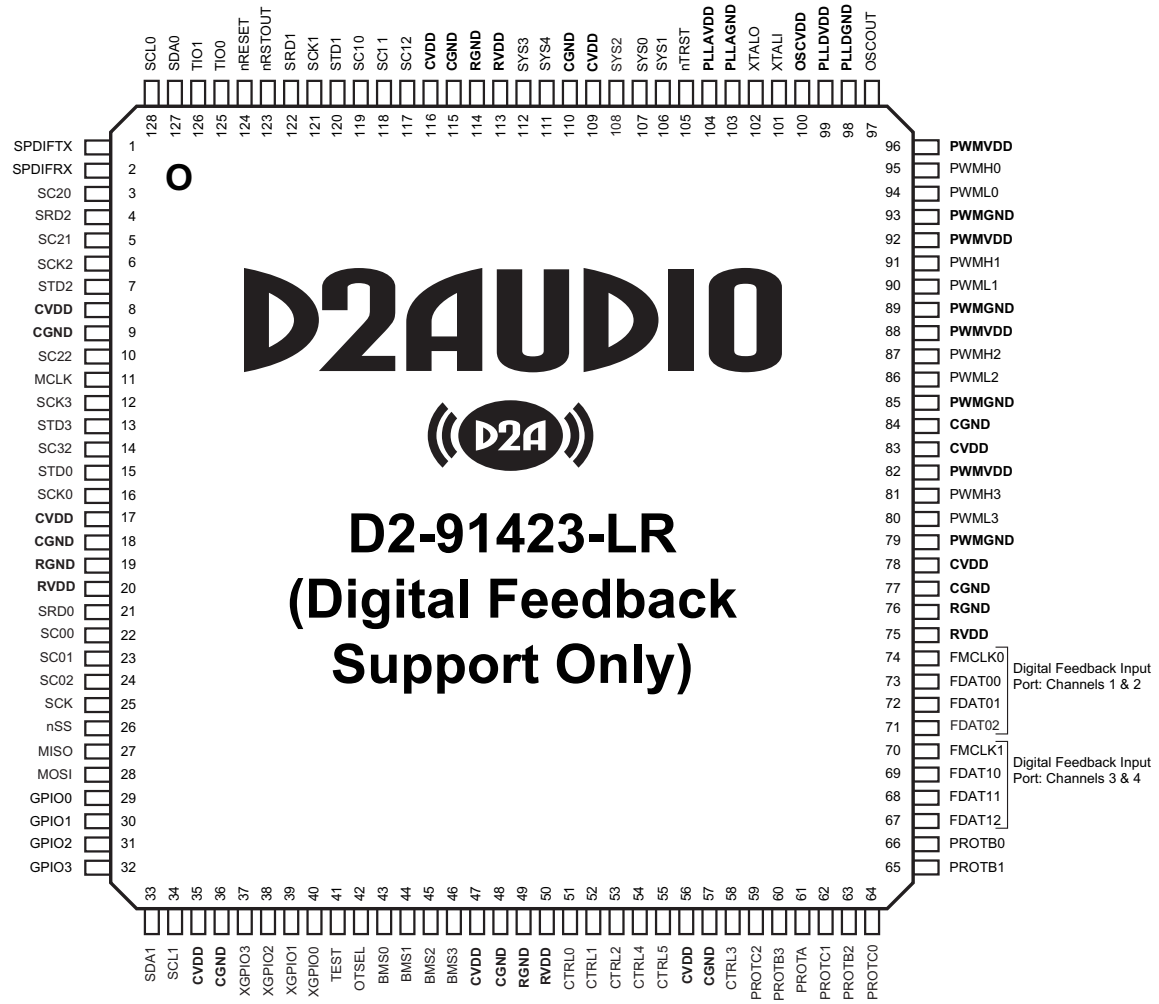


FIGURE 10: D2-91423-LR Package Pinout

PRELIMINARY

5 D2-91433-LR PACKAGE PINOUT

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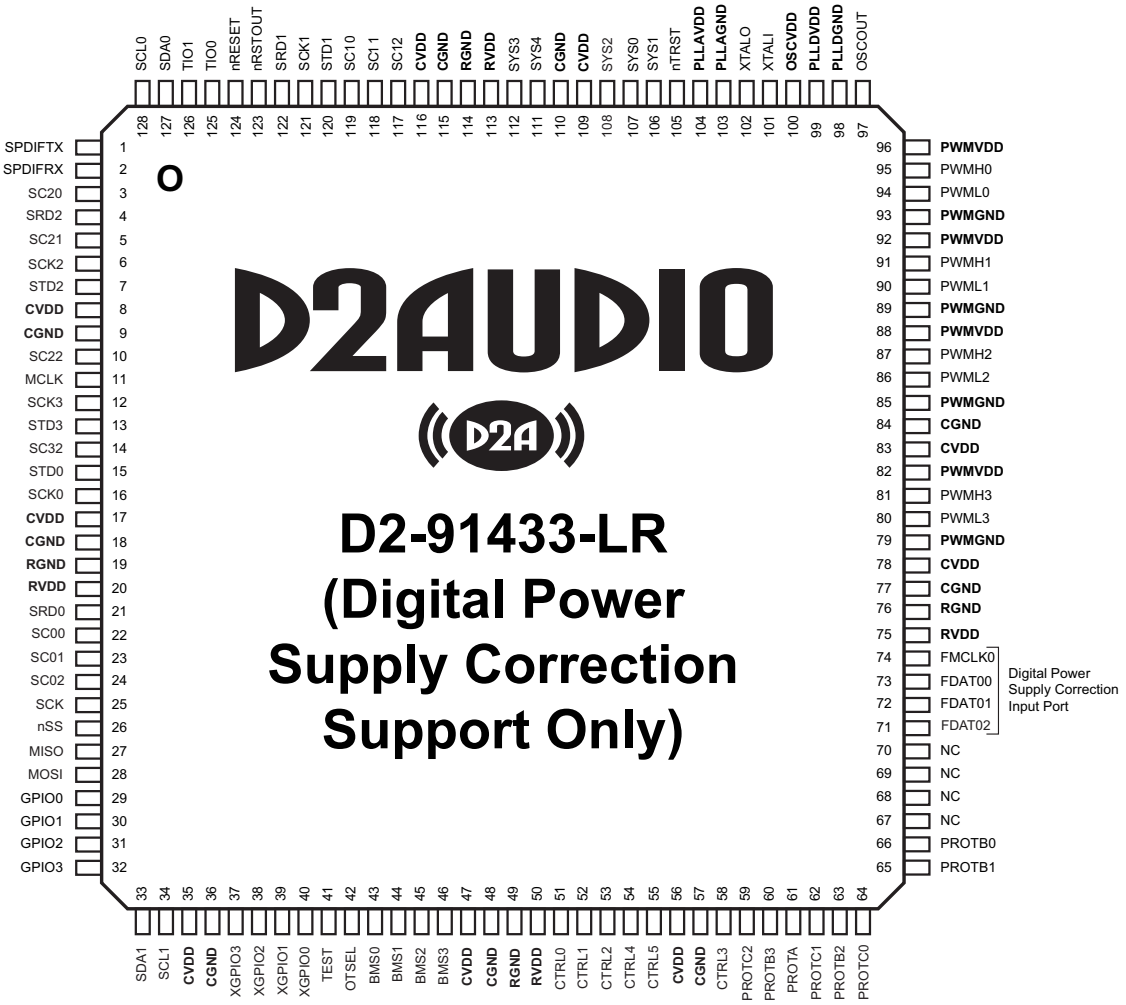
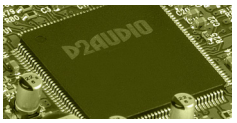


FIGURE 11: D2-91433-LR Package Pinout

5.1 D2-914XX-LR PIN DEFINITIONS



PRELIMINARY

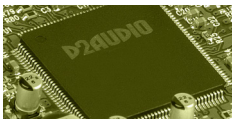
Serial Audio Pins (SAI/SAO)			
Pin Number	**Port Name**	**Type**	**Description**
11	MCLK	Output	Master clock.
3	SC20	I/O	Serial Audio Bit Clock Receiver 0 (SCKR0)
5	SC21	I/O	Serial Audio Left/Right Clock Receiver 0 (LRCKR0)
4	SRD2	Input	Serial Audio Data In 0 (SDIN0)
6	SCK2	I/O	Serial Audio Bit Clock Receiver 1 (SCKR1)
10	SC22	I/O	Serial Audio Left/Right Clock Receiver 1 (LRCKR1)
7	STD2	Input	Serial Audio Data In 1 (SDIN1)
12	SCK3	I/O	Serial Audio Bit Clock Transmitter (SCKT)
14	SC32	I/O	Serial Audio Left/Right Clock Transmitter (LRCKRT)
13	STD3	Output	Serial Audio Data Output (SDO)
S/PDIF Pins			
Pin Number	**Port Name**	**Type**	**Description**
1	SPDIFTX	Output	S/PDIF data output
2	SPDIFRX	Input	S/PDIF data input
PWM Pins			
Pin Number	**Port Name**	**Type**	**Description**
95	PWMH0	Output	Channel 0 PWM high side output
94	PWML0	Output	Channel 0 PWM low side output
91	PWMH1	Output	Channel 1 PWM high side output
90	PWML1	Output	Channel 1 PWM low side output
87	PWMH2	Output	Channel 2 PWM high side output
86	PWML2	Output	Channel 2 PWM low side output
81	PWMH3	Output	Channel 3 PWM high side output
80	PWML3	Output	Channel 3 PWM low side output
42	OTSEL	Input	Output topology select input
2-Wire Serial Pins			
Pin Number	**Port Name**	**Type**	**Description**
128	SCL0	I/O	Two wire port 0 serial clock
127	SDA0	I/O	Two wire port 0 serial data
34	SCL1	I/O	Two wire port 1 serial clock
33	SDA1	I/O	Two wire port 1 serial data
SPI Pins			
Pin Number	**Port Name**	**Type**	**Description**
26	nSS	I/O	SPI slave select IO
25	SCK	I/O	SPI clock IO
27	MISO	Input	SPI master input
28	MOSI	Output	SPI master output
GPIO Pins			
Pin Number	**Port Name**	**Type**	**Description**
32, 31, 30, 29	GPIO[3:0]	I/O	General purpose I/O
37, 38, 39, 40	XGPIO[3:0]	I/O	General purpose I/O
Reset and Test Pins			
Pin Number	**Port Name**	**Type**	**Description**
124	nRESET	Input	Reset - active low
105	nTRST	Input	Test Reset - active low
123	nRSTOUT	Output	Reset output- active low output

TABLE 8: Pin Definitions

PRELIMINARY

41	TEST	Input	Hardware test pin
Crystal Oscillator and PLL Pins			
Pin Number	**Port Name**	**Type**	**Description**
97	OSCOUT	Output	Oscillator output to slave device
101	XTALI	Input	Crystal Oscillator input
102	XTALO	Output	Crystal Oscillator output
Audio Interface Channel (AIC) Pins			
Pin Number	**Port Name**	**Type**	**Description**
74	FMCLK0	Output	Analog Interface Channel Master Clock 0 (Used for Digital Feedback Input Port: Channels 1 & 2 in D2-91413-LR and D2-91423-LR, Used for Digital Power Supply Correction Input Port: D2-91433-LR)
71, 72, 73	FDAT0[2:0]	Input	Analog Interface Channel Data 0 (Used for Digital Feedback Input Port: Channels 1 & 2 in D2-91413-LR and D2-91423-LR, Used for Digital Power Supply Correction Input Port: D2-91433-LR)
70	FMCLK1	Output	Analog Interface Control Master Clock 1 (Used for Digital Feedback Input Port: Channels 3 & 4 in D2-91413-LR and D2-91423-LR)
67, 68, 69	FDAT1[2:0]	Input	Analog Interface Channel Data 1 (Used for Digital Feedback Input Port: Channels 3 & 4 in D2-91413-LR and D2-91423-LR)
59, 62, 64	FDAT2[2:0]	Input	Analog Interface Channel Data 1 (Used for Digital Power Supply Correction Input Port: D2-91413-LR)
Serial Audio Interface Pins			
Pin Number	**Port Name**	**Type**	**Description**
16	SCK0	I/O	Serial Audio Interface 0 serial clock port
121	SCK1	I/O	Serial Audio Interface 1 serial clock port
24, 23, 22	SC0[2:0]	I/O	Serial Audio Interface 0 serial control ports
117, 118, 119	SC1[2:0]	I/O	Serial Audio Interface 1 serial control ports
21	SRD0	I/O	Serial Audio Interface 0 serial receive data ports
122	SRD1	I/O	Serial Audio Interface 1 serial receive data ports
15	STD0	I/O	Serial Audio Interface 0 serial transmit data
120	STD1	I/O	Serial Audio Interface 1 serial transmit data ports
System Control Pins			
Pin Number	**Port Name**	**Type**	**Description**
46, 45, 44, 43	BMS[3:0]	Input	Boot mode select
51	CTRL0	I/O	Power supply pump control, high side or GPIO.
52	CTRL1	I/O	Power supply pump control, low side or GPIO
53	CTRL2	I/O	PWM sync
58	CTRL3	I/O	Power supply sync
54	CTRL4	I/O	Power temperature protection
55	CTRL5	I/O	Power over-current protection
107	SYS0	I/O	Reserved for factory test
106	SYS1	Input	
108	SYS2	Input	
112	SYS3	Input	
111	SYS4	Output	
Timer (TIO) Pins			
Pin Number	**Port Name**	**Type**	**Description**
126, 125	TIO[1:0]	I/O	Timer I/O ports
PWM Protection Pins			
Pin Number	**Port Name**	**Type**	**Description**

TABLE 8: Pin Definitions (Continued)



61	PROTA	I/O	PWM Temperature status input, or GPIO
60, 63, 65, 66	PROTB	I/O	PWM Over Current Protection inputs, or GPIO.
59, 62, 64	PROTC	I/O	PWM Shoot Through Current inputs or GPIO.
Power Pins			
Pin Number	**Port Name**	**Type**	**Description**
104	PLLAVDD	Power	PLL Analog power
103	PLLAGND	Ground	PLL Analog ground
99	PLLDVDD	Power	PLL Digital power
98	PLLDGND	Ground	PLL Digital ground
100	OSCVDD	Power	Oscillator power
116, 109, 83, 78, 56, 47, 35, 17, 8	CVDD	Power	Core power - 9 pins
115, 110, 84, 77, 57, 48, 36, 18, 9	CGND	Ground	Core ground - 9 pins
96, 92, 88, 82	PWMVDD	Power	PWM output pin power - 4 pins
93, 89, 85, 79	PWMGND	Ground	PWM output pin ground.- 4 pins
113, 75, 50, 20	RVDD	Power	Digital pad ring power - 4 pins
114, 76, 49, 19	RGND	Ground	Digital pad ring ground- 4 pins

TABLE 8: Pin Definitions (Continued)

PRELIMINARY

5.2 PIN DESCRIPTIONS

Pins are 100% firmware and Reference Design dependent for their functionality. Output pins have one of 3 drive strengths - 4mA, 8mA, or 16mA. These strengths are characterized by the current that the pin will source or sink at the specified output voltage level.

5.2.1 SERIAL AUDIO (SAI/SAO) PINS

MCLK — **Master Clock Output**
Master Clock output for external ADC/DAC components with 16mA drive strength. Pin drives low on reset.

SC20 — **SAI Receiver Bit Clock 1**
SAI Receiver 0 bit clock is an output when D2-914xx is a master, or an input when D2-914xx is a slave. Defaults to an input on reset. Output has 8mA drive strength. Input has hysteresis.

SC21 — **SAI Receiver Left/Right Clock 0**
SAI Receiver 0 left/right audio frame clock is an output when D2-914xx is a master or an input when D2-914xx is a slave. Defaults to an input on reset. Output has 8mA drive strength.

SRD2 — **SAI Receiver Serial Data Input 0**
SAI Receiver 0 data input.

SCK2 — **SAI Receiver Bit Clock 1**
SAI Receiver 1 bit clock is an output when D2-914xx is a master, or an input when D2-914xx is a slave. Defaults to an input on reset. Output has 8mA drive strength. Input has hysteresis.

SC22 — **SAI Receiver Left/Right Clock 1**
SAI Receiver 1 left/right audio frame clock is an output when D2-914xx is a master or an input when D2-914xx is a slave. Defaults to an input on reset. Output has 4mA drive strength.

STD2 — **SAI Receiver Serial Data Input 1**
SAI Receiver 1 data input.

SCK3 — **SAI Transmitter Bit Clock**
SAI Transmitter bit clock is an output when D2-914xx is a master, or an input when D2-914xx is a slave. Defaults to an input on reset. Output has 8mA drive strength. Input has hysteresis.

SC32 — **SAI Receiver Left/Right Clock**
SAI Transmitter left/right audio frame clock is an output when D2-914xx is a master or an input when D2-914xx is a slave. Defaults to an input on reset. Output has 8mA drive strength.

STD3 — **SAI Receiver Serial Data Output**
SAI Transmitter data output with 8mA drive strength.

5.2.2 SPDIF PINS

SPDIFRX — **S/PDIF Data Input**
This pin is the S/PDIF audio input and accepts a 3.3V stereo input up to 192kHz. To drive this pin, appropriate buffer and/or isolation circuits may be necessary to convert the S/PDIF cable input signal to proper logic levels.

SPDIFTX — **S/PDIF Data Output**
This pin is the S/PDIF audio output and drives a 3.3V stereo output up to 192kHz with 4mA drive strength.

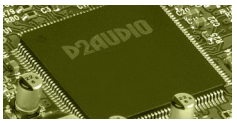
5.2.3 PWM PINS

PWMxH — **PWM High Side Driver Outputs**
PWM high side driver outputs, where x is 0 to 3, with 16mA drive strength. Pin drives to state determined by OTSEL on reset.

PWMxL — **PWM Low Side Driver Outputs**
PWM low side driver outputs, where x is 0 to 3, with 16mA drive strength. Pin drives low on reset.

OTSEL — **Output Topology Select Input**
Output topology select input. OTSEL pin state controls the PWMxH drive polarity. Typically, OTSEL will be tied either high for active-low PWMxH FET drivers, or tied low for active-high PWMxH FET drivers.

PRELIMINARY



PRELIMINARY

5.2.4 2-WIRE SERIAL PINS

SCL0 — **Serial Clock 0**
Two-Wire Serial clock port 0, open drain driver with 8mA drive strength. Bidirectional signal is used by both the master and slave controllers for clock signaling.

SDA0 — **Serial Data 0**
Two-Wire Serial data port 0, open drain driver with 8mA drive strength. Bidirectional signal used by both the master and slave controllers for data transport.

SCL1 — **Serial Clock 1**
Two-Wire Serial clock port 1, open drain driver with 8mA drive strength. Bidirectional signal is used by both the master and slave controllers for clock signaling.

SDA1 — **Serial Data 1**
Two-Wire Serial data port 1, open drain driver with 8mA drive strength. Bidirectional signal used by both the master and slave controllers for data transport.

5.2.5 SPI PINS

nSS — **Slave Select**
SPI slave select IO. May be used as GPIO with 4mA driver. Resets to input.

SCK — **SPI Clock**
SPI clock IO with hysteresis input. May be used as GPIO with 4mA driver. Resets to input.

MISO — **Master In Slave Out**
SPI master input, slave output data signal. May be used as GPIO with 4mA driver. Resets to input.

MOSI — **Master Out Slave In**
SPI master output, slave input data signal. May be used as GPIO with 4mA driver. Resets to input.

5.2.6 RESET AND TEST PINS

nRESET — **System Reset Input**
Active low reset input with hysteresis. Low level activates system level reset, initializing all internal logic and program operations. System latches boot mode selection on the IRQ input pins on the rising edge.

nTRST — **Test Reset Input**
Active low reset input. Low level activates test reset, initializing test hardware. Must be driven low with nRESET.

nRSTOUT — **System Reset Output**
Active low reset output with 16mA driver. Pin drives low on any of POR output, 3.3V brown out detector, 1.8V brown out detector.

TEST — **Test Mode Input**
Hardware test mode control. For D2Audio use only. Must be tied low.

5.2.7 CRYSTAL OSCILLATOR PINS

OSCOUT — **Oscillator Output**
Analog oscillator output to slave D2-914xx devices. OSCOUT drives a buffered version of the crystal oscillator signal from the XTALI pin.

XTALI — **Crystal Oscillator Input**
Crystal oscillator analog input port. An external clock source would be driven into the this port. In multi-D2-914xx systems, the OSCOUT from the master D2-914xx would drive the XTALI pin.

XTALO — **Crystal Oscillator Output**
Crystal oscillator analog output port. When using an external clock source, this pin must be open. XTALO does not have a drive strength specification.

5.2.8 GPIO PINS

GPIO[3:0] — **General Purpose I/O**
Bidirectional GPIO ports with 16mA driver. Resets to input ports.

XGPIO[3:0] — **Extra General Purpose I/O**
Bidirectional GPIO ports with 16mA driver. Resets to input ports.

PRELIMINARY

5.2.9 TIMER (TIO) PINS

TIO[1:0] **Timer**
Timer I/O ports with 16mA driver. May be configured as GPIO.

5.2.10 PWM PROTECTION PINS

PROTA **PWM Protection A Input**
PWM protection A input with 4mA driver and hysteresis input. May be configured as GPIO.

PROTB[3:0] **PWM Protection B Inputs**
PWM protection B inputs with 4mA drivers and hysteresis inputs. May be configured as GPIO.

PROTC[2:0] **PWM Protection C Inputs**
PWM protection C inputs with 4mA drivers and hysteresis inputs. May be configured as GPIO.

5.2.11 AUDIO INTERFACE CHANNEL (AIC)

FMCLK0 **AIC Channel 0 Master Clock**
Analog Interface Channel Master Clock 0, with 16mA driver and hysteresis receiver.

FDAT0[2:0] **AIC Channel 0 Data**
Analog Interface Channel Data 0 inputs.

FMCLK1 **AIC Channel 1 Master Clock**
Analog Interface Control Master Clock 1, with 16mA driver and hysteresis receiver.

FDAT1[2:0] **AIC Channel 1 Data**
Analog Interface Channel Data 0 inputs.

5.2.12 SERIAL AUDIO INTERFACE PINS

SCK0 **Serial Clock 0**
Serial Audio Interface 0 serial clock port with 8mA driver and hysteresis receiver. Resets to input port. May be configured as GPIO.

SCK1 **Serial Clock 1**
Serial Audio Interface 1 serial clock port with 8mA driver and hysteresis receiver. Resets to input port. May be configured as GPIO.

SC0[2:0] **Serial Control 0**
Serial Audio Interface 0 serial control ports with 8mA driver. Resets to input port. May be configured as GPIO. SC00 input has hysteresis.

SC1[2:0] **Serial Control 1**
Serial Audio Interface 1 serial control ports with 8mA driver. Resets to input port. May be configured as GPIO. SC10 input has hysteresis.

SRD0 **Serial Receive Data 0**
Serial Audio Interface 0 serial receive data ports with 4mA driver. Resets to input port. May be configured as GPIO.

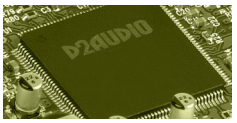
SRD1 **Serial Receive Data 1**
Serial Audio Interface 1 serial receive data ports with 4mA driver. Resets to input port. May be configured as GPIO.

STD0 **Serial Transmit Data 0**
Serial Audio Interface 0 serial transmit data ports with 8mA driver. Resets to input port. May be configured as GPIO.

STD1 **Serial Transmit Data 1**
Serial Audio Interface 1 serial transmit data ports with 8mA driver. Resets to input port. May be configured as GPIO.

5.2.13 CONTROL PINS

CTRL0 **Power Supply Pump High**
High side power supply pump output with 16mA driver. May be used as GPIO. Drives low on reset. Provides control means for operating an external switching power supply.



CTRL1 **Power Supply Pump Low**
Low side power supply pump output with 16mA driver. May be used as GPIO. Drives low on reset. Provides control means for operating an external switching power supply.

CTRL2 **Power Supply Sync**
Switching power supply synchronization signal with 16mA driver. May be used as GPIO. Resets to input port.

CTRL3 **PWM Synchronization**
PWM synchronization port with 16mA drive. Used in multi-D2-914xx configurations to synchronize the PWM controllers. The master D2-914xx will drive synchronization data to the slave D2-914xx(s), thus the pin will be an output on the master D2-914xx and an input on the slave D2-914xx(s). Pin floats on reset.

CTRL4 **Power Supply Temperature Protection**
Power supply timer protection input. May be used as GPIO with 4mA driver. Resets to input port.

CTRL5 **Power Supply Current Protection**
Power supply timer protection input. May be used as GPIO with 4mA driver. Resets to input port.

SYS[4:0] **System Pins**
Reserved for factory test. Tie high with 10k ohm resistor.

5.2.14 BOOT MODE SELECT PINS

BMS[3:0] **Boot Mode Select Inputs**
External boot mode select inputs. On nRESET deassertion, these pins specify the boot mode selection.

5.2.15 POWER PINS

PLLAVDD/PLLAGND **PLL Analog power and ground**
PLL analog supply/return. This 1.8V supply is used for the jitter-critical sections of the PLL.

PLLDVDD/PLLDGND **PLL Digital power and ground**
PLL digital supply/return. This 1.8V supply is used for the "dirty" sections of the PLL, and provides the pad supplies for all of the analog pads. Note that PLLDGND and CGND are connected through the substrate.

OSCVDD **Oscillator power**
Oscillator supply. This 1.8V supply is used for the crystal oscillator and oscillator bias circuits only.

CVDD/CGND **Core power and ground**
Core supply/return. This 1.8V supply is used in the chip interior logic and pad ring interfaces. There are 9 core supply pad pairs internally connected around the pad ring.

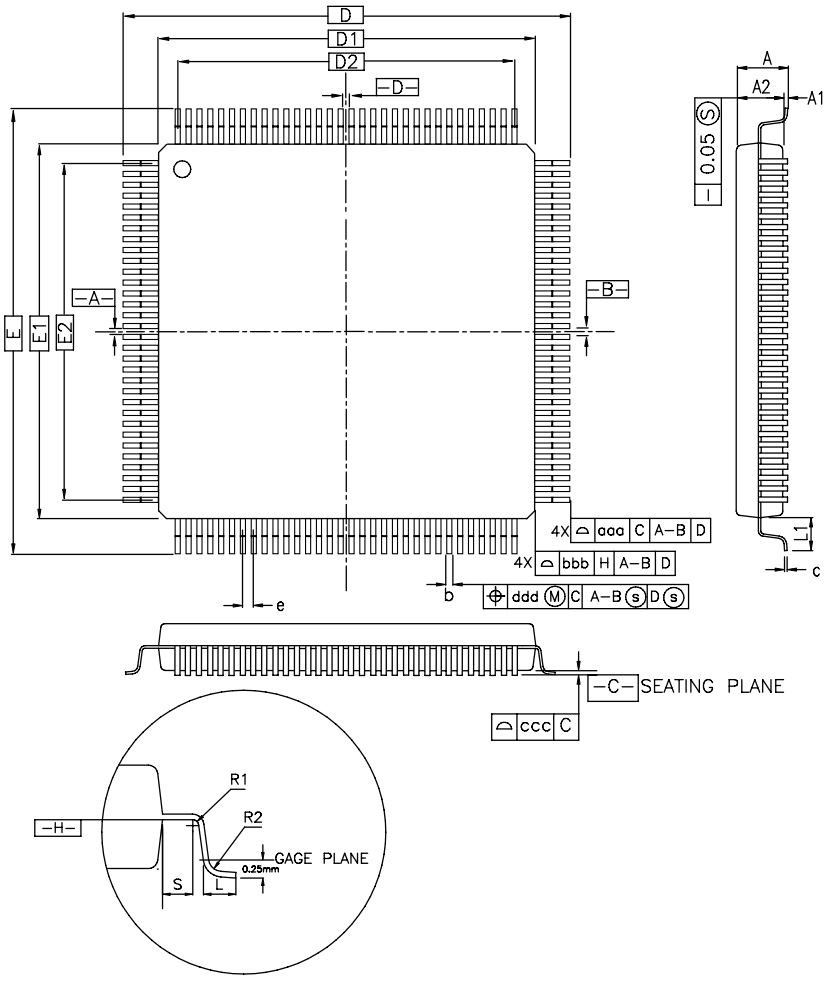
PWMVDD/PWMGND **PWM driver power and ground**
PWM I/O pad driver supply/return. This 3.3V supply is used for the PWM pad drivers only. There are 4 PWM internally connected supply pairs, one for each PWM data channel.

RVDD/RGND **Pad Ring power and ground**
Ring I/O pad driver supply/return. This 3.3V supply is used for all the digital I/O pad drivers and receivers except for the PWM and analog pads. There are 4 ring supply pairs internally connected around the pad ring.

PRELIMINARY

6 PACKAGE PHYSICAL DIMENSIONS

PRELIMINARY

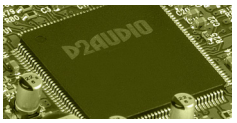


CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	16.00 BSC.			0.630 BSC.		
D1	14.00 BSC.			0.551 BSC.		
D2	12.40			0.488		
E	16.00 BSC.			0.630 BSC.		
E1	14.00 BSC.			0.551 BSC.		
E2	12.40			0.488		
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
b	0.13	0.16	0.23	0.005	0.006	0.009
c	0.09	—	0.20	0.004	—	0.008
e	0.40 BSC.			0.016 BSC.		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003		

FIGURE 12: D2-914xx Package Dimensions

7 D2-914XX RESET AND BOOT MODES



7.1 RESET

D2-914xx has a two reset inputs - the nRESET and nTRST input pins. The nRESET input pin is effectively a power-on system reset. All internal state logic, except internal test hardware, is initialized by nRESET. While reset is active the system is held in the reset condition. The reset condition is defined as all internal reset signals being active, the crystal oscillator is running, and the PLL disabled. The nTRST input resets internal factory test hardware only.

To assure proper system initialization, the nTRST input pin must be driven low along with nRESET.

7.2 BOOT MODES

The boot mode is determined by the BMS pin inputs. The BMS pin state is latched on the deassertion of system reset. It is expected that the application board will have pull-ups in the BMS pins, so that the desired boot mode is selected by default. The following table defines the boot modes.

Mode	BMS	M/S	Interface Speed	Description
0	0000			RESERVED
1	0001	M	400kb/s	ROM on 2-wire 0 port
2	0010	M	TBD	SPI ROM on SPI port
3	0011	S	per Master	SPI slave
7	0111	S	384Kb/s	Fast Asynchronous slave boot (ex: D2-914xx to D2-914xx)
8	1000			RESERVED
9	1001			RESERVED
A	1010			RESERVED
B	1011			RESERVED
C	1100	S	per Master	2-wire port 1 slave boot from micro, address = 1000101x
D	1101			RESERVED
E	1110			RESERVED
F	1111			RESERVED

TABLE 9: Boot Modes

The Interface Speed specification is the speed at which the interface is configured to operate by the boot code. For the selection where the interface speed is "per Master", the interface must operate within the requirements of the selected interface specification.

PRELIMINARY

8 IC PART ORDERING

8.1 IC PART NUMBERING SCHEME

PRELIMINARY

Nomenclature

D2-[A][D][C][P][K]-[R][E]

A = IC Product Class (single digit number)
"9" = 9-Series Advanced PWM Controller with Integrated Digital Audio Engine (4 Channel DSP + PWM Controller offered 128-pin LQFP packages)

D = Chip Instantiation/Derivation Version (single digit hexadecimal number)
"1" = First Instantiation of IC Architecture

C = Number of PWM Outputs Channels (single digit hexadecimal number)
Channel count offerings:
"2" = 2 Channels
"4" = 4 Channels
(Note: The number of PWM output channels is not to be confused with the number of digital audio input channels that are available via Serial Audio Interface port.)

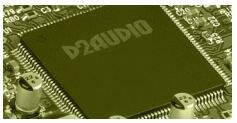
P = Performance (single digit hexadecimal number)
Performance Level offerings:
"0" = Customizable Functionality and Sonic Quality
"1" = THX® Ultra2™/Ultra-High-End Fixed-Level Performance
"2" = THX® Select™/High-End Fixed-Level Performance
"3" = Mid-End Performance

K = Pin Count (single digit hexadecimal number)
Current pin count offerings:
"1" = Undefined
"2" = 144-pin
"3" = 128-pin

R = Package Type (single character)
Current package Type offerings:
"E" = Engineering Prototype
"L" = LQFP
"P" = DIP
"S" = SOIC
"B" = BGA
"M" = Integrated Power Stage (Module IC) or Integrated Power Stage + Filter (Module IC)

E = Environment Category (single character)
Current Prohibited Material Usage Compliance Level:
"G" = D2Audio "Green Compliant"
"R" = RoHS Compliant (Pb-Free)
"P" = non-RoHS/non-Green Compliant

8.2 AVAILABLE PART NUMBERS



Part Number	Description
D2-91413-LR	9-Series Advanced PWM Controller with Integrated Digital Audio Engine, 4 channels, Full-Bridge, Feedforward and Feedback, Digital Amplifier Processor, 128-pin package, LQFP, RoHS Compliant (Pb-Free)
D2-91423-LR	9-Series Advanced PWM Controller with Integrated Digital Audio Engine, 4 channels, Half-Bridge, Feedforward or Feedback, Digital Amplifier Processor, 128-pin package, LQFP, RoHS Compliant (Pb-Free)
D2-91433-LR	9-Series Advanced PWM Controller with Integrated Digital Audio Engine, 4 channels, Half-Bridge, Feedforward only, Digital Amplifier Processor, 128-pin package, LQFP, RoHS Compliant (Pb-Free)

Table 10: Part Numbers and Feature Sets

PRELIMINARY

9 DOCUMENT REVISION HISTORY

09/08/05 Revision 0.0.1 - First Internal Release.
Converted from 814xx datasheet.

09/27/05 Revision 0.0.2 - Second Internal Release.
Updated Cover Page, fixed and updated block diagram, fixed and updated pinout diagram, updated pin descriptions, updated IC part numbering scheme.

10/20/05 Revision 0.0.3 - Third Internal Release.
Updated cover page, updated OTSEL pin description, removed internal pin names except for Serial Audio port, added 2-Wire interface section, added firmware and reference design disclaimers, updated BMS Table 9 on page 25, updated part numbers.

11/07/05 Revision 0.0.4 - Fourth Internal Release.
Added D2-91412-LR, D2-91422-LR, D2-91432-LR block diagrams, replaced SPI timing diagram, updated FDAT* pin table descriptions.

11/08/05 Revision 0.0.5 - Fifth Internal Release.
Updated D2-91413-LR, D2-91423-LR, D2-91433-LR part number instances.

2/15/06 Revision 1.0.0
Added Junction Temperature to Table 1, "Absolute Maximum Ratings," on page 9 in addition to Note 1 on Operating Temperature, Storage Temperature and Storage Temperature. Added Table 4, "Thermal Characteristics," on page 10 which shows Theta J_A values for 128-pin LQFP packages.

2/15/06 Revision 1.1.0
Updated Table 4, "Thermal Characteristics," on page 10 to include Theta J_C values for both 128-pinLQFP packages.

3/27/06 Revision 1.1.1
Updated Theta J_C values in Table 4, "Thermal Characteristics," on page 10.

PRELIMINARY

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