Analog Pulse Width Modulation Amplifier

Schematic Rev 3

PCB Rev B

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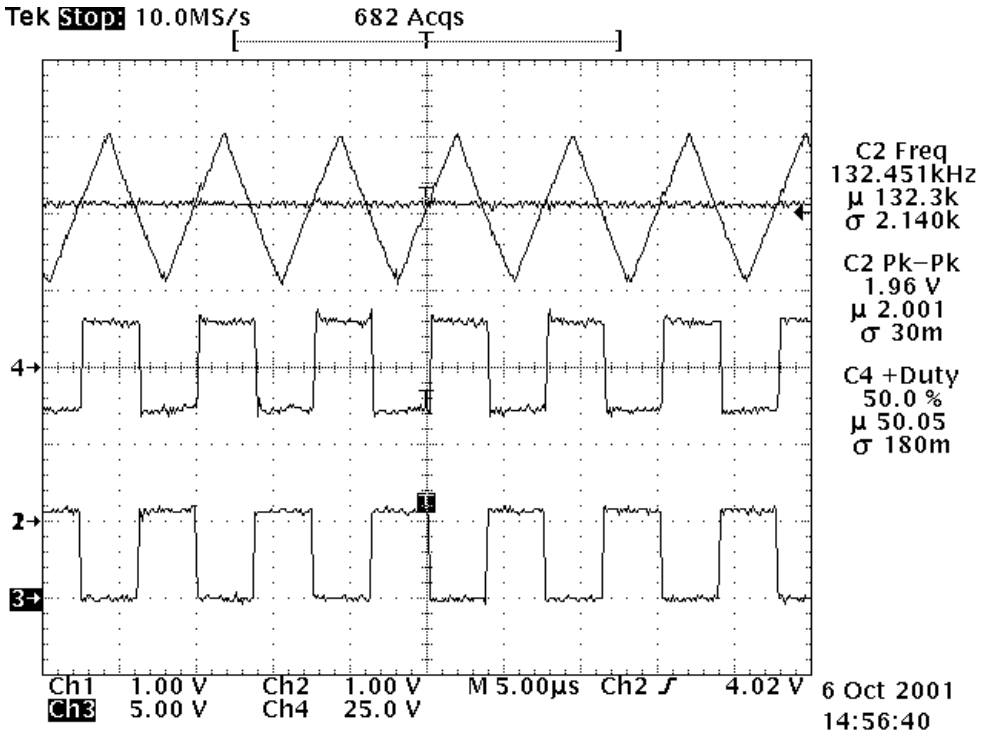
ECE 369 Lab Procedure:

BE SURE TO TURN OFF THE POWER WHEN MAKING ANY CONNECTIONS TO THE PWM AMP!!!

1. Set the power supply for approximately 14 V, with the current limit set to 1.5 A. Connect the power supply to the PWM AMP via a wire harness with a red MTA push-on header. Observe proper polarity. The PWM AMP is not extensively protected and reverse polarity could damage the amp.

2. Use the differential probe to connect the oscilloscope to the output of the bridge. Test points TP8 and TP9 provide access to the square wave bridge output. TP10 and TP11 provide access to the output. Observe polarity.

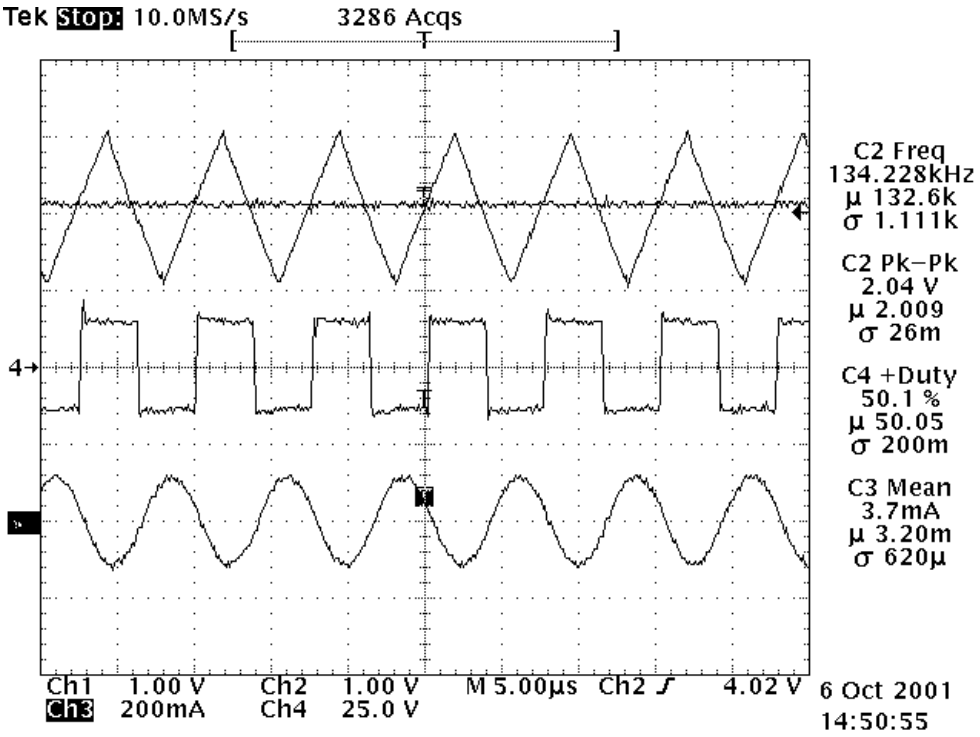
3. Connect a standard oscilloscope probe to TP1, TP2, TP3 to observe the modulating function, the carrier function, and the PWM output respectively. Turn on the supply and ensure the PWM AMP is functioning. You should see waveforms similar to those below. Plot *your* waveforms.



Top trace is the triangle function TP2 and vs. the unconnected input TP1.
Middle trace is the output of the bridge measured by the differential probe TP8 and TP9.
Bottom trace is the signal at TP3, the PWM out.

4. Adjust the triangle wave for a peak-to-peak voltage of about 2V (resistor R23). Adjust the duty ratio of the bridge output to 50% (resistor R5). Adjust the switching frequency to approximately 130 kHz (resistor R3).

5. Connect a resistive load, approximately 8 Ω to the output of the PWM AMP, and add a current probe to monitor the output current. Turn on the supply. You should see waveforms similar to those below. Plot *your* waveforms.



Top trace is the triangle function TP2 and vs. the unconnected input TP1.
Middle trace is the output of the bridge measured by the differential probe TP8 and TP9.
Bottom trace is the current out of the red banana jack.

6. Measure the average input current, and both the average and "ac" load voltage (after the filter). What would you expect the average voltage to be?

Modulating function input:

7. Set the function generator to a sine wave. Set the amplitude to match the peak to peak amplitude of the triangle function on your PWM AMP, and set the frequency to 1 kHz. Use the function generator as the input to the amplifier.

8. Observe the output at various values of the "volume" attenuator (resistor R6), including 0% and 100%.

9. When R6 is at about 75%, plot the modulating function, the carrier function, the bridge output (square pulse), and the current into the load together. Record the input average current, and both the average and "ac" load voltage (after the filter).

Audio source:

10. Connect an audio source to the amplifier input, with the volume at 0%. Connect a loudspeaker to the output jacks. Turn on the amplifier power supply.

11. Verify that the output of the output of the bridge is still a 50%-duty square wave. Set the volume at a comfortable level. Plot the modulating function, the carrier function, the bridge output (square pulse), and the current into the load together.

Dead-time gate drive signals:

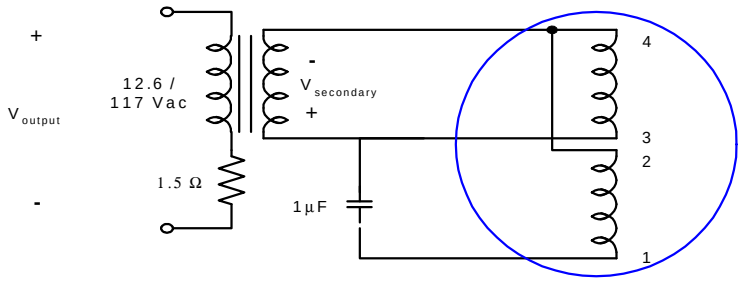
12. Connect a standard oscilloscope probe to each of the four gate drive signals TP4-TP7. Set the scope to display about 2 periods for each waveform. Identify the dead-time action. Measure and record the dead-time.

AC motor drive

13. Reconnect the amplifier for 19 V dc input, function generator 60 Hz ac input, and motor output. See the figure below. Initially, substitute a 1 kΩ resistor for the motor itself.

14. Turn on the power supply and adjust for effective operation at 60 Hz, with an output voltage close to the maximum available. **CAUTION: The output voltage can get high enough to cause a shock hazard!**

15. Turn off power and connect the motor in place of the resistor. Restore power. Observe the voltage of the secondary of the transformer, the motor current into terminal 4, and the motor operation as the "volume" setting and drive frequency are adjusted. Explore the range from about 30 Hz to about 180 Hz.



Theory of Operation:

Pulse width modulation, when used as the basis for an amplifier, is termed a “class D” or sometimes “class S” circuit. The principle is that the switch duty ratios can be made to follow any desired waveform, provided only that switching is fast. The duty ratio signal can be recovered with a simple low-pass filter step. The next few pages describe the configurations of a specific bridge PWM inverter intended for use as a class-D amplifier.

Power Supply:

The amplifier receives DC power through the 4 pin header J2. Pins are labeled as appropriate (see PCB plots attached). For general lab experimentation, the only voltage that you need to supply to the PWM AMP is V_{CC} (and ground). Depending on the desired amplitude of the output, V_{CC} can be selected within the range of $\mathbf{12 < V_{CC} < 20}$. Anything less than 12V will not be enough to power the ICs. Voltages above 20V will damage the FET driver ICs.

The PWM amplifier is designed both electrically and mechanically to interface with a small 12 V power supply. A piece of sheet steel may be needed as a barrier between the PWM AMP and the power supply. A solid ground connection between the PWM AMP circuit common and the power supply ground should be made. However, a lab power supply can be substituted for instructional purposes. Two series regulators provide regulated 12V and 5V for internal use within the amplifier circuit.

Analog input:

Analog input is supplied through the 3.5mm stereo headphone jack. Internally, the left and right channels are summed into a mono signal. The attenuator POT R6 is a 50K linear variable resistor that attenuates the applied input signal prior to the comparator. The input is ac coupled into the comparator stage through C2. R5 sets the dc bias (offset) on the analog input. Use this to adjust the input offset to compensate for any drift in the amplifier and to achieve a 50% output waveform for a 0V input. Turning R5 CW increases the DC bias.

Carrier and PWM Generation:

The triangle carrier function is generated by the LM566 VCO labeled U1 as seen on page 1 of the schematic. The frequency of the triangle carrier is set by C1 and R3. Turning R3 CW (clock

wise) increases the frequency. R23 sets the peak to peak amplitude of the triangle function. Turning R23 CW increases the amplitude.

General purpose comparator LM311 is used to create the PWM waveform by comparing the modulating function (analog input) with the carrier function (triangle waveform).

Dead-time circuit:

The PWM waveform resulting from the comparator stage is passed into the dead-time circuit comprised of U3 and U4 as seen on page 2 of the schematic. The result is two gate drive signals and their complement. These four gate drive signals ensure that one set of switches completely turns off before another set turns on. This break before make feature ensures that both switches in one leg of the H bridge output stage are not both on, eliminating the possibility for shoot through current and FET failure. The four gate signals are available on the orange test points TP4-TP7.

Soft-start circuitry (R15, C11, C22,C23) provides approximately a 200ms startup period to allow the power supply to stabilize before the bridge is allowed to run.

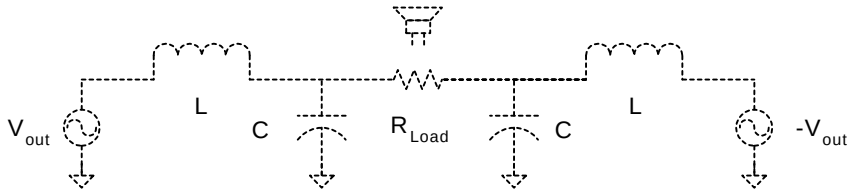
OUTPUT:

The output is derived from an "H bridge," based on the fact that the four FET switches are used in a geometry that resembles the letter H. Switches M1 and M4 operate as a one pair and M2 and M3 operate as the second pair. When M1 and M4 are on they provide a current path in the positive reference direction. When M2 and M3 are on, they provide a current path in the negative voltage reference. Thus the H bridge can supply both positive and negative output voltages from a single supply.

Low Pass Filtering:

The output square wave from the bridge is low-pass filtered by L1, L2, C19, and C20. The frequency response has a –3dB point at about 37.5 kHz and is characteristic of a 2 pole second order filter. See attached plot for the calculated complete frequency response of the output filter. For carrier frequencies above 100 kHz, the low pass filter should yield adequate performance and low standby ripple current.

Output Filter for Analog PWM AMP



$L := 20 \times 10^{-6}$ $C := 900 \cdot 10^{-9}$

$R_{Load} := 8$

$f_{-3db} = \dfrac{\dfrac{1}{\sqrt{L \cdot C}}}{2\pi} = 3.751 \times 10^{4}$

$\dfrac{\dfrac{R_{Load}}{L}}{2\pi} = 6.366 \times 10^{4}$

Full Bridge: KCL & KVL Equations

$$\frac{V_i - V_1}{j \cdot w \cdot L} = \frac{V_1}{\frac{1}{j \cdot w \cdot C}} + \frac{V_1 - V_2}{R_{Load}} \quad (1)$$

$$\frac{V_1 - V_2}{R_{Load}} = \frac{V_2}{\frac{1}{j \cdot w \cdot C}} + \frac{V_2 - (-V_i)}{j \cdot w \cdot L} \quad (2)$$

$$V_{out} = V_1 - V_2 \quad (3)$$

Substitute (3)

$$\frac{V_i - V_1}{j \cdot w \cdot L} = \frac{V_1}{\frac{1}{j \cdot w \cdot C}} + \frac{V_{out}}{R_{Load}}$$

Substitute (3)

$$\frac{V_{out}}{R_{Load}} = \frac{V_2}{\frac{1}{j \cdot w \cdot C}} + \frac{V_2 - (-V_i)}{j \cdot w \cdot L}$$

Solve for V_2

$$V_2 = -V_{out} + V_1$$

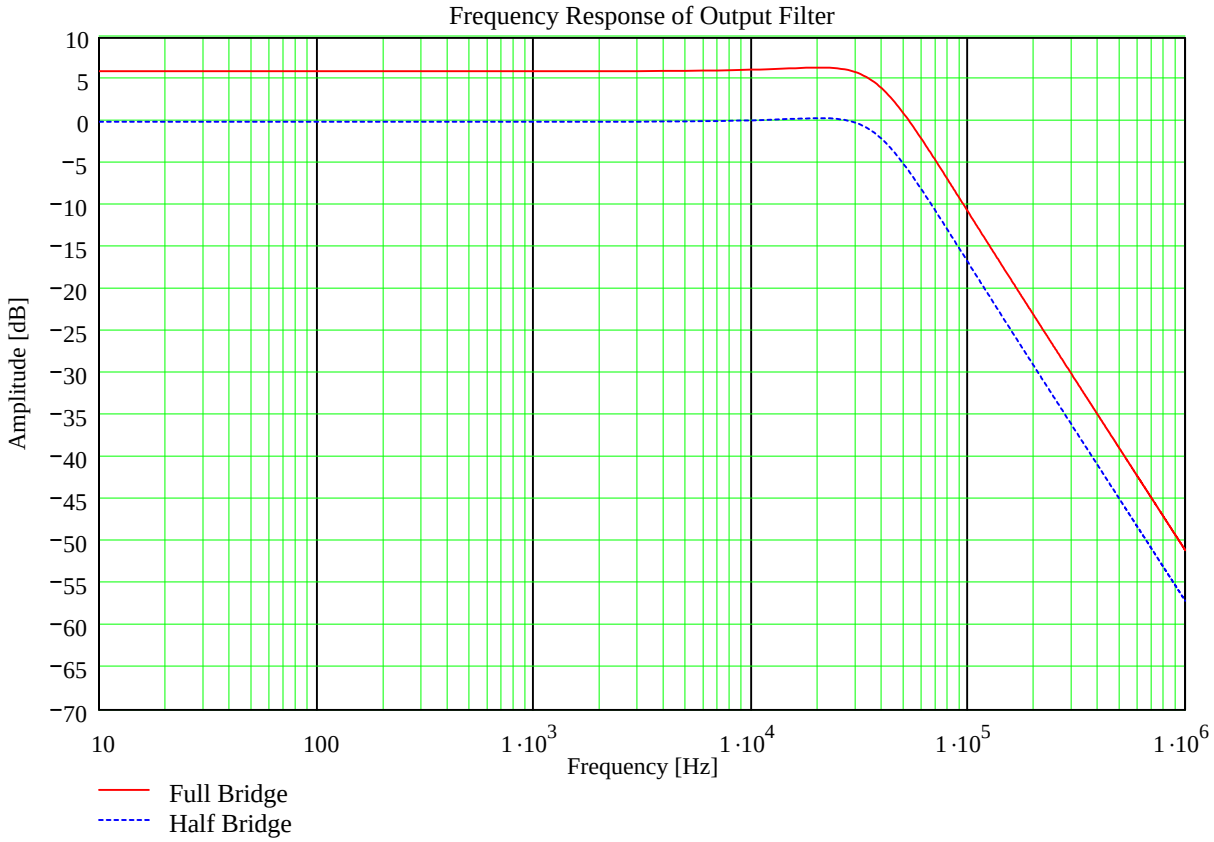
$$\frac{V_{out}}{V_i} = \frac{-2}{L \cdot C \cdot w^2 - \frac{2 \cdot i \cdot w \cdot L}{R_{Load}} - 1}$$

$$V_1 = -i \cdot \frac{\left(V_{out} \cdot w \cdot L + i \cdot w^2 \cdot C \cdot R_{Load} \cdot L \cdot V_{out} - i \cdot R_{Load} \cdot V_{out} + i \cdot R_{Load} \cdot V_i\right)}{R_{Load} \cdot \left(w^2 \cdot C \cdot L - 1\right)}$$

$$A(w) := 20 \cdot \log\left[\left|\frac{2}{1 + (j w)^2 \cdot L \cdot C + \frac{2 \cdot j \cdot w \cdot L}{R_{Load}}}\right|\right]$$

Half Ckt transfer function

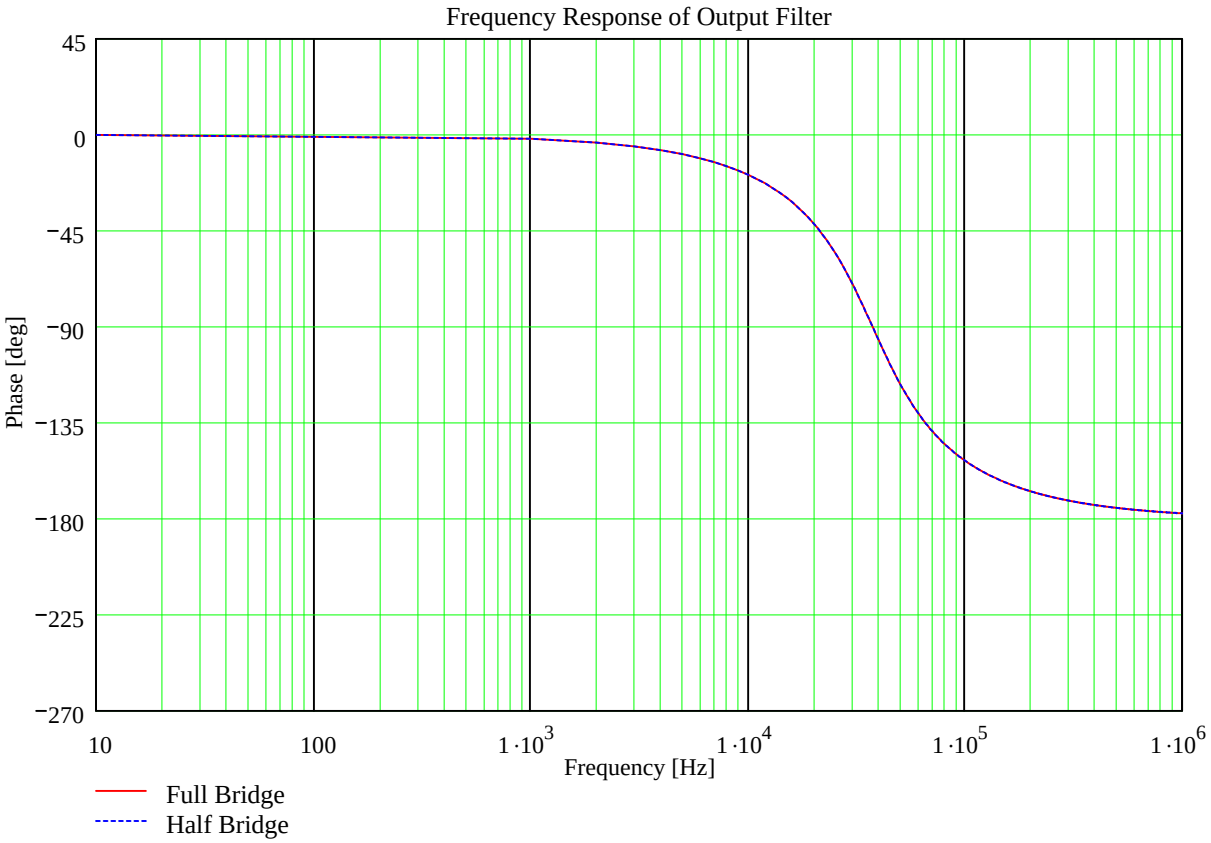
$$H(w) := 20 \cdot \log\left[\left|\frac{1}{1 + (j \cdot w)^2 \cdot L \cdot C + \frac{2 \cdot j \cdot w \cdot L}{R_{Load}}}\right|\right]$$

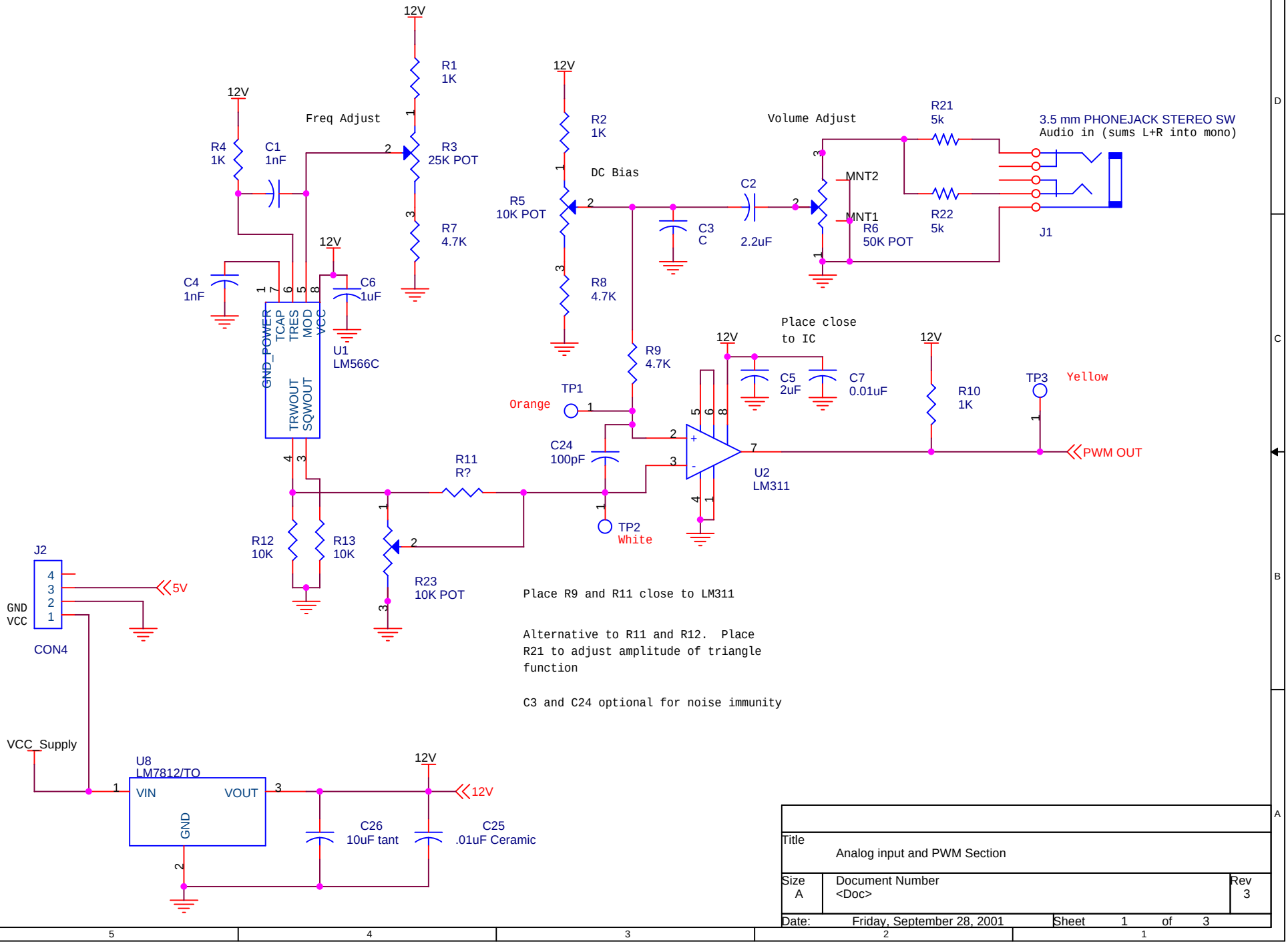


$$AP(w) := \frac{180}{\pi} \arg\left[\frac{2}{1 + (jw)^2 \cdot L \cdot C + \frac{2 \cdot j \cdot w \cdot L}{R_{Load}}}\right]$$

Half Ckt
transfer function

$$HP(w) := \frac{180}{\pi} \arg\left[\frac{1}{1 + (j \cdot w)^2 \cdot L \cdot C + \frac{2 \cdot j \cdot w \cdot L}{R_{Load}}}\right]$$





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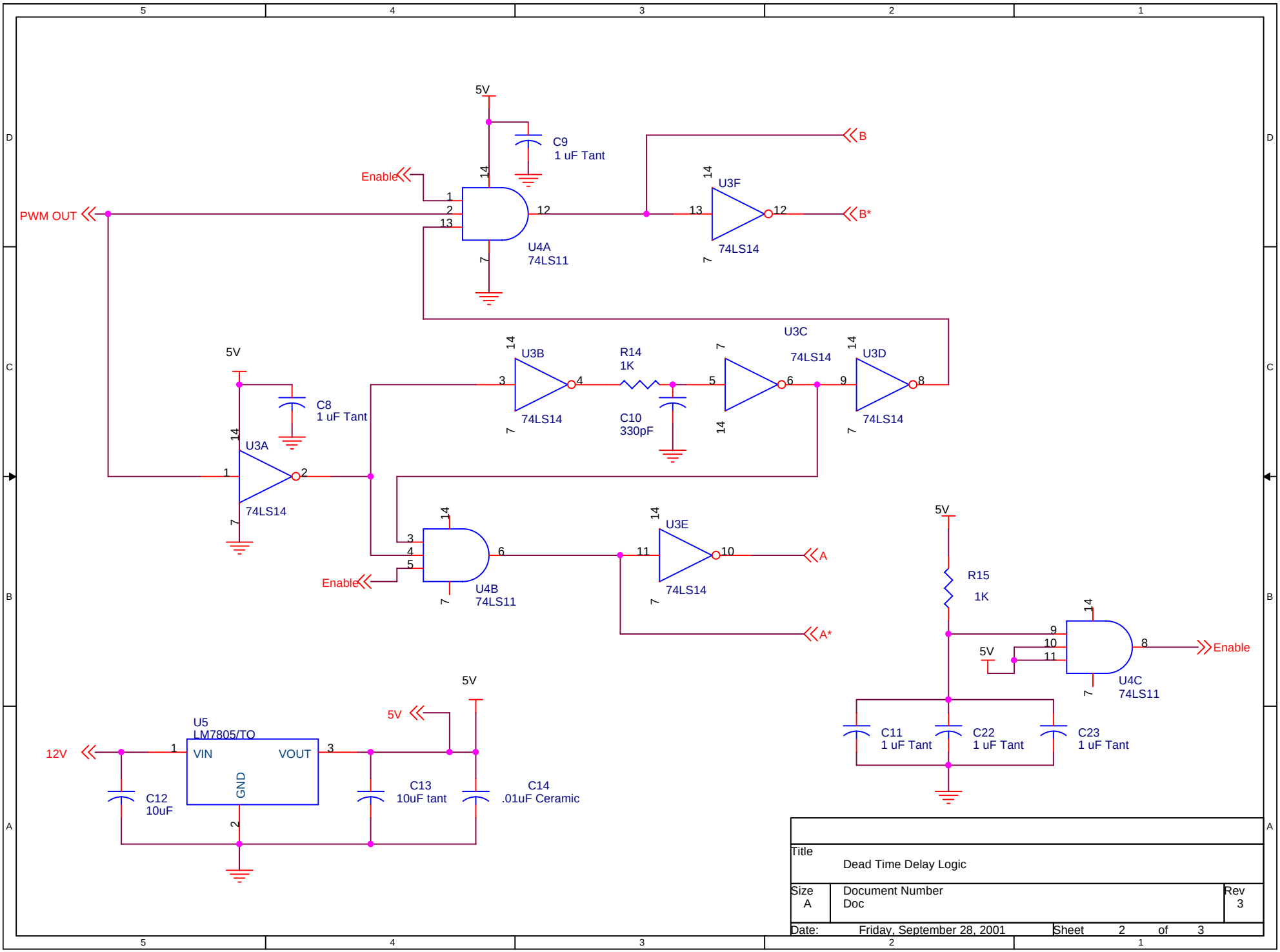
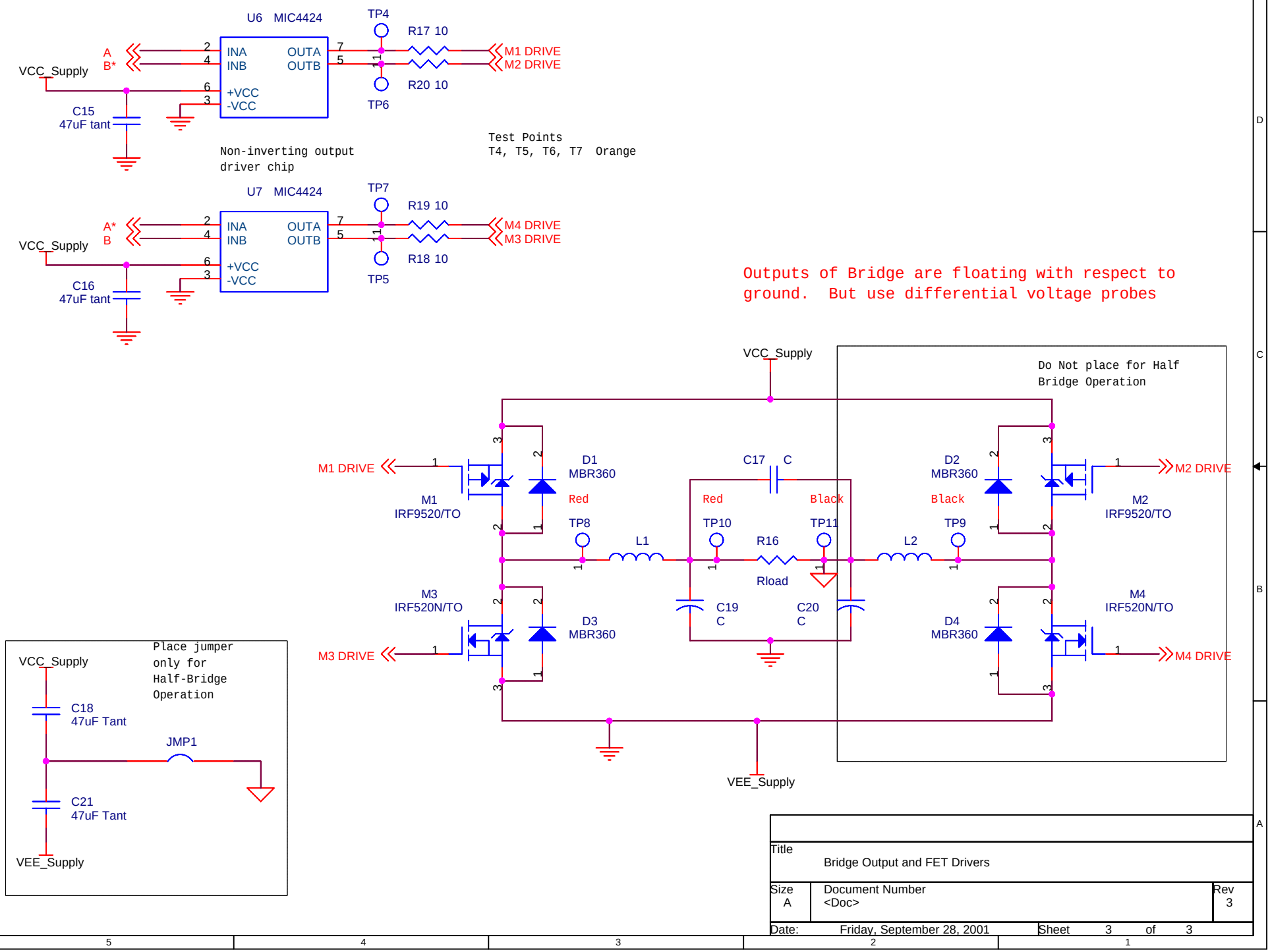
Size A	Document Number <Doc>	Rev 3
Date: Friday, September 28, 2001	Sheet 1 of 3	



Title	Dead Time Delay Logic	
Size A	Document Number Doc	Rev 3
Date: Friday, September 28, 2001	Sheet 2 of 3	



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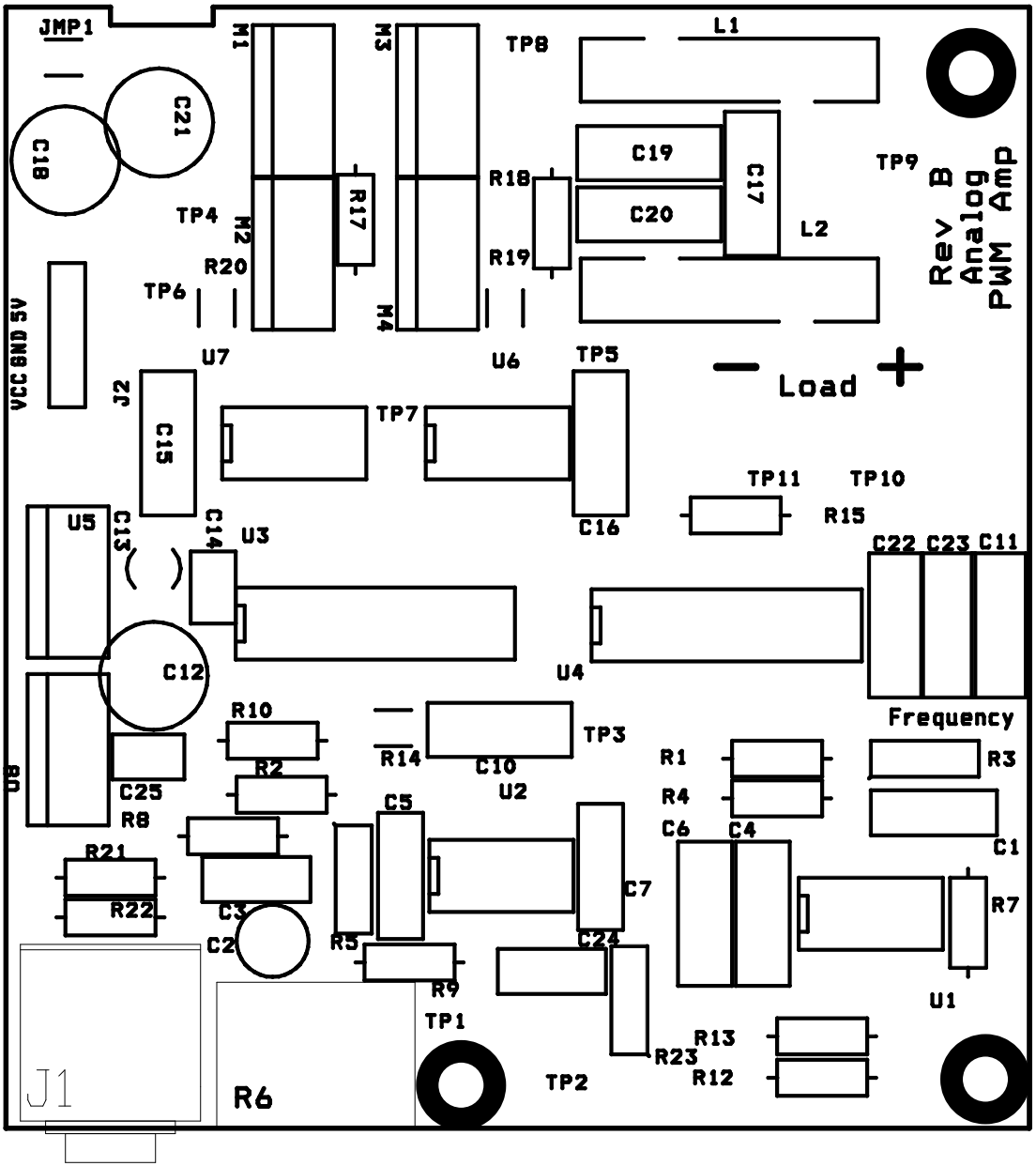
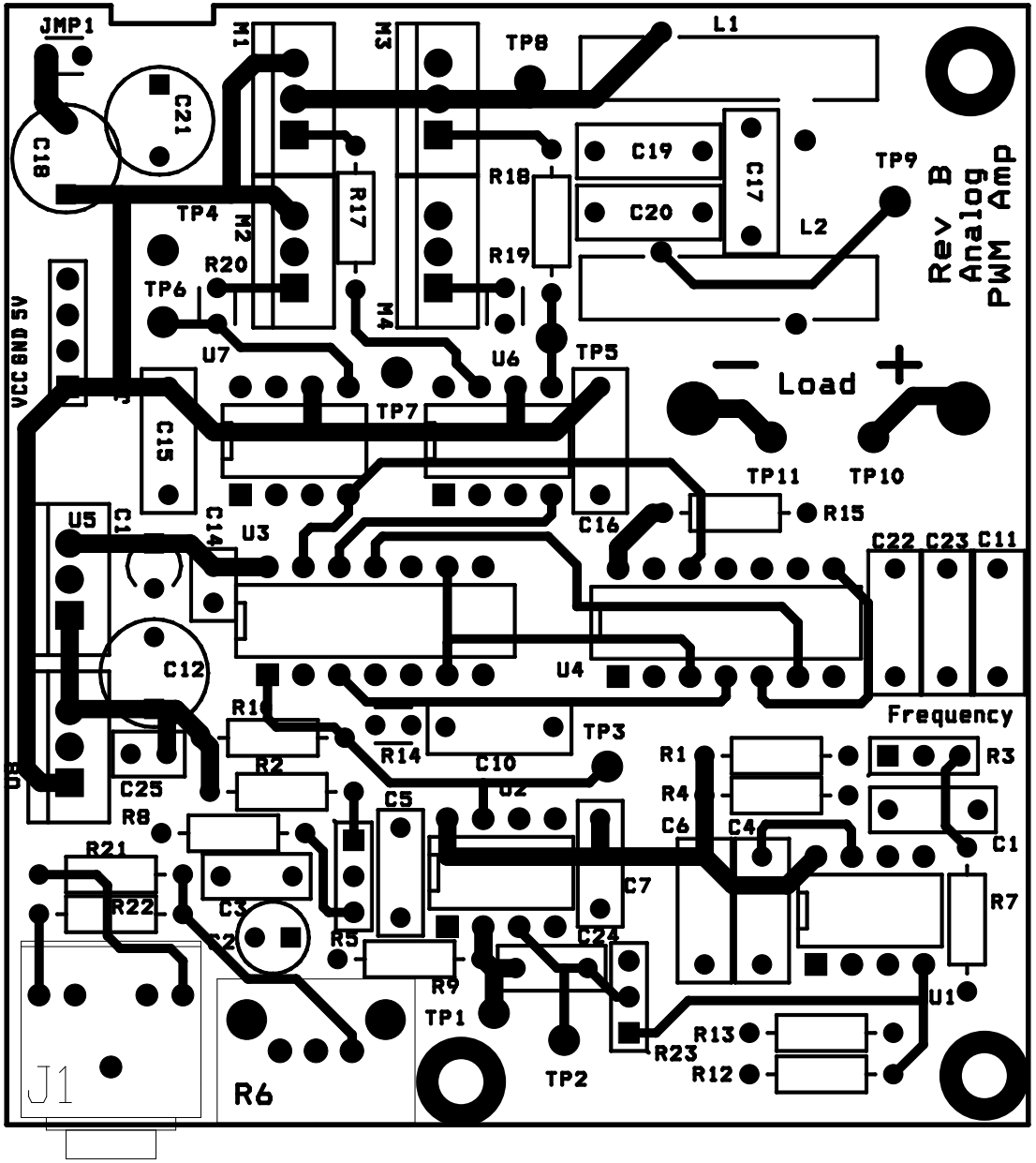
Size A	Document Number <Doc>	Rev 3
Date: Friday, September 28, 2001	Sheet 3 of 3	


JMP1
M1
M3
TP8
L1
C21
C18
C19
C17
TP9
Rev B
Analog
PWM Amp
TP4
M2
R17
R18
C20
L2
R20
R19
TP6
M4
VCC GND 5V
U7
U6
TP5
J2
Load
C15
TP7
TP11
TP10
U5
C13
C14
U3
R15
C22
C23
C11
C16
C12
U4
R10
TP3
Frequency
R14
C10
R1
R3
U8
R2
U2
R4
C25
R8
C5
C6
C4
C1
R21
C7
R7
R22
C3
C2
R5
C24
R9
U1
TP1
R13
J1
R23
TP2
R12
R6



JMP1
M1
M3
TP8
L1
C21
C18
C19
C17
TP9
R18
R17
C20
TP4
M2
L2
Rev B
Analog
PWM Amp
R20
R19
TP6
M4
VCC GND 5V
U7
U6
TP5
Load
TP7
C15
TP11
TP10
R15
U5
C1
C14
U3
C16
C22
C23
C11
C12
U4
Frequency
R1
TP3
R14
C10
R3
R2
R1
R4
C25
C5
U2
R8
C6
C4
C1
R21
C7
R7
R22
C3
C2
R5
C24
R9
U1
TP1
R13
R23
R12
TP2
J1
R6