AN1848

Class D Audio Amplifier Using PIC24FV16KM202

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INTRODUCTION

Class D amplifiers have become a popular audio amplifier topology due to their high efficiency and subsequent low cost. The high current output stage is implemented using binary switches, resulting in minimal heat generation and power loss. This allows for the power supply, heat sink and overall physical size of the amplifier to be minimized. Typical efficiency of a class D amplifier is over 90%, as opposed to 50% for a typical class AB amplifier. In an AB design, most of the inefficiency is a result of the output stage devices being required to operate in the linear region. As current flows though the devices, it is converted to heat instead of being delivered to the load.

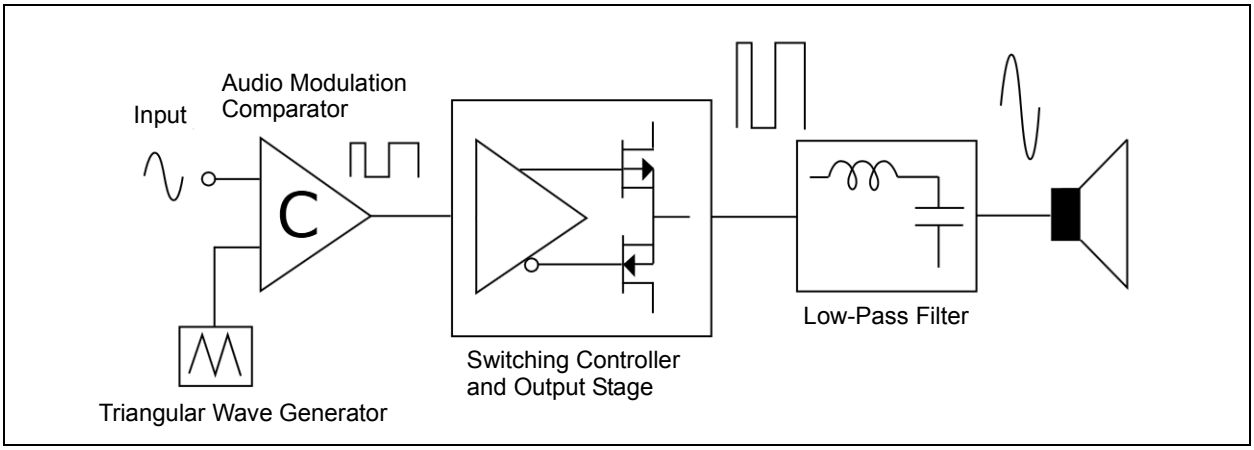
This application note provides a method to implement a class D amplifier using only the analog features of the PIC24FV16KM202 and minimal external components. This leaves the processor completely available for other application processes. The design presented is a single channel, full bridge (push-pull) Class D amplifier.

CLASS D TOPOLOGY OVERVIEW

A Class D audio amplifier is essentially a PWM amplifier. The input audio signal is used as the modulation reference for a PWM carrier. The resulting PWM signal is used to drive a higher power output stage, and filtered to recover the amplified audio. A class D amplifier is composed of 4 main functions as shown in Figure 1. These functions are:

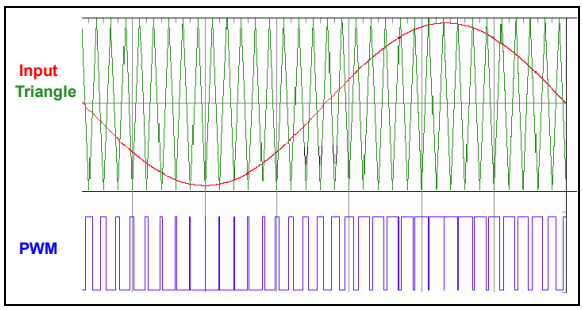
- Triangle wave generator
- Audio modulation comparator
- Switch controller and output stage
- Low pass filter

FIGURE 1: CLASS D AMPLIFIER BLOCK DIAGRAM



The analog audio signal is first compared to a high frequency triangle wave, using a comparator, to create a pulse waveform that is directly proportional to the instantaneous values of the audio signal. This results in a digital representation of the analog signal that can now be used to drive the output devices only in 'on' and 'off' states, as shown in Figure 2. Additional logic is used to produce the inverse of the digital signal to drive the complementary switch pair. Next, a switch controller provides signal timing and gate drive voltages for the output devices. The output switches provide voltage gain proportional to the supply voltage, and high current capability to drive the speaker coil. Finally, a low pass filter is used to remove the carrier frequency and recreate the analog audio signal.

FIGURE 2: CLASS D ANALOG AND DIGITAL WAVEFORMS



ANALOG INPUT STAGE

The incoming audio signal needs to be conditioned and filtered before it is compared to the triangle wave. A low pass filter should be used to prevent aliasing, and the level should be limited to below that of the triangle wave. The amplitude of the audio signal may need to be attenuated or amplified to match that of the comparator supplies and triangle wave amplitude. To improve signal-to-noise ratio, the peak level audio input should be as close to system full scale as possible. Depending on the application and loudspeaker to be driven, it may be beneficial to band limit the input signal. For example, if a small speaker is used that cannot produce tones below 100 Hz, the input should be high pass filtered to reduce wasted energy and possible speaker damage.

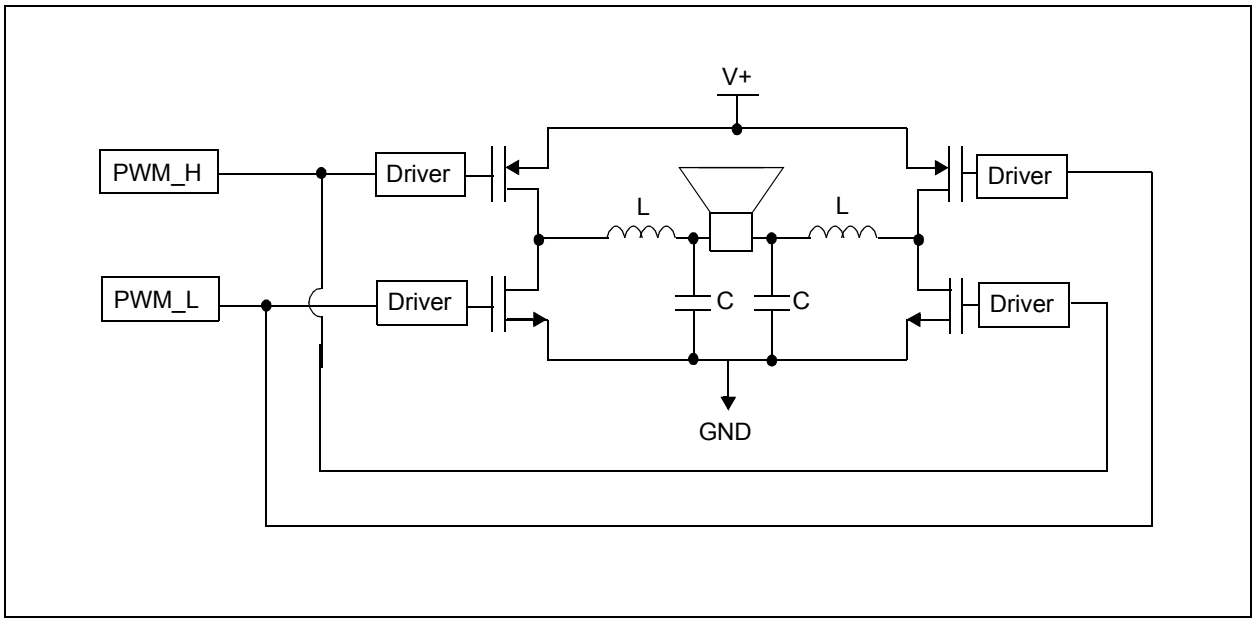
AMPLIFIER POWER SUPPLY CONSIDERATIONS

A stable DC power supply is important for a class D design. The power supply plays a critical role in the performance of the amplifier including gain, THD and noise. Class D amplifiers have little to no power supply noise rejection; any noise or voltage drops from loading will be passed on to the output. Due to the digital nature of the class D design, the power supply has to deliver large current transients each time the output devices switch. The power supply can also be affected from the energy storage elements in the low pass filter and loud speaker coil.

OUTPUT STAGE DESIGN

Using a full bridge output stage reduces the power supply's effect on performance degradation, and can be implemented with a single rail design. Some amount of 'dead time' is needed to prevent damaging current flow though the switches. Dead time is a delay in driving a switch high due to the capacitive settling effects of the output switch. This prevents both switches from being closed at the same time, effectively shorting V+ to GND. The amount of dead-time is dependent on the switches on/off delay, and will affect THD. A full bridge topology has reduced offset and THD compared to a half bridge, and can be implemented without a feedback circuit. When idle, the PWM duty cycle is 50% and the average voltage on both ends of the speaker coil is V+/2. Figure 3 shows a full bridge output design.

FIGURE 3: FULL BRIDGE OUTPUT CIRCUIT DIAGRAM



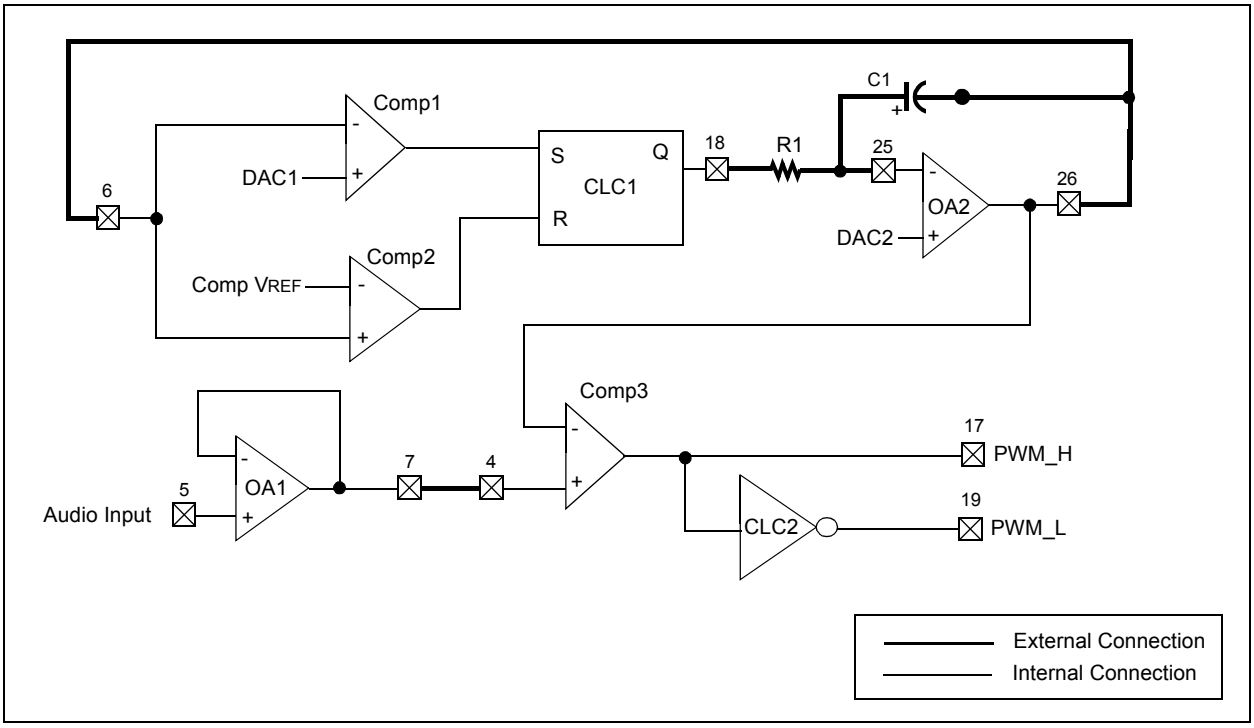
OUTPUT FILTER DESIGN

A typical class D output filter is a 2nd order L-C low pass filter with no resistive components to waste power. The filter cut off frequency should be at least four times lower than the switching frequency of the triangle generator. The application's speaker nominal impedance will guide the initial values of the inductors and capacitors. However, the speaker coil's own inductance and capacitance also interact with the filter elements and should be considered in the design. The power level of the amplifier and resulting current delivered though the filter guides the power rating of the filter elements. Lastly, some designs may have restrictions on radiated emissions (EMI). The filter design, physical location and trace routing need to be considered for best performance.

IMPLEMENTING A CLASS D AMPLIFIER USING THE PIC24FV16KM202

The PIC24FV16KM202 has a wide range of analog and digital peripherals that can be used to create an analog class D amplifier. The KM device also has configurable internal connections between the peripherals that reduce external PCB routing and free up I/O pins for other uses. The 'FV' variant of the KM family was chosen for its 5V operation, improving the signal-to-noise ratio of the system. The peripherals and connections used for the amplifier are shown in Figure 4.

FIGURE 4: PIC24FV16KM202 PERIPHERAL CONNECTIONS



Op amp OA1 is used as a buffer for the incoming audio signal. The triangle generator is implemented using a pair of comparators, a CLC module setup as an SR latch and an op amp configured as an integrator. The comparators are wired as a windowed comparator, with thresholds set by DAC1 and the comparator voltage reference. The windowed comparator's output is then converted to a square wave using the SR latch, and finally a triangle wave via the integration function of opamp1. The triangle wave is fed back to the window comparator completing the self resonator circuit. Comparator Comp3 creates the pulse waveform by comparing the triangle waveform to the audio input. CLC2 configured as an inverter provides the complement signal for the full bridge topology.

Comparators

Three comparators are used in the design. Comparator Comp1 and Comp2 function as a windowed comparator using the comparator voltage reference and DAC1 to set the voltage threshold levels. Comparator inputs C1INB and C2IND are chosen as they are on the same pin and do not need and external traces.

Comparator Comp3 is used to compare the audio signal to the triangle wave to create the digital PWM signal shown in Figure 2. Comparator input C3INA is chosen as it is on the same pin and op amp OA2's output.

Operational amplifiers

Op amp OA1 is utilized as a buffer for the incoming analog audio signal. It is set up as a voltage follower utilizing the selectable internal connection from the output to the inverting input. Optionally, op amp OA1 can be setup as a filter with or without gain. Op amp OA2 is used in the triangle generator as an integrator, with its output fed back to the window comparator to create an oscillator.

DACs

The Digital to Analog Converters (DACs) are used in a static state to provide a programmable DC voltage level for the triangle generator. DAC1 is internally connected to comparator 1's non-inverting input as the upper voltage threshold of the window comparator. DAC2 is internally connected to op amp OA2's non-inverting input and used to set the DC bias level, at 2.5V (V+/2).

Configurable logic Cells (CLCs)

The CLCs provide digital logic for the triangle wave generator and digital output. CLC1 is configured as an RS flip flop to create a single square wave from the window comparator's outputs. CLC1's inputs are internally connected to the comparator outputs. CLC2 is set up as an inverter to create a complementary PWM signal for the low side switches.

OTHER USES OF THE MICROCONTROLLER IN CLASS D AMPLIFIER DESIGN

The use of only the analog peripherals allows the microcontroller's processor and other peripherals to be available for use. Below are some examples of additional features that are specific to audio amplifiers.

Switch Mode Power Supply Control

The PIC24FV16KM202's Capture/Compare/PWM (MCCP and SCCP) and ADC peripherals are capable of controlling a switch mode power supply. The power supply can be used to boost DC voltages for higher amplifier output, or to convert line AC power to DC.

Thermal Overload and Over Current Protection

The PIC24FV16KM202's ADC or digital I/O can be used to sense the operational conditions of the amplifier and take action if needed. A temperature sensor can be used to measure amplifier output switch temperature and shut down the amplifier if a threshold is exceeded. If the speaker leads are accidentally shorted, the system can sense excessive current and shut down the amplifier. Indication of either of these conditions can be accomplished with I/O pins directly driving LEDs.

Automatic On/Off Sense

Some applications benefit from the ability to sense whether an audio input signal is present, and enable/disable the amplifier. This can be especially useful when there is no other way for the amplifier to communicate with the rest of the audio system. For low-power applications, the PIC24FV16KM202 can shut down the amplifier and put itself to sleep to conserve energy until it is needed again.

Remote Gain Control

User control of volume level is desired in some amplifier applications. The location of this remote control can be a long distance away and in a noisy environment where routing the audio signal there and back is not desired. One of the PIC24FV16KM202's several digital communication peripherals can be used to communicate to the remote control.

Audio Tone Generation

If the application has buttons or user inputs, it may be useful to use audio tones as confirmations. The PIC24FV16KM202's CCP peripheral can be used as a tone generator, and the output can be mixed into the audio signal with one of the op amps.

DESIGN DETAILS AND PERFORMANCE RESULTS

The design presented in Figure :A was built and its performance was evaluated. For ideal symmetry of the triangle wave, a frequency of 32 kHz was selected. To determine the R1 and C1 values for the integrator, the desired frequency and voltage amplitude are used as shown in Equation 1. For a nominal frequency of 32 kHz, 560 Ohms and 10 nf values were chosen. The triangle wave minimum and maximum voltage of 1V (V_{REF}) and 3.75V (DAC1) were chosen to sample an audio input amplitude of 2.5V, with a DC offset of 2.5V.

EQUATION 1: TRIANGLE GENERATOR INTEGRATOR FREQUENCY

$$F = \frac{1}{2 \cdot R1 \cdot C1 \cdot Vpk - pk}$$

where Vpk – pk = VDAC1 – V_{REF}

The system's upper frequency limit is set 2 octaves below the PWM frequency, at 8 kHz. The input band-pass filter is designed with corner frequencies of 60 Hz and 8.25 kHz. The output low pass LC filter is also designed with a corner frequency of 8 Khz, using the equations for a full bridge output show in Equation 2.

EQUATION 2: FULL BRIDGE LC OUTPUT FILTER EQUATIONS FREQUENCY

$$F = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C}}$$

For a critically damped alignment with Q of 0.707, L and C are:

$$C = \frac{1}{\pi \cdot f \cdot \sqrt{2}}$$

$$L = \frac{R \cdot \sqrt{2}}{4 \cdot \pi \cdot f}$$

Where R is speaker impedance

For an 8 Ohm speaker, standard C and L values of 3.3 µF and 100 µH results in a corner frequency of 8.7 kHz and a Q of 0.73.

With a 12 VDC power supply, the amplifier delivered 9 Watts into 8 Ohms with less than 1% THD. The resulting bandwidth is sufficient for most applications using a single, small to medium sized speaker. Alternatively, this Class D design can also be used for a subwoofer amplifier application.

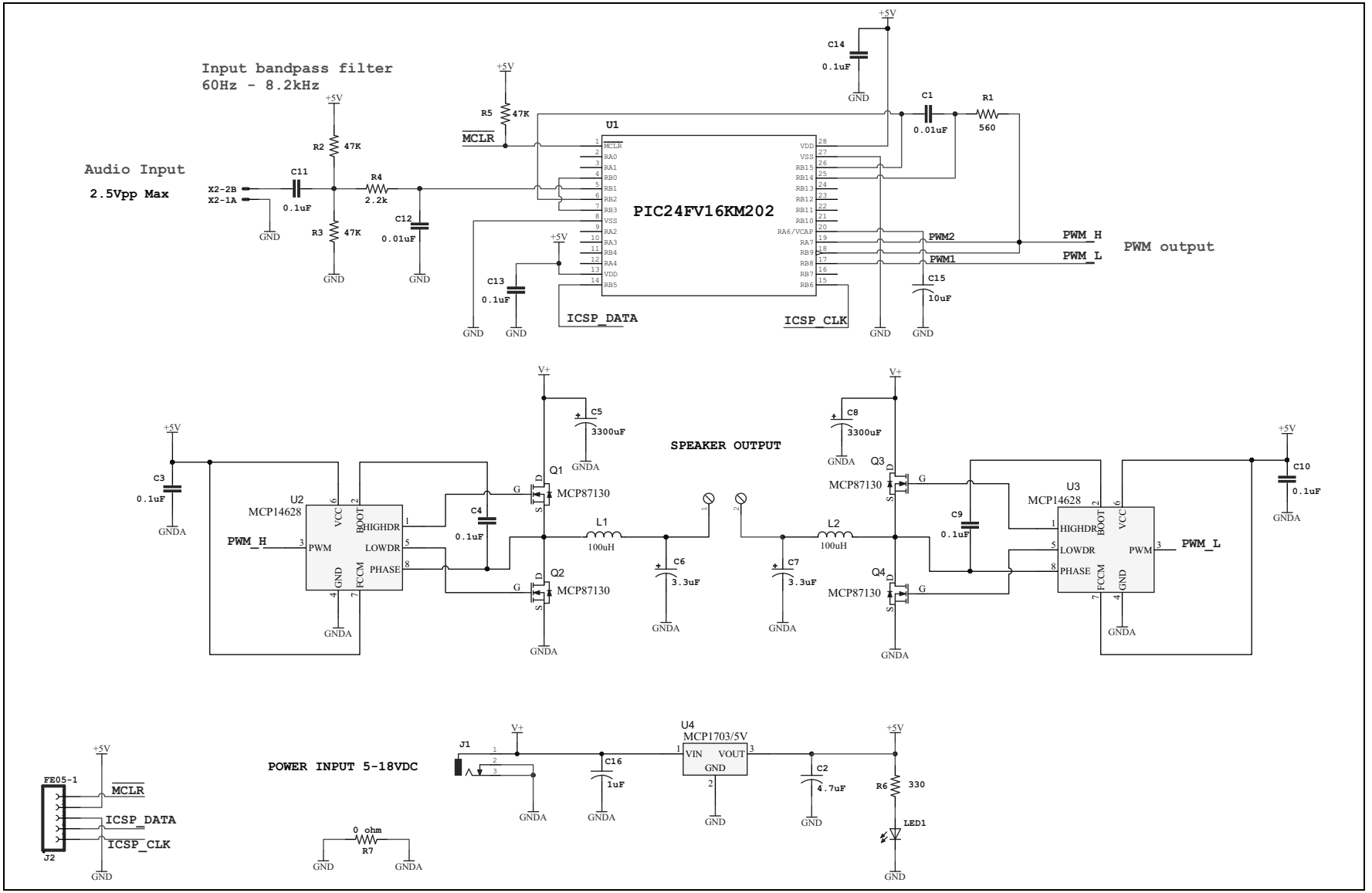
For additional information on Microchip power supply products and solutions, see:
http://www.microchip.com/intelligentpower/

CONCLUSION

The PIC24FV16KM202's wide range of analog and digital peripherals allows it to be used to create complete solutions including a class D amplifier. The internal connections between peripherals reduce the pin count needed for implementation, leaving the I/O pins available for other uses. Using the PIC24FV16KM202's peripherals instead of discrete components to realize a Class D design minimizes PCB area and overall cost.

APPENDIX A: SCHEMATICS

FIGURE A: PIC24FV16KM202 CLASS D AMPLIFIER



APPENDIX B: APPLICATION CODE

EXAMPLE 1: INITIALIZATION CODE

```
// Port setup for OpAmps
_TRISB1 = 1;              // OpAmp1 non-inverting input, Analog input, Pin 5
_ANSB1 = 1;
_TRISB3 = 1;              // OpAmp1 output, Analog input (see Errata), Pin 7
_ANSB3 = 1;

_TRISB15 = 1;             // OpAmp2 output, Analog input (see Errata)
_ANSB15 = 1;
_TRISB14 = 1;             // OpAmp2 inverting input, Analog input, Pin 25
_ANSB14 = 1;

// Port setup for Comparators
_TRISB2 = 1;              // Comparator 1 inverting input B, Analog input, Pin 6
_ANSB2 = 1;

_TRISB2 = 1;              // Comparator 2 inverting input D, Analog input, Pin 6
_ANSB2 = 1;

_TRISB0 = 1;              // Comparator 3 inverting input D, Analog input, Pin 4
_ANSB0 = 1;
_TRISB15 = 1;             // Comparator 3 non-inverting input A, Analog input, Pin 26
_ANSB15 = 1;
_TRISB8 = 0;              // Comparator 3 output, Analog output, Pin 17
_ANSB8 = 0;

// Port setup for CLCs
_TRISB9 = 0;              // CLC1, Digital ouptut, Pin 18
_ANSB9 = 0;

_TRISB7 = 0;              // CLC2, Digital output, Pin 19
_ANSB7 = 0;

// Port setup for DACs
_TRISB12 = 0;             // DAC1 Output, Analog output, Pin 23
_ANSB12 = 1;

// Comparator Reference initialization
CVRCONbits.CVRSS = 0;     // Use AVdd and AVss as reference source
CVRCONbits.CVR = 0x07;    // Comp Vref value select, 7 / 32 * 5V = 1.09V
CVRCONbits.CVREN = 1;     // Enable comparator voltage reference

// DAC1 initialization
DAC1CONbits.DACREF = 2;   // DAC Vref = AVdd
DAC1DAT = 192;            // Vout = 192 / 256 * 5V = 3.75 V
DAC1CONbits.DACOE = 0;    // Output disabled, use internal connection to comp2
DAC1CONbits.DACEN = 1;    // Enable DAC1
```

EXAMPLE 1: INITIALIZATION CODE (CONTINUED)

```
// DAC2 initialization
DAC2CONbits.DACREF = 2;     // DAC Vref = Avdd
DAC2CONbits.DACOE = 0;      // Output disabled, use internal connection to OA2
DAC2DAT = 128;              // Vout = 128 / 256 * 5V = 2.5V
DAC2CONbits.DACEN = 1;      // Enable DAC2

// Comparator initialization
CM1CONbits.CREF = 2;        // Connect non-inverting input to DAC1 output
CM1CONbits.CCH = 0;         // Connect inverting input  to C1INB (pin 6)
CM1CONbits.CPOL = 1;        // Invert output
CM1CONbits.COE = 0;         // Output disabled, use internal connection to CLC1
CM1CONbits.CON = 1;         // Enable Comparator 1

CM2CONbits.CREF = 1;        // Connect non-inverting input to comparator reference
CM2CONbits.CCH = 2;         // Connect inverting input to C2IND (pin 6)
CM2CONbits.COE = 1;         // Output disabled, use internal connection to CLC1
CM2CONbits.CON = 1;         // Enable Comparator 2

CM3CONbits.CREF = 0;        // Connect non-inverting input to C3INA (pin 26)
CM3CONbits.CCH = 2;         // Connect inverting input to C3IND (pin 4)
CM3CONbits.CPOL = 1;        // Invert output
CM3CONbits.COE = 1;         // Ouptut enabled
CM3CONbits.CON = 1;         // Enable Comparator 3

// CLC1 initialization (SR Latch)
CLC1CONL = 0x8083;         // CLC enabled, Output enabled, Mode = 3 (SR latch)
CLC1CONH = 0x0000;         // No Gate inversions
CLC1SELL = 0x0220;         // MUX 3 = Comp 2 output, MUX 2 = Comp 1 output
CLC1GLSL = 0x0008;         // Gate 1 = Data 2 (Comp 1)
CLC1GLSH = 0x0020;         // Gate 3 = Data 3 (Comp 2)

// CLC2 initialization (inverter)
CLC2CONL = 0x8081;         // CLC enabled, Output enabled, Mode = 1 (OR-XOR)
CLC2CONH = 0x0000;         // No Gate inversions
CLC2SELL = 0x2005;         // Data 4 = Comp 3 output, Data 1 = Logic 0
CLC2GLSL = 0x0040;         // Gate 1 = Data 4 (Comp 3, inverted)
CLC2GLSH = 0x0200;         // Gate 4 = Data 1 (logic 0).

// OpAmp 1 initialization (Audio buffer)
AMP1CONbits.SPDSEL = 1;     // High speed mode
AMP1CONbits.NINSEL = 5;     // OpAmp 1 negative input connected internally as voltage follower
AMP1CONbits.PINSEL = 1;     // OpAmp 1 positive input connected to OA1INA (pin 5)
AMP1CONbits.AMPEN = 1;      // Enable OpAmp

// OpAmp 2 initialization (Intergrator for triangle wave generator)
AMP2CONbits.SPDSEL = 1;     // High speed mode
AMP2CONbits.NINSEL = 2;     // OpAmp 1 negative input connected to OP2IND (pin 25)
AMP2CONbits.PINSEL = 5;     // OpAmp 1 positive input connected to DAC2 output
AMP2CONbits.AMPEN = 1;      // Enable OpAmp
```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