D2AUDIO XM100 DATA SHEET

Intelligent digital amplifier module for manufacturers of multi-room distributed audio systems

CONSUMER

PRELIMINARY

Complete Class-D Amplifier Solution
- D2Audio™ Intelligent Digital Controller IC, PWM Driver, MOSFET Output Stage and Output Filter in one package
- Designed for compliance with FCC, UL, CSA, CE

High-Performance Sound
- 100 watts per channel into 8 ohms [1]
- 3 or 4 zone versions (6 or 8 channels)
- >105 dB Dynamic Range
- <0.05% THD+N (8Ω, 1W, 20Hz to 20kHz)
- 20 Hz to 20 kHz, +/-0.5dB frequency response

93% Efficiency Reduces Heat and System Size
- Heat sink with thermally-controlled low noise variable RPM fan

Pure Digital Path
- 4 I²S audio inputs (32 -96 kHz, 16-24-bit)
- Simple controller interface for external microcontrollers
- Independent Sample Rate Conversion (SRC) on all digital inputs

Graceful Protection and Auto Recovery
- Complete short-circuit, thermal, over-current fault protection
- Graceful handling of complex and lower impedance loads

16x24 Zone Matrix Mixing
- D2 MultiMix™ 16x24 using 3 modules

Flexible Audio Configuration
- AudioSource Processing: Tone Control, Volume Control, 3 input and 5 output bands of Parametric EQ per channel
- Programmable compression per channel
- Master Volume Control

Advanced Audio Options
- High Performance Differential Analog Inputs
- Dual S/PDIF inputs
- D2 SPID™ automatic speaker identification
- D2 SPEQ™ automatic speaker equalization
- D2 Page-In™ assignable paging input
- D2Audio Canvas™ GUI; an intuitive point-and-click audio configuration utility for OEMs, ODMs, and system designers

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The D2Audio™ XM100 is a self-contained 100 watts per channel digital amplifier module for manufacturers of multi-room distributed audio systems. The XM100 contains a D2Audio intelligent, high-performance digital switching controller IC, PWM driver, MOSFET output stages and high-quality output filter stages. The module is housed in an EMI-shielded package and designed for compliance with FCC, UL, CSA, and CE requirements.

The XM100 is capable of driving up to 4 stereo zones (8 channels) at 100 watts into an 8-ohm load per FTC all channels driven.

The XM100 offers up to 8x8 Zone Matrix Mixing with optional D2 MultiMix for up to 16x24 Zone Matrix Mixing across three modules. Several advanced audio options include D2 SPID, D2 SPEQ, D2 Page-In, 8 channels of high-performance ADC, and dual S/PDIF digital audio inputs. The XM100 module provides configurable per channel audio processing including Parametric Equalization, Volume Control, Tone Control, and Dynamic Range Compression/Limiting.

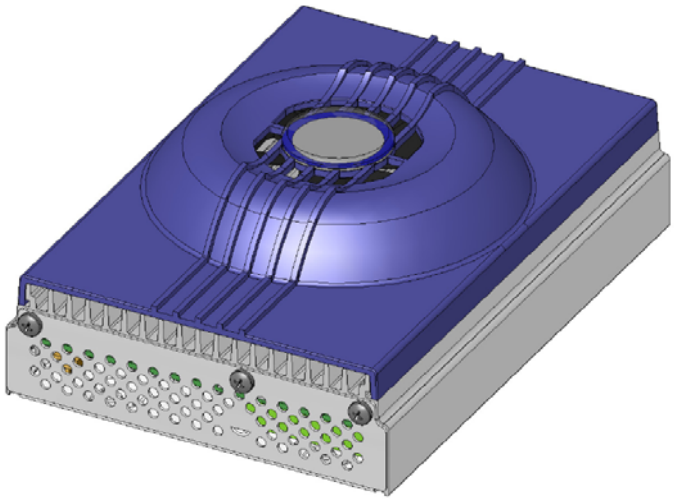
Included are up to 8-channels of digital audio inputs supporting I²S (16-24-bit, 32-96 kHz) format.

The XM100 module features D2Audio Canvas, a Windows application with an intuitive graphical user interface (GUI). "Point-and-click" options simplify audio configuration and avoid complex programming.

The amplifier may be configured to start and run automatically without requiring an external controller. For more advanced configurations a simple controller interface is provided.

D2AUDIO XM100

- **Complete digital amplifier for distributed audio systems**
- **D2Audio Intelligent Controller IC**
- **100 watts/channel[1]**
- **<.05% THD+N, >105dB SNR**
- **3 or 4 Zone versions**
- **Up to 16x24 zone matrix mixing w/optional D2 MultiMix**
- **Optional D2 SPID, D2 SPEQ, D2 Page-In, ADC, dual S/PDIF**
- **Pure digital audio signal path**
- **93% efficient**
- **Graceful protection /automatic fault recovery**



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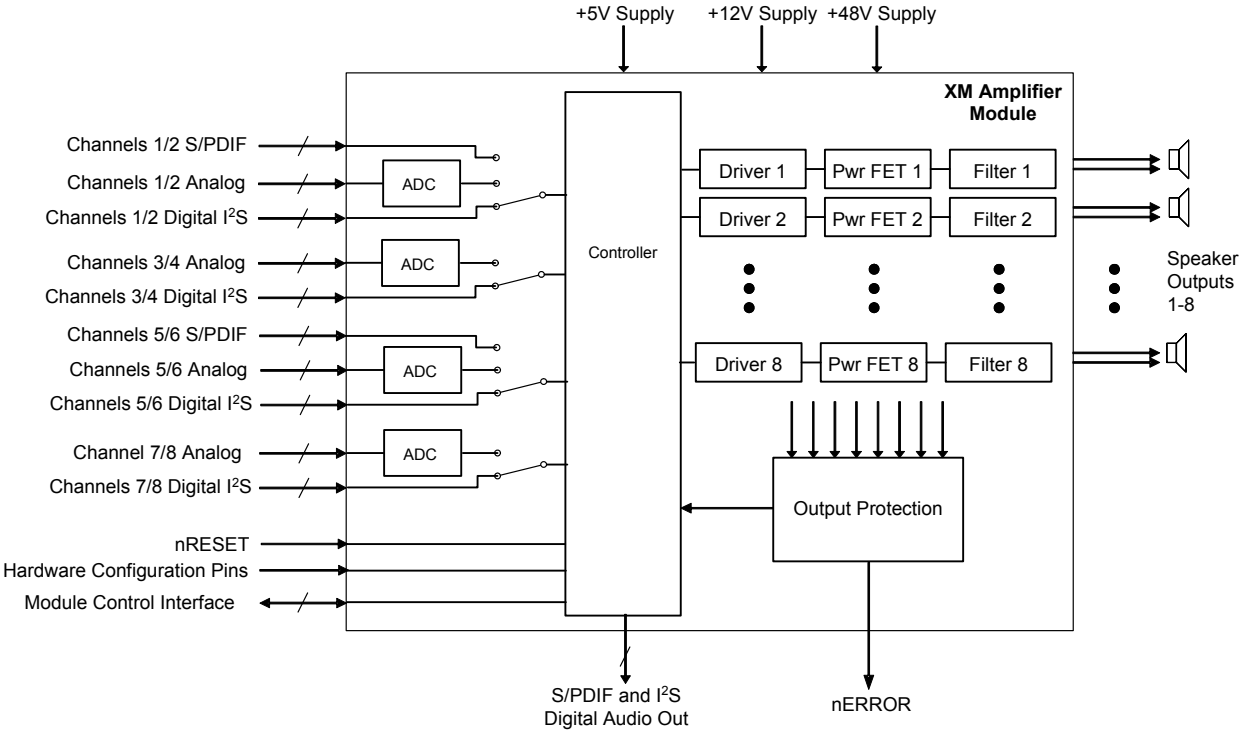

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D2Audio products are not authorized for use as critical components in life support systems, equipment used in hazardous environments or nuclear control systems without the express written consent of D2Audio Corporation.

1. FTC Testing Method

Product meets or exceeds FTC power testing method with all channels driven.

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1 SPECIFICATIONS

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1.1 ABSOLUTE MAXIMUM RATINGS

Parameter	Condition	Min	Max	Unit
High Voltage Supply	+48V DC Supply	0	50	V
Low Voltage Supply	+12V DC Supply	0	12.6	V
Signal Voltage Supply	+5V DC Supply	0	5.5	V
Digital Input Signal Level[1]	All inputs	-0.6	3.90	V
Analog Input Signal Level[2]	Peak voltage		5	V
Input Current, any pin but supplies			+/-10	mA
Nominal Operating Temperature Range[3]	Module ambient temperature Module heat sink temperature	-10 -10	45 60	°C
Absolute Operating temperature Range before Automatic Shutdown[4]	Module ambient temperature Module heat sink temperature		75 90	°C
Storage Temperature Range	Ambient temperature		105	°C
Lead Temperature	Soldering 10 Seconds		300	°C

Note 1: -0.6V undershoots and 3.9V overshoots allowed for 4ns maximum
Note 2: Analog inputs are AC coupled internally
Note 3: Normal Operation refers to running the unit in accordance with FTC test methods.
Note 4: Please refer to Figure 20, "Nominal Operating Range," on page 53 for the operating range and derating curves.

TABLE 1: Absolute Maximum Ratings

1.2 ELECTRICAL CHARACTERISTICS

T_A = 25° C, typical power supply, Ground = 0V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input low voltage	V_{IL}	All inputs			0.8	V
Input high voltage	V_{IH}	All inputs	2.3			V
Output low voltage	V_{OL}	4 mA Load			0.4	V
Output high voltage	V_{OH}	4 mA Load	2.4			V
Input leakage	I_L	Input Leakage - LRCK[3:0], SCLK[3:0], SDIN[3:0], SPDIFRX[1:0]			+/-10	uA
Input current	I_C	All digital inputs with resistive pulls - BOOT[2:0], MM_CONFIG[1:0], nRESET, nERROR, nERROR[x-x], PSSYNC, DIGx/ANL, SDA[1:0], SCL[1:0], SPDIFEN[1:0]			+/-0.4	mA
R_I	R_I	Analog input resistance - all analog audio inputs		20		kOhms Differential
Analog full scale	V_{IFS}	Differential analog input voltage to get full scale from ADC		2.0		Vrms Differential Sine Wave

TABLE 2: Electrical Characteristics

1.3 PERFORMANCE CHARACTERISTICS

Resistance load = 8Ω, T_A = 25°C, V_{+48V}=48V, V_{+12VDC}=12V, V_{+5VDC}=5V, Ground = 0V

Specification	Condition	Min	Typ	Max	Unit
Output Power	FTC All channels driven test method		100		W
Frequency Response	20 Hz to 20 kHz	-0.5		0.5	dB
Dynamic Range (digital inputs)			105		dB
Output Distortion (THD+N)	20 Hz to 20 kHz, 1W			0.05	%

TABLE 3: Performance Characteristics

1.4 DC POWER REQUIREMENTS

Resistance load = 8Ω, T_A = 25°C, V_{+48V}=48V, V_{+12VDC}=12V, V_{+5VDC}=5V, Ground = 0V

Symbol	Description	Min	Typ	Max	Unit
V_{+48V}	High Voltage Supply (HV)	0[1]	48	50	V
V_{+12VDC}	+12V Supply (LV)	11.5	12	12.6	V
V_{+5VDC}	+5V Supply (+5V)	4.75	5	5.5	V

Note 1: Amplifier operation with High Voltage supply less than the maximum will result in reduced output power. For operations where the High Voltage supply is less than the maximum limit, the output power can be approximated from the following formula, where HV is the high-voltage supply value, and R is the load impedance:

$$P = 0.43 \times \left(\frac{HV^2}{R}\right)$$

TABLE 4: DC Voltage Requirements

Symbol	Description	Min	Idle	Max	Unit
I_{HV}	High Voltage Supply Current, per channel	0[1]	0.035	2.5[3,4]	A
I_{LV}	+12V Supply Current()	0[1]	0.35[2]	0.40[3]	A
I_{+5V}	+5V Supply Current		0.850		A

Note 1: Minimum current measured with either the nRESET line asserted active-low, or the overload protection circuit activated for the particular channel

Note 2: Idle current measured with the amplifier in operation, but no input applied

Note 3: Maximum current measured with 1kHz sine wave output at rated power. The XM100 module is designed to meet FTC all channels driven specifications. Under normal conditions for most applications, all channels may not need to be driven at full power simultaneously. More typically, the power output requirement is 1/8 to 1/3 of the total amplifier output. However if the amplifier is allowed to be driven into high distortion ("clipping"), the power supply current may approach 20% more than required for a full scale output. It is therefore up to the system designer to determine how much power output will be allowed to be produced, and hence determine the maximum and average power supply current requirements.

Note 4: Current specification based on 8Ω loads under FTC all channels driven specification. For THX-Ultra 2, this specification may increases to 12.5A for specific loads and test conditions.

TABLE 5: DC Current Requirements

1.5 SWITCHING CHARACTERISTICS - SERIAL AUDIO PORT

T_A = 25°C, V_{+48V}=48V, V_{+12VDC}=12V, V_{+5VDC}=5V, Ground = 0V,Sample Rate 32kHz-96kHz

Symbol	Description	Min	Typ	Max	Unit
t_cSCLK	SCLK frequency			12.5	MHz
t_wSCLK	SCLK pulse width (high and low)	40			ns
t_sLRCLK	LRCLK setup to SCLK rising	20			ns
t_hLRCLK	LRCLK hold from SCLK rising	20			ns
t_sSDI	SDIN setup to SCLK rising	20			ns
t_hSDI	SDIN hold from SCLK rising	20			ns
t_dSDO	SDO delay from SCLK falling			20	ns

TABLE 6: Serial Audio Port Timing

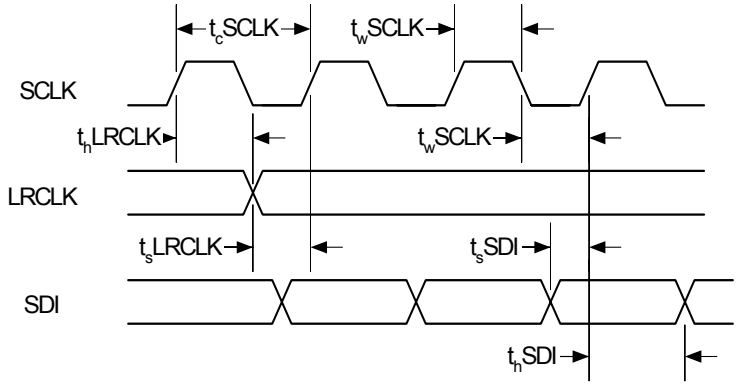

FIGURE 1: Serial Audio Port Timing

1.6 SWITCHING CHARACTERISTICS - PSSYNC PIN

T_A = 25°C, V_{+48V}=48V, V_{+12VDC}=12V, V_{+5VDC}=5V, Ground = 0V

Description	Min	Typ	Max	Unit
PSSYNC Frequency		384		kHz
PSSYNC Duty Cycle		50		%

TABLE 7: PSSYNC Pin Characteristics

1.7 SWITCHING CHARACTERISTICS - MODULE CONTROL INTERFACE

T_A = 25°C, V_{+48V}=48V, V_{+12VDC}=12V, V_{+5VDC}=5V, Ground = 0V

Symbol	Description	Min	Max	Unit
fSCL	SCL frequency		100	kHz
t_{buf}	Bus free time between transmissions	4.7		us
t_wSCL	SCL clock low	4.7		us
t_wSCL	SCL clock high	4.0		us
t_sSTA	Setup time for a (repeated) Start	4.7		us
t_hSTA	Start condition Hold time	4.0		us
t_hSDA	SDA hold from SCL falling (see note)	0		us
t_sSDA	SDA setup time to SCL rising	250		ns
t_dSDA	SDA delay time from SCL falling		3.5	us
t_r	Rise time of both SDA and SCL		1	us
t_f	Fall time of both SDA and SCL		300	ns
t_sSTO	Setup time for a Stop condition	4.7		us
Note: Data must be held sufficient time to bridge the 300ns transition time of SCL				

TABLE 8: Module Control Interface Port Timing

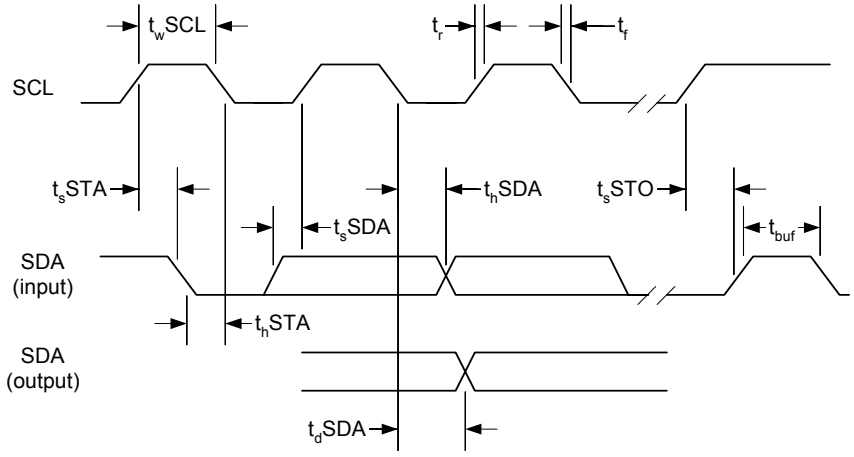

FIGURE 2: Module Control Interface Timing

1.8 PERFORMANCE PLOTS

The following graphs show the amplifier performance. All inputs are driven with the same input signal, all inputs are mapped to their respective outputs. The output channels are tested one at a time and only the output channel being measured is terminated with an 8-ohm load. The other outputs are open.

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1.8.1 FREQUENCY RESPONSE AT 1W (8 OHM LOAD)

Conditions: Typical supplies, Room temperature, 1W output power, 1channel

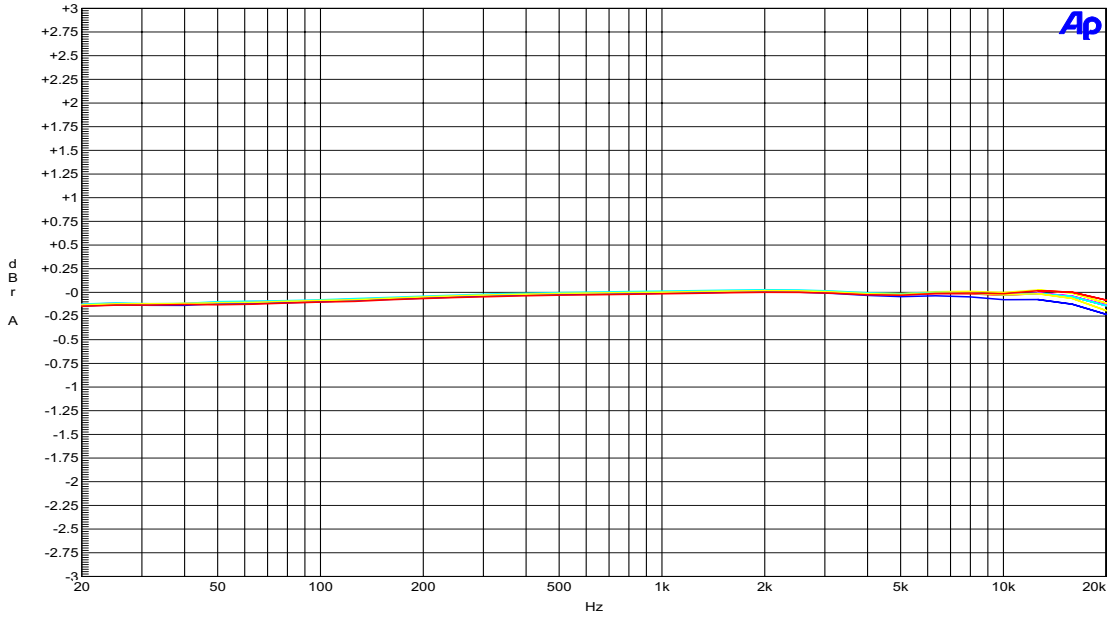


FIGURE 3: Frequency Response

1.8.2 THD+N VS. FREQUENCY (8 OHM LOAD)

Conditions: Digital input, typical supplies, Room temperature, 1W (blue trace) and 100W (green trace) output power

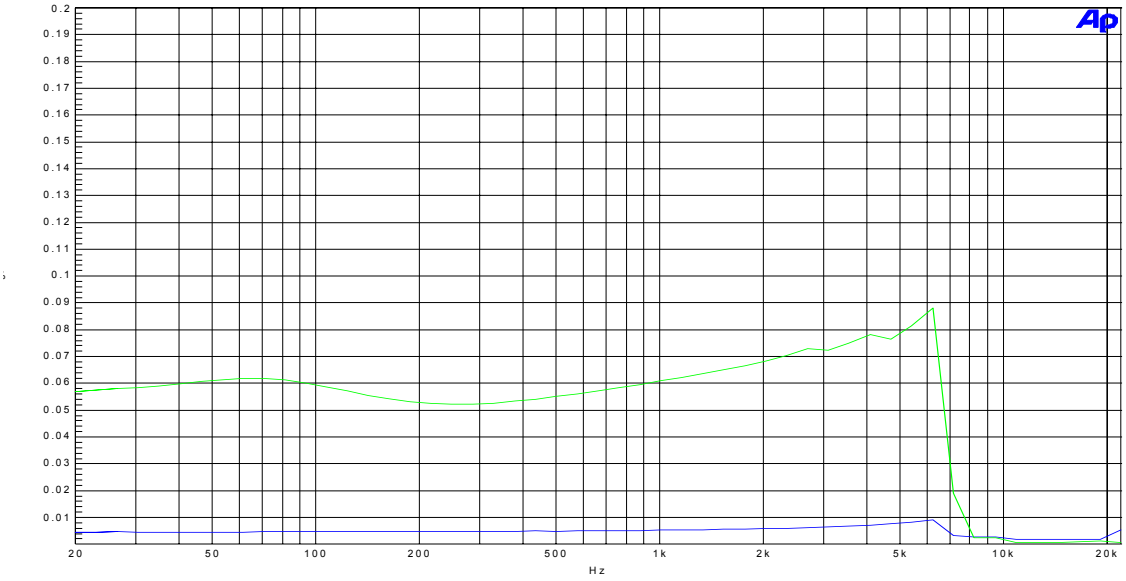


FIGURE 4: THD+N vs. Frequency

1.8.3 THD+N VS. OUTPUT POWER (8 OHM LOAD)

Conditions: Typical supplies, Room temperature, 1kHz digital input

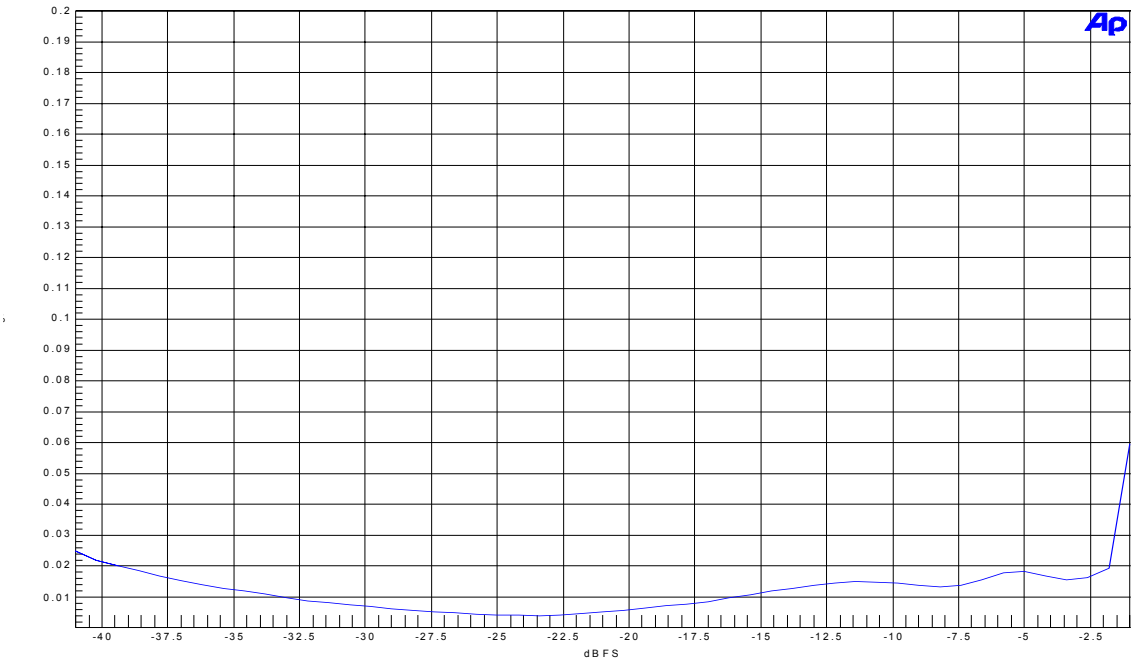


FIGURE 5: THD+N vs. Power

1.8.4 NOISE FLOOR (8 OHM LOAD)

Conditions: Typical supplies, Room temperature, no input

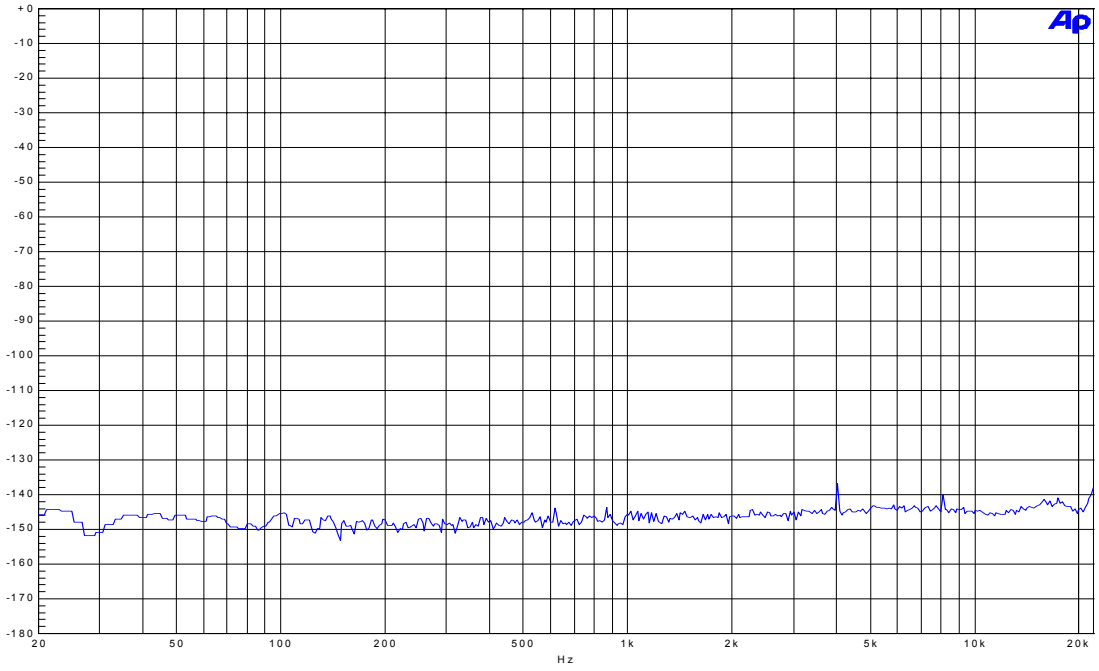
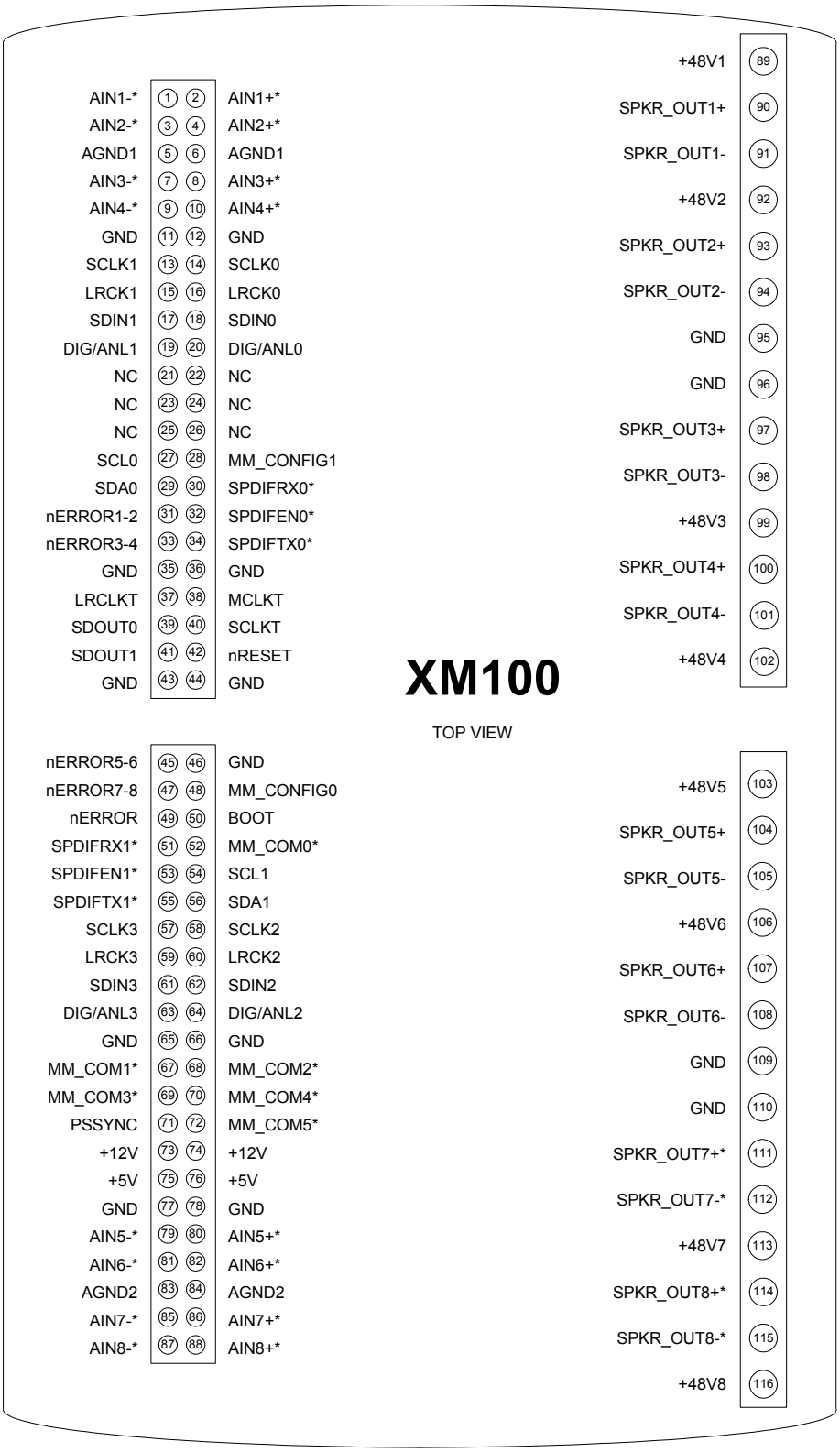


FIGURE 6: Noise Floor

2 MODULE PINOUT



* Pins denoted with * are optional based on part number. Leave unconnected if not used.

FIGURE 7: XM100 Amplifier Pinout

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2.1 PIN DEFINITION

Pin #	Pin Name	I/O	Description
37	LRCLKT	O	Left/right clock output
38	MCLKT	O	Master clock output
40	SCLKT	O	Serial data clock output
39	SDOUT0	O	Serial output data 0
41	SDOUT1	O	Serial output data 1
30	SPDIFRX0	I	S/PDIF receiver input 0
34	SPDIFTX0	O	Downmixed S/PDIF output 0
51	SPDIFRX1	I	S/PDIF receiver input 1
55	SPDIFTX1	O	Downmixed S/PDIF output 1
16	LRCK0	I	Channel 1/2 left/right clock
14	SCLK0	I	Channel 1/2 serial data bit clock
18	SDIN0	I	Channel 1/2 input data
15	LRCK1	I	Channel 3/4 left/right clock
13	SCLK1	I	Channel 3/4 serial data bit clock
17	SDIN1	I	Channel 3/4 input data
60	LRCK2	I	Channel 5/6 left/right clock
58	SCLK2	I	Channel 5/6 serial data bit clock
62	SDIN2	I	Channel 5/6 input data
59	LRCK3	I	Channel 7/8 left/right clock
57	SCLK3	I	Channel 7/8 serial data bit clock
61	SDIN3	I	Channel 7/8 input data

TABLE 9: Digital Audio Signal Pins

Pin #	Pin Name	I/O	Description
2	AIN1+	I	Channel 1 positive analog input
1	AIN1-	I	Channel 1 negative analog input
4	AIN2+	I	Channel 2 positive analog input
3	AIN2-	I	Channel 2 negative analog input
8	AIN3+	I	Channel 3 positive analog input
7	AIN3-	I	Channel 3 negative analog input
10	AIN4+	I	Channel 4 positive analog input
9	AIN4-	I	Channel 4 negative analog input
80	AIN5+	I	Channel 5 positive analog input
79	AIN5-	I	Channel 5 negative analog input
82	AIN6+	I	Channel 6 positive analog input
81	AIN6-	I	Channel 6 negative analog input
86	AIN7+	I	Channel 7 positive analog input
85	AIN7-	I	Channel 7 negative analog input
88	AIN8+	I	Channel 8 positive analog input
87	AIN8-	I	Channel 8 negative analog input

TABLE 10: Analog Input Pins

Pin #	Pin Name	I/O	Description
50	BOOT	I	Boot select control
49	nERROR	O	Overall amplifier error indication, active low
31	nERROR1-2	O	Channels 1/2 amplifier error indication, active low
33	nERROR3-4	O	Channels 3/4 amplifier error indication, active low
45	nERROR5-6	O	Channels 5/6 amplifier error indication, active low
47	nERROR7-8	O	Channels 7/8 amplifier error indication, active low
42	nRESET	I	Amplifier reset, active low, Open Collector Drive
71	PSSYNC	O	Power supply sychronization clock
20	DIG/ANL0	I	Input select, channels 1/2
19	DIG/ANL1	I	Input select, channels 3/4
64	DIG/ANL2	I	Input select, channels 5/6
63	DIG/ANL3	I	Input select, channels 7/8
27	SCL0	I/O	Module control interface clock- channels 1-4
29	SDA0	I/O	Module control interface data- channels 1-4
54	SCL1	I/O	Module control interface clock- channels 5-8
56	SDA1	I/O	Module control interface data- channels 5-8
32	SPDIFEN0	I	S/PDIF enable receiver 0
53	SPDIFEN1	I	S/PDIF enable receiver 1

TABLE 11: Module Control Interface Signal Pins

Pin #	Pin Name	I/O	Description
90	SPKR_OUT1+	O	Channel 1 Positive Loudspeaker Output
91	SPKR_OUT1-	O	Channel 1 Negative Loudspeaker Output
93	SPKR_OUT2+	O	Channel 2 Positive Loudspeaker Output
94	SPKR_OUT2-	O	Channel 2 Negative Loudspeaker Output
97	SPKR_OUT3+	O	Channel 3 Positive Loudspeaker Output
98	SPKR_OUT3-	O	Channel 3Negative Loudspeaker Output
100	SPKR_OUT4+	O	Channel 4 Positive Loudspeaker Output
101	SPKR_OUT4-	O	Channel 4Negative Loudspeaker Output
104	SPKR_OUT5+	O	Channel 5Positive Loudspeaker Output
105	SPKR_OUT5-	O	Channel 5 Negative Loudspeaker Output
107	SPKR_OUT6+	O	Channel 6 Positive Loudspeaker Output
108	SPKR_OUT6-	O	Channel 6 Negative Loudspeaker Output
111	SPKR_OUT7+	O	Channel 7 Positive Loudspeaker Output
112	SPKR_OUT7-	O	Channel 7 Negative Loudspeaker Output
114	SPKR_OUT8+	O	Channel 8 Positive Loudspeaker Output
115	SPKR_OUT8-	O	Channel 8 Negative Loudspeaker Output

TABLE 12: Loudspeaker Output Pins

Pin #	Pin Name	I/O	Description
28, 48	MM_CONFIG[1:0]	I	Master/slave/listener selection
52, 67:70, 72	MM_COM[5:0]	I/O	Multi-module serial data communication

TABLE 13: Multi-module Communication Pins

Pin #	Pin Name	I/O	Description
5:6	AGND1	-	Analog ground for analog inputs 1-4
83:84	AGND2	-	Analog ground for analog inputs 5-8
11:12, 35:36, 43:44, 4665:66, 77:78, 95:96, 109:110	GND	-	General purpose ground
89	+48V1	-	+48 VDC High Voltage Power Channel 1
92	+48V2	-	+48 VDC High Voltage Power Channel 2
99	+48V3	-	+48 VDC High Voltage Power Channel 3
102	+48V4	-	+48 VDC High Voltage Power Channel 4
103	+48V5	-	+48 VDC High Voltage Power Channel 5
106	+48V6	-	+48 VDC High Voltage Power Channel 6
113	+48V7	-	+48 VDC High Voltage Power Channel 7
116	+48V8	-	+48 VDC High Voltage Power Channel 8
73:74	+12VDC	-	+12 VDC Power
75:76	+5VDC	-	+5 VDC Power

TABLE 14: Power Supply Pins

Pin #	Pin Name	I/O	Description
21:26	NC	-	No Connect- leave unconnected on PCB. Note that some pins have optional functionality, based on part number. If these pins are not used, leave them unconnected.

TABLE 15: No Connect Pins

2.2 PIN DESCRIPTION

2.2.1 DIGITAL SERIAL AUDIO INPUTS (SAI PORTS)

LRCK[3:0] **Left/Right Clock**

These pins are the framing clocks for the respective Serial Data Inputs. The serial input data is transmitted as two channels every sample rate period. LRCK determines the start of each data pair. The LRCK frequency determines the input sample rate (Fs). LRCK is a 3.3 volt input.

SCLK[3:0] **Shift Clock**

These pins are the Shift Clock input for the respective Serial Data Inputs. The serial clock is used to frame each input bit of the serial input data. The shift clock frequency is typically 64*Fs. SCLK is a 3.3 volt input.

SDIN[3:0] **Serial Data Input**

These pins are the serial data inputs. Serial Data inputs are arranged as four left/right input pairs. The input format options are I^2S or Left Justified. 16, 18, 20, and 24 bit data lengths are available. The SDIN pins are 3.3 volt inputs.

2.2.2 DIGITAL S/PDIF AUDIO INPUTS

SPDIFRX[1:0] **S/PDIF Data Input**

These pins are S/PDIF audio inputs. They will accept a stereo input up to 96kHz and are 3.3V inputs. An appropriate transformer or optical coupler is necessary for external interface.

2.2.3 ANALOG INPUTS

AIN[8:1]+/- **Differential Analog Inputs**

Each pair of AIN pins is a differential unbuffered analog input. The input is terminated differentially with 20k-ohms and then AC coupled to the internal ADC. The analog inputs for each stereo pair of channels are selected by pulling the appropriate DIG/ANL pin low.

2.2.4 DIGITAL AUDIO OUTPUTS

MCLKT — **Master System Clock Output**

This pin is the master clock output. The master clock is an integer multiple of the LRCLK frequency. The default master clock is 12.288 MHz, which corresponds to a 48 kHz sample rate (Fs) * 256.

LRCLKT — **Output Left/Right Clock**

This pin is the framing clock for the digital audio outputs. The serial output data is transmitted as two channels every sample rate period. LRCKT determines the start of each data pair. The LRCKT frequency determines the output sample rate (Fs). LRCKT is a 3.3 volt output.

SCLKT — **Output Shift Clock**

This pin is the Shift Clock output for the serial output data on SDO[1:0]. The serial clock is used to frame each bit of the serial output data. The shift clock frequency is typically 64*Fs. SCLKT is a 3.3 volt output.

SDO[1:0] — **Serial Data Outputs**

These pins provide two Serial Data Outputs. Serial Data is arranged as one left/right pair. SDO is a 3.3 volt output.

SPDIFTX[1:0] — **S/PDIF Data Output**

These pins are downmixed S/PDIF audio outputs. SPDIFTX is a 3.3 volt output.

2.2.5 CONTROL SIGNAL PINS

BOOT — **Boot Selection**

This pin is the boot selection input. The boot selection picks the source location for the DSP boot code and is predominantly used for firmware upgrade. See Section 3.2, “Activating the amplifier,” on page 19 for further information. This pin is pulled low internally to ground via a 10 kΩ resistor.

nERROR — **Amplifier Error**

The error signal is an open-drain output with 10k ohm internal pullup to 3.3V that, when low, indicates a fault condition has occurred in the amplifier, or that the amplifier has not been initialized. Fault conditions include over-temperature, over-current, short circuit, and output power stage disabled. See Section 3.6, “Amplifier Overload Protection,” on page 20 for further details.

nERROR[x-x] — **Channel Amplifier Error**

These error signals function identically to nERROR, except they indicate an error condition on a pair of channels and do not include over-temperature.

nRESET — **Reset**

This pin is the active-low reset input to the module. Driving the reset to active low for 10 ms will bring all internal devices to their default state. During the power on sequence, the reset line must be active low during the high voltage supply ramp period and held for a minimum of 100ms after the high voltage supply reaches 95% of its nominal value. The nReset is a bidirectional pin and is used to issue a reset between modules in a master/slave configuration. The reset pin must be driven with an open collector or open drain driver.

PSSYNC — **Power Supply Synchronization**

This pin is a power supply synchronization output and may be used to synchronize any external switching power supply to the 384kHz PWM output switch rate.

DIG/ANL[3:0] — **Digital/Analog Input Selection**

When tied high or left unconnected, these pins select the SAI port as the input source to each pair of channels. When tied low, these pins select the Differential Analog Inputs as the input source to each pair of channels. The state of these pins are internally sensed by the module at the completion of reset or power up, therefore a change in configuration requires a reset of the module to take effect. These pins are pulled high internally to 3.3 volts via a 10 kΩ resistor. Alternatively, the SAI port and Differential Analog Input selection may be made without a hardware reset through the use of software commands- see Section 6, “Software Control Settings,” on page 26.

SPDIFEN[1:0] — **S/PDIF Input Enable**

When tied low, the SPDIFEN[1:0] pins enable the SPDIFRX[1:0] S/PDIF input sources to channels 1/2 and 5/6. The state of these pins are read during the initialization of the internal controller after power up or a hardware reset. To recognize a hardware change to the SPDIFEN inputs requires a reset of the module. When the SPDIFEN[1:0] pins are tied high or left open, the input sources are determined by the DIG/ANL[3:0] pins (see Section 3.1, “Hardware Configuration,” on page 18). The SPDIFEN[1:0] pins are pulled high internally to 3.3 volts via a 10 kΩ resistor. Alternatively, SPDIFEN[1:0] may be configured

without a hardware reset through the use of software commands- see Section 6, “Software Control Settings,” on page 26

SCL[1:0] **Module Control Interface Clock**

These pins are the serial clock input lines of the module control interface. A separate clock line is provided for each controller. These may be tied together on the system board if a single clock line for both controllers is desired. These pins are pulled high internally to 3.3 volts via a 10 kΩ resistor.

SDA[1:0] **Serial Data**

These pins are the bidirectional serial data lines of the module control interface. A separate data line is provided for each controller. These may be tied together on the system board if a single data line for both controllers is desired. These pins are pulled high internally to 3.3 volts via a 10 kΩ resistor.

2.2.6 MULTI-MODULE COMMUNICATION PINS

MM_CONFIG[1:0] **Multi-Module Master/Slave/Listen Selection**

The MM_CONFIG[1:0] pins identify the amplifier as a timing master, timing slave or listen as shown in the following table. For a single module system, these pins must be tied high or left unconnected. For a multi-module system, see Section 4.4, “Matrix-Mixing Across Multiple Modules,” on page 21 for information on configuring these pins. MM_CONFIG[1:0] pins are pulled high internally to 3.3 volts via a 10 kΩ resistor.

MM_CONFIG[1]	MMCONFIG[0]	Description
0	0	Slave
0	1	Listen
1	0	Reserved
1	1	Master

Table 16: MM_CONFIG Selection

MM_COM[5:0] **Multi-Module Communication Data Bus**

These signals provide multi-channel high speed communication capability between the amplifier modules to allow for multi-channel matrix mixing. For single-module systems, leave these pins unconnected. See Section 4.4, “Matrix-Mixing Across Multiple Modules,” on page 21 for further information regarding MM_COM. NOTE: When two or more modules are connected via the MM_COM bus under no circumstances should they be disconnected when the modules are powered.

2.2.7 LOUDSPEAKER OUTPUTS

SPKR_OUT[8:1]+,- **Loudspeaker Channel Outputs**

These pins provide the Power Amplifier Outputs. Each channel of the amplifier is a full-bridge output configuration consisting of a positive (+) and negative (-) output. The outputs must remain floating and must not be connected to ground.

3 AMPLIFIER OPERATION

The amplifier module may be operated with any combination of analog or digital inputs. Each pair of amplifier channels has one digital SAI port and one optional pair of analog inputs. In addition, there are two optional S/PDIF digital inputs. Through software settings, any input can be mixed and/or routed to any output. By connecting two or three modules together with the Multi-Module Communication Pins, up to 16 stereo sources can be mixed/routed to 12 stereo zones.

3.1 HARDWARE CONFIGURATION

The DIG/ANL[3:0] pins provide a means to select between the SAI port and analog inputs for each pair of channels through hardware. The SPDIFEN[1:0] pins provide a means to enable the S/PDIF inputs through hardware. Hardware source selection pins are read once after reset. Therefore, a change in state of these pins requires a reset of the module for the changes to take effect. Alternatively, the input selection can be made with out a hardware reset through software commands, which overrides the hardware settings- see Section 6, “Software Control Settings,” on page 26.

The following table illustrates the functionality of the hardware configuration pins on the module. Note that when tied low, the setting of the SPDIFEN[1:0] pins override the setting of the DIG/ANL0 and DIG/ANL2 pins:

SPDIFEN Setting	DIG/ANLx Setting	Input Source Selection
SPDIFEN0 = 1	DIG/ANL0 = 1	SAI port 0 connected to channels 1/2
SPDIFEN0 = 1	DIG/ANL0 = 0	AIN1/2 connected to channels 1/2
SPDIFEN0 = 0	DIG/ANL0 = x	SPDIFRX0 connected to channels 1/2
-	DIG/ANL1 = 0	AIN3/4 connected to channels 3/4
-	DIG/ANL1 = 1	SAI port 1 connected to channels 3/4
SPDIFEN1 = 1	DIG/ANL2 = 1	SAI port 2 connected to channels 5/6
SPDIFEN1 = 1	DIG/ANL2 = 0	AIN5/6 connected to channels 5/6
SPDIFEN1 = 0	DIG/ANL2 = x	SPDIFRX1 connected to channels 5/6
-	DIG/ANL3 = 0	AIN7/8 connected to channels 7/8
-	DIG/ANL3 = 1	SAI port 3 connected to channels 7/8

TABLE 17: Audio Source Selection through Hardware Pins

3.2 ACTIVATING THE AMPLIFIER

After reset the XM100 module DSP typically boots from internal EEPROM. There are two boot mode selections as defined in the following table.

BOOT	Description
0	Default mode. Boot from internal EEPROM
1	Boot through the module control interface

Table 18: Boot Selection

When BOOT is low, the amplifier will boot from the internal EEPROM. When BOOT is high, the amplifier gets the boot code from an external device via the module control interface. An external controller is expected to load the boot code. The BOOT pin is used primarily for field firmware upgrades.

3.3 POWER SUPPLY SEQUENCING AND RESET

For power up, the +12V and +5V supplies must be on and stable before applying the +48V supply. nRESET must be active-low prior to activating the +48V supply. nRESET may be released 100ms after the +48V supply is stable. It is acceptable to use voltage regulators to derive the +12V and +5V from the +48V supply if only a single +48V supply is available in the system. Reset must be asserted prior to or concurrent with the application of the +5V supply

The amplifier should be muted prior to power down. The 12V and 5V supplies must remain stable until the +48V supply is removed.
The 12V and 5V supplies must not drop below minimum specified operating values at any time if the +48V supply is active. Asserting nRESET active-low or muting the amplifier before any supply change will ensure safe transitions

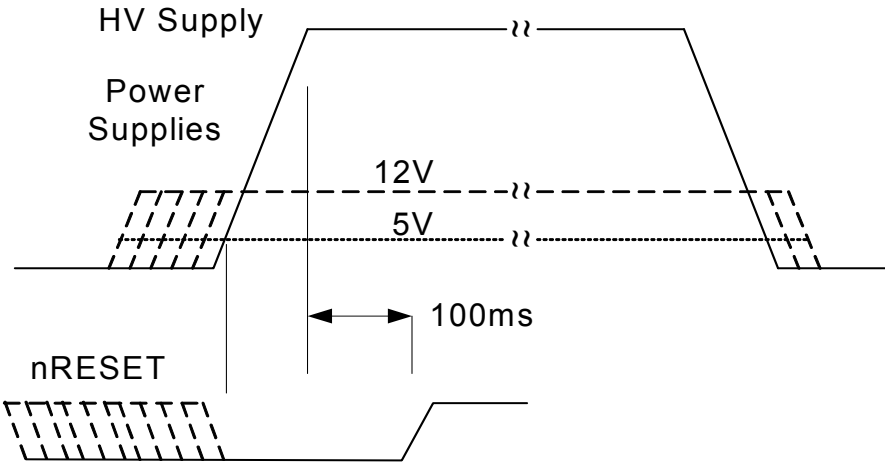

FIGURE 8: Power Supply Sequencing

3.4 ADJUSTING CONTROL SETTINGS

All control settings for the amplifier are adjusted by writing to configuration registers through the module control interface bus (see Section 4, "Digital Audio Interface," on page 20). The DSP within the module will automatically provide a smooth transition between changes to most control settings in order to avoid pops. It is recommended that input selection be changed with the amplifier muted to avoid pops.

3.5 OPERATIONAL LIMITATIONS

Do not generate audio output with a frequency content higher than 20kHz with no load. Peaking in the output filter can cause the output voltages to exceed the filter capacitor voltage rating. Avoid test tones above 20kHz.

3.6 AMPLIFIER OVERLOAD PROTECTION

The amplifier monitors output currents in each power stage and monitors the heat sink temperature. The current sensors protect the output stage from over-current and short-circuit faults. The temperature sensor protects the amplifier from excessive operating temperature. Configuration and register settings are not altered by amplifier protection actions.

3.6.1 SHORT-CIRCUIT/OVER-CURRENT PROTECTION

If an over-current or short-circuit event is detected, the affected Loudspeaker output channels will be shut down, the appropriate nERRORx output will change to active low and the nERROR output will change to active low. Recovery from an over-current or short-circuit shut down is automatic. Approximately 5 seconds after the shut down, the Loudspeaker outputs will activate. If the condition that caused the shut down persists, the amplifier channels will shut down again.

3.6.2 OVER-TEMPERATURE PROTECTION

A temperature sensor monitors the amplifier's temperature. As the internal temperature begins to reach critical levels, the controller will begin to limit the output power. If the temperature exceeds the critical level, the amplifier will shut down all output channels and the nERROR[x-x] output will be driven active low indicating an over-temperature fault. Recovery from an over-temperature shut down is automatic and includes an amount of hysteresis to allow for proper cooling before reactivation. See Section 7.3, "Ambient Operating Conditions," on page 52 for normal operating temperature ranges.

4 DIGITAL AUDIO INTERFACE

The XM100 module has one digital SAI port for each pair of channels, as well as two optional S/PDIF input sources.

4.1 SERIAL AUDIO INPUTS (SAI PORTS)

The XM100 module contains one SAI port for each pair of channels. Each input can support an individually selectable sample rate from 32kHz to 96kHz. All digital audio inputs are 3.3V CMOS logic. The SAI port is designed to interface with standard digital audio components and to accept I²S or left justified data formats. For each SAI port, the left channel data is assigned to the odd-numbered input (channels 1, 3, 5 and 7). Right channel data is then assigned to the even-numbered input.

For I²S format, the left channel data is read when LRCK is low. For the left justified format, the left channel data is read when LRCK is high. Either format requires data to be valid on the rising edge of SCLK and sent MSB-first on SDIN with 32 bits of data per channel. Each set of digital inputs runs asynchronously to the others and may accept different sample rates and formats.

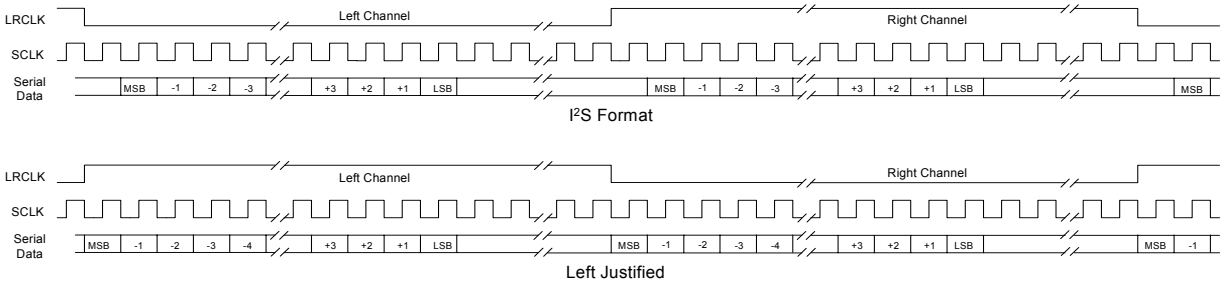

FIGURE 9: SAI port Data Formats

4.2 S/PDIF DIGITAL AUDIO INPUTS

The S/PDIF input on the SPDIFR[1:0] pins accept the IEC60958 standard format, but use TTL or CMOS signal levels. An external receiver is required for level conversion. The S/PDIF input is always asynchronous to the other digital audio ports. Clock and serial data are extracted from the incoming bit stream. The S/PDIF inputs support two-channel sources only.

4.3 DIGITAL SERIAL AUDIO OUTPUTS (SAO PORTS)

The XM100 module contains two SAO ports using the MCLKT, LRCKT, SCLKT, and SDOUT[1:0] pins. The digital audio outputs are formatted as I²S data with an MCLK frequency of 12.288MHz and a sample rate of 48kHz. The XM100 module has two optional two-channel digital S/PDIF audio outputs using the SPDIFTX[1:0] pins. The S/PDIF digital audio outputs are IEC60958 compliant, with a fixed sample rate of 48kHz.

4.4 MATRIX-MIXING ACROSS MULTIPLE MODULES

Matrix mixing can be performed across multiple XM modules by using the Multi-Module Communication Bus. The bus can accommodate up to 8 input channel pairs from two modules. Additional outputs can be added by connecting up to three modules to the bus.

4.4.1 16 X 16 MATRIX-MIXING

The following configuration should be used for a two-module system:

- One module must be designated as the timing master by connecting both MM_CONFIG pins to 3.3 volts. The other module must be designated as the timing slave by connecting both MM_CONFIG pins to ground.
- The four audio input pairs on the master are designated 1-4, while the four audio input pairs on the slave are designated 5-8. These designations remain the same in the software for both modules.
- Connect each of the MM_COM pins on the master module to the pin of the same name on the slave.
- Connect nRESET of each module together. nRESET must be driven with an open collector driver.
- The channels within the master module are designated channels 1-8, while the channels within the slave module are designated channels 9-16.

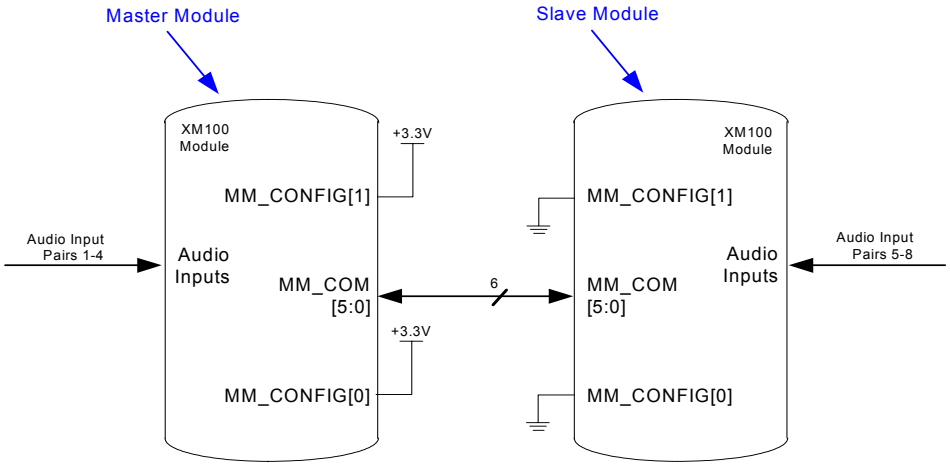

FIGURE 10: Two-Module Matrix Mixing

4.4.2 16 X 24 MATRIX-MIXING

Eight input channel pairs can be mixed up to a maximum of 24 output channels by adding a third module to the Multi-Module Communication Bus and configuring the third module for "listen" mode. The following configuration should be used for a system with three modules:

- One module must be designated as the timing master by connecting both MM_CONFIG pins to 3.3 volts. This module will provide audio input pairs 1-4 to the system.
- One module must be designated as the timing slave by connecting both MM_CONFIG pins to ground. This module will provide audio input pairs 5-8 to the system.
- The third module is placed in a "listen" mode by connecting MM_CONFIG[1] to ground and MM_CONFIG[0] to 3.3 volts.
- Connect each MM_COM pins of each module.
- Connect nRESET of each module together. nRESET must be driven with an open collector driver.
- The SAI, S/PDIF, and analog inputs for the "listen" module are disabled. The 16 inputs to the "listen" module's mixer are obtained from the "master" and the "slave" modules via the MM_COM bus.

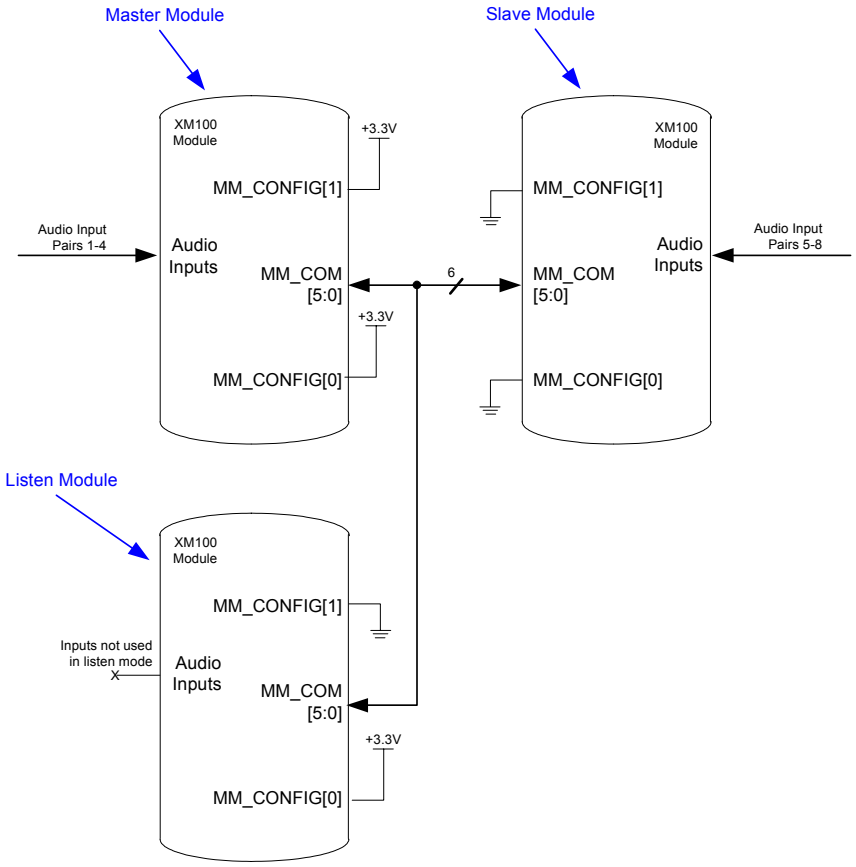

FIGURE 11: Matrix Mixing with more than two modules

5 MODULE CONTROL INTERFACE (MCI) SPECIFICATION

The controller inside the XM100 module provides a number of registers that are used to control its behavior. The module control interface (MCI) communication protocol is used to set and query these registers through the SDA and SCL pins. This protocol defines any device that sends data on to the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. For this interface, the definition of the master is an external micro-controller or control logic. All modules in the system are logically slaves to the external micro-controller. This should not be confused with the MASTER, SLAVE, or LISTEN definition used with the MM_COM interface for the transfer of audio source material exchanged between modules. The master always starts the transfer and provides the serial clock for synchronization. The XM100 module controller only functions as a slave device in all of its communications and will not function with multiple masters.

5.1 MODULE CONTROL INTERFACE STATES

5.1.1 DATA TRANSITION OR CHANGE

Transitions on the SDA line during a data transaction are only allowed while the clock is in the low state. An SDA transition while the clock is high is used to identify a START or STOP condition.

5.1.2 START CONDITION

START is identified by a high to low transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A START condition must precede any command for data transfer.

5.1.3 STOP CONDITION

STOP is identified by low to high transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A STOP condition terminates communication between XM100 module and the bus master.

5.1.4 DATA INPUT

During the data input, the XM100 module samples the SDA signal on the rising edge of clock SCL. For correct device operation the SDA signal must be stable during the rising edge of the clock and the data can change only when the SCL clock signal is low.

5.1.5 ACKNOWLEDGE

All data transfers across the module control interface bus must be acknowledged. Each byte transferred is followed by an acknowledge bit. When data is being written to the module, it will generate the ACK; when being read, the bus master generates the ACK. In the following descriptions, ACK refers to a true-acknowledge and NACK refers to a not-acknowledge. In general, ACK means continue or ready and NACK means terminate or not ready. The bus master is responsible for correctly interpreting the acknowledge response.

5.2 DEVICE ADDRESS CHANNEL GROUPINGS

To start communication between the master and the XM100 module, the master must initiate with a start condition. Following this, the master sends onto the SDA line 8-bits (MSB first) corresponding to the device select address and read or write mode. If the device address matches that of the XM100, the module will acknowledge the address during the 9th bit time. The 7 most significant bits are the device address identifiers. The 8th bit (LSB) identifies read or write operation R/W. This bit is set to 1 in read mode and 0 for write mode.

Four hardware device addresses are used to identify the module - two for channels 1 through 4 and two for channels 5 through 8. The device addresses correspond to the setting of the MM_CONFIG pins as shown in the following table:::

Master MM_CONFIG[1:0]	Audio Input Pairs	Controller Device Address
11	1-2	B2h
	3-4	B4h

Table 19: Master Module Device Address

Slave MM_CONFIG[1:0]	Audio Input Pairs	Controller Device Address
00	5-6	B6h
	7-8	B8h

Table 20: Slave Module Device Address

Listen MM_CONFIG[1:0]	Audio Input Pairs	Controller Device Address
01		BAh
		BCh

Table 21: Listen Module Device Address

5.3 CONTROLLER I/O PROCEDURES

CONSUMER

PRELIMINARY

5.3.1 CONTROLLER WRITE PROCEDURE

All writes to the XM100 module controller registers must begin with the Start Condition, followed by the Device Address byte (with read/write bit cleared), three Register Address bytes, three Data bytes and a Stop Condition. The XM100 module (MCI) controller acknowledges each byte by pulling SDA low on the bit immediately following each byte. These bytes are described below:

Byte	Read/Write	Name	Description
0	W	Device Address + Read/Write Bit	Device Address of channel group, with R/W bit cleared
1	W	Register Address [23:16]	Upper 8 bits of register address
2	W	Register Address [15:8]	Middle 8 bits of register address
3	W	Register Address [7:0]	Lower 8 bits of register address
4	W	Data[23:16]	Upper 8 bits of register data to write
5	W	Data[15:8]	Middle 8 bits of register data to write
6	W	Data[7:0]	Lower 8 bits of register data to write

Table 22: Controller Write Byte Sequence Description

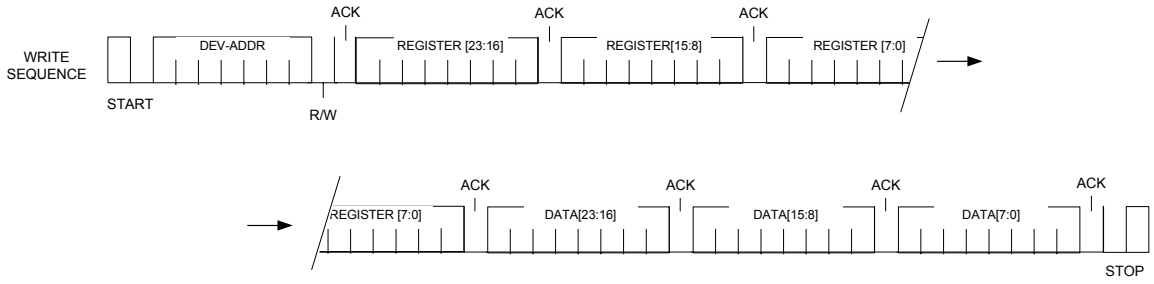

FIGURE 12: Controller Write Sequence Diagram

5.3.2 CONTROLLER READ PROCEDURE

All reads from the XM100 module controller registers require two steps. During the first step, the master must send the Start Condition, followed by the Device Address byte (with read/write bit low), and three Register Address bytes. The XM100 module controller acknowledges each byte in the first step by pulling SDA low on the bit immediately following each byte.

Immediately following the first step, the master must send another Start Condition, followed by the Device Address byte (with read/write bit high). The XM100 module controller will acknowledge the Device Address byte by pulling SDA low on the bit immediately following the Device Address. The next 3 bytes are sent by the XM100 module controller to the master, and contain the three Data bytes to be read. The master must acknowledge the first two Data bytes by pulling SDA low on the bit immediately following the Device Address. After the third Data byte, the master should not send an acknowledgement to the module. At the end of the second step, the master must send the Stop Condition.

Step	Byte	Master Read/Write	Name	Description
1	0	W	First Device Address + Read/Write Bit	Device Address of channel group, with R/W bit low
	1	W	Register Address [23:16]	Upper 8 bits of register address
	2	W	Register Address [15:8]	Middle 8 bits of register address
	3	W	Register Address [7:0]	Lower 8 bits of register address

Table 23: Controller Read Byte Sequence Description

Step	Byte	Master Read/Write	Name	Description
2	Repeat Start Condition			
	4	W	Second Device Address + Read/Write Bit	Device Address of channel group, with R/W bit set
	5	R	Data[23:16]	Upper 8 bits of register data to read
	6	R	Data[15:8]	Middle 8 bits of register data to read
	7	R	Data[7:0]	Lower 8 bits of register data to read

Table 23: Controller Read Byte Sequence Description

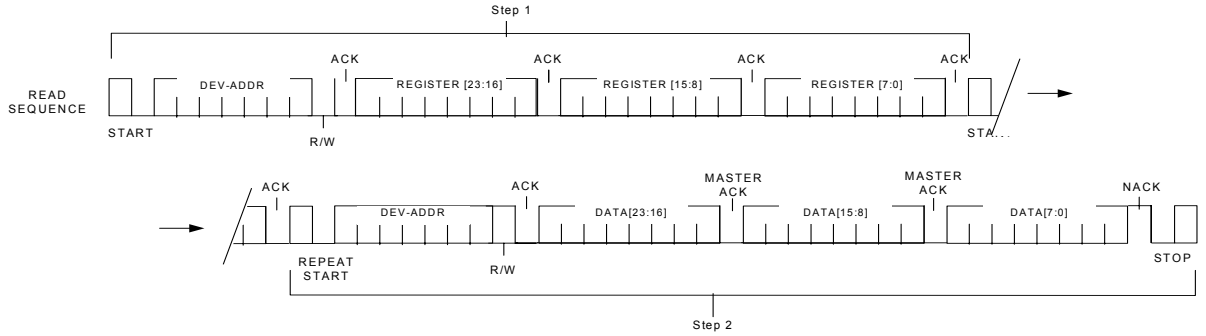

FIGURE 13: Controller Read Sequence Diagram

5.4 STORE TO EEPROM COMMAND

An EEPROM within the amplifier module stores the default values of each register for recall on reset or powerup. The EEPROM settings may be updated at any time. The following module control interface command will cause all of the current software settings to become the default settings by storing them into the EEPROM. This command will update the EEPROM values for a group of channels identified by the Device Address. In order to update the EEPROM for all channels within a module, the command must be issued twice- once for each Device Address within the module. Note: The input source selection is not stored in the EEPROM. The input source is selected at power up or module reset. If an input source is changed via software control, its configuration will be lost at power down or during reset.

Byte	Read/Write	Name	Description
0	W	Device Address + Read/Write Bit	Device Address of channel group, with R/W bit cleared
1	W	Register Address [23:16]	Set to 0x80 for EEPROM write
2	W	Register Address [15:8]	Set to 0x00 for EEPROM write
3	W	Register Address [7:0]	Set to 0x00 for EEPROM write
4	W	Data[23:16]	Set to 0x00 for EEPROM write
5	W	Data[15:8]	Set to 0x00 for EEPROM write
6	W	Data[7:0]	Set to 0x00 for EEPROM write

Table 24: Store to EEPROM Command Byte Description

6 SOFTWARE CONTROL SETTINGS

All control settings for the amplifier are adjusted by writing to configuration registers through the module control interface bus (see Section 5, “Module Control Interface (MCI) Specification,” on page 23). While changing Input Source settings, the amplifier should be muted to avoid pops. For all other settings, the amplifier will automatically provide a smooth transition between changes in order to avoid pops.

6.1 INTERNAL EEPROM

CONSUMER

An EEPROM within the amplifier module stores the default values of each register for recall on reset or power up. Note that the default values for input selection are determined by the Hardware Configuration Pins and not by the EEPROM. The DSP within the module has the capability to update the EEPROM contents at any time. For more information, see section Section 5.4, "Store to EEPROM Command," on page 26.

6.2 DSP PROCESSING ORGANIZATION

The XM100 module controller contains a powerful DSP engine which provides a group of processing blocks, including Input Select, Tone Control, 3 and 5 band Parametric EQ,Adjustable Time Delay, Compression, and Level Control. A Master Volume control is available for each controller and its corresponding 2 audio input pairs. and XM100 illustrate the pre-mixer and post mixer DSP processing blocks.

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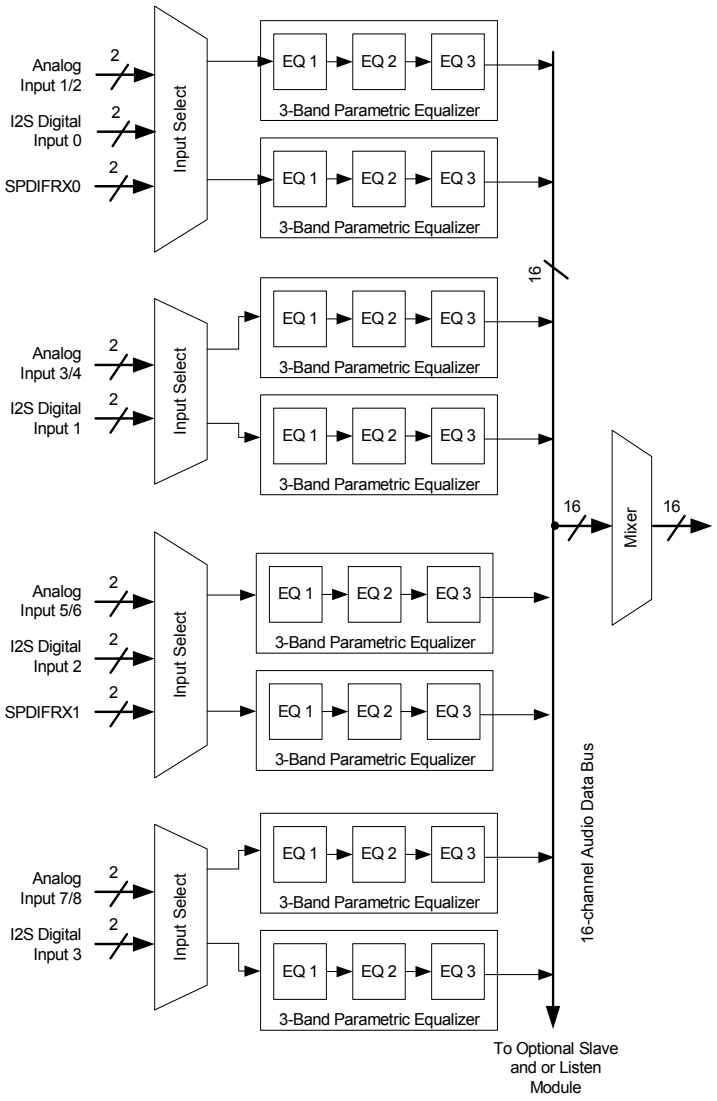

FIGURE 14: Pre-mix DSP Processing Blocks

PRELIMINARY

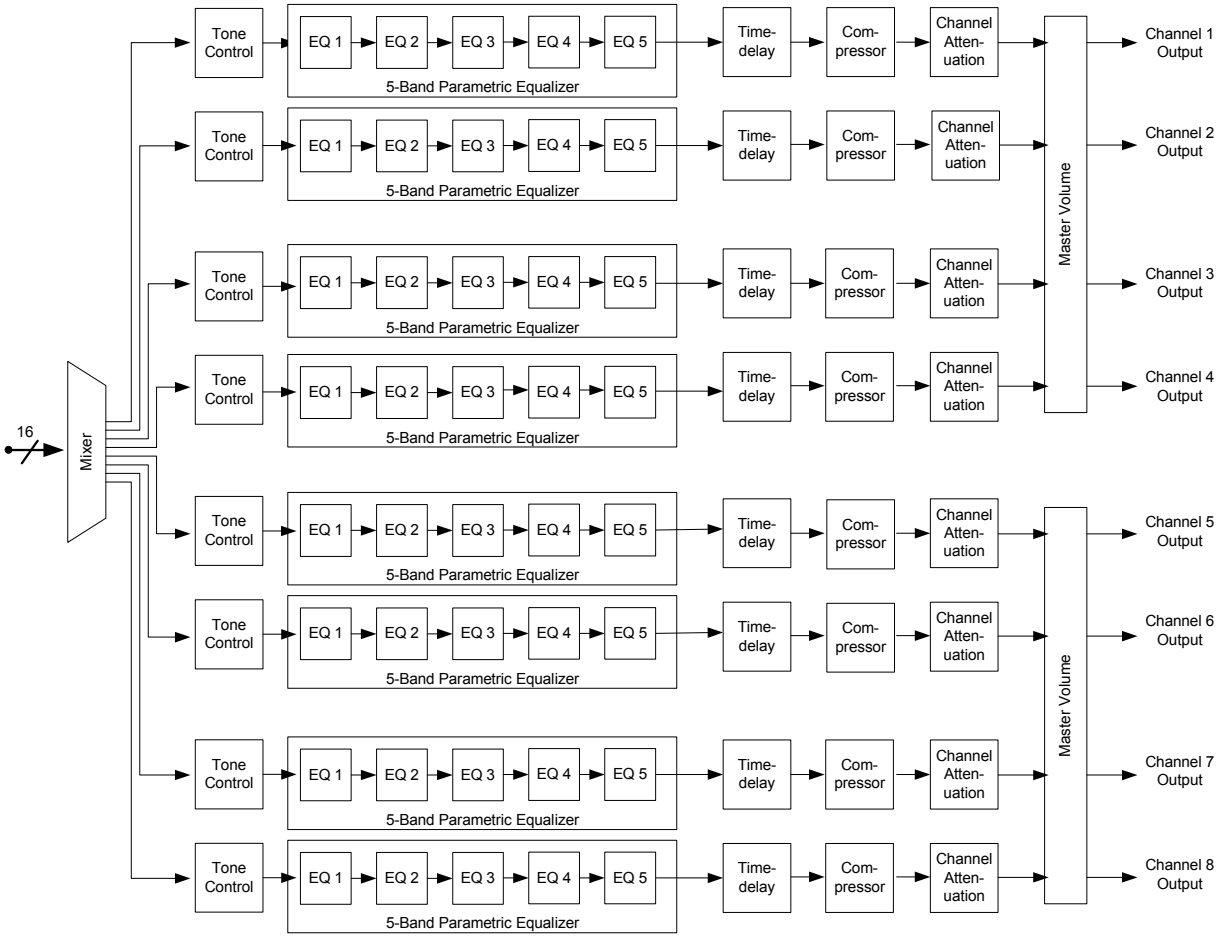

FIGURE 15: Post-mix DSP Processing Blocks

6.3 GAIN MANAGEMENT

Careful attention must be paid to the signal level at the input and at each stage through the DSP in order to prevent clipping. Changes to DSP parameters must be made only after thorough consideration of the effects on signal level throughout the entire signal path from input to output. **Though reducing the gain of the input signal will result in additional DSP headroom, this action will cause a corresponding reduction in the signal-to-noise ratio of the amplifier.**

6.3.1 DSP GAIN STRUCTURE

At the input to the DSP, an attenuation of -6dB is applied to allow for headroom within the DSP processing blocks. At the DSP output, +18dB of gain is applied prior to driving the PWM amplifier outputs. This organization is shown in the following figure:

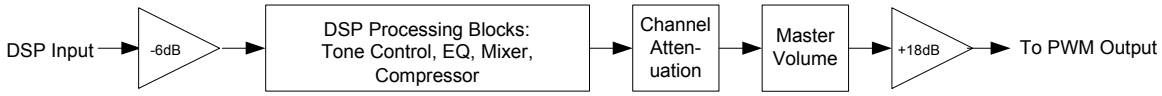

FIGURE 16: DSP Gain Stages

Thus, with a full-scale (0 dBFS) digital input signal, -12dB of attenuation must be applied prior to the PWM output to avoid clipping. For this reason, the default value for each Channel Attenuation is -12dB.

6.3.2 GAIN CALCULATIONS

Proper gain management begins with determining the maximum module input level that is expected for the system design. If the S/PDIF or I2S inputs are used, the maximum level can be as high as 0dBFS if connected directly to source material. If the analog inputs are used, a 2.0Vrms sine wave signal is required to produce an input of 0dBFS to the DSP.

Once a signal is input, 6dB of headroom is provided for all of the DSP processing blocks and volume controls. Clipping will occur if any of the DSP processing blocks cause the signal level to exceed 0dBFS. At the output of the DSP processing, 18dB of gain is added prior to the PWM amplifier outputs. Therefore, the sum of the gains for all DSP processing blocks and volume controls for each channel must equal -12dB in order to prevent clipping with a 0dBFs input on any source.

6.4 SOFTWARE REGISTER ADDRESSING

Changes to each of the DSP Processing Blocks are made by writing to a software register set within the module. Each software register is accessed using a module control device address and an internal register address. The internal register addresses are repeated for each group of four channels. The module control device address is used to identify the appropriate set of four.

Register locations are defined as a Module Control Interface device address followed by a 24bit register location. The Register Table syntax list the register location as $AA:xxxxxx where AA is the Module control Address followed by the "xxxxxx"register offset. An example of muting all channels in the amplifier would be a write to $C2:000000 and a write to $C4000000 to mute all 8 channels. For a multi-module configuration, MCI addresses may range from $B2: through $C4

6.5 INPUT SOURCE CONFIGURATION

Analog, digital SAI port, or digital S/PDIF inputs are available. The default value for Input Selection is read on reset through the hardware pins DIG/ANL[3:0] and SPDIFEN[1:0]. At any time, the Input Selection may be changed in software through the following registers. The amplifier outputs must be muted during changes to Input Selection to avoid pops.For each SAI port, the left channel data is assigned to the odd-numbered input (channels 1, 3, 5 and 7). Right channel data is then assigned to the even-numbered input. Note that the input select is not used if a module is configured for "listen" mode in a multi-module system.

Register 020001h is defined as the input selection register InputSelectReg. The functions of the bits in InputSelectReg are as follows:

InputSelectReg 020001h Bits	[23:8]	[7:5]	4	3	2	1	0
Value	Reserved Always set to F800h	Reserved Always set to 0	JUSTIFY	DIG_ANL_H	DIG_ANL_L	Reserved Always set to 0	SPDIFEN

Table 25: Input Selection Register

Bits [23:8] **Reserved**
These bits should always be set to F800h when writing to InputSelectReg.

Bits [7:5] **Reserved**
These bits should always be set to 0 when writing to InputSelectReg.

Bit 4 **JUSTIFY**
When a '1' is written to JUSTIFY, both SAI ports will accept digital audio data in left-justified format. When a '0' is written to JUSTIFY, both SAI ports will accept digital audio data in I2S format. The default value for JUSTIFY is 0.

Bit 3 **DIG_ANL_H**
When a '1' is written to DIG_ANL_H, the SAI port is selected for the higher-ordered pair of channels channels corresponding to the controller device address. When a '0' is written to DIG_ANL_H, the differential analog inputs are selected. Upon reset, the value of DIG_ANL_H is equal to the state of the DIG/ANL pin for the corresponding pair of channels.

Bit 2 **DIG_ANL_L**
When a '1' is written to DIG_ANL_L, the SAI port is selected for the lower-ordered pair of channels corresponding to the controller device address. When a '0' is written to DIG_ANL_L, the differential analog inputs are selected. DIG_ANL_L is only valid when SPDIFEN is 0. Upon reset, the value of DIG_ANL_L is equal to the state of the DIG/ANL pin for the corresponding pair of channels.

Bit 1 **Reserved**

This bit should always be set to a '0' when writing to InputSelectReg.

Bit 0 **SPDIFEN**

When SPDIFEN is set to a '1', the SPDIF input is selected for the lower-ordered pair of channels corresponding to the controller device address. When a '0' is written to SPDIFEN, the input selection for these channels is determined by DIG_ANL_L. Upon reset, the value of SPDIFEN is equal to the state of the SPDIFEN hardware pin for the corresponding pair of channels.

Each module contains two sets of input select registers- one for each group of 4 input channels. The controller device address is used to determine which group of 4 channels is accessed. The following table illustrates the interaction between controller device address and InputSelectReg:

Master Controller Device Address	SPDIFEN Setting	DIG_ANL_x Setting	Input Source Selection
B2:020001h	SPDIFEN = 0	DIG_ANL_L = 1	SAI port 0 connected to channels 1/2
B2:020001h	SPDIFEN = 0	DIG_ANL_L = 0	AIN1/2 connected to channels 1/2
B2:020001h	SPDIFEN = 1	DIG_ANL_L = x	SPDIFRX0 connected to channels 1/2
B2:020001h	-	DIG_ANL_H = 0	AIN3/4 connected to channels 3/4
B2:020001h	-	DIG_ANL_H = 1	SAI port 1 connected to channels 3/4
B4:020001h	SPDIFEN = 0	DIG_ANL_L = 1	SAI port 2 connected to channels 5/6
B4:020001h	SPDIFEN = 0	DIG_ANL_L = 0	AIN5/6 connected to channels 5/6
B4:020001h	SPDIFEN = 1	DIG_ANL_L = x	SPDIFRX1 connected to channels 5/6
B4:020001h	-	DIG_ANL_H = 0	AIN7/8 connected to channels 7/8
B4:020001h	-	DIG_ANL_H = 1	SAI port 3 connected to channels 7/8

TABLE 26: Master Module Audio Source Selection through Input Selection Register

Slave Controller Device Address	SPDIFEN Setting	DIG_ANL_x Setting	Input Source Selection
B6:020001h	SPDIFEN = 0	DIG_ANL_L = 1	SAI port 0 connected to channels 1/2
B6:020001h	SPDIFEN = 0	DIG_ANL_L = 0	AIN1/2 connected to channels 1/2
B6:020001h	SPDIFEN = 1	DIG_ANL_L = x	SPDIFRX0 connected to channels 1/2
B6:020001h	-	DIG_ANL_H = 0	AIN3/4 connected to channels 3/4
B8:020001h	-	DIG_ANL_H = 1	SAI port 1 connected to channels 3/4
B8:020001h	SPDIFEN = 0	DIG_ANL_L = 1	SAI port 2 connected to channels 5/6
B8:020001h	SPDIFEN = 0	DIG_ANL_L = 0	AIN5/6 connected to channels 5/6
B8:020001h	SPDIFEN = 1	DIG_ANL_L = x	SPDIFRX1 connected to channels 5/6
B8:020001h	-	DIG_ANL_H = 0	AIN7/8 connected to channels 7/8

TABLE 27: Slave Module Audio Source Selection through Input Selection Register

Note: The audio source selected via software through the Input Section Registers are not stored in EEprom. The input source is determined via a set of hardware pins at power up or module reset. Changes made through a software command will be lost on power off or system reset.

6.6 TONE CONTROL

The XM100 module provides individual software-controlled Tone Controls for each channel. These are implemented as low-pass and high-pass shelving filters for bass and treble control, respectively, which are added back into the signal flow. Each filter contains a first-order (6dB/octave) rolloff, with programmable corner frequency and gain. The DSP within the module will automatically provide a smooth transition between changes to the Tone Control.

6.6.1 CORNER FREQUENCY CALCULATION

The Corner Frequency of the Tone Control is defined as the frequency at which the gain of the filter is +-3dB. For a given Corner Frequency, the appropriate parameter is a signed, 24-bit number calculated using the following equations.

First, determine the intermediate value Θ, then use Θ to calculate the frequency corner parameter value (note that Θ is in radians). Valid range for Corner Frequency is 20Hz to 24,000Hz.

$$\Theta(radians) = Frequency \times 9.817477 \times 10^{-5}$$

$$ToneControlCornerFrequencyParameter = 2^{23} \times \left(\frac{\sin(\Theta) - 1}{\cos(\Theta)}\right)$$

6.6.2 GAIN CALCULATION

For a given Gain in dB, the appropriate parameter is a signed, 24-bit number calculated using the following equation. Valid range for Tone Control Gain is -10dB to +9.542dB.

$$ToneControlGainParameter = 2^{23} \times \left[\frac{10^{\left(\frac{Gain}{20}\right)} - 1}{2}\right]$$

6.6.3 TONE REGISTER SUMMARY

Register Name	Minimum Value	Maximum Value	Description
BassToneControlCorner FrequencyParameter	804047h	3504F3h	Per-channel corner frequency parameter for bass tone control shelving filter.
BassToneControlGain Parameter	C0002Ah	7FFFFFh	Per-channel gain for bass tone control shelving filter
TrebleToneControlCornerFrequencyParameter	804047h	3504F3h	Per-channel corner frequency parameter for treble tone control shelving filter.
TrebleToneControlGain Parameter	C0002Ah	7FFFFFh	Per-channel gain for treble tone control shelving filter

Table 28: Tone Control Register Summary

6.6.4 TONE REGISTER ADDRESS TABLE

Register Name	Master Channel 1 Register Address	Master Channel 2 Register Address	Master Channel 3 Register Address	Master Channel 4 Register Address
BassToneControlCorner FrequencyParameter	B2:000015h	B2:000019h	B2:00001Dh	B2:000021h
BassToneControlGain Parameter	B2:000016h	B2:00001Ah	B2:00001Eh	B2:000022h
TrebleToneControlCorner FrequencyParameter	B2:000017h	B2:00001Bh	B2:00001Fh	B2:000023h
TrebleToneControlGain Parameter	B2:000018h	B2:00001Ch	B2:000020h	B2:000024h

Table 29: Master Module Tone Control Register Address Table

Register Name	Master Channel 5 Register Address	Master Channel 6 Register Address	Master Channel 7 Register Address	Master Channel 8 Register Address
BassToneControlCorner FrequencyParameter	B4:000015h	B4:000019h	B4:00001Dh	B4:000021h
BassToneControlGain Parameter	B4:000016h	B4:00001Ah	B4:00001Eh	B4:000022h
TrebleToneControlCorner FrequencyParameter	B4:000017h	B4:00001Bh	B4:00001Fh	B4:000023h
TrebleToneControlGain Parameter	B4:000018h	B4:00001Ch	B4:000020h	B4:000024h

Table 30: Slave Module Tone Control Register Address Table

Register Name	Slave Channel 1 Register Address	Slave Channel 2 Register Address	Slave Channel 3 Register Address	Slave Channel 4 Register Address
BassToneControlCorner FrequencyParameter	B6:000015h	B6:000019h	B6:00001Dh	B6:000021h
BassToneControlGain Parameter	B6:000016h	B6:00001Ah	B6:00001Eh	B6:000022h
TrebleToneControlCorner FrequencyParameter	B6:000017h	B6:00001Bh	B6:00001Fh	B6:000023h
TrebleToneControlGain Parameter	B6:000018h	B6:00001Ch	B6:000020h	B6:000024h

Table 31: Slave Module Tone Control Register Address Table

Register Name	Slave Channel 5 Register Address	Slave Channel 6 Register Address	Slave Channel 7 Register Address	Slave Channel 8 Register Address
BassToneControlCorner FrequencyParameter	B8:000015h	B8:000019h	B8:00001Dh	B8:000021h
BassToneControlGain Parameter	B8:000016h	B8:00001Ah	B8:00001Eh	B8:000022h
TrebleToneControlCorner FrequencyParameter	B8:000017h	B8:00001Bh	B8:00001Fh	B8:000023h
TrebleToneControlGain Parameter	B8:000018h	B8:00001Ch	B8:000020h	B8:000024h

Table 32: Slave Module Tone Control Register Address Table

Register Name	Listener Channel 1 Register Address	Listener Channel 2 Register Address	Listener Channel 3 Register Address	Listener Channel 4 Register Address
BassToneControlCorner FrequencyParameter	BA:000015h	BA:000019h	BA:00001Dh	BABA:000021h
BassToneControlGain Parameter	BA:000016h	BA:00001Ah	BA:00001Eh	BA:000022h
TrebleToneControlCorner FrequencyParameter	BA:000017h	BA:00001Bh	BA:00001Fh	BA:000023h
TrebleToneControlGain Parameter	BA:000018h	BA:00001Ch	BA:000020h	BA:000024h

Table 33: Slave Module Tone Control Register Address Table

Register Name	Listener Channel 5 Register Address	Listener Channel 6 Register Address	Listener Channel 7 Register Address	Listener Channel 8 Register Address
BassToneControlCorner FrequencyParameter	BC:000015h	BC:000019h	BC:00001Dh	BC:000021h
BassToneControlGain Parameter	BC:000016h	BC:00001Ah	BC:00001Eh	BC:000022h
TrebleToneControlCorner FrequencyParameter	BC:000017h	BC:00001Bh	BC:00001Fh	BC:000023h
TrebleToneControlGain Parameter	BC:000018h	BC:00001Ch	BC:000020h	BC:000024h

Table 34: Listen Tone Control Register Address Table

6.7 PARAMETRIC EQUALIZER

Eight parametric equalizer bands are available on each channel- 3 prior to mixing and 5 post-mixing. Each band contains adjustable Frequency, Gain and Q. Setting the Gain to 0 disables a band. The DSP within the module will automatically provide a smooth transition between changes to the Parametric EQ. The 5 pre-mix bands are not used if a module is configured for "listen" mode in a multi-module system.

6.7.1 EQ CENTER FREQUENCY CALCULATION

For a given center frequency, the appropriate parameter is a signed, 24-bit number calculated using the following equation. Valid range for center frequency is 20Hz to 24,000Hz.

$$EQCenterFrequencyParameter = 2^{23} \times Frequency \times 31.25 \times 10^{-6}$$

6.7.2 EQ QUALITY FACTOR CALCULATION

For a given Q, the appropriate parameter is a signed, 24-bit number calculated using the following equation.
Valid range for Q is 0.5 < Q <= 10. (Note that a value of 0.5 for Q results in an EQQParameter value of 800000h, which is invalid)

$$EQQParameter = 2^{23} \times \left(\frac{1}{2 \times Q}\right)$$

6.7.3 EQ GAIN CALCULATION

For a given Gain in dB, the appropriate parameter is a signed, 24-bit number calculated using the following equation. Valid range for gain is -60dB to +6dB.

$$EQGainParameter = -2^{23} \times \left[1 - 10^{\left(\frac{Gain}{20}\right)}\right]$$

6.7.4 EQ REGISTER SUMMARY

Register Name	Minimum Value	Maximum Value	Description
EQCenterFrequency Parameter	00147Ah	600000h	Center frequency for Parametric EQ, 8 bands per channel
EQQParameter	066666h	7FFFFFh	Quality factor for Parametric EQ, 8 bands per channel
EQGainParameter	8020C5h	7F64C1h	Gain for Parametric EQ, 8 bands per channel

Table 35: Parametric EQ Register Summary

6.7.5 PRE-MIXER EQ REGISTER ADDRESS TABLE

Register Name	Master Channel 1 Register Address	Master Channel 2 Register Address	Master Channel 3 Register Address	Master Channel 4 Register Address
EQCenterFrequency Parameter, band 1	B2:000061h	B2:00006Ah	B2:000073h	B2:00007Ch
EQQParameter, band 1	B2:000062h	B2:00006Bh	B2:000074h	B2:00007Dh
EQGainParameter, band 1	B2:000063h	B2:00006Ch	B2:000075h	B2:00007Eh
EQCenterFrequency Parameter, band 2	B2:000064h	B2:00006Dh	B2:000076h	B2:00007Fh
EQQParameter, band 2	B2:000065h	B2:00006Eh	B2:000077h	B2:000080h
EQGainParameter, band 2	B2:000066h	B2:00006Fh	B2:000078h	B2:000081h
EQCenterFrequency Parameter, band 3	B2:000067h	B2:000070h	B2:000079h	B2:000082h
EQQParameter, band 3	B2:000068h	B2:000071h	B2:00007Ah	B2:000083h
EQGainParameter, band 3	B2:000069h	B2:000072h	B2:00007Bh	B2:000084h

Table 36: Master Module Channel 1- 4 Pre-Mixer Parametric EQ Register Address Table

Register Name	Master Channel 5 Register Address	Master Channel 6 Register Address	Master Channel 7 Register Address	Master Channel 8 Register Address
EQCenterFrequency Parameter, band 1	B4:000061h	B4:00006Ah	B4:000073h	B4:00007Ch
EQQParameter, band 1	B4:000062h	B4:00006Bh	B4:000074h	B4:00007Dh
EQGainParameter, band 1	B4:000063h	B4:00006Ch	B4:000075h	B4:00007Eh
EQCenterFrequency Parameter, band 2	B4:000064h	B4:00006Dh	B4:000076h	B4:00007Fh
EQQParameter, band 2	B4:000065h	B4:00006Eh	B4:000077h	B4:000080h
EQGainParameter, band 2	B4:000066h	B4:00006Fh	B4:000078h	B4:000081h
EQCenterFrequency Parameter, band 3	B4:000067h	B4:000070h	B4:000079h	B4:000082h
EQQParameter, band 3	B4:000068h	B4:000071h	B4:00007Ah	B4:000083h
EQGainParameter, band 3	B4:000069h	B4:000072h	B4:00007Bh	B4:000084h

Table 37: Master Module Channel 5-8 Pre-Mixer Parametric EQ Register Address Table

Register Name	Slave Channel 5 Register Address	Slave Channel 6 Register Address	Slave Channel 7 Register Address	Slave Channel 8 Register Address
EQCenterFrequency Parameter, band 1	B8:000061h	B8:00006Ah	B8:000073h	B8:00007Ch
EQQParameter, band 1	B8:000062h	B8:00006Bh	B8:000074h	B8:00007Dh
EQGainParameter, band 1	B8:000063h	B8:00006Ch	B8:000075h	B8:00007Eh
EQCenterFrequency Parameter, band 2	B8:000064h	B8:00006Dh	B8:000076h	B8:00007Fh
EQQParameter, band 2	B8:000065h	B8:00006Eh	B8:000077h	B8:000080h
EQGainParameter, band 2	B8:000066h	B8:00006Fh	B8:000078h	B8:000081h
EQCenterFrequency Parameter, band 3	B8:000067h	B8:000070h	B8:000079h	B8:000082h
EQQParameter, band 3	B8:000068h	B8:000071h	B8:00007Ah	B8:000083h
EQGainParameter, band 3	B8:000069h	B8:000072h	B8:00007Bh	B8:000084h

Table 38: Slave Module Channel 5-8 Pre-Mixer Parametric EQ Register Address Table

6.7.6 POST_MIXER EQ REGISTER ADDRESS TABLE

Register Name	Master Channel 5 Register Address	Master Channel 6 Register Address	Master Channel 7 Register Address	Master Channel 8 Register Address
EQCenterFrequency Parameter, band 1	B4:000025h	B4:000034h	B4:000043h	B4:000052h
EQQParameter, band 1	B4:000026h	B4:000035h	B4:000044h	B4:000053h
EQGainParameter, band 1	B4:000027h	B4:000036h	B4:000045h	B4:000054h
EQCenterFrequency Parameter, band 2	B4:000028h	B4:000037h	B4:000046h	B4:000055h
EQQParameter, band 2	B4:000029h	B4:000038h	B4:000047h	B4:000056h
EQGainParameter, band 2	B4:00002Ah	B4:000039h	B4:000048h	B4:000057h
EQCenterFrequency Parameter, band 3	B4:00002Bh	B4:00003Ah	B4:000049h	B4:000058h
EQQParameter, band 3	B4:00002Ch	B4:00003Bh	B4:00004Ah	B4:000059h
EQGainParameter, band 3	B4:00002Dh	B4:00003Ch	B4:00004Bh	B4:00005Ah
EQCenterFrequency Parameter, band 4	B4:00002Eh	B4:00003Dh	B4:00004Ch	B4:00005Bh
EQQParameter, band 4	B4:00002Fh	B4:00003Eh	B4:00004Dh	B4:00005Ch
EQGainParameter, band 4	B4:000030h	B4:00003Fh	B4:00004Eh	B4:00005Dh
EQCenterFrequency Parameter, band 5	B4:000031h	B4:000040h	B4:00004Fh	B4:00005Eh
EQQParameter, band 5	B4:000032h	B4:000041h	B4:000050h	B4:00005Fh
EQGainParameter, band 5	B4:000033h	B4:000042h	B4:000051h	B4:000060h

Table 39: Master Module Channel 5-8 Post-Mixer Parametric EQ Register Address Table

Register Name	Slave Channel 1 Register Address	Slave Channel 2 Register Address	Slave Channel 3 Register Address	Slave Channel 4 Register Address
EQCenterFrequency Parameter, band 1	B6:000025h	B6:000034h	B6:000043h	B6:000052h
EQQParameter, band 1	B6:000026h	B6:000035h	B6:000044h	B6:000053h
EQGainParameter, band 1	B6:000027h	B6:000036h	B6:000045h	B6:000054h
EQCenterFrequency Parameter, band 2	B6:000028h	B6:000037h	B6:000046h	B6:000055h
EQQParameter, band 2	B6:000029h	B6:000038h	B6:000047h	B6:000056h
EQGainParameter, band 2	B6:00002Ah	B6:000039h	B6:000048h	B6:000057h
EQCenterFrequency Parameter, band 3	B6:00002Bh	B6:00003Ah	B6:000049h	B6:000058h
EQQParameter, band 3	B6:00002Ch	B6:00003Bh	B6:00004Ah	B6:000059h
EQGainParameter, band 3	B6:00002Dh	B6:00003Ch	B6:00004Bh	B6:00005Ah
EQCenterFrequency Parameter, band 4	B6:00002Eh	B6:00003Dh	B6:00004Ch	B6:00005Bh
EQQParameter, band 4	B6:00002Fh	B6:00003Eh	B6:00004Dh	B6:00005Ch
EQGainParameter, band 4	B6:000030h	B6:00003Fh	B6:00004Eh	B6:00005Dh
EQCenterFrequency Parameter, band 5	B6:000031h	B6:000040h	B6:00004Fh	B6:00005Eh
EQQParameter, band 5	B6:000032h	B6:000041h	B6:000050h	B6:00005Fh
EQGainParameter, band 5	B6:000033h	B6:000042h	B6:000051h	B6:000060h

Table 40: Slave Module Channel 1- 4 Post-Mixer Parametric EQ Register Address Table

Register Name	Slave Channel 1 Register Address	Slave Channel 2 Register Address	Slave Channel 3 Register Address	Slave Channel 4 Register Address
EQCenterFrequency Parameter, band 1	B8:000025h	B8:000034h	B8:000043h	B8:000052h
EQQParameter, band 1	B8:000026h	B8:000035h	B8:000044h	B8:000053h
EQGainParameter, band 1	B8:000027h	B8:000036h	B8:000045h	B8:000054h
EQCenterFrequency Parameter, band 2	B8:000028h	B8:000037h	B8:000046h	B8:000055h
EQQParameter, band 2	B8:000029h	B8:000038h	B8:000047h	B8:000056h
EQGainParameter, band 2	B8:00002Ah	B8:000039h	B8:000048h	B8:000057h
EQCenterFrequency Parameter, band 3	B8:00002Bh	B8:00003Ah	B8:000049h	B8:000058h
EQQParameter, band 3	B8:00002Ch	B8:00003Bh	B8:00004Ah	B8:000059h
EQGainParameter, band 3	B8:00002Dh	B8:00003Ch	B8:00004Bh	B8:00005Ah
EQCenterFrequency Parameter, band 4	B8:00002Eh	B8:00003Dh	B8:00004Ch	B8:00005Bh
EQQParameter, band 4	B8:00002Fh	B8:00003Eh	B8:00004Dh	B8:00005Ch
EQGainParameter, band 4	B8:000030h	B8:00003Fh	B8:00004Eh	B8:00005Dh
EQCenterFrequency Parameter, band 5	B8:000031h	B8:000040h	B8:00004Fh	B8:00005Eh
EQQParameter, band 5	B8:000032h	B8:000041h	B8:000050h	B8:00005Fh
EQGainParameter, band 5	B8:000033h	B8:000042h	B8:000051h	B8:000060h

Table 41: Slave Module Channel 1- 4 Post-Mixer Parametric EQ Register Address Table

Register Name	Listen Channel 1 Register Address	Listen Channel 2 Register Address	Listen Channel 3 Register Address	Listen Channel 4 Register Address
EQCenterFrequency Parameter, band 1	BA:000025h	BA:000034h	BA:000043h	BA:000052h
EQQParameter, band 1	BA:000026h	BA:000035h	BA:000044h	BA:000053h
EQGainParameter, band 1	BA:000027h	BA:000036h	BA:000045h	BA:000054h
EQCenterFrequency Parameter, band 2	BA:000028h	BA:000037h	BA:000046h	BA:000055h
EQQParameter, band 2	BA:000029h	BA:000038h	BA:000047h	BA:000056h
EQGainParameter, band 2	BA:00002Ah	BA:000039h	BA:000048h	BA:000057h
EQCenterFrequency Parameter, band 3	BA:00002Bh	BA:00003Ah	BA:000049h	BA:000058h
EQQParameter, band 3	BA:00002Ch	BA:00003Bh	BA:00004Ah	BA:000059h
EQGainParameter, band 3	BA:00002Dh	BA:00003Ch	BA:00004Bh	BA:00005Ah
EQCenterFrequency Parameter, band 4	BA:00002Eh	BA:00003Dh	BA:00004Ch	BA:00005Bh
EQQParameter, band 4	BA:00002Fh	BA:00003Eh	BA:00004Dh	BA:00005Ch
EQGainParameter, band 4	BA:000030h	BA:00003Fh	BA:00004Eh	BA:00005Dh
EQCenterFrequency Parameter, band 5	BA:000031h	BA:000040h	BA:00004Fh	BA:00005Eh
EQQParameter, band 5	BA:000032h	BA:000041h	BA:000050h	BA:00005Fh
EQGainParameter, band 5	BA:000033h	BA:000042h	BA:000051h	BA:000060h

Table 42: Listen Module Channel 1 - 4 Post-Mixer Parametric EQ Register Address Table

Register Name	Listen Channel 1 Register Address	Listen Channel 2 Register Address	Listen Channel 3 Register Address	Listen Channel 4 Register Address
EQCenterFrequency Parameter, band 1	BC:000025h	BC:000034h	BC:000043h	BC:000052h
EQQParameter, band 1	BC:000026h	BC:000035h	BC:000044h	BC:000053h
EQGainParameter, band 1	BC:000027h	BC:000036h	BC:000045h	BC:000054h
EQCenterFrequency Parameter, band 2	BC:000028h	BC:000037h	BC:000046h	BC:000055h
EQQParameter, band 2	BC:000029h	BC:000038h	BC:000047h	BC:000056h
EQGainParameter, band 2	BC:00002Ah	BC:000039h	BC:000048h	BC:000057h
EQCenterFrequency Parameter, band 3	BC:00002Bh	BC:00003Ah	BC:000049h	BC:000058h
EQQParameter, band 3	BC:00002Ch	BC:00003Bh	BC:00004Ah	BC:000059h
EQGainParameter, band 3	BC:00002Dh	BC:00003Ch	BC:00004Bh	BC:00005Ah
EQCenterFrequency Parameter, band 4	BC:00002Eh	BC:00003Dh	BC:00004Ch	BC:00005Bh
EQQParameter, band 4	BC:00002Fh	BC:00003Eh	BC:00004Dh	BC:00005Ch
EQGainParameter, band 4	BC:000030h	BC:00003Fh	BC:00004Eh	BC:00005Dh
EQCenterFrequency Parameter, band 5	BC:000031h	BC:000040h	BC:00004Fh	BC:00005Eh
EQQParameter, band 5	BC:000032h	BC:000041h	BC:000050h	BC:00005Fh
EQGainParameter, band 5	BC:000033h	BC:000042h	BC:000051h	BC:000060h

Table 43: Listen Module Channel 5 - 8 Post-Mixer Parametric EQ Register Address Table

6.8 MIXER

Any inputs of the XM100 module can be mixed and/or routed to any outputs through the Mixer. A configuration of up to 16-inputs/16-outputs is supported using two modules. The DSP within the module will automatically provide a smooth transition between changes to the Mixer.

6.8.1 MIXER GAIN CALCULATION

For each output channel, the Mixer contains 16 registers- one corresponding to each input channel, along with one corresponding to each input channel on a second module that is connected according to Section 4.4, "Matrix-Mixing Across Multiple Modules," on page 21. Each mixer register specifies the gain of a specific input channel that is mixed into a specific output channel.

When two or more modules are connected together to enable matrix-mixing, the registers for inputs 1-8 correspond to the 8 inputs of the module configured as the Master, while the registers for inputs 9-16 correspond to the 8 inputs of the module configured as the Slave. It is important to note that this register mapping is the same in both Master and Slave modules.

For a given Gain in dB, the appropriate parameter is a signed, 24-bit number calculated using the following equation. Valid range for Gain is -100dB to 0dB. Note that the value for Gain is always negative and the resulting parameter is also always negative.

$$MixerGainParameter = -\left[2^{23} \times 10^{\left(\frac{Gain}{20}\right)}\right]$$

The following figure illustrates the organization of MixerGainParameter (MGP) registers. The first number in each entry is the input channel, and the second number is the output channel:

PRELIMINARY

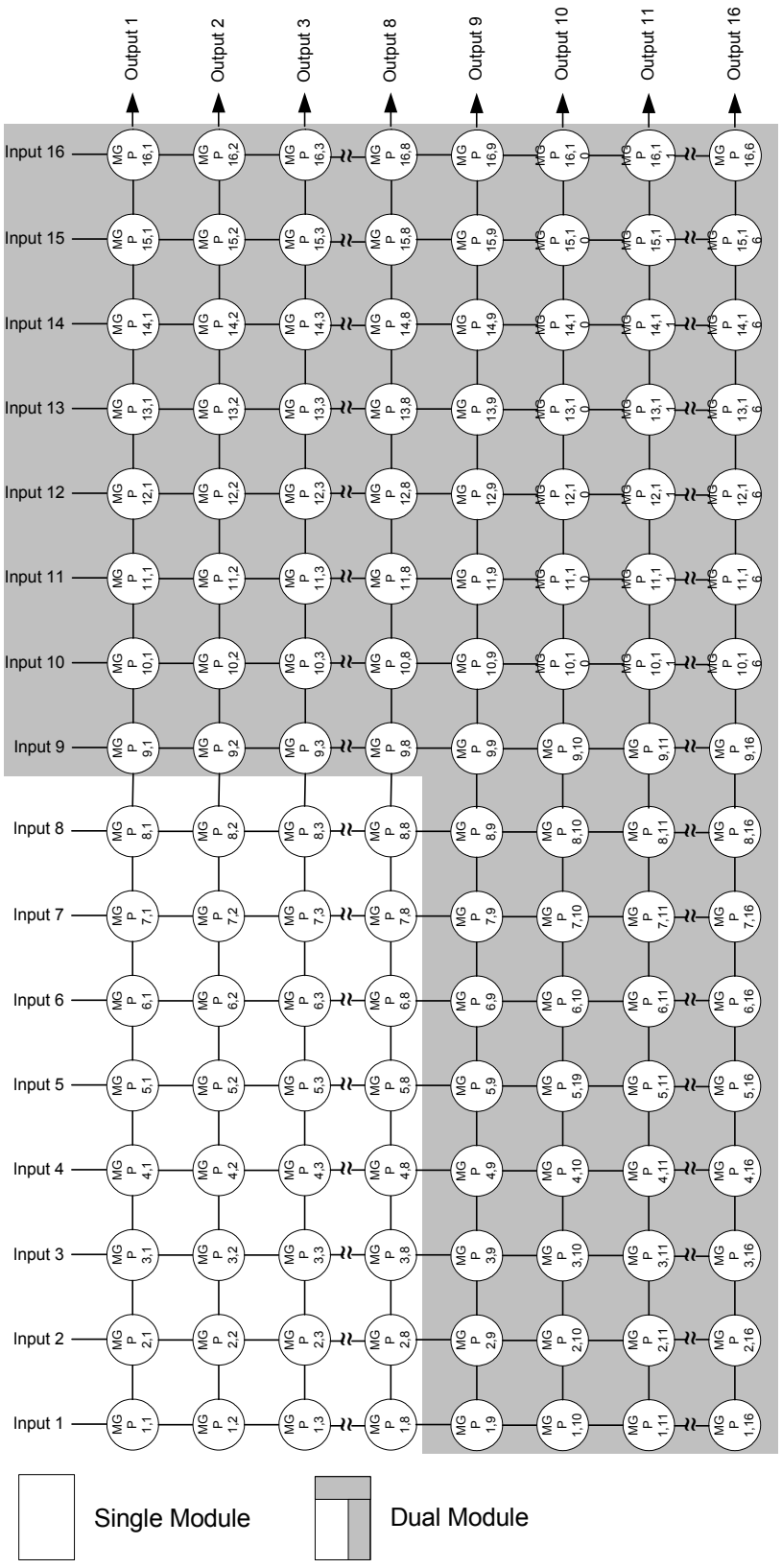

FIGURE 17: Mixer Gain Parameter (MGP) Channel Organization

6.8.2 MIXER REGISTER SUMMARY

Register Name	Minimum Value	Maximum Value	Description
MixerGainParameter	FFFFFFh	800001h	Mixer gain for a given input channel that is mixed into a given output channel

Table 44: Mixer Register Summary

6.8.3 MIXER REGISTER TABLE

Register Name	Master Output Channel 1 Register Address (MGP x,1)	Master Output Channel 2 Register Address (MGP x,2)	Master Output Channel 3 Register Address (MGP x,3)	Master Output Channel 4 Register Address (MGP x,4)
MixerGainParameter, Input Channel 1 (MGP 1,x)	B2:000005h	B2:000009h	B2:00000Dh	B2:000011h
MixerGainParameter, Input Channel 2 (MGP 2,x)	B2:000006h	B2:00000Ah	B2:00000Eh	B2:000012h
MixerGainParameter, Input Channel 3 (MGP 3,x)	B2:000007h	B2:00000Bh	B2:00000Fh	B2:000013h
MixerGainParameter, Input Channel 4 (MGP 4,x)	B2:000008h	B2:00000Ch	B2:000010h	B2:000014h
MixerGainParameter, Input Channel 5 (MGP 5,x)	B2:0000D1h	B2:0000DDh	B2:0000E9h	B2:0000F5h
MixerGainParameter, Input Channel 6 (MGP 6,x)	B2:0000D2h	B2:0000DEh	B2:0000EAh	B2:0000F6h
MixerGainParameter, Input Channel 7 (MGP 7,x)	B2:0000D3h	B2:0000DFh	B2:0000EBh	B2:0000F7h
MixerGainParameter, Input Channel 8 (MGP 8,x)	B2:0000D4h	B2:0000E0h	B2:0000ECh	B2:0000F8h
MixerGainParameter, Input Channel 9 (MGP 9,x)	B2:0000D5h	B2:0000E1h	B2:0000EDh	B2:0000F9h
MixerGainParameter, Input Channel 10 (MGP 10,x)	B2:0000D6h	B2:0000E2h	B2:0000EEh	B2:0000FAh
MixerGainParameter, Input Channel 11 (MGP 11,x)	B2:0000D7h	B2:0000E3h	B2:0000EFh	B2:0000FBh
MixerGainParameter, Input Channel 12 (MGP 12,x)	B2:0000D8h	B2:0000E4h	B2:0000F0h	B2:0000FCh
MixerGainParameter, Input Channel 13 (MGP 31,x)	B2:0000D9h	B2:0000E5h	B2:0000F1h	B2:0000FDh
MixerGainParameter, Input Channel 14 (MGP 14,x)	B2:0000DAh	B2:0000E6h	B2:0000F2h	B2:0000FEh

Table 45: Master Module Channel 1- 4 Mixer Register Address Table

Register Name	Master Output Channel 1 Register Address (MGP x,1)	Master Output Channel 2 Register Address (MGP x,2)	Master Output Channel 3 Register Address (MGP x,3)	Master Output Channel 4 Register Address (MGP x,4)
MixerGainParameter, Input Channel 15 (MGP 15,x)	B2:0000DBh	B2:0000E7h	B2:0000F3h	B2:0000FFh
MixerGainParameter, Input Channel 16 (MGP 16,x)	B2:0000DCh	B2:0000E8h	B2:0000F4h	000100h

Table 45: Master Module Channel 1- 4 Mixer Register Address Table

Register Name	Master Output Channel 5 Register Address (MGP x,1)	Master Output Channel 6 Register Address (MGP x,2)	Master Output Channel 7 Register Address (MGP x,3)	Master Output Channel 8 Register Address (MGP x,4)
MixerGainParameter, Input Channel 1 (MGP 1,x)	B4:000005h	B4:000009h	B4:00000Dh	B4:000011h
MixerGainParameter, Input Channel 2 (MGP 2,x)	B4:000006h	B4:00000Ah	B4:00000Eh	B4:000012h
MixerGainParameter, Input Channel 3 (MGP 3,x)	B4:000007h	B4:00000Bh	B4:00000Fh	B4:000013h
MixerGainParameter, Input Channel 4 (MGP 4,x)	B4:000008h	B4:00000Ch	B4:000010h	B4:000014h
MixerGainParameter, Input Channel 5 (MGP 5,x)	B4:0000D1h	B4:0000DDh	B4:0000E9h	B4:0000F5h
MixerGainParameter, Input Channel 6 (MGP 6,x)	B4:0000D2h	B4:0000DEh	B4:0000EAh	B4:0000F6h
MixerGainParameter, Input Channel 7 (MGP 7,x)	B4:0000D3h	B4:0000DFh	B4:0000EBh	B4:0000F7h
MixerGainParameter, Input Channel 8 (MGP 8,x)	B4:0000D4h	B4:0000E0h	B4:0000ECh	B4:0000F8h
MixerGainParameter, Input Channel 9 (MGP 9,x)	B4:0000D5h	B4:0000E1h	B4:0000EDh	B4:0000F9h
MixerGainParameter, Input Channel 10 (MGP 10,x)	B4:0000D6h	B4:0000E2h	B4:0000EEh	B4:0000FAh
MixerGainParameter, Input Channel 11 (MGP 11,x)	B4:0000D7h	B4:0000E3h	B4:0000EFh	B4:0000FBh
MixerGainParameter, Input Channel 12 (MGP 12,x)	B4:0000D8h	B4:0000E4h	B4:0000F0h	B4:0000FCh
MixerGainParameter, Input Channel 13 (MGP 13,x)	B4:0000D9h	B4:0000E5h	B4:0000F1h	B4:0000FDh
MixerGainParameter, Input Channel 14 (MGP 14,x)	B4:0000DAh	B4:0000E6h	B4:0000F2h	B4:0000FEh
MixerGainParameter, Input Channel 15 (MGP 15,x)	B4:0000DBh	B4:0000E7h	B4:0000F3h	B4:0000FFh

Table 46: Master Module Channel 5 - 8 Mixer Register Address Table

Register Name	Master Output Channel 5 Register Address (MGP x,1)	Master Output Channel 6 Register Address (MGP x,2)	Master Output Channel 7 Register Address (MGP x,3)	Master Output Channel 8 Register Address (MGP x,4)
MixerGainParameter, Input Channel 16 (MGP 16,x)	B4:0000DCh	B4:0000E8h	B4:0000F4h	B4:000100h

Table 46: Master Module Channel 5 - 8 Mixer Register Address Table

Register Name	Slave Output Channel 1 Register Address (MGP x,1)	Slave Output Channel 2 Register Address (MGP x,2)	Slave Output Channel 3 Register Address (MGP x,3)	Slave Output Channel 4 Register Address (MGP x,4)
MixerGainParameter, Input Channel 1 (MGP 1,x)	B6:000005h	B6:000009h	B6:00000Dh	B6:000011h
MixerGainParameter, Input Channel 2 (MGP 2,x)	B6:000006h	B6:00000Ah	B6:00000Eh	B6:000012h
MixerGainParameter, Input Channel 3 (MGP 3,x)	B6:000007h	B6:00000Bh	B6:00000Fh	B6:000013h
MixerGainParameter, Input Channel 4 (MGP 4,x)	B6:000008h	B6:00000Ch	B6:000010h	B6:000014h
MixerGainParameter, Input Channel 5 (MGP 5,x)	B6:0000D1h	B6:0000DDh	B6:0000E9h	B6:0000F5h
MixerGainParameter, Input Channel 6 (MGP 6,x)	B6:0000D2h	B6:0000DEh	B6:0000EAh	B6:0000F6h
MixerGainParameter, Input Channel 7 (MGP 7,x)	B6:0000D3h	B6:0000DFh	B6:0000EBh	B6:0000F7h
MixerGainParameter, Input Channel 8 (MGP 8,x)	B6:0000D4h	B6:0000E0h	B6:0000ECh	B6:0000F8h
MixerGainParameter, Input Channel 9 (MGP 9,x)	B6:0000D5h	B6:0000E1h	B6:0000EDh	B6:0000F9h
MixerGainParameter, Input Channel 10 (MGP 10,x)	B6:0000D6h	B6:0000E2h	B6:0000EEh	B6:0000FAh
MixerGainParameter, Input Channel 11 (MGP 11,x)	B6:0000D7h	B6:0000E3h	B6:0000EFh	B6:0000FBh
MixerGainParameter, Input Channel 12 (MGP 12,x)	B6:0000D8h	B6:0000E4h	B6:0000F0h	B6:0000FCh
MixerGainParameter, Input Channel 13 (MGP 13,x)	B6:0000D9h	B6:0000E5h	B6:0000F1h	B6:0000FDh
MixerGainParameter, Input Channel 14 (MGP 14,x)	B6:0000DAh	B6:0000E6h	B6:0000F2h	B6:0000FEh
MixerGainParameter, Input Channel 15 (MGP 15,x)	B6:0000DBh	B6:0000E7h	B6:0000F3h	B6:0000FFh
MixerGainParameter, Input Channel 16 (MGP 16,x)	B6:0000DCh	B6:0000E8h	B6:0000F4h	B6:000100h

Table 47: Slave Module Channel 1- 4 Mixer Register Address Table

Register Name	Slave Output Channel 5 Register Address (MGP x,1)	Slave Output Channel 6 Register Address (MGP x,2)	Slave Output Channel 7 Register Address (MGP x,3)	Slave Output Channel 8 Register Address (MGP x,4)
MixerGainParameter, Input Channel 1 (MGP 1,x)	B8:000005h	B8:000009h	B8:00000Dh	B8:000011h
MixerGainParameter, Input Channel 2 (MGP 2,x)	B8:000006h	B8:00000Ah	B8:00000Eh	B8:000012h
MixerGainParameter, Input Channel 3 (MGP 3,x)	B8:000007h	B8:00000Bh	B8:00000Fh	B8:000013h
MixerGainParameter, Input Channel 4 (MGP 4,x)	B8:000008h	B8:00000Ch	B8:000010h	B8:000014h
MixerGainParameter, Input Channel 5 (MGP 5,x)	B8:0000D1h	B8:0000DDh	B8:0000E9h	B8:0000F5h
MixerGainParameter, Input Channel 6 (MGP 6,x)	B8:0000D2h	B8:0000DEh	B8:0000EAh	B8:0000F6h
MixerGainParameter, Input Channel 7 (MGP 7,x)	B8:0000D3h	B8:0000DFh	B8:0000EBh	B8:0000F7h
MixerGainParameter, Input Channel 8 (MGP 8,x)	B8:0000D4h	B8:0000E0h	B8:0000ECh	B8:0000F8h
MixerGainParameter, Input Channel 9 (MGP 9,x)	B8:0000D5h	B8:0000E1h	B8:0000EDh	B8:0000F9h
MixerGainParameter, Input Channel 10 (MGP 10,x)	B8:0000D6h	B8:0000E2h	B8:0000EEh	B8:0000FAh
MixerGainParameter, Input Channel 11 (MGP 11,x)	B8:0000D7h	B8:0000E3h	B8:0000EFh	B8:0000FBh
MixerGainParameter, Input Channel 12 (MGP 12,x)	B8:0000D8h	B8:0000E4h	B8:0000F0h	B8:0000FCh
MixerGainParameter, Input Channel 13 (MGP 31,x)	B8:0000D9h	B8:0000E5h	B8:0000F1h	B8:0000FDh
MixerGainParameter, Input Channel 14 (MGP 14,x)	B8:0000DAh	B8:0000E6h	B8:0000F2h	B8:0000FEh
MixerGainParameter, Input Channel 15 (MGP 15,x)	B8:0000DBh	B8:0000E7h	B8:0000F3h	B8:0000FFh
MixerGainParameter, Input Channel 16 (MGP 16,x)	B8:0000DCh	B8:0000E8h	B8:0000F4h	B8:000100h

Table 48: Slave Module Channel 5 - 8 Mixer Register Address Table

Register Name	Listen Output Channel 1 Register Address (MGP x,1)	Listen Output Channel 2 Register Address (MGP x,2)	Listen Output Channel 3 Register Address (MGP x,3)	Listen Output Channel 4 Register Address (MGP x,4)
MixerGainParameter, Input Channel 1 (MGP 1,x)	BA:000005h	BA:000009h	BA:00000Dh	BA:000011h

Table 49: Listen Module Channel 1 - 4 Mixer Register Address Table

Register Name	Listen Output Channel 1 Register Address (MGP x,1)	Listen Output Channel 2 Register Address (MGP x,2)	Listen Output Channel 3 Register Address (MGP x,3)	Listen Output Channel 4 Register Address (MGP x,4)
MixerGainParameter, Input Channel 2 (MGP 2,x)	BA:000006h	BA:00000Ah	BA:00000Eh	BA:000012h
MixerGainParameter, Input Channel 3 (MGP 3,x)	BA:000007h	BA:00000Bh	BA:00000Fh	BA:000013h
MixerGainParameter, Input Channel 4 (MGP 4,x)	BA:000008h	BA:00000Ch	BA:000010h	BA:000014h
MixerGainParameter, Input Channel 5 (MGP 5,x)	BA:0000D1h	BA:0000DDh	BA:0000E9h	BA:0000F5h
MixerGainParameter, Input Channel 6 (MGP 6,x)	BA:0000D2h	BA:0000DEh	BA:0000EAh	BA:0000F6h
MixerGainParameter, Input Channel 7 (MGP 7,x)	BA:0000D3h	BA:0000DFh	BA:0000EBh	BA:0000F7h
MixerGainParameter, Input Channel 8 (MGP 8,x)	BA:0000D4h	BA:0000E0h	BA:0000ECh	BA:0000F8h
MixerGainParameter, Input Channel 9 (MGP 9,x)	BA:0000D5h	BA:0000E1h	BA:0000EDh	BA:0000F9h
MixerGainParameter, Input Channel 10 (MGP 10,x)	BA:0000D6h	BA:0000E2h	BA:0000EEh	BA:0000FAh
MixerGainParameter, Input Channel 11 (MGP 11,x)	BA:0000D7h	BA:0000E3h	BA:0000EFh	BA:0000FBh
MixerGainParameter, Input Channel 12 (MGP 12,x)	BA:0000D8h	BA:0000E4h	BA:0000F0h	BA:0000FCh
MixerGainParameter, Input Channel 13 (MGP 31,x)	BA:0000D9h	BA:0000E5h	BA:0000F1h	BA:0000FDh
MixerGainParameter, Input Channel 14 (MGP 14,x)	BA:0000DAh	BA:0000E6h	BA:0000F2h	BA:0000FEh
MixerGainParameter, Input Channel 15 (MGP 15,x)	BA:0000DBh	BA:0000E7h	BA:0000F3h	BA:0000FFh
MixerGainParameter, Input Channel 16 (MGP 16,x)	BA:0000DCh	BA:0000E8h	BA:0000F4h	BA:000100h

Table 49: Listen Module Channel 1 - 4 Mixer Register Address Table

Register Name	Listen Output Channel 4 Register Address (MGP x,1)	Listen Output Channel 5 Register Address (MGP x,2)	Listen Output Channel 6 Register Address (MGP x,3)	Listen Output Channel 7 Register Address (MGP x,4)
MixerGainParameter, Input Channel 1 (MGP 1,x)	BC:000005h	BC:000009h	BC:00000Dh	BC:000011h
MixerGainParameter, Input Channel 2 (MGP 2,x)	BC:000006h	BC:00000Ah	BC:00000Eh	BC:000012h

Table 50: Listen Module Channel1 - 4 Mixer Register Address Table

Register Name	Listen Output Channel 4 Register Address (MGP x,1)	Listen Output Channel 5 Register Address (MGP x,2)	Listen Output Channel 6 Register Address (MGP x,3)	Listen Output Channel 7 Register Address (MGP x,4)
MixerGainParameter, Input Channel 3 (MGP 3,x)	BC:000007h	BC:00000Bh	BC:00000Fh	BC:000013h
MixerGainParameter, Input Channel 4 (MGP 4,x)	BC:000008h	BC:00000Ch	BC:000010h	BC:000014h
MixerGainParameter, Input Channel 5 (MGP 5,x)	BC:0000D1h	BC:0000DDh	BC:0000E9h	BC:0000F5h
MixerGainParameter, Input Channel 6 (MGP 6,x)	BC:0000D2h	BC:0000DEh	BC:0000EAh	BC:0000F6h
MixerGainParameter, Input Channel 7 (MGP 7,x)	BC:0000D3h	BC:0000DFh	BC:0000EBh	BC:0000F7h
MixerGainParameter, Input Channel 8 (MGP 8,x)	BC:0000D4h	BC:0000E0h	BC:0000ECh	BC:0000F8h
MixerGainParameter, Input Channel 9 (MGP 9,x)	BC:0000D5h	BC:0000E1h	BC:0000EDh	BC:0000F9h
MixerGainParameter, Input Channel 10 (MGP 10,x)	BC:0000D6h	BC:0000E2h	BC:0000EEh	BC:0000FAh
MixerGainParameter, Input Channel 11 (MGP 11,x)	BC:0000D7h	BC:0000E3h	BC:0000EFh	BC:0000FBh
MixerGainParameter, Input Channel 12 (MGP 12,x)	BC:0000D8h	BC:0000E4h	BC:0000F0h	BC:0000FCh
MixerGainParameter, Input Channel 13 (MGP 31,x)	BC:0000D9h	BC:0000E5h	BC:0000F1h	BC:0000FDh
MixerGainParameter, Input Channel 14 (MGP 14,x)	BC:0000DAh	BC:0000E6h	BC:0000F2h	BC:0000FEh
MixerGainParameter, Input Channel 15 (MGP 15,x)	BC:0000DBh	BC:0000E7h	BC:0000F3h	BC:0000FFh
MixerGainParameter, Input Channel 16 (MGP 16,x)	BC:0000DCh	BC:0000E8h	BC:0000F4h	BC:000100h

Table 50: Listen Module Channel1 - 4 Mixer Register Address Table

6.9 ADJUSTABLE TIME DELAY

Each channel of the XM100 module contains an Adjustable Time Delay for each channel. The DSP within the module will automatically provide a smooth transition between changes to the Adjustable Time Delay.

6.9.1 TIME DELAY CALCULATION

For a given Delay in milliseconds, the appropriate parameter is an unsigned, 24-bit integer calculated using the following equation. Valid range for Delay is 0 to 3.984375 mS which is based on a range of 0 to 255 for TimeDelayParameter.

$$TimeDelayParameter = Delay \times 64$$

6.9.2 TIME DELAY REGISTER SUMMARY

Register Name	Minimum Value	Maximum Value	Description
TimeDelayParameter	000000h	0000FFh	Per-channel Time Delay

Table 51: Adjustable Time Delay Register Summary

6.9.3 TIME DELAY REGISTER ADDRESS TABLE

Register Name	Master Channel 1 Register Address	Master Channel 2 Register Address	Master Channel 3 Register Address	Master Channel 4 Register Address
TimeDelayParameter	B2:000B5h	B2:000B6h	B2:000B7h	B2:000B8h

Table 52: Master Module Channel 1- 4 Adjustable Time Delay Register Address Table

Register Name	Master Channel 5 Register Address	Master Channel 6 Register Address	Master Channel 7 Register Address	Master Channel 8 Register Address
TimeDelayParameter	B4:000B5h	B4:000B6h	B4:000B7h	B4:000B8h

Table 53: Master Module Channel 5 - 8 Adjustable Time Delay Register Address Table

Register Name	Slave Channel 1 Register Address	Slave Channel 2 Register Address	Slave Channel 3 Register Address	Slave Channel 4 Register Address
TimeDelayParameter	B6:000B5h	B6:000B6h	B6:000B7h	B6:000B8h

Table 54: Slave Module Channel 1- 4 Adjustable Time Delay Register Address Table

Register Name	Slave Channel 5 Register Address	Slave Channel 6 Register Address	Slave Channel 7 Register Address	Slave Channel 8 Register Address
TimeDelayParameter	B8:000B5h	B8:000B6h	B8:000B7h	B8:000B8h

Table 55: Slave Module Channel 5 - 8 Adjustable Time Delay Register Address Table

Register Name	Slave Channel 1 Register Address	Slave Channel 2 Register Address	Slave Channel 3 Register Address	Slave Channel 4 Register Address
TimeDelayParameter	BA:000B5h	BA:000B6h	BA:000B7h	BA:000B8h

Table 56: Listen Module Channel 1- 4 Adjustable Time Delay Register Address Table

Register Name	Slave Channel 5 Register Address	Slave Channel 6 Register Address	Slave Channel 7 Register Address	Slave Channel 8 Register Address
TimeDelayParameter	BC:000B5h	BC:000B6h	BC:000B7h	BC:000B8h

Table 57: Listen Module Channel 5 - 8 Adjustable Time Delay Register Address Table

6.10 COMPRESSOR

The XM100 module provides individual software-controlled Compressors for each channel. Each Compressor has configurable Compression Ratio, Threshold, Attack and Release Time, as well as Makeup Gain. The DSP within the module will automatically provide a smooth transition between changes are written to the Compressor settings.

6.10.1 THRESHOLD CALCULATION

The Compressor reduces the gain of signals which exceed a given threshold. For a given Threshold in dB, the appropriate parameter is a signed, 24-bit number calculated using the following equation. Valid range for Threshold is -90dB to 0dB.

$$CompressorThresholdParameter = 2^{23} \times [(0.010381025 \times Threshold) + 0.96875]$$

6.10.2 ATTACK TIME CALCULATION

The Attack Time is the rate at which the gain is reduced when the input exceeds the Threshold. For a given Attack Time in milliseconds, the appropriate parameter is a signed, 24-bit number. Valid range for attack time is 1ms to 100ms. Below is a table of values for Attack Time. Other values can be calculated by linearly interpolating between these sample values.

Attack Time	CompressorAttackTime Parameter
1ms	1C2F43h
10ms	032900h
100ms	0051D1h

Table 58: Values for Attack Time

6.10.3 RELEASE TIME CALCULATION

The Release Time is the rate at which the gain is increased when the input falls below the Threshold. For a given Release Time in milliseconds, the appropriate parameter is a signed, 24-bit number. Valid range for Release Time is 1ms to 100ms. Below is a table of values for Release Time. Other values can be calculated by linearly interpolating between these sample values.

Release Time	CompressorReleaseTime Parameter
1ms	1C2F43h
10ms	032900h
100ms	0051D1h

Table 59: Values for Release Time

6.10.4 COMPRESSOR RATIO CALCULATION

The Compressor Ratio is the number of dB above the Threshold that the input level must increase in order to increase the output level by 1dB. For a given Compressor Ratio in dB, the appropriate parameter is a signed, 24-bit number calculated using the following equation. Valid range for Compressor Ratio is 1 to 100. Note that a ratio of 1 disables the compressor, while a ratio of above 10 causes the Compressor to behave as a Limiter.

$$CompressorRatioParameter = 2^{23} \times \left(1 - \left(\frac{1}{Ratio}\right)\right)$$

6.10.5 MAKEUP GAIN CALCULATION

Depending on the settings for Threshold and Compressor Ratio, additional Makeup Gain may be necessary to reach a full-scale output. For a given Makeup Gain in dB, the appropriate parameter is a signed, 24-bit number calculated using the following equation. Valid range for Makeup Gain is 0dB to +18.06dB.

$$CompressorMakeupGainParameter = 2^{23} \times 10^{[(Gain \times 0.05) - 0.90309]}$$

6.10.6 COMPRESSOR REGISTER SUMMARY

Register Name	Minimum Value	Maximum Value	Description
CompressorThreshold Parameter	04691Ch	7C0000h	Per-channel Compressor threshold

Table 60: Compressor Register Summary

Register Name	Minimum Value	Maximum Value	Description
CompressorAttackTime Parameter	0051D1h	1C2F43h	Per-channel Compressor attack time
CompressorReleaseTime Parameter	0051D1h	1C2F43h	Per-channel Compressor release time
CompressorRatioParameter	000000h	7EB851h	Per-channel Compressor ratio
CompressorMakeupGain Parameter	0FFFFFh	7FFFFFh	Per-channel Compressor makeup gain

Table 60: Compressor Register Summary

6.10.7 COMPRESSOR REGISTER ADDRESS TABLE

Register Name	Master Channel 1 Register Address	Master Channel 2 Register Address	Master Channel 3 Register Address	Master Channel 4 Register Address
CompressorThreshold Parameter	B2:000BAh	B2:000C0h	B2:000C6h	B2:000CCh
CompressorAttackTime Parameter	B2:000BCh	B2:000C2h	B2:000C8h	B2:000CEh
CompressorReleaseTime Parameter	B2:000BDh	B2:000C3h	B2:000C9h	B2:000CFh
CompressorRatioParameter	B2:000BBh	B2:000C1h	B2:000C7h	B2:000CDh
CompressorMakeupGain Parameter	B2:000BEh	B2:000C4h	B2:000CAh	B2:000D0h

Table 61: Master Module Channel 1- 4 Compressor Register Address Table

Register Name	Master Channel 5 Register Address	Master Channel 6 Register Address	Master Channel 7 Register Address	Master Channel 8 Register Address
CompressorThreshold Parameter	B4:000BAh	B4:000C0h	B4:000C6h	B4:000CCh
CompressorAttackTime Parameter	B4:000BCh	B4:000C2h	B4:000C8h	B4:000CEh
CompressorReleaseTime Parameter	B4:000BDh	B4:000C3h	B4:000C9h	B4:000CFh
CompressorRatioParameter	B4:000BBh	B4:000C1h	B4:000C7h	B4:000CDh
CompressorMakeupGain Parameter	B4:000BEh	B4:000C4h	B4:000CAh	B4:000D0h

Table 62: Master Module Channel 5 - 8 Compressor Register Address Table

Register Name	Slave Channel 1 Register Address	Slave Channel 2 Register Address	Slave Channel 3 Register Address	Slave Channel 4 Register Address
CompressorThreshold Parameter	B6:000BAh	B6:000C0h	B6:000C6h	B6:000CCh
CompressorAttackTime Parameter	B6:000BCh	B6:000C2h	B6:000C8h	B6:000CEh
CompressorReleaseTime Parameter	B6:000BDh	B6:000C3h	B6:000C9h	B6:000CFh
CompressorRatioParameter	B6:000BBh	B6:000C1h	B6:000C7h	B6:000CDh

Table 63: Slave Module Channel 1- 4 Compressor Register Address Table

Register Name	Slave Channel 1 Register Address	Slave Channel 2 Register Address	Slave Channel 3 Register Address	Slave Channel 4 Register Address
CompressorMakeupGain Parameter	B6:000BEh	B6:000C4h	B6:000CAh	B6:000D0h

Table 63: Slave Module Channel 1- 4 Compressor Register Address Table

Register Name	Slave Channel 5 Register Address	Slave Channel 6 Register Address	Slave Channel 7 Register Address	Slave Channel 8 Register Address
CompressorThreshold Parameter	B8:000BAh	B8:000C0h	B8:000C6h	B8:000CCh
CompressorAttackTime Parameter	B8:000BCh	B8:000C2h	B8:000C8h	B8:000CEh
CompressorReleaseTime Parameter	B8:000BDh	B8:000C3h	B8:000C9h	B8:000CFh
CompressorRatioParameter	B8:000BBh	B8:000C1h	B8:000C7h	B8:000CDh
CompressorMakeupGain Parameter	B8:000BEh	B8:000C4h	B8:000CAh	B8:000D0h

Table 64: Slave Module Channel 5 - 8 Compressor Register Address Table

Register Name	Listen Channel 1 Register Address	Listen Channel 2 Register Address	Listen Channel 3 Register Address	Listen Channel 4 Register Address
CompressorThreshold Parameter	BA:000BAh	BA:000C0h	BA:000C6h	BA:000CCh
CompressorAttackTime Parameter	BA:000BCh	BA:000C2h	BA:000C8h	BA:000CEh
CompressorReleaseTime Parameter	BA:000BDh	BA:000C3h	BA:000C9h	BA:000CFh
CompressorRatioParameter	BA:000BBh	BA:000C1h	BA:000C7h	BA:000CDh
CompressorMakeupGain Parameter	BA:000BEh	BA:000C4h	BA:000CAh	BA:000D0h

Table 65: Listen Module Channel 1- 4 Compressor Register Address Table

Register Name	Listen Channel 5 Register Address	Listen Channel 6 Register Address	Listen Channel 7 Register Address	Listen Channel 8 Register Address
CompressorThreshold Parameter	BC:000BAh	BC:000C0h	BC:000C6h	BC:000CCh
CompressorAttackTime Parameter	BC:000BCh	BC:000C2h	BC:000C8h	BC:000CEh
CompressorReleaseTime Parameter	BC:000BDh	BC:000C3h	BC:000C9h	BC:000CFh
CompressorRatioParameter	BC:000BBh	BC:000C1h	BC:000C7h	BC:000CDh
CompressorMakeupGain Parameter	BC:000BEh	BC:000C4h	BC:000CAh	BC:000D0h

Table 66: Listen Module Channel 5 - 6 Compressor Register Address Table

6.11 VOLUME CONTROL

CONSUMER

Software-controlled Master Volume Control is provided, which controls the final gain for all output channels. Individual attenuators are also provided for each channel. The DSP within the module will automatically provide a smooth transition between changes to the Volume Control.

6.11.1 MASTER VOLUME CALCULATION

For a given Master Volume in dB, the appropriate parameter is a signed, 24-bit number calculated using the following equation. Valid range for Master Volume is -100dB to +18.06dB.

$$MasterVolumeParameter = 2^{23} \times 10^{\left[\frac{(MasterVolume - 18.06)}{20}\right]}$$

6.11.2 CHANNEL ATTENUATION CALCULATION

For a given Channel Attenuation in dB, the appropriate parameter is a signed, 24-bit negative number calculated using the following equation. Valid range for Channel Attenuation is 0dB to 120dB. Note that channel attenuation is positive, such that a value of 0dB results in no attenuation.

$$ChannelAttenuationParameter = -\left[2^{23} \times 10^{\left(\frac{-Attenuation}{20}\right)}\right]$$

The Channel Attenuation Parameter can also be used to invert the polarity of a channel. To do this, remove the negative sign from the formula above and recalculate the ChannelAttenuationParameter:

$$InvertedChannelAttenuationParameter = 2^{23} \times 10^{\left(\frac{-Attenuation}{20}\right)}$$

Register Name	Minimum Value	Maximum Value	Description
MasterVolumeParameter	00000Ah	7FFFFFh	Master Volume for channels 1-4
ChannelAttenuationParamter (with polarity inversion)	FFFFFFh 7FFFFFh	800001h 000000h	Per-channel attenuation setting Per-channel attenuation setting (with polarity inversion)

Table 67: Volume Control Register Summary

PRELIMINARY

6.11.3 VOLUME CONTROL REGISTER SUMMARY

6.11.4 VOLUME CONTROL REGISTER ADDRESS TABLE

Register Name	Master Channel 1 Register Address	Master Channel 2 Register Address	Master Channel 3 Register Address	Master Channel 4 Register Address
MasterVolumeParameter	B2:000000h			
ChannelAttenuation Parameter	B2:000001h	B2:000002h	B2:000003h	B2:000004h

Table 68: Master Module Channel 1- 4 Volume Control Register Address Table

Register Name	Master Channel 5 Register Address	Master Channel 6 Register Address	Master Channel 7 Register Address	Master Channel 8 Register Address
MasterVolumeParameter	B4:000000h			
ChannelAttenuation Parameter	B4:000001h	B4:000002h	B4:000003h	B4:000004h

Table 69: Master Module Channel 5 - 8 Volume Control Register Address Table

Register Name	Slave Channel 1 Register Address	Slave Channel 2 Register Address	Slave Channel 3 Register Address	Slave Channel 4 Register Address
MasterVolumeParameter	B6:000000h			
ChannelAttenuation Parameter	B6:000001h	B6:000002h	B6:000003h	B6:000004h

Table 70: Slave Module Channel 1- 4 Volume Control Register Address Table

Register Name	Slave Channel 5 Register Address	Slave Channel 6 Register Address	Slave Channel 7 Register Address	Slave Channel 8 Register Address
MasterVolumeParameter	B8:000000h			
ChannelAttenuation Parameter	B8:000001h	B8:000002h	B8:000003h	B8:000004h

Table 71: Slave Module Channel 5 - 8 Volume Control Register Address Table

Register Name	Listen Channel 1 Register Address	Listen Channel 2 Register Address	Listen Channel 3 Register Address	Listen Channel 4 Register Address
MasterVolumeParameter	BA:000000h			
ChannelAttenuation Parameter	BA:000001h	BA:000002h	BA:000003h	BA:000004h

Table 72: Listen Module Channel 1- 4 Volume Control Register Address Table

Register Name	Listen Channel 5 Register Address	Listen Channel 6 Register Address	Listen Channel 7 Register Address	Listen Channel 8 Register Address
MasterVolumeParameter	BC:000000h			
ChannelAttenuation Parameter	BC:000001h	BC:000002h	BC:000003h	BC:000004h

Table 73: Listen Module Channel 5 - 8 Volume Control Register Address Table

7 PHYSICAL DIMENSIONS

CONSUMER

PRELIMINARY

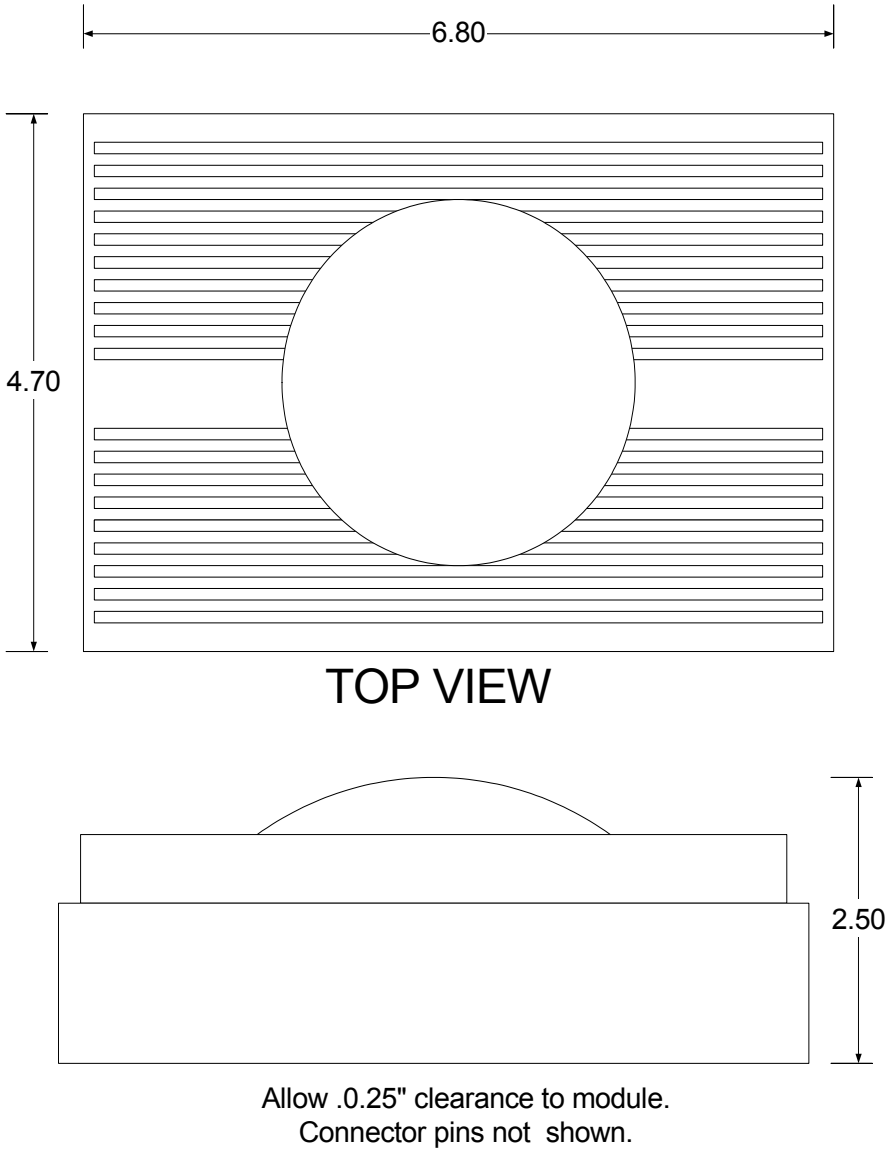

FIGURE 18: Physical Dimensions (not to scale) Outline represents the maximum physical dimension. Final product appearance is subject to change.

7.1 PIN LOCATIONS AND PCB DIMENSIONS

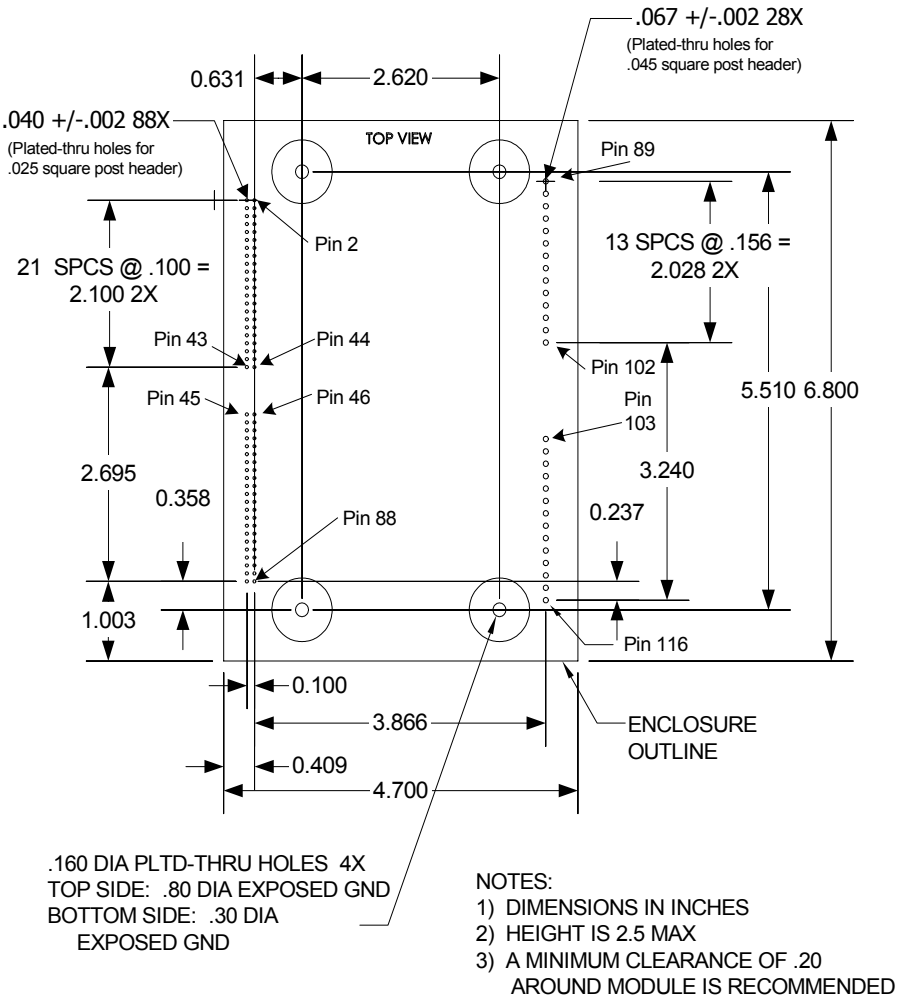

FIGURE 19: Pin Locations (View from top, not to scale)

7.2 MOUNTING HARDWARE

It is recommended that the module be secured to its PWB assemble with a M3 thread forming machine screw in 4 places.

7.3 AMBIENT OPERATING CONDITIONS

The amplifier generates modest heat and is designed to dissipate that heat to the ambient environment.When the ambient temperature surrounding the module exceeds a safe operating point, the amplifier will gracefully reduce output power of the amplifier. This allows the amplifier to run at a reduced capability rather than an abrupt power down. A “fail-safe” mode will disable the amplifier if the internal temperature exceeds a safe operating limit. The amplifier will return to normal operation when the operating temperatures fall below the “fail-safe” or reduced power temperature thresholds. Figure 20 shows a recommended operating range and power derating temperatures.

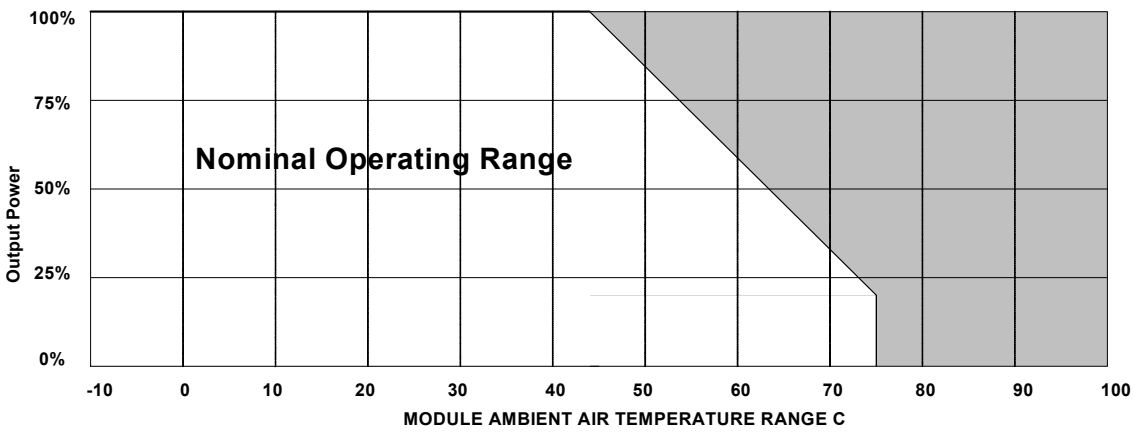

FIGURE 20: Nominal Operating Range

8 DOCUMENT REVISION HISTORY

5/7/2004 - Revised mechanical pin locations shown in data sheet versions shown in data sheets 0.5xx or earlier
Revised Pinout as shown in data sheet versions 0.5xx or earlier.
Revised mechanical dimensions
Updated module controller interface addressing mode
Revised Register addressing tables
Added Nominal Operating Range
Added Master/Slave/Listen Register Addresses
Revised 16 x 24 Multi-Module Mixing
Revised Electrical level specifications
Reset input pin is polarity is now active low. Reset must be driven with open collector driver.
Tone control and 5 channel EQ now post mixer
3 band EQ now pre mixer
Added Document Table Of Contents

5/10/04 Revision 1.11
Corrected supported sample rates for I^2S and S/PDIF inputs.