

# A CONCEPTUALLY NEW HIGH-FREQUENCY SWITCHED-MODE POWER AMPLIFIER TECHNIQUE ELIMINATES CURRENT RIPPLE

SLOBODAN ĆUK AND ROBERT W. ERICKSON

## ABSTRACT

A new switching power amplifier is proposed which has a number of advantages over the conventional buck type design. The new amplifier is based on a recently announced optimum topology switching dc-to-dc converter used in a push-pull-like configuration. All of the advantages of the new converter, such as high efficiency, small size and weight, excellent dynamic performance, together with both input and output current nonpulsating, are present in the new design. In addition, the use of coupled-inductor extension of the new converter results in a high performance amplifier with complete elimination of the switching ripple. Thus, the new switching amplifier has a potential for a wide range of applications: from high efficiency, small size and weight servo power amplifier to a low cost, high performance audio power amplifier.

## 1. INTRODUCTION

Switching power supplies and regulators ("switchers") are coming into a widespread use. Owing to their much higher efficiency, smaller size and weight and relatively low cost, they are displacing the conventional linear power supplies even at lower power levels (25 Watts at present). While a substantial effort was made in recent years toward the development of modelling as well as design techniques for these complex switching systems, substantially less work and attention has been devoted to their natural outgrowth - switching power amplifiers.

It is quite natural, then, that the principles of the operation of switching power amplifiers are not widely known. Therefore, a brief review of their operation is included in Section 2. This review of switching power amplifiers, which are at present all based on a modification of the buck power stage, reveals substantial performance deficiencies originating from the buck power stage itself. There is a need for two power supplies, and the pulsating

currents drawn from them require addition of input filters. In addition, a very complex driving scheme ("floating" drives) is required to operate power transistor switches. Thus a need arose to find a better and more suitable basic converter stage to replace the modified buck power stage.

Such converters have already been found [2,3,4] and the principles of their operation as well as their main advantages over the conventional switching dc-to-dc converters are briefly outlined in Section 3, and their dynamic (ac small signal) equivalent circuit models presented. Also, as a culmination of these efforts a practical hardware implementation, which allows bidirectional current (and power) flow is demonstrated.

Although the new converters had a number of advantages, devising a new switching power stage for switching amplifiers, which preserves all their good properties and possibly introduces further improvement is not an easy task, as demonstrated in Section 4. The push-pull-like topology, coupled with bidirectional current switch implementation, is, however, shown to be a sought superior solution.

In Section 5, the investigation of the dc gain of newly developed power stage has the objective to arrive at the optimum parameter values which will result in the maximally linearized dc gain characteristic, hence in a low amplifier distortion.

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Design-oriented analysis of Section 6, has as a goal the development of simple, yet accurate enough analytical criteria which will lead to the design of the switching power amplifier with the most favorable frequency response characteristics.

Finally, in Section 7 the experimental verification of the new switching power amplifier is made, and its hardware design compared with the design of the conventional switching power amplifier based on the buck power stage.

## 2. REVIEW OF THE CONVENTIONAL SWITCHING POWER AMPLIFIER DESIGN BASED ON THE BUCK CONVERTER

All present switching power amplifiers are based on employing a certain modification of the well-known buck converter of Fig. 1, as its power stage. Therefore, we will first review the fundamental principles of the operation of switching power amplifiers based on this converter type.

As this development proceeds the necessary requirements which any switching power stage has to meet in order to be used in switching power amplifier applications will become transparent. This will, in turn, pave the way toward the development of a new push-pull switching power amplifier topology [1], and furthermore toward replacing the buck power stage by the recently disclosed new switching dc-to-dc converter [2,3,4] or its coupled inductor extension [4,5], leading to the new push-pull switching power amplifier [1].

### 2.1 Development of the switching power stage with either voltage (arbitrary) polarity

In the buck converter of Fig. 1 periodic opening and closing of the switch S (for interval  $DT_s$  in position A, and interval  $D'T_s = (1-D)T_s$  in position B, where D is the switch duty ratio and  $f_s = 1/T_s$  is the constant clocked switching frequency), results in the duty ratio controlled output dc voltage  $V = DV_g$  of positive polarity.

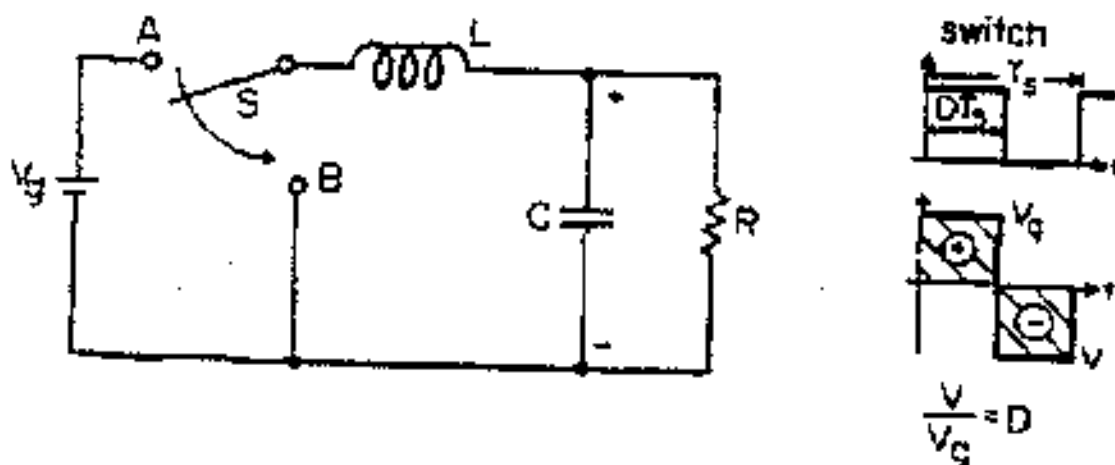


Fig. 1. Conventional buck power stage.

Let us now modify the buck converter into a power stage whose output voltage can have either polarity (positive or negative wrt. ground) depending on the value of the duty ratio of the switch. One way to achieve this is to use two power supplies  $+V_g$  and  $-V_g$  as the input to the buck type converter stage, with S switching between positive and negative power supplies as shown in Fig. 2.

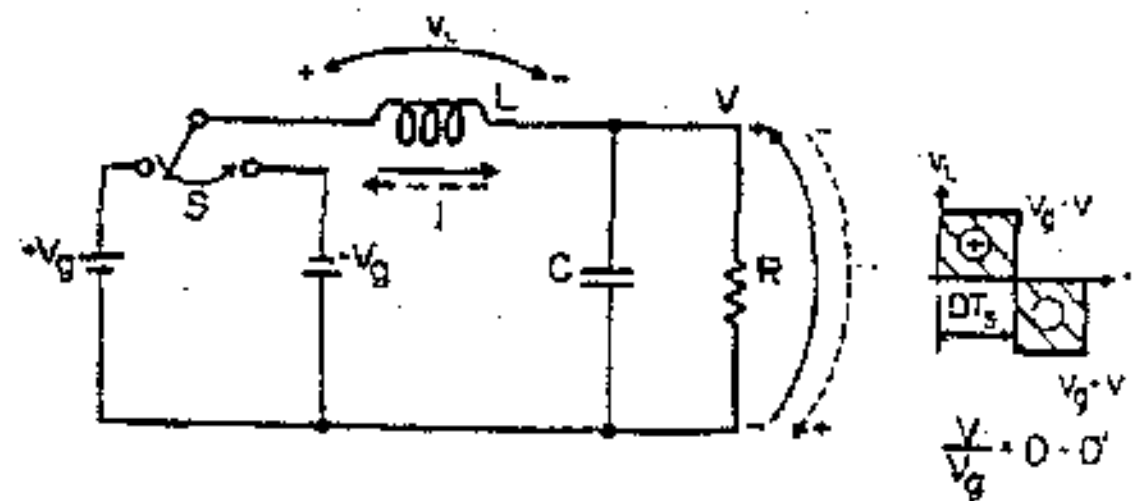


Fig. 2. Modified buck power stage with output voltage of either polarity.

By use of the customary Volt-sec balance condition on the inductor in the steady-state, we obtain:

$$(V_g - V)DT_s = (V_g + V)D'T_s \quad (1)$$

or

$$\frac{V}{V_g} = D - D' = 2D - 1 \quad (2)$$

Thus, the dc voltage gain is a linear function of duty ratio D as shown in Fig. 3, and for  $D > 0.5$  the output voltage is of positive polarity, while for  $D < 0.5$  it is of negative polarity.

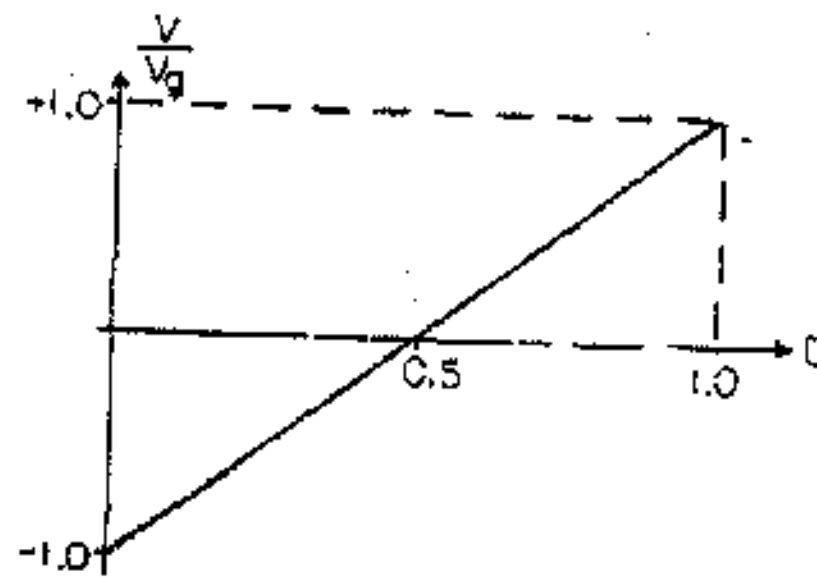


Fig. 3. Dc voltage gain of the power stage in Fig. 2.

While the actual hardware implementation of the ideal switch S in a buck converter of Fig. 1 by use of the bipolar transistor and diode is rather obvious, the reversal of the output voltage in the converter of Fig. 2 makes the hardware realization of its ideal switch S less apparent, and necessitates reexamination of the requirements imposed on it. Namely, since the average inductor

current generates the output dc voltage, reversal of the output voltage polarity is accompanied by reversal of the inductor current direction, as shown by full and dotted line arrows in Fig. 2. Hence, the hardware implementation of the switch S has to permit this bidirectional current flow. This is readily accomplished by the two-transistor, two diode circuit of Fig. 4.

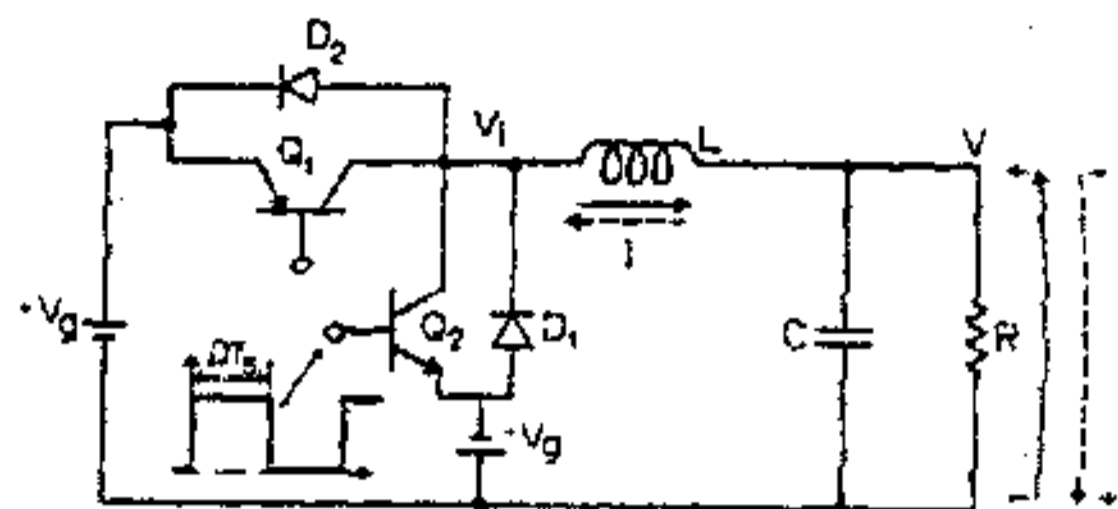


Fig. 4. Practical implementation of the converter in Fig. 2.

Transistors  $Q_1$  and  $Q_2$  in Fig. 4 are alternatively turned on and off by their drives (when  $Q_1$  is turned on for interval  $DT_s$ ,  $Q_2$  is turned off, and vice versa), while diodes  $D_1$  and  $D_2$  work in synchronism with them. Namely, for  $D > 0.5$  (positive output voltage polarity) when  $Q_1$  is turned on  $V_1 = V$  (saturation voltage neglected), the average dc current  $I$  is positive. When  $Q_1$  is switched off, the inductor forces  $D_1$  to conduct and  $V_1 = -V$  (diode drop neglected). If  $Q_2$  is switched on at this moment, its base-collector junction is forward biased, but the net effect on the circuit operation and diode  $D_1$  conduction is negligible. When transistor  $Q_2$  switches on again  $V_1 = V$  and  $D_1$  diode turns off. Transistor  $Q_2$  and diode  $D_2$  operate similarly for the other current direction (shown by the dotted arrow in Fig. 4) for  $D < 0.5$ .

The bidirectional current switch implementation of Fig. 4 is in fact the same as that used in the buck converter of Fig. 1 to prevent its discontinuous inductor current mode of operation, as further illustrated in Fig. 5.

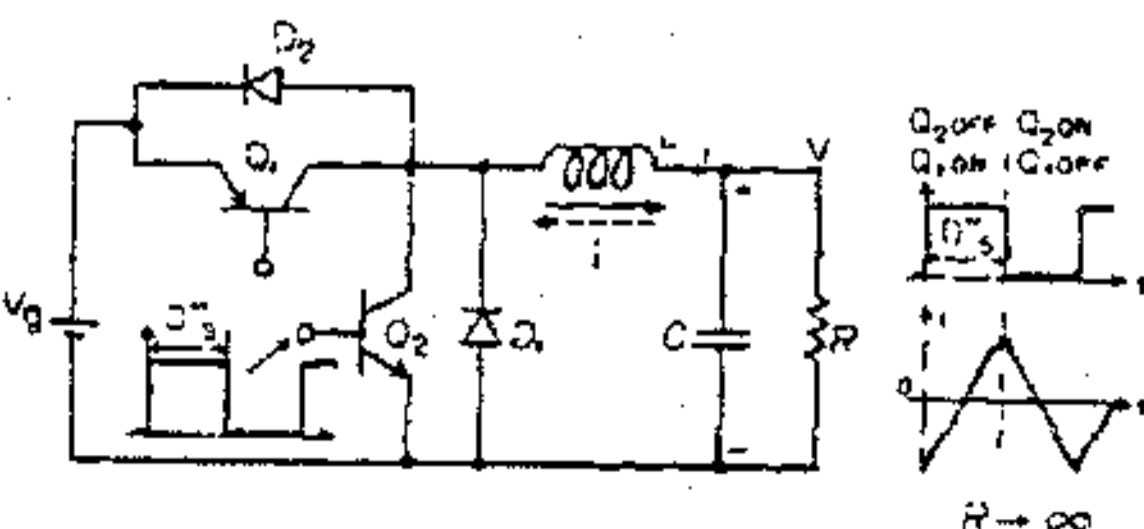


Fig. 5. Bidirectional current switch implementation leads to continuous conduction mode for any load  $R$ .

Specifically, in the absence of transistor  $Q_2$  and diode  $D_2$ , the inductor current, for large enough load [resistance value  $R$ ], falls to zero before the end of the switching cycle (during interval  $D'T_s$ ), the diode  $D$  opens and the inductor current stays at zero during the remaining interval, resulting in the discontinuous conduction mode [6]. However, if the transistor  $Q_2$  and diode  $D_2$  are added, and  $Q_2$  turned on for interval  $D'T_s$ , it provides a path for reversal of the current when diode  $D_1$  opens (actually energy stored in the capacitor will be transferred to the inductor with inductor current reversal). Thus even with no load, (zero dc output voltage) the converter operates in the continuous inductor current mode as shown by the waveforms in Fig. 5. Note, however, that the output dc voltage is of the same polarity. If, for example, the load  $R$  is replaced by a rechargeable battery, and source  $V$  is a bus voltage, the bidirectional current nature of the switch allows both charging the battery or discharging it, depending on the bus to battery voltage. Therefore, the converters of Figs. 4 and 5 could both be described as "two-quadrant converters," as illustrated in Fig. 6, though with different  $V$ - $I$  characteristics. The  $V$ - $I$  characteristic in Fig. 6a is required for the power stage in switching power amplifier applications, while the one in Fig. 6b is the type necessary for battery charger/discharger applications.

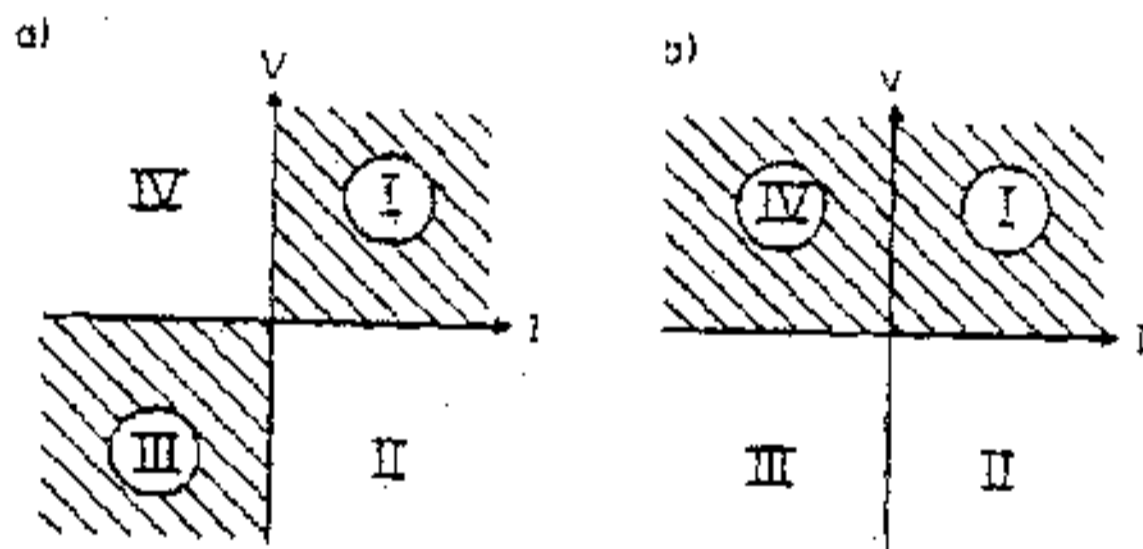


Fig. 6. Two quadrant converter viewpoint: a) switching amplifier  $V$ - $I$  characteristic, b) battery charger/discharger  $V$ - $I$  characteristic.

It now becomes apparent how connection of transistor  $Q_2$  and diode  $D_2$  to a negative supply, as in Fig. 4, instead of to ground as in Fig. 5, leads to both output dc voltage and current reversal.

Let us now demonstrate how the converter power stage of Fig. 4 with its main characteristic shown in Fig. 6a may easily be used to obtain a switching power amplifier.

## 2.2 Principle of the switching power amplifier operation

A conceptual block diagram of a switching power amplifier operated in an open-loop manner, and incorporating the power stage of Fig. 4, is shown in Fig. 7.

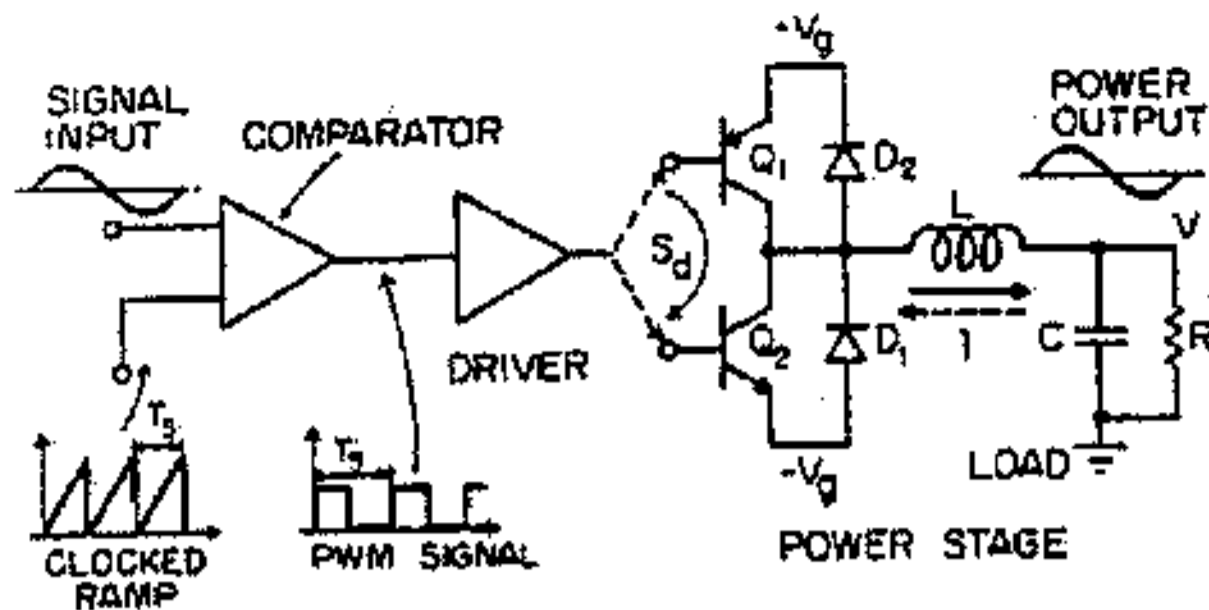


Fig. 7. Open-loop buck type switching power amplifier.

The diagram is the same as that for the open-loop switching dc-to-dc converter operated at constant switching frequency  $f_s = 1/T_s$  (clocked type), with the only difference that a time varying (sinusoidal, for example) input signal is used at the comparator input instead of a dc reference voltage. Thus, the need for a power stage with output voltage of either polarity, developed previously, now becomes evident: for the positive half-cycle of a sinusoidal audio signal, the comparator generates a duty ratio  $D > 0.5$  and output voltage of positive polarity, while for the negative half-cycle  $D < 0.5$ , a negative output voltage is generated. In fact, comparison of the low frequency input signal and the high frequency sawtooth (clocked ramp), generates a pulse width modulated (PWM) signal, whose low frequency spectrum is recovered by low-pass filtering. Hence a close replica of the input signal but now at high power level is generated at the output.

The comparison of this switching power amplifier approach with the customary conventional linear power amplifier design with respect to the two foremost constraints in the power amplifier design, that is the efficiency and distortion, becomes now apparent. In terms of efficiency, this approach boasts the usual advantages of switching power supplies over linear, that is, significantly lower power dissipation. Namely, its theoretical 100% efficiency is usually only slightly degraded (very often efficiency is above 90%), owing to the most efficient use of semiconductor devices as power processing elements, that is as switches. Power dissipation problems are thus minimized, and become functions of the transistor saturation voltage, its switching time and parasitic resistances of storage elements in the power path. Distortion, however, is a function of switching frequency in this switching amplifier approach, rather than dependent on the linearity of transistor I-V characteristics. Specifically, for low distortion switching frequency  $f_s$  has to be an order of magnitude or so higher than the signal frequency  $f$  to avoid overlapping sidebands in the PWM signal, even when the clocked ramp is of ideal linearity.

On the other hand, one would like to avoid an excessively high switching frequency for several reasons. Linearity of the sawtooth waveform may be hard to realize at higher switching frequencies. The storage time of the transistor switch then may represent a significant portion of the switching period thus further introducing distortion, and degrading the efficiency as well. Bandwidth vs. output ripple constitutes another trade-off. A general rule of thumb used by designers of switching power supplies is that for low ripple, the switching frequency must be at least two decades above the corner frequency  $f_c = 1/2\pi\sqrt{LC}$  of the L-C averaging filter. Thus, to obtain flat amplitude frequency response out to 20 kHz in audio power amplifier applications, the averaging filter corner frequency in the open-loop configuration of Fig. 7 must be at least 20 kHz. Therefore, one must either switch at 2 MHz (too high a frequency to be practical) or sacrifice low output switching ripple. In addition, several other drawbacks originate from this open-loop approach. Any nonlinearity of the sawtooth waveform (clocked ramp) and of the dc gain characteristic of the power stage, shows up as additional distortion in the output. Thus, the linear dc gain characteristic (Fig. 3) of the buck-converter in Fig. 4 becomes mandatory in this open-loop approach. Finally, both power supplies (positive and negative), have to be well regulated to avoid yet another source of distortion. The solution to these problems lies, of course, in the use of negative feedback as shown by the block diagram of the closed-loop buck type switching power amplifier in Fig. 8.

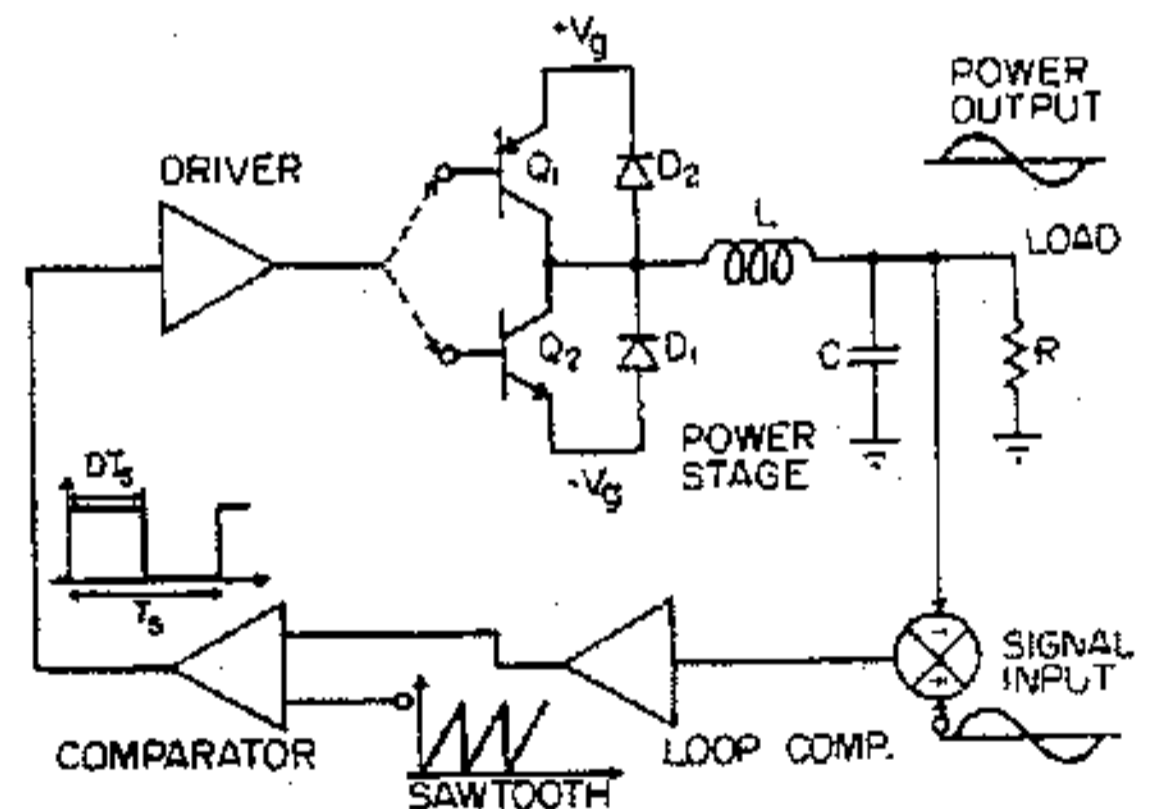


Fig. 8. Closed-loop buck type switching power amplifier.

Several benefits generally associated with the use of negative feedback are obtained. The corner frequency of the L-C averaging filter may now be placed at a lower frequency of 2 kHz, for example, and then negative feedback used to extend the closed-loop gain bandwidth out to 20 kHz as desired for a good audio power amplifier frequency response. A switching frequency of 200 kHz or higher would then provide low switching ripple. Also a significant improvement in accuracy and dc stabilization is

obtained. Furthermore, a certain degree of non-linearity in both the sawtooth waveform as well as dc gain of the power stage could be tolerated, and overall distortion of the amplifier reduced by the amount of feedback loop gain introduced. In addition, the amplifier becomes less sensitive to noise introduced by the power supply, transistor switching delay times and other nonidealities. Of course, the price one has to pay for these improvements is increased complexity and possible stabilization problems. However, this does not seem to pose any serious limitations. Namely, as seen in Fig. 8, the block diagram of the switching mode power amplifier is the same as for the switching mode regulator, and thus, all the techniques for analysis of the closed loop-gain stability and regulator performance developed [2,7,8,9], as well as measurement techniques are equally applicable to the switching audio power amplifier [10]. In fact, the simplicity of the state-space averaging method and canonical equivalent circuit models for switching converters [2,6,8,9], and yet its high accuracy, makes the design of proper feedback compensation network a relatively easy task, as will be demonstrated later in Sections 6 and 7.

It may be noted for completeness that another closed-loop feedback scheme built around the same buck power stage of Fig. 4 is sometimes used [11] for switching power amplifiers. It is essentially based on the so called free-running, buck regulator closed-loop configuration, often referred to as "ripple regulator," and has the same fundamental drawbacks of the ripple regulator: due to the nature of its operation switching frequency varies over a wide range of frequencies (often 20 kHz - 200 kHz), preventing its optimum weight and size design and causing more severe EMI problems.

The analysis of the operational principles of switching power amplifiers, even though based on the buck power stage as the only thus far known configuration, demonstrates that in principle any switching regulator (based on other switching power stages) or even open-loop driven switching converter can be made into a power amplifier, provided its power stage is appropriately modified to result in a two quadrant V-I characteristic of Fig. 6a. The fact that the buck power stage is the only one used so far may be quite misleading. This is probably caused by the failure of initial attempts to appropriately modify boost or buck-boost power stages for switching amplifier applications. One of the possible ways to achieve this will be shown later in Section 4.

Despite the negative feedback and constant (clocked) switching frequency  $f_s$ , the closed-loop switching amplifier of Fig. 8 still has several drawbacks which originate directly from the buck power stage itself. In particular, the current drawn from the power supplies is pulsating and can generate tremendous amounts of noise. This is a serious problem if left uncorrected. For example, trying to listen to the radio in the noise-contaminated environment caused by this amplifier would probably result in frustration. Thus, a properly

designed input filter [12] must be added to each power supply preferably with little effect upon the loop-gain. Another drawback is that there is a need for two power supplies of opposite polarity. Also, a quite elaborate scheme for driving the transistors of the buck power stage in Fig. 4 is required, since neither of the transistors is referred to ground. Therefore either floating isolated drives are necessary, or a push-pull nonisolated drive scheme which requires two additional power supplies (above  $+V_s$  and below  $-V_s$ ) to turn of the transistors  $Q_1$  and  $Q_2$  would have to be implemented. In addition, very careful precautions have to be taken to prevent simultaneous turn on of transistors  $Q_1$  and  $Q_2$ , thus shorting the two power supplies and resulting in transistor destruction. Finally, a relatively high switching frequency (300 kHz or so) is still necessary to reduce switching ripple.

Thus, we have come to the conclusion that a new switching converter (power stage) with properties superior to those of a buck converter (Fig. 1 and Fig. 5) is needed to replace the buck-power stage in the feedback arrangement of Fig. 8. We therefore set as a goal to find such a switching converter which will remove all above deficiencies. In fact, such a converter has already been found [2,3,4] and its properties and various useful extensions discussed in detail in [2,3,4,5]. Thus, only the highlights of the original new optimum topology switching converter [2,3,4] and its coupled-inductor extension as related to the switching power amplifier application will be included here in Section 3. Nevertheless, the objective of incorporating these new switching converters into a switching power amplifier topology, having maximum performance (wide bandwidth, low noise and distortion, small and eventually zero switching ripple, and not excessively high switching frequency  $f_s$ ) and the minimum number and size of parts will by no means be an easy one. This challenging task will be then pursued in Section 4.

### 3. NEW OPTIMUM TOPOLOGY SWITCHING CONVERTER AND ITS COUPLED INDUCTOR EXTENSION

The nature of the physical operation and the main properties of the optimum topology switching converter and its coupled-inductor extension are now briefly reviewed. With the high efficiency constraint in mind and because the real components are not ideal, but have parasitic resistive losses, the design objective in switching dc-to-dc converters is to use the minimum number of switches and storage elements that will permit the required dc conversion, and yet to achieve the maximum performance (both input and output current nonpulsating, for example), by their optimum interconnection. These goals have been achieved in the new converter [2,3,4], which essentially combines all the desirable properties of the buck and boost power stages alone, without acquiring any of their undesirable attributes, and yet with a retention of a very simple structure.

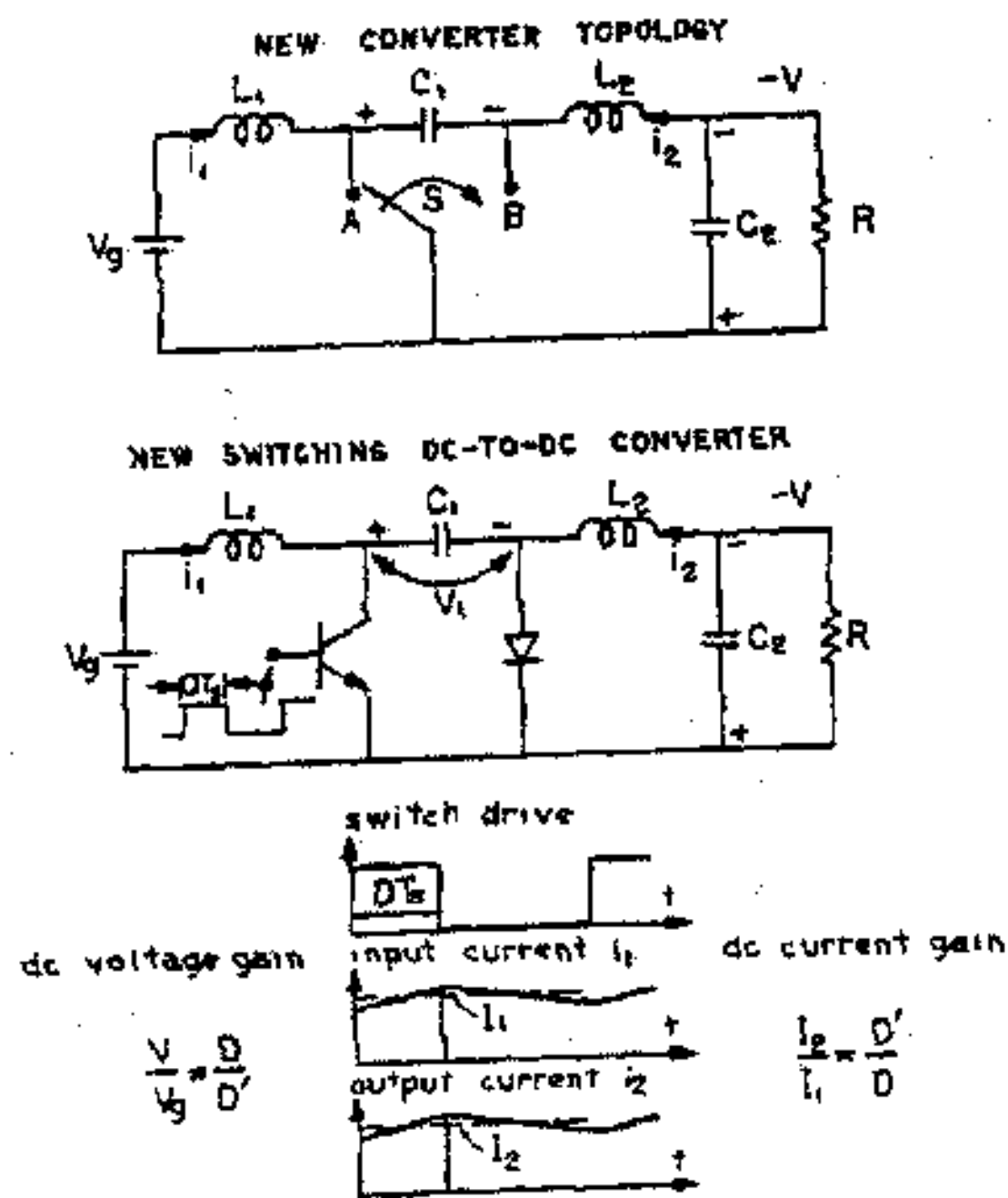


Fig. 9. Hardware realization of the new switching converter using bipolar transistor and diode.

The new converter shown in Fig. 9 operates as follows. During the interval  $D'T = (1-D)T$  when the transistor is off, the diode is forward biased and the capacitance  $C_1$  is charging in the positive direction. The collector-to-emitter voltage of the transistor is therefore positive, and it can be turned on for the subsequent interval  $DT$ . However, as soon as it turns on, capacitance  $C_1$  becomes connected across the diode, thus reverse biasing and effectively disconnecting it from the circuit. During this interval  $DT$  the capacitance  $C_1$  discharges to the load the charge accumulated in previous interval  $D'T$ , thus charging the output capacitance  $C_2$  to a negative voltage. As seen from the waveform sketches in Fig. 9, both the input current  $i_1$  and the output current  $i_2$  are nonpulsating (essentially dc with a small ripple proportional to inductance values) in the continuous conduction mode, and energy is transferred from the input to the output circuit via capacitive storage on  $C_1$ , in contrast to the inductive energy transfer process of conventional converters. It can easily be shown that the dc-to-dc conversion ratio is  $V/V_g = D/(1-D)$ , hence the same as that of the conventional buck-boost converter which has, however, both input and output currents pulsating. The following conclusion can now be made.

The new dc-to-dc converter (Fig. 9) has an optimum topology (maximum performance for the minimum number of components). Namely, to have both input and output current nonpulsating, one needs at least two inductances, one in series with the input source, the other in series with the load. To obtain a dc level conversion, an energy transferring network with storage capabilities must be used. Here it is a single capacitance. To enable it to serve as an energy transferring device, at least one switch is necessary, here realized by the bipolar transistor diode combination of Fig. 9. Finally, an output capacitance  $C_2$ , even though not essential for proper operation of the converter, is put across the load further to reduce output voltage ripple.

Some of the important advantages of the new converter over the other existing converters are:

- 1) Provides buck/boost that is up/down dc conversion capability.
- 2) Both input and output currents are nonpulsating, i.e. consist of dc with small ripple, unlike in the conventional buck-boost converter; hence, no need for input or output filters and yet EMI problems are reduced.
- 3) Offers significantly higher efficiency.
- 4) Superior dynamic properties to the conventional buck-boost converter; enables simple compensation in a switching regulator implementation.
- 5) Much simpler transistor drive circuitry, since the switching transistor is referenced to ground (grounded emitter).
- 6) Achieves all these properties with minimum number of elements.

The unique topology of the new converter makes also possible several extensions, and especially that of coupling the inductors in the original converter [4,5], with even further reduction in switching current ripple, as shown next.

### 3.2 Coupled-inductor extension of a new switching converter

Observation of the equal switching voltage waveforms on the two inductors in the converter of Fig. 9 (by use of Volt-sec balance on inductors, for example) leads to a conclusion that the two inductors  $L_1$  and  $L_2$  can be coupled without affecting the basic dc conversion property as shown in Fig. 10. Besides further reduction in size, weight and component count by use of a single core for a transformer, instead of two cores for two noncoupled inductors, this coupling is shown [5] to effect a substantial reduction in both input and output current ripples.

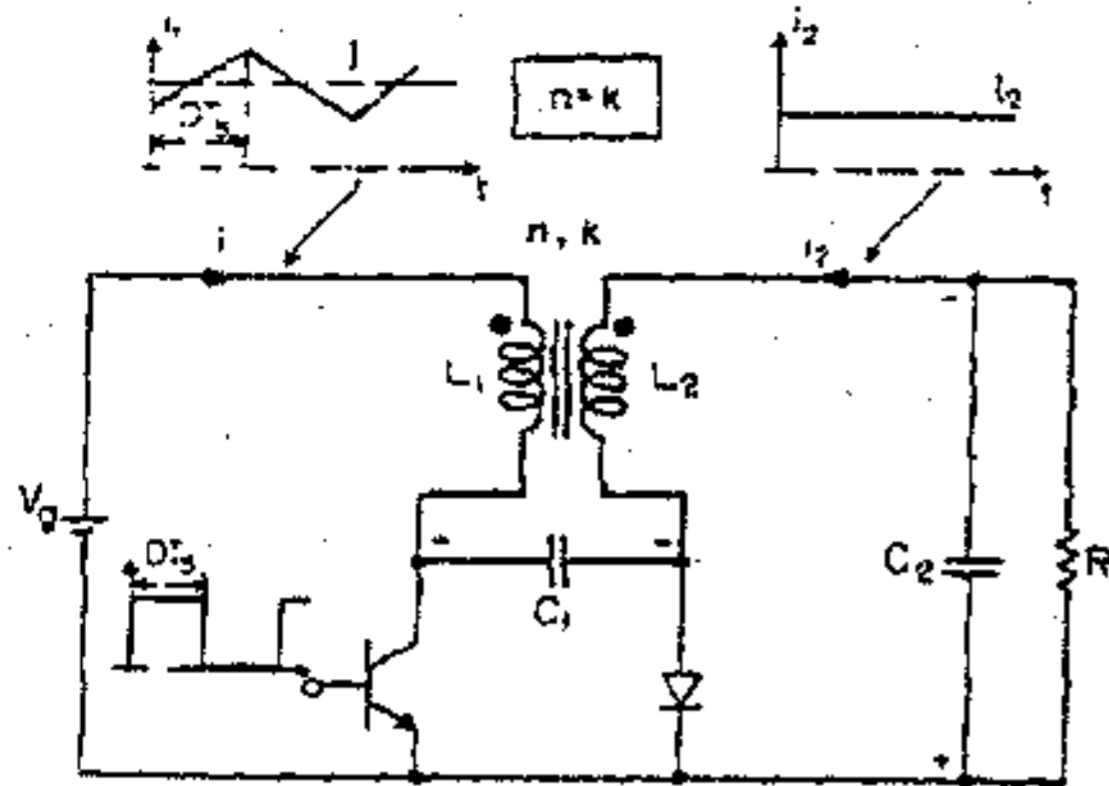


Fig. 10. Coupled Inductor Extension, showing dc output current only (no ripple) when matching condition  $n = k$  is achieved.

When the transformer in the coupled-inductor converter of Fig. 10 is modeled by use of effective turns ratio  $n$  and coupling coefficient parameter  $k$  defined by

$$n \triangleq \sqrt{\frac{L_1}{L_2}} \quad (3)$$

$$k \triangleq \frac{L_m}{\sqrt{L_1 L_2}} \quad (4)$$

(where  $L_1$ ,  $L_2$  are the self-inductances of the primary and secondary, and  $L_m$  the mutual inductance), the more detailed theoretical analysis of [5] leads to two interesting cases. When  $n = 1 \neq k$ , the so called balanced reduction case, both the input and the output current ripples are cut approximately in half, or more correctly reduced by a factor of  $(1+k)$  from the uncoupled value. However, the more interesting case is that of unbalanced reduction when  $n$  approaches  $k$ , where almost no current ripple reduction is obtained at the primary, but an order of magnitude of more (10 to 100) in current ripple reduction is obtained at the secondary as experimentally verified in [6]. In fact, it is even shown in [13] experimentally that the limiting case of the so called matching condition

$$n = k \quad (5)$$

may be practically achieved by a proper transformer design, thus resulting in a complete elimination of the current ripple at the output (transformer secondary) as shown by the current waveforms in Fig. 10. The matching condition (5) is solely a property of the transformer itself, and to a first order is independent of the converter operating point (switching frequency  $f_s$ , duty ratio  $D$ ) or element values (load  $R$ ,  $C_2$ ,  $L_1$ ,  $L_2$  etc.), thus allowing full benefit of zero output current ripple throughout the converter dynamic range. In addition, zero output current ripple completely

eliminates the need for output capacitance  $C_2$ , thus further reducing the size and weight and significantly simplifying the converter dynamic response. Both of these features will be used later in Sections 6 and 7 in the design of the New Push-Pull Switching Power Amplifier.

The coupled-inductor converter thus has the simplest possible structure, consisting of a single transformer, commutation capacitance  $C_1$  and a single switch, and yet it achieves the maximum performance (both input and output current non-pulsating with one of them even being pure dc current with no ripple) in a topology which offers the smallest possible size and weight and highest efficiency.

### 3.3 Canonical circuit models of new converter and its coupled-inductor extension

By use of the modelling technique [2,8,9] the canonical circuit model of the coupled-inductor switching converter is as shown in Fig. 11 with the generators modelling the effect of the small signal duty ratio modulation  $\hat{d}$  defined as:

$$e(s) = \frac{V}{D^2} \frac{1 - D(DL_1 + D'L_m)s/D'^2R + (L_1 - L_m)C_1s^2/D'}{1 - s^2L_mC_1/DD'} \quad (6)$$

$$j(s) = \frac{V}{D'^2R} \frac{1 - sC_1RD'/D^2}{1 - s^2L_mC_1/DD'} \quad (7)$$

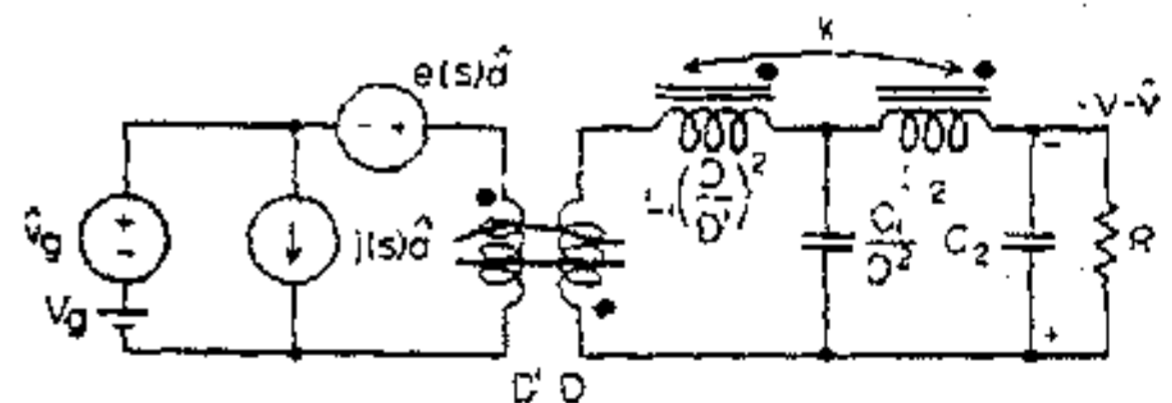


Fig. 11. Canonical circuit model of the Coupled-Inductor Switching Converter.

This circuit model, together with (6) and (7), for the case of no coupling ( $k = 0$  or  $L_m = 0$ ) reduces to the canonical circuit model of the new converter of Fig. 9, which is really its special case. Although (6) implies that the duty ratio to output transfer function contains complex right half-plane zeros, with potential stabilization problems in closed-loop applications, when the parasitic resistances of the inductors are included in the model, they usually become desirable left-half plane complex zero's, thus aiding in the loop compensation and producing a favorable frequency response as shown in [2,3]. For simplicity, they have not been included in the model. The effect of inductor

parasitic resistances  $R_{e1}$  and  $R_{e2}$  upon the dc voltage gain and efficiency is the same as for a new converter, namely

$$\frac{V}{V_g} = \frac{D}{D'} \cdot \frac{1}{1 + \alpha_1 (D/D')^2 + \alpha_2} \quad (8)$$

where

$$\alpha_1 = \frac{R_{e1}}{R}, \quad \alpha_2 = \frac{R_{e2}}{R} \quad (9)$$

Now that both steady-state (dc) and dynamic (ac) models for new converters have been characterized, one more property, that is bidirectional current (and energy) flow, needs to be investigated before the development of the new switching power amplifier based on these two converters may be undertaken.

### 3.4 Bidirectional current (and power) flow in the new switching converters

The original configuration of the new converter shown in Fig. 9 is capable only of unidirectional current (and power) flow. However, symmetrical implementation of the transistor/diode combination by addition of a single pnp transistor and diode removes this constraint and results in bidirectional current and power flow as shown in Fig. 12.

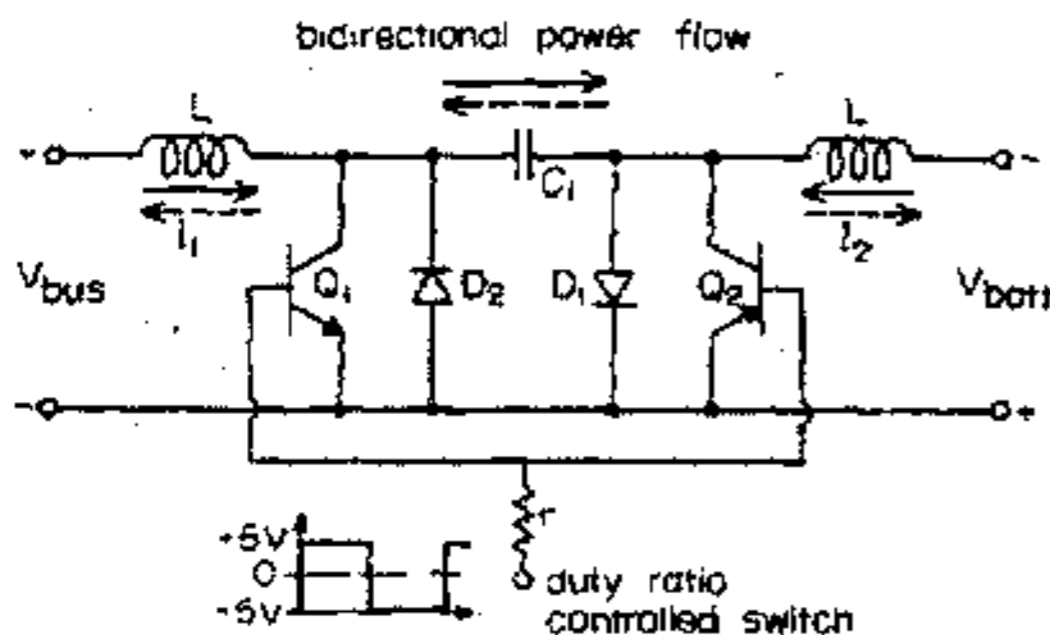


Fig. 12. Symmetrical new converter capable of bidirectional current flow.

The entire converter is thus symmetrical, and the input and output terminals can be arbitrarily designated. In addition, each of the terminals can behave either as a current source or as a current sink, owing to the bidirectional current implementation of the ideal switch  $S$  in Fig. 9. Thus the configuration of Fig. 12 becomes ideal for the battery charger/discharger application where both functions are realized by this single converter structure [15]. The direction of current flow through the converter is determined by whether the duty ratio is greater or less than the value that just matches the conversion ratio to the ratio of

the bus to battery voltages. For comparison purposes, this bidirectional switch realization is analogous to the one employed in Fig. 5 for the buck converter stage and also leads to the typical two-quadrant characteristic in Fig. 6b for the battery charger/discharger. Also, in quite the same way, the bidirectional current feature of the converter realization of Fig. 12, results in the "continuous conduction mode" of operation even when there is a zero power throughput. Thus the dynamics of the converter does not change between the "continuous" and "discontinuous" conduction mode and the dynamic models of Section 3.3 for continuous conduction mode are equally applicable for this transitional region between two power flow directions. Note also that this bidirectional current switch implementation is equally applicable to the coupled-inductor extension (Fig. 10) of the new switching converter.

However, the converter configuration of Fig. 12 does have some very important advantages. For example, both transistors in Fig. 12 are referenced to ground and are easier to drive than those of Fig. 5. Moreover use of the single drive source for the complementary npn and pnp switches, as shown in Fig. 12, not only tremendously simplifies the driving scheme, but also automatically prevents simultaneous turn-on of both transistors  $Q_1$  and  $Q_2$  (and thus prevents shorting capacitance  $C_1$ ), in spite of the presence of transistor switch storage time.

Therefore all of the problems associated with the buck converter stage of Fig. 4 mentioned earlier have been resolved with the converter configuration of Fig. 12. It now remains to find how this configuration can be included in the switching power amplifier scheme of Fig. 8, since it still does not possess the two quadrant characteristic of Fig. 6a, but rather that of Fig. 6b.

### 4. NEW PUSH-PULL SWITCHING POWER AMPLIFIER

We now pose the problem to invent a power stage based on the new converter of Fig. 9, which will, depending on a switch duty ratio  $D$ , produce an output voltage of either polarity, thus having the characteristic of Fig. 6a. Although there are probably several ways that this could be accomplished, we are looking for the simplest and the most suitable modification, which will preserve all the good properties of the new converter previously outlined, and possibly add some more. After some initial attempts we realized that a two power supply strategy employed previously in Section 2 to modify buck power stage of Fig. 1 would result in a loss of some of these good properties of the new converter. Therefore the additional desirable feature of a single power supply comes to mind and leads to the push-pull like topology of Fig. 13, in which two new switching converters (Fig. 9) are operated in tandem (parallel) from a single power supply.

Let us now assume that the two converters are operated switching out of phase, that is with complementary switch drive ratios. Namely, when switch  $S_1$  is in position  $A_1$  for interval  $DT_1$ , switch  $S_2$  is in position  $B_2$  for the same interval. Suppose also



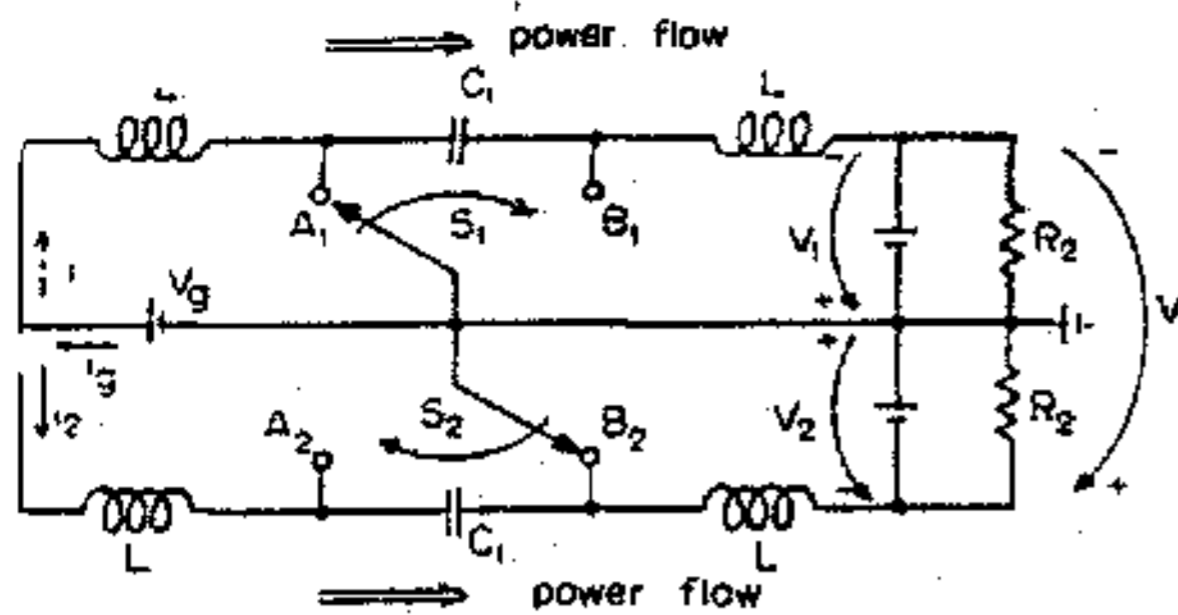


Fig. 13. Two new switching converters operated in tandem/parallel from a single power supply.

that the two loads  $R_2$  and the operating conditions are such that both converters are operating in the continuous conduction mode. Then the output voltages  $V_1$  and  $V_2$  of the two converters are ideally (no parasitic resistances taken into account):

$$V_1 = \frac{D}{D'} V_g \quad (10)$$

$$V_2 = \frac{D'}{D} V_g \quad (11)$$

As seen from (10) and (11) the two output voltages are equal only for  $D = 0.5$  while one or the other becomes greater for other duty ratios. Thus, evaluating their difference  $V = V_1 - V_2$  leads to:

$$\frac{V}{V_g} = \frac{D - D'}{DD'} \quad (12)$$

which is sketched as a function of duty ratio  $D$  in heavy line in Fig. 14. The individual converter gains  $V_1/V_g$  and  $-V_2/V_g$  are shown in dotted line.

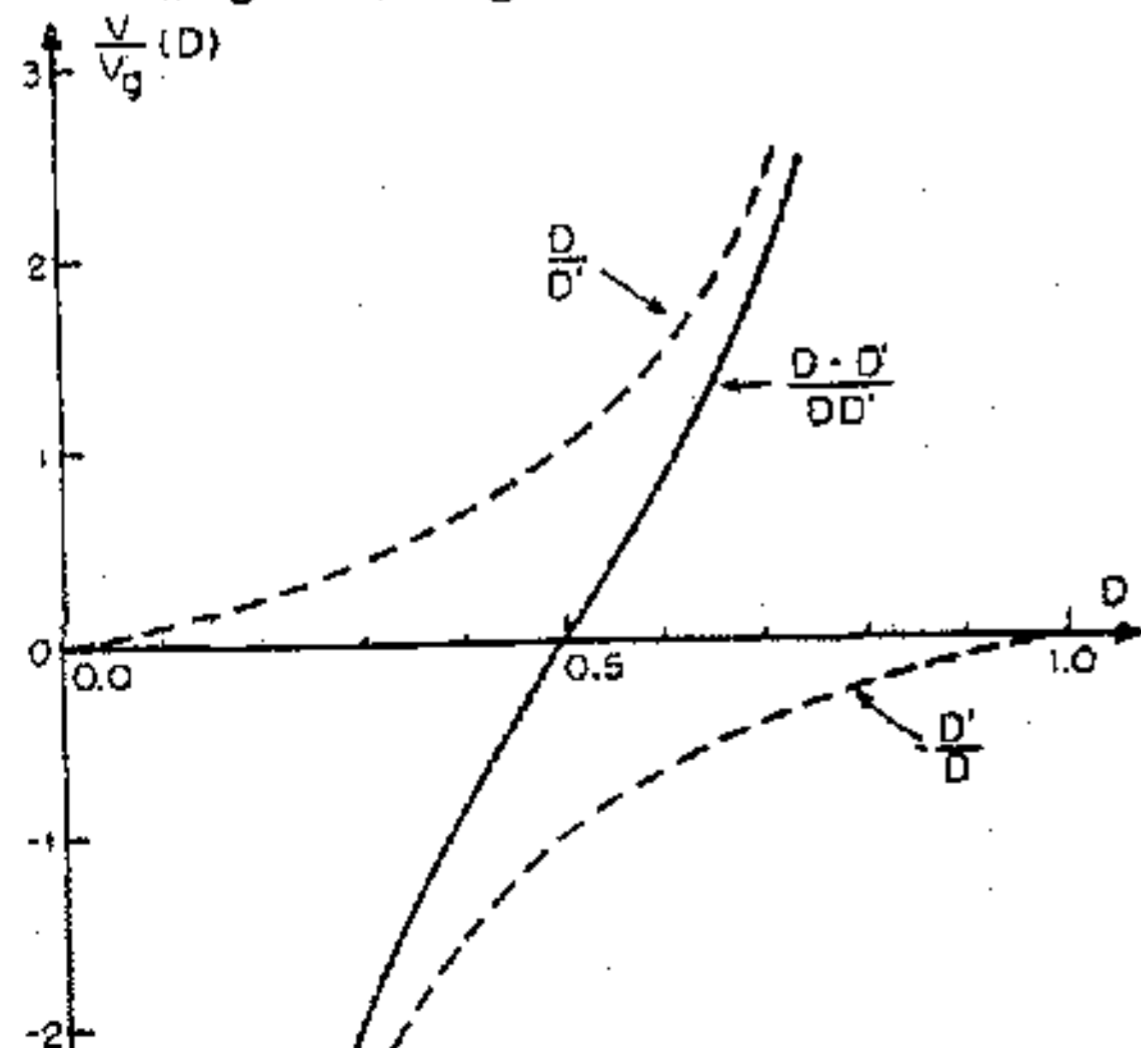


Fig. 14. Differential voltage gain  $V/V_g$  of power stage in Fig. 13.

As seen in Fig. 14, differential gain (12) is just the one needed for switching power amplifier applications, since it has the same required polarity change property as the dc voltage gain of Fig. 3 has for the modified buck power stage. The only trouble, however, is that there is not yet a load between two converter outputs to draw any power from the stage. Thus an interesting question arises:

Is it possible to connect a load between the outputs of the two converters running in parallel without violating some basic laws or disturbing the individual proper operation of the converters?

The answer to this question is affirmative and is a key to the success of the new push-pull switching power amplifier design. Thus, with the two loads  $R_2$  in the converter of Fig. 13 replaced by a differential ("floating") load  $R$ , the new push-pull power stage of Fig. 15 is obtained.

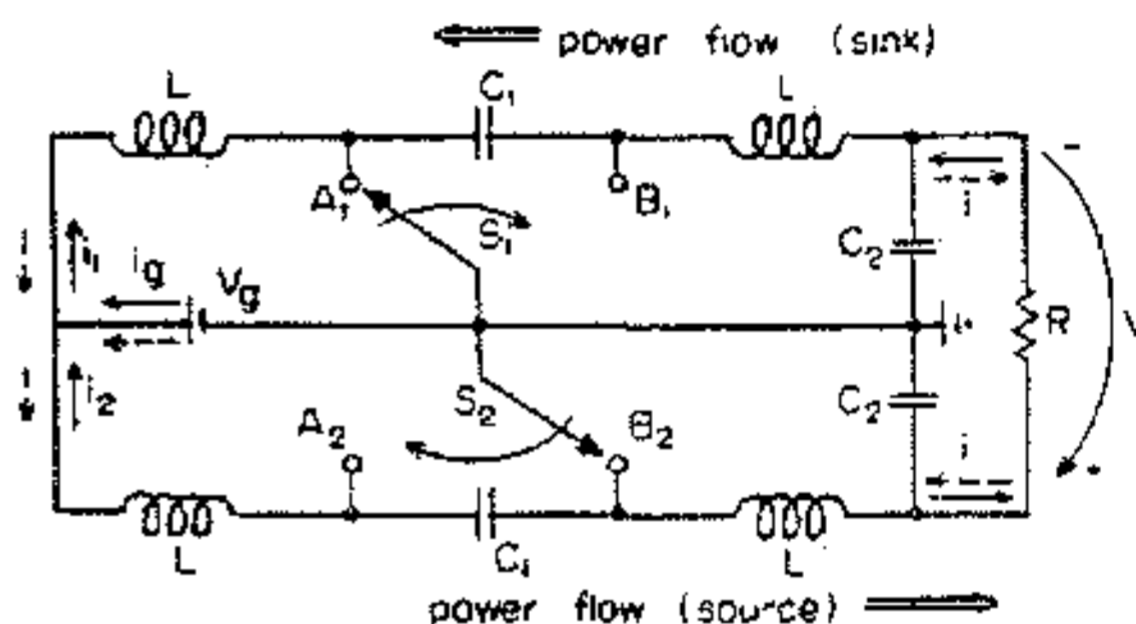


Fig. 15. New push-pull switching power stage.

Comparison with the power stage of Fig. 13 from which it originated now seems in order. In the power stage of Fig. 13 the two switching converters do not affect each others operation, and both have a unidirectional current (and power) flow as shown. However, this is not so in the push-pull power stage of Fig. 15. Namely, owing to the differential ("floating") connection of the load, between the two individual converter stages, its load current  $i$  is sourcing at one converter output and sinking at other converter output, resulting in the opposite current flow in the two constituent converters. For example, for the direction of current  $i$  in heavy line on Fig. 15, the lower converter behaves as a current source, while the upper becomes current sink. With the opposite polarity of the output current  $i$  (dotted line), the role of the two converters is reversed. Thus, switches  $S_1$  and  $S_2$  have to permit this bidirectional flow of current (and power) depending on the duty ratio  $D$ . In other words, a part of the energy delivered by the lower converter is consumed by the load, and the remainder returned via the upper converter to the source. The actual hardware implementation of the bidirectional current (and power) flow is, however, easily accomplished by use of the results of Section 3.4 and Fig. 12, as shown in Fig. 16.

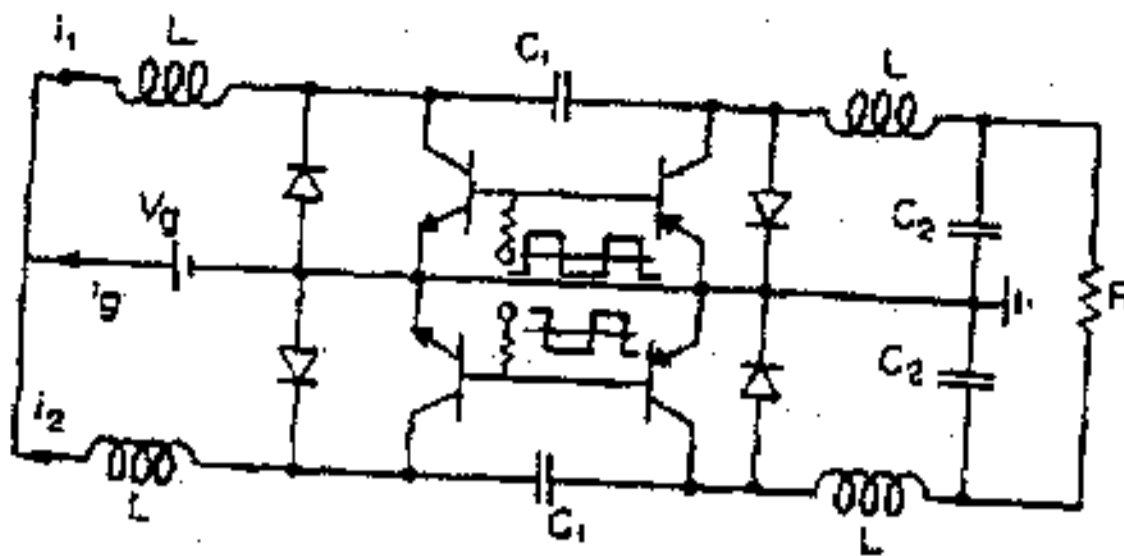


Fig. 16. Hardware implementation of the power stage in Fig. 15.

A convenient feature of this hardware implementation of the switching scheme is that all four transistors are referred to ground (grounded emitter), making them easy to drive. In addition, the npn and pnp transistor of each stage can be driven with the same PWM drive source as shown. Therefore, the overlap of the transistor on times is automatically prevented, even in the presence of significant transistor storage times.

It may also be noticed that this bidirectional current implementation avoids the transition to discontinuous conduction mode (i.e. the power stage always operates in continuous conduction mode), justifying the assumptions (10) and (11) made earlier.

An additional very desirable feature is still derived from the push-pull connection itself. Namely the current  $i_g$  drawn from the source  $V_g$  at any time is

$$i_g = i_1 - i_2 \quad (13)$$

where currents  $i_1$  and  $i_2$  are both positive (directions as in Fig. 16), and their slopes are inversely proportional to their inductance values.

As seen in Fig. 17, an interesting situation is obtained when  $L_1 = L_2 = L$ : the current  $i_g$  drawn by the power supply is dc only with no ripple at all. Namely, while the inductor current  $i_1$  is increasing at some rate (for interval  $DT_s$ ), the other inductor current  $i_2$  is returning at the same rate, thus supplying the rate increase of  $i_1$ . Hence, overall only dc current is drawn from the power supply. This very desirable extra feature results from the push-pull configuration itself.

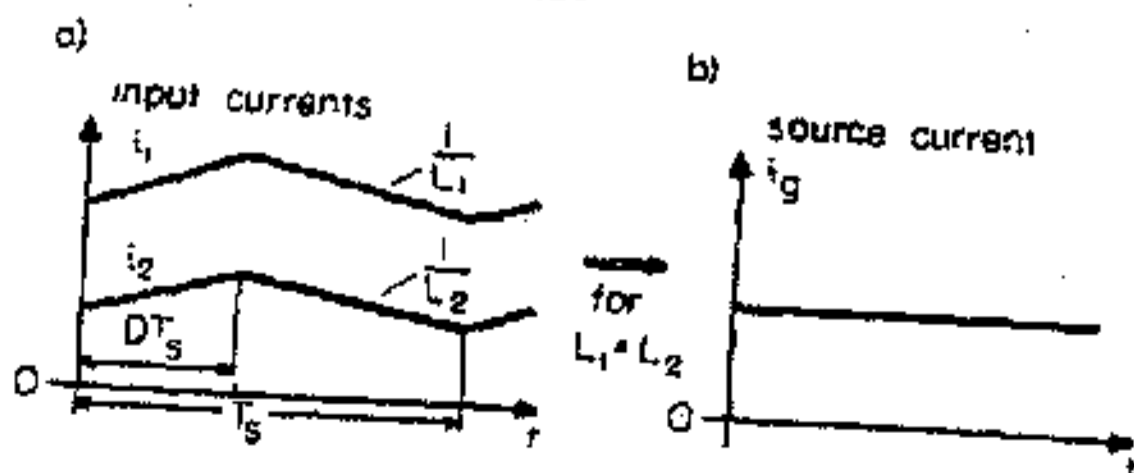


Fig. 17. Input currents and source current for the converter of Fig. 16.

This same technique of the push-pull like topology, differential load, and bidirectional current switch implementation, which has been used to obtain the new power stage of Fig. 16 from the original new converter, can now be applied to other known converter types, such as boost, or buck-boost converter. As an example, a power stage based on the boost converter and suitable for switching power amplifier is shown in Fig. 18. Also, the buck power stage so modified would result in a single power supply configuration as compared to the two power supply strategy with which we have originally started (Fig. 2). However, either design still has all the drawbacks mentioned earlier when compared to the power stage in Fig. 16 based on the new converter.

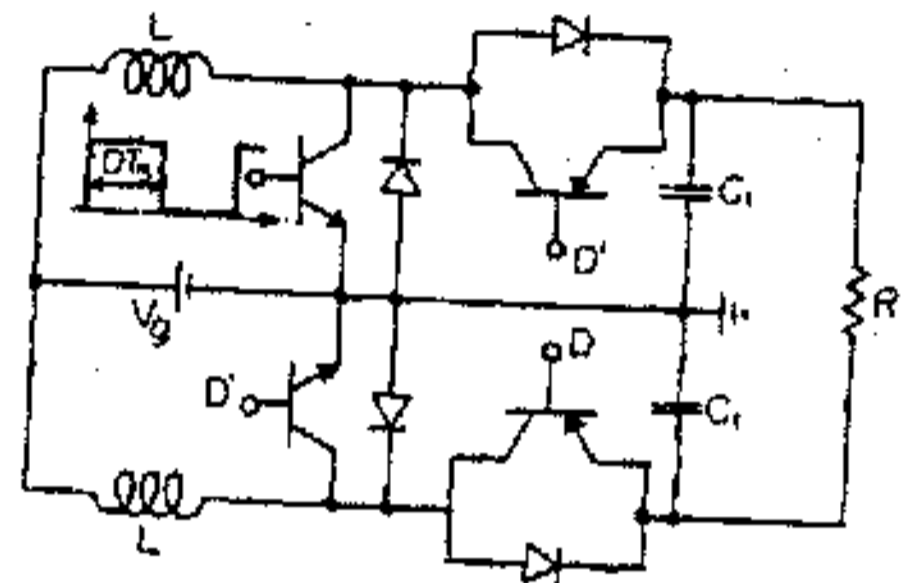


Fig. 18. Push-pull topology, differential load and bidirectional current switch technique applied to boost converter.

The most advantageous configuration is obtained, however, when the coupled-inductor extension of the power stage in Fig. 16 is used, as shown in Fig. 19, which also represents a complete conceptual closed-loop block diagram of the new push-pull switching power amplifier. As seen in Fig. 19, when

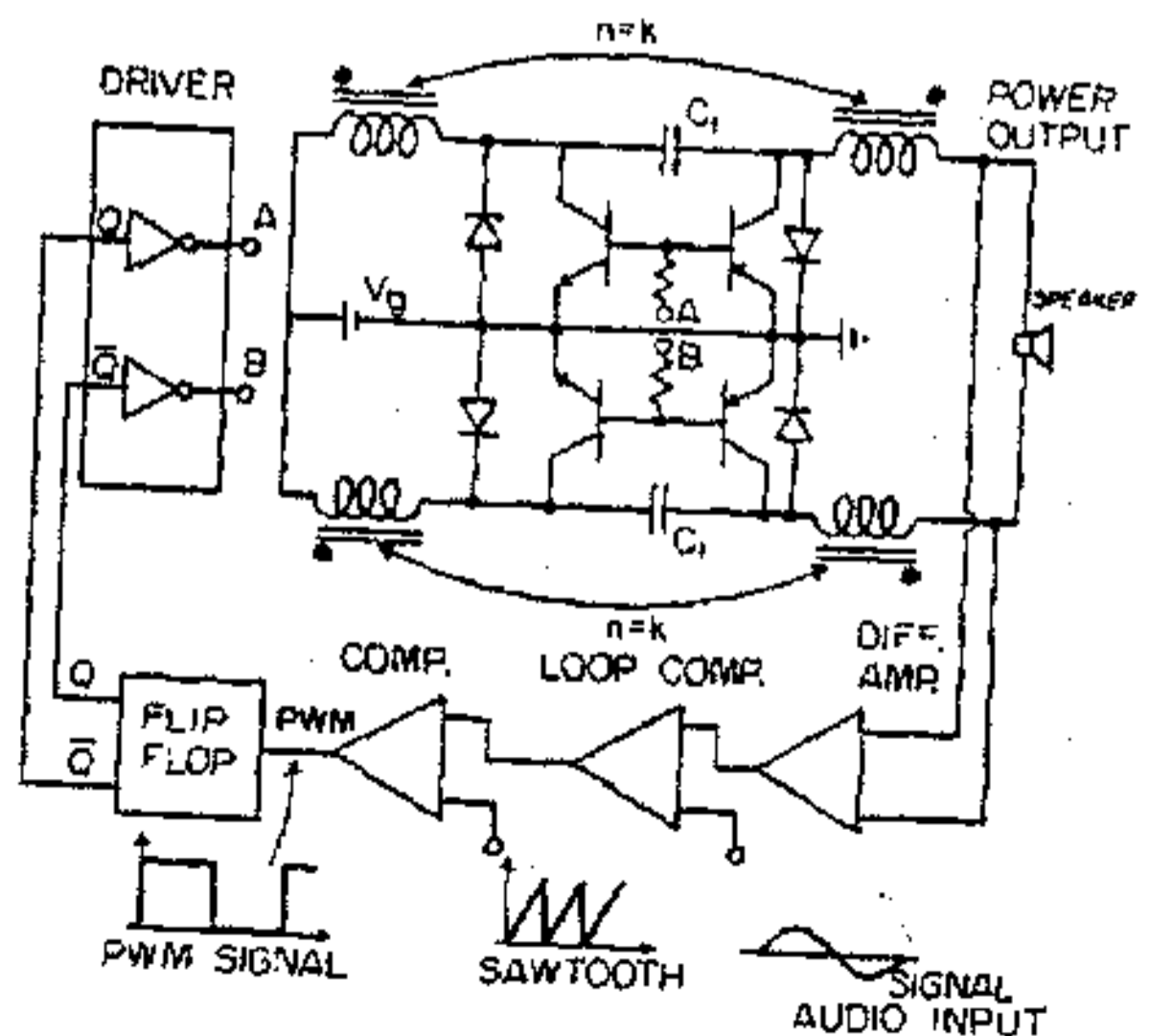


Fig. 19. New push-pull switching power amplifier.

the two transformers (coupled-inductors) are designed to satisfy the matching condition (5), zero current ripple is obtained at the output and the need for output capacitors is *completely eliminated*. The elimination of output capacitors further results in simplified and extremely favorable loop-gain dynamics (effectively single pole frequency response) as will be shown later, which permits closing the feedback loop directly, even without any compensation network, and yet resulting in a high degree of stability. Also there is no longer any need for an excessively high switching frequency to reduce the amplifier ripple, thus resulting in further improvement. Therefore, the closed-loop switching amplifier configuration of Fig. 19 has a number of advantages which will become even more evident when a comparison of the two experimental breadboards, one based on the conventional buck type design of Fig. 8, and the other on the new push-pull switching power amplifier of Fig. 19, is made in Section 7.

However, one important property of the new power stage of Fig. 16 and the coupled-inductor version of Fig. 19, that is, the linearity of the dc differential voltage gain, needs further investigation. Although the feedback will tend to reduce to a certain degree the nonlinearity of the power stage, obtaining a high performance, low distortion amplifier demands a good dc gain linearity of the power stage. Note, however, that although the dc gain characteristic of the individual converters constituting new power stage of Fig. 15 are highly nonlinear as shown by the dotted lines in Fig. 14, the differential voltage gain obtained (heavy line in Fig. 14), has a very linear characteristic around duty ratio  $D = 0.5$ , just where it is needed the most, in its useful dynamic range.

To get a measure of the degree of the linearity of dc gain characteristic, as well as quantitative predictions of the amount of distortion introduced by its nonlinearity, a separate investigation is now made.

### 5. HARMONIC DISTORTION ANALYSIS AND OPTIMIZATION OF THE DC GAIN LINEARITY CHARACTERISTIC

In the subsequent analysis the theoretical total harmonic distortion introduced by the ideal dc gain characteristic of Fig. 15 (heavy line), and given by (12), is found analytically, and thus a quantitative measure of its nonlinearity obtained. This will then lead to an informed choice as to the range around  $D = 0.5$  to which the duty ratio excursions should be limited in order to keep the total harmonic distortion as low as desired. Furthermore, the chosen range of duty ratio excursions and maximum load power requirement will help determine the needed input power supply voltage.

When the nonidealities (parasitic resistances of inductors) are taken into account it is found that they actually *tend to linearize* dc gain characteristic. In fact, it is shown that they can be chosen in an *optimal way* to maximally linearize dc gain characteristic and extend the useful range of duty ratio excursions.

#### 5.1 Harmonic distortion analysis

To assess the nonlinearity of the differential dc gain characteristic (Fig. 14) and its effect upon distortion, let us assume that the duty ratio  $D$  varies sinusoidally around its zero-input operating point  $D = 0.5$ , that is

$$D = 0.5 + A \sin \omega t \quad (14)$$

where amplitude  $A$  is limited to  $|A| < 0.5$ .

Substitution of (14) into (12) thus results in

$$V(A \sin \omega t) = \frac{2 A \sin \omega t}{0.25 - A^2 \sin^2 \omega t} V_g \quad (15)$$

This is a periodical function of  $t$ , and since it is also an odd function, it can be decomposed into odd *Fourier series*. Therefore, the output voltage will contain, besides the fundamental  $A_1 \sin \omega t$ , odd numbered harmonics. This is, as should be expected, since the push-pull connection if considered ideally symmetrical, as here, results in the cancellation of even order harmonics. By finding the rms value of (15) as well as of the first harmonic, the total harmonic distortion can be obtained. Quite complex integrals, however, can be evaluated in the closed form to get the total harmonic distortion analytically as:

$$\frac{A_d}{A_1} = \frac{A^2}{(1-4A^2)^{3/4}} \frac{1 - 4A^2 + \sqrt{1 - 4A^2}}{1 - 2A^2 + \sqrt{1 - 4A^2}} \quad (16)$$

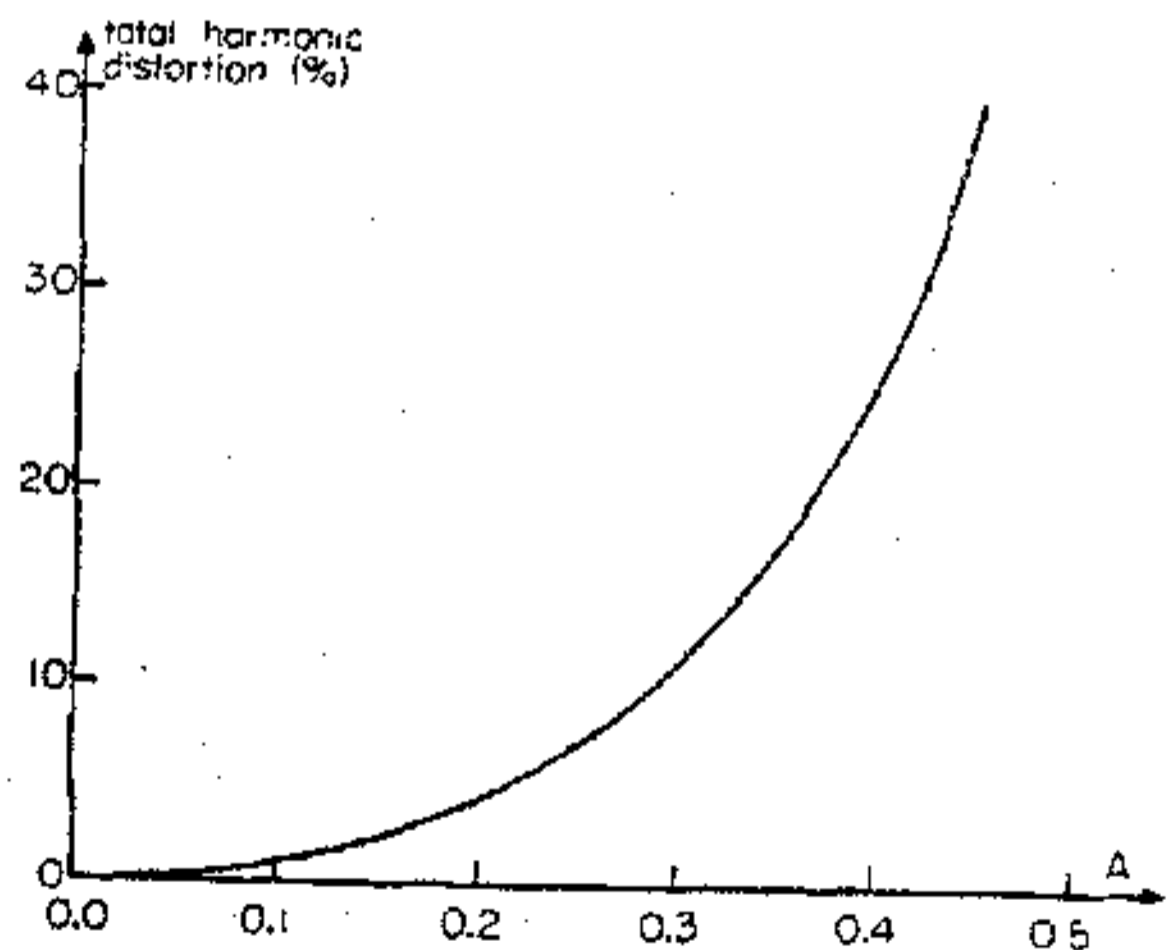


Fig. 20. Total harmonic distortion.

As seen in Fig. 20, the total harmonic distortion increases very rapidly with increase of amplitude  $A$ . Even though the harmonic distortion will be reduced by an order of magnitude or so when the feedback loop such as that of Fig. 19 is closed,

still the objective is to keep the open-loop distortion (just theoretically calculated for the power stage alone) as low as possible. Thus in a practical implementation (such as the one discussed in Section 7), by keeping the amplitude of duty-ratio excursions  $A < 0.1$ , the open-loop total harmonic distortion will be less than 1%, which by itself is considered quite low distortion in an open-loop application. Even with  $A = 0.2$ , the total distortion figure of 4.36% obtained may be considered quite acceptable for many applications, since sometimes the linearity of the clocked ramp (sawtooth) signal is no better than that, especially when a high switching frequency is used.

Although a limitation in amplitude variation to  $A < 0.1$  (or extended to 0.2 as shown later by proper optimization method), may at first look quite restrictive, it is not at all so. Namely, for  $A = 0.1$ , a differential dc gain of  $V/V_g = 0.83$  is obtained, while for  $A = 0.12$ , the dc gain becomes  $V/V_g = 1.02$ . Thus for input power supply voltage  $V_g = 24$  V, and for  $A = 0.12$ , a sinusoidal output voltage of amplitude slightly over 24 V is obtained. The comparable switching power amplifier based on the buck power stage (Figs. 7 and 8) and with the same source  $V_g = 24$  V, would have to undergo the full range of the duty ratio change, that is  $A = 0.5$ , to develop sinusoidal output voltage of the same magnitude. Thus, the restricted range of variation of  $A$ , due to nonlinear dc gain characteristic of the new power stage (Figs. 13 and 14) is largely offset by its higher gain. For example, the slope of dc gain characteristic evaluated at  $D = 0.5$  is 8 in a new power stage (Fig. 14) while it is only 2 (Fig. 3) for the buck power stage of Fig. 2. Therefore, a 4:1 increase in gain, allows proportional reduction in duty ratio excursions needed for a given power level. In fact, the power stage developed has the advantage that it is capable of step-up of input voltage (for  $A > 0.12$ ), while buck power stage (Fig. 4) has only the step-down property. Consequently, the new power stage (Fig. 16) can work satisfactorily from lower power supply voltages than the buck one (Fig. 4) for the same load power requirement.

To get a quick estimate for the limited low distortion range defined by  $A < 0.2$ , equation (16) is very well approximated by a quadratic (parabolic) dependence as:

$$\frac{A_d}{A_1} \approx A^2 \quad (17)$$

The relatively low distortion ( $< 4\%$ ) given by (17), gives motivation to investigate closer the linearity of the dc gain characteristic and possible means for its further improvement.

### 5.2 Optimization of the dc gain linearity characteristics

Quite low harmonic distortion ( $< 1\%$  for  $A < 0.1$ ) for new amplifier power stage has already been obtained, suggesting a very linear dc gain

characteristic around  $D = 0.5$ , as seen on Fig. 14. However, when the parasitic resistances of the two inductances are accounted for to model more correctly the finite voltage gain of the power stage, the dc gain characteristic appears to be still further linearized around  $D = 0.5$ , as seen on Fig. 21.

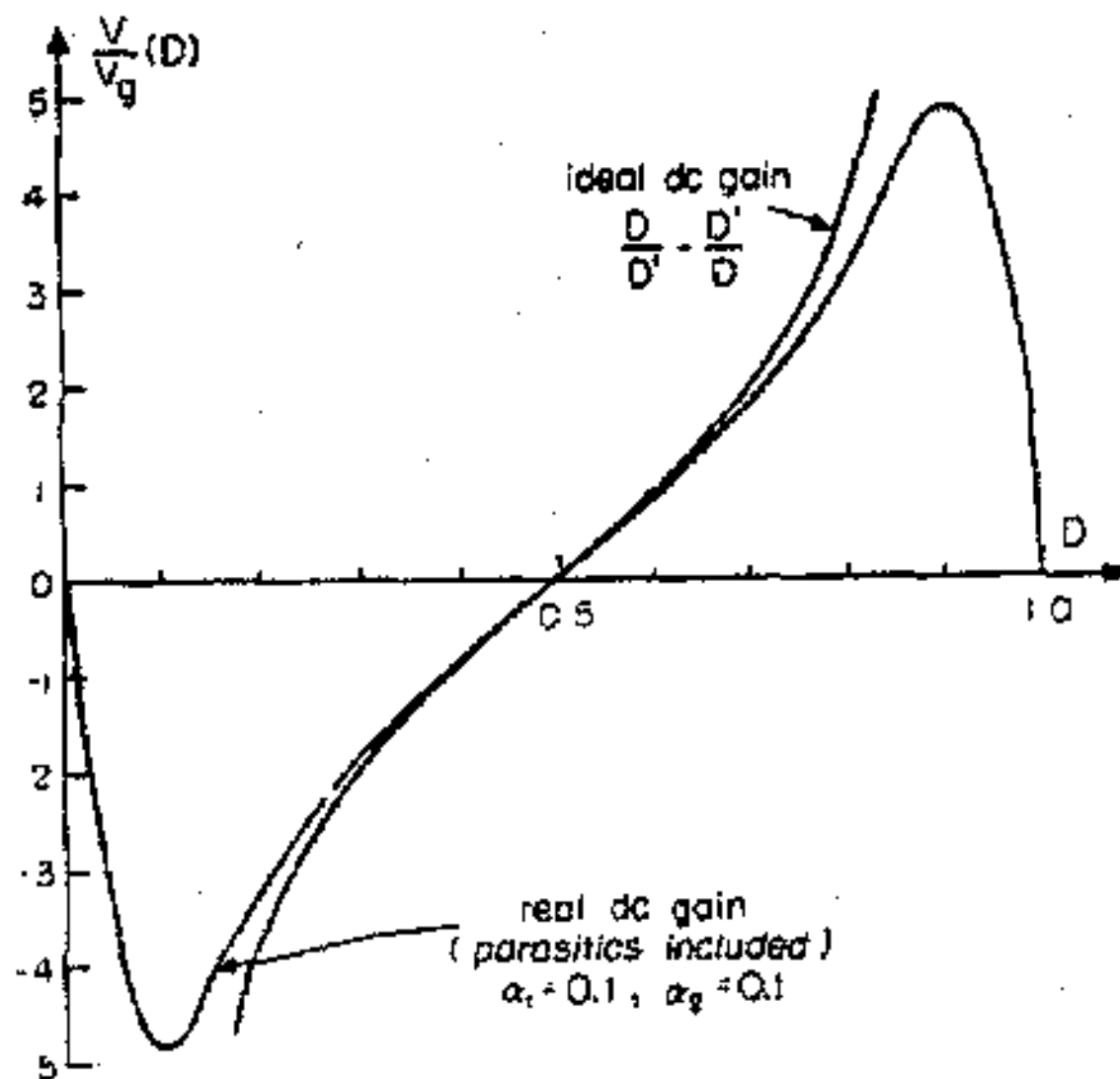


Fig. 21. Dc gain characteristic of the power stage with parasitic resistances of inductors included.

By use of (8) and definition (9), the differential dc voltage gain of the power stage with parasitic effects included is:

$$\frac{V}{V_g} = \frac{D}{D'} \frac{1}{1 + \alpha_1 (D/D')^2 + \alpha_2} \quad *$$

$$\frac{D'}{D} \frac{1}{1 + \alpha_1 (D'/D)^2 + \alpha_2} \quad (18)$$

Thus we may pose the following optimization problem:

Find the parameters  $\alpha_1$  and  $\alpha_2$ , such that the differential dc voltage gain characteristic (18) is maximally linearized around the operating point  $D = 0.5$ .

It is now convenient to redefine the dc gain (18) in terms of the variation  $A$  from 0.5 nominal point ( $D = 0.5 + A$ ) as:

$$\frac{V}{V_g} (A) = \frac{0.5}{1 - 4A^2} \frac{1 - \alpha_1 / (1 + \alpha_2)}{K(A)} \quad (19)$$

\* See correction in the Appendix.

where:

$$K(A) = 1 + \alpha_2 + \frac{\alpha_1^2}{1 + \alpha_2} + 2\alpha_1 \frac{1 + 24A^2 + 16A^4}{(1 - 4A^2)^2} \quad (20)$$

As seen from (19) and (20) for  $\alpha_1 = 0$ ,  $\alpha_2 = 0$ , the ideal dc gain is a nonlinear function of  $A$  owing to the factor  $(1 - 4A^2)$  in the denominator of (19). However, in the presence of parasitics we may now minimize the effect of this nonlinear factor by including it into  $K(A)$  factor. Then, since  $A < 0.5$ , the series expansion of  $(1 - 4A^2)K(A)$  in powers of  $A^2$  leads to:

$$(1 - 4A^2)K(A) = (1 + \alpha_1 + \alpha_2)^2 / (1 + \alpha_2) + 4A^2 [14\alpha_1 - (1 + \alpha_2 + \frac{\alpha_1^2}{1 + \alpha_2})] + \dots \quad (21)$$

As seen from (21), the factor  $(1 - 4A^2)K(A)$  will be made least sensitive to the changes in  $A$ , and thus dc gain characteristic (19) maximally linearized, when the proportionality factor in the  $A^2$  term in (21) is made to vanish, that is:

$$14\alpha_1 - (1 + \alpha_2 + \frac{\alpha_1^2}{1 + \alpha_2}) = 0 \quad (22)$$

To simplify this relationship, one can solve the quadratic equation in  $(1 + \alpha_2)$  to get two solutions:

$$1 + \alpha_2 = (7 \pm 4\sqrt{3})\alpha_1 \quad (23)$$

Note, however, that the negative sign in (23) leads to a solution for  $\alpha_1 = (7 + 4\sqrt{3})(1 + \alpha_2)$ ,  $13.93(1 + \alpha_2) > 13.93$  which would require that the parasitic resistance of input inductor is almost 14 times larger than the useful load, hence on physical grounds it is rejected. However, the other solution in (23) is completely physically feasible and leads to optimality criterion:

$$\alpha_1 = (7 - 4\sqrt{3})(1 + \alpha_2) \quad (24)$$

Thus, from (24), for a given  $\alpha_2$ , the optimal value for  $\alpha_1$  can be chosen. However, for efficiency reasons  $\alpha_2$  is usually very small ( $\alpha_2 \ll 1$ ), which makes  $\alpha_1$  almost insensitive to  $\alpha_2$  and equal to:

$$\alpha_{1opt} = 0.0718 \text{ for } \alpha_2 \ll 1 \quad (25)$$

This for an  $8 \Omega$  load leads to the optimum value of the parasitic resistance  $R_{L1}$  of input inductors:

$$R_{L1opt} = 0.58 \Omega \quad (26)$$

When  $\alpha_1$  and  $\alpha_2$  are chosen to satisfy the optimality criteria (24) or (25), the dc gain transfer curve is maximally linearized over the widest range of amplitude  $A$  as seen on the plot of Fig. 22. The comparison with the ideal dc gain curve (no parasitics included), shows almost perfect linearity of the optimal dc gain curve for  $A < 0.2$ . Computer program verified further the reduction of the third harmonic distortion for this optimum dc transfer characteristic to well below 0.1%.

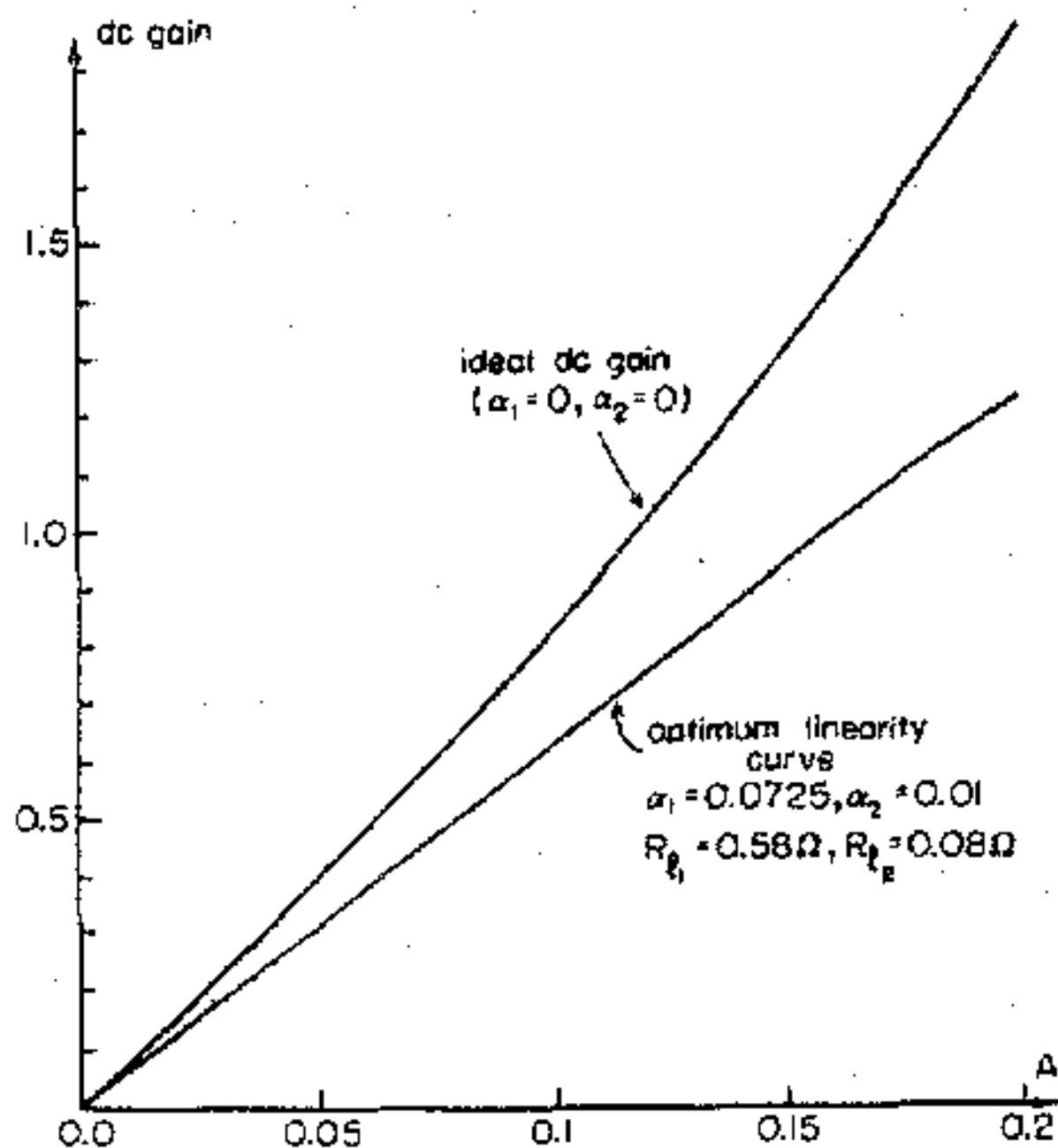


Fig. 22. Optimum dc gain transfer characteristic.

The measurements on the experimental breadboard of the new amplifier stage (Section 7) further confirmed extreme linearity of dc gain curve when the resistances have been added to the input inductors to satisfy optimality criteria (26). Although this resulted in slightly degraded efficiency, it was still in the 90% range.

It now remains to investigate the frequency response of the switching power amplifier of Fig. 19, in order to arrive at design equations for the actual hardware implementation of the new push-pull power amplifier.

## 5. DESIGN-ORIENTED ANALYSIS OF SWITCHING AMPLIFIER DYNAMIC RESPONSE

We now undertake the task of obtaining the dynamic frequency response of the push-pull power stage of Fig. 19. The objective is to derive the set of analytical expressions for the location of the poles and zeros of the loop-gain of the switching power amplifier. The approach used will be to derive the simplest possible analytical results, yet accurate enough to ensure proper design guidance. This will then lead to the design criteria of how to best choose the power stage element values that will result in the most favorable frequency response and least stabilization problems. Therefore, the path we will follow is that of analysis, but with an ultimate goal - the set of analytical design guidelines. The final product of this design-oriented analysis will be the particular choice of the component element values found to be the most suitable for the hardware implementation of the push-pull switching power amplifier.

The canonical circuit model (Fig. 11) for the coupled-inductor converter of Fig. 11 with output capacitance  $C_2$  left out, and for the matching condition (5) ( $n = k$  or  $L_2 = L_1$ ), leads to the duty ratio modulation  $\hat{d}$  to output voltage  $\hat{v}$  transfer function  $G(D) = \frac{\hat{v}}{\hat{d}}$ :

$$G(D) = \frac{V_g \left( 1 - \frac{DL_1}{D'^2 R} s \right)}{D'^2 \left( 1 + s \frac{L_1(D^2 + 2DD') + L_2 D'^2}{D'^2 R} + s^2 \frac{L_1 C_1}{D'^2} + s^3 \frac{L_1 C_1 L_e}{D'^2 R} \right)} \quad (27)$$

where  $L = L_2 - L_1$  is the "leakage" inductance, while  $L_1^e$  and  $L_2$  are self-inductances of the transformer primary and secondary, respectively. We can now find the duty ratio modulation  $\hat{d}$  to differential output voltage  $\hat{v}_d$  transfer function  $G_d(D) = \frac{\hat{v}_d}{\hat{d}}$  of the push-pull power stage of Fig. 19 by use of the result (27) for a single converter stage, but with due caution to the proper meaning and interpretation of  $\hat{d}$  for each of the two constituent converters. Namely, if the upper power stage half in Fig. 19 is operating with duty ratio  $D$  and has transfer function  $G(D)$ , it may seem, at first, as though the lower power stage transfer function is  $G(D')$ , since it is operating with complementary duty ratio  $D'$ , and its transfer function could be obtained from (27) by simple substitution  $D \leftrightarrow D'$ . However, this will lead to the differential transfer function  $G_d(D) = G(D) - G(D')$  which is obviously wrong since at the nominal operating point  $D = 0.5$  this results, even at low frequencies in a differential gain of zero instead of 8, (slope of the differential dc gain characteristic of Fig. 14 at  $D = 0.5$ ). Nevertheless, this difficulty is easily

resolved by a proper interpretation of the duty ratio modulation  $\hat{d}$ . Specifically, if the upper power stage is operated with duty ratio  $d$  and lower with  $d'$ , their perturbations lead respectively to

$$d = D + \hat{d} \quad ; \quad d' = D' - \hat{d} \quad (28)$$

Thus, from (28) the following conclusion can be made. As far as small signal perturbations are concerned, the upper converter is modulated by  $+\hat{d}$ , but the lower one is modulated by the negative duty ratio modulation, that is  $-\hat{d}$  (increase in duty ratio of upper converter reflects as decrease of duty ratio in lower converter). Therefore, their respective transfer functions are  $G(D)$  and  $-G(D')$  (not  $+G(D')$  as previously concluded wrongly), leading to the correct differential transfer function  $G_d(D)$  as

$$G_d(D) = G(D) + G(D') \quad (29)$$

where  $G(D)$  is as given by (27).

As demonstrated in the previous section, to keep the open-loop distortion low, we have restricted the change of duty ratio to a relatively small range ( $A < 0.1$ ) around  $D = 0.5$ , which corresponds to  $D \in [0.4, 0.6]$ . Therefore, without a loss of generality and in order to simplify the analysis of the frequency response and arrive at useful design criteria, we will investigate first the dynamic (ac small-signal modal) for duty ratio  $D = 0.5$ . The frequency response for other values of  $D$  in the range  $D \in [0.4, 0.6]$  will qualitatively be the same, with only minor quantitative modifications (a slight shift in pole and zero locations).

By use of (27) in (29) for  $D = 0.5$ , the differential transfer function  $G_d = \hat{v}_d / \hat{d}$  becomes:

$$G_d = 8 V_g \frac{1 - 2 \frac{L_1}{R} s}{1 + s \frac{3L_1 + L_2}{R} + 4s^2 L_1 C_1 + 4s^3 \frac{L_1 C_1 L_e}{R}} \quad (30)$$

As seen from (30) correct low frequency gain of 8 is obtained. The third order polynomial in the denominator of (30) may now be analytically separated into two complex poles and a real pole, resulting in:

$$G_d = 8 V_g \frac{1 - 2 \frac{L_1}{R} s}{\left( 1 + s \frac{4L_1}{R} + s^2 4L_1 C_1 \right) \left( 1 + s \frac{L_e}{R} \right)} \quad (31)$$

The above analytical separation is a very good approximation provided

$$C_1 R \gg \frac{L_e}{R} \quad (32)$$

\* See correction in the Appendix.

which is for all practical purposes always satisfied, since leakage inductance  $L_e$  is usually very small. For the same reason (low leakage inductance  $L_e$ ), the real pole is at much higher frequencies than the complex poles, or real zero, and does not affect the frequency response appreciably in the range of frequencies of interest. This now permits the following choice of component element values for the practical hardware realization of the push-pull switching audio amplifier (with coupled inductor parameters  $L_1$  and  $L_e$  measured):

$$C = 180 \mu\text{F}, \quad L_1 = 138.5 \mu\text{H}, \quad L_e = 37.5 \mu\text{H} \quad (33)$$

which for an  $R = 8 \Omega$  speaker load results in the following open-loop gain:

$$G_d = 8 \frac{V_g}{V_g} \frac{1 - \frac{s}{\omega_z}}{[1 + \frac{s}{Q\omega_c} + (\frac{s}{\omega_c})^2](1 + \frac{s}{\omega_p})} \quad (34)$$

where

$$f_c = \frac{1}{4\pi L_1 C_1} = 504 \text{ Hz}, \quad Q = \frac{R}{2} \sqrt{\frac{C_1}{L_1}} = 4.6 \quad (35)$$

$$f_z = \frac{R}{4\pi L_1} = 4.6 \text{ kHz}, \quad f_p = \frac{R}{2L_e} = 34 \text{ kHz} \quad (36)$$

Note that equation (32) used for analytical separation of the third order polynomial is very well satisfied ( $1440 \gg 4.7$ ).

The typical magnitude plot of the frequency response of the push-pull power stage will be as in Fig. 23.

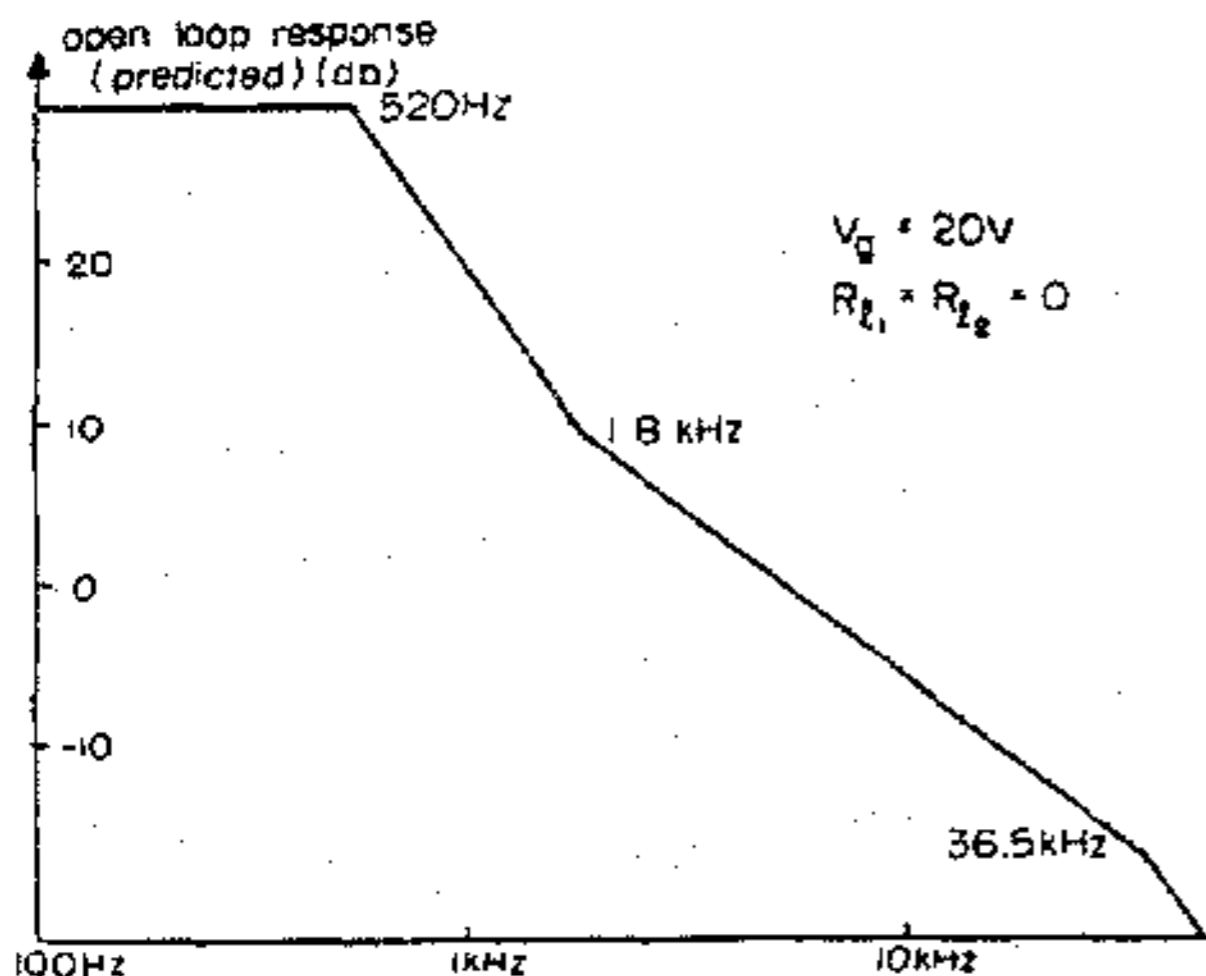


Fig. 23. Typical frequency response of the push-pull power stage in Fig. 19.

Thus, the amplitude frequency response has the very desirable feature of a single pole slope ( $-20$  dB/decade) at the 0 db crossover. Note, however, that the real zero in (30) is in the *right-half plane* (nonminimum phase response), which looks as though some potentially serious problems in stabilizing the loop gain  $T$  may be encountered. This is not so, as has been shown in [2,3]. Namely, when the parasitic resistances  $R_{L1}$  and  $R_{L2}$  of the inductors are included, they have a profound and stabilizing effect upon the converter dynamic ac properties. In particular, their inclusion in the model [2,3], results in a negligible effect on the pole locations (provided  $R_{L1} \ll R$  and  $R_{L2} \ll R$ ), while it does affect to a *first order* the location of the real zero, such that the numerator in (30) becomes

$$1 - 2s(\frac{L_1}{R} - R_{L1}C_1) \quad (37)$$

As seen from (37) the original *right-half-plane* zero (with no parasitics included), may now become a *left-half plane* zero if the following condition is met:

$$\frac{L_1}{R} - R_{L1}C_1 < 0 \quad (38)$$

Therefore, owing to the corrective term  $R_{L1}C_1$ , the frequency response may be *qualitatively* changed to a *minimum phase* response and hence stabilization problems completely eliminated. This is, however, what should be expected, since the input series resistance  $R_{L1}$  effectively adds more damping to the power stage. In fact, very often even a very small inherent resistance in the input inductors will result in this desirable frequency response, as experimentally confirmed in Section 7. Further control of the exact location of the zero may be achieved by adding some small damping input resistance. This will move this zero to a lower frequency, and may eventually result in cancellation with one of the low frequency poles. In that case, a previously very good frequency response is transformed into an excellent one. In fact due to this effective single pole frequency response the need for a feedback compensation network is *completely eliminated* and yet a high degree of *stability* obtained.

Another very interesting feature demonstrated is that the frequency response analysis of the push-pull power stage of Fig. 19 is no more difficult than that of the single coupled-inductor converter in Fig. 10. Even though the push-pull power stage consists of 6 storage elements, hence 6th order behaviour is expected in general, its analysis has been effectively reduced to the third order. The inclusion of the input parasitic resistance  $R_{L1}$  leads to a further order reduction, resulting in an equivalent and most desirable single pole response.

Twofold benefits are derived from the appropriate inclusion of the parasitic resistance of the

input inductors: frequency response is significantly improved, and an almost exact linear dc gain characteristic achieved, with only a slight degradation in efficiency. How these analytical results can be implemented in practice is demonstrated next.

## 7. EXPERIMENTAL VERIFICATION OF THE NEW PUSH-PULL SWITCHING POWER AMPLIFIER

The experimental verification of the analytical predictions made earlier is obtained on the circuit breadboard of the new push-pull switching power amplifier [Fig. 30], which was designed by use of the results in Section 6. In particular, the significant improvements obtained by use of optimal input resistances (26) are shown experimentally to lead to a rather linear dc gain characteristic in the power stage and to further improvement in the already acceptable frequency response, resulting in a most desirable, effectively single-pole, loop-gain frequency response. This in turn permitted closing the feedback loop directly without any compensation networks, and yet achieving a high degree of stability (phase margin).

These detailed experimental results for the new switching power amplifier are then followed by a brief description of actual hardware implementation of both the new switching amplifier (Fig. 30) and a conventional design based on the buck converter (Fig. 29). Comparison of their hardware designs further reveals and emphasizes the advantages gained by the new switching power amplifier topology.

### 7.1 Push-pull switching audio power amplifier

A detailed circuit schematic of the push-pull switching audio amplifier is shown in Fig. 30. The power stage was designed by use of the values (33) suggested in the analytical results. For the chosen power supply voltage  $V_g = 25$  V, and with duty ratio excursions limited to less than 0.1 ( $A < 0.1$  to keep the open-loop distortion very low), the maximum output voltage was approximately 25 V, and roughly 40 Watts of sinusoidal audio power was obtained. The switching frequency used was  $f_g = 80$  kHz.

First, several experiments and measurements were performed on the power stage itself, followed by some open-loop dc as well as ac gain measurements. The first experiment verified the dc gain characteristic (Fig. 22) by direct measurements of the differential output dc voltage vs. the duty ratio of the power switch. The parasitic resistances of the coupled-inductors were  $R_{L1} = R_{L2} = 0.04 \Omega$ , and a characteristic very closely approaching the ideal dc gain characteristic of Fig. 22 was measured. Then, the resistances of  $R_p = 0.53 \Omega$  were added in series with the input inductors (as shown in Fig. 30), resulting in the total optimal input resistance  $R_p^{opt} = 0.57 \Omega$ . The linearity of the measured dc gain characteristic tremendously improved as

was predicted by Fig. 22 and Section 5.2. However, for lower power supply voltages ( $V_g = 10$  V or smaller), a deviation from the linear characteristic was observed for low output voltages (duty ratios close to 0.5). This has been attributed to transistor saturation voltages and diode forward drops, which were not accounted for in the analysis. At higher output voltages and for higher input supply voltages, their effect becomes negligible, and approaches the optimal linearity curve of Fig. 22.

The next experiment measured the overall open-loop dc gain linearity (hence including the non-linearity of the ramp and any other source of nonlinearity). Still operating in an open-loop, a small dc signal  $V_{in}$  was injected at audio signal input, (Fig. 30) and output voltage  $V_{out}$  measured resulting in the open-loop dc gain characteristic of Fig. 24. As seen in Fig. 24 relatively good overall linearity was observed. This measurement was, of course, done with an optimum dc gain characteristic of the power stage, hence  $R_p = 0.53 \Omega$  was included.

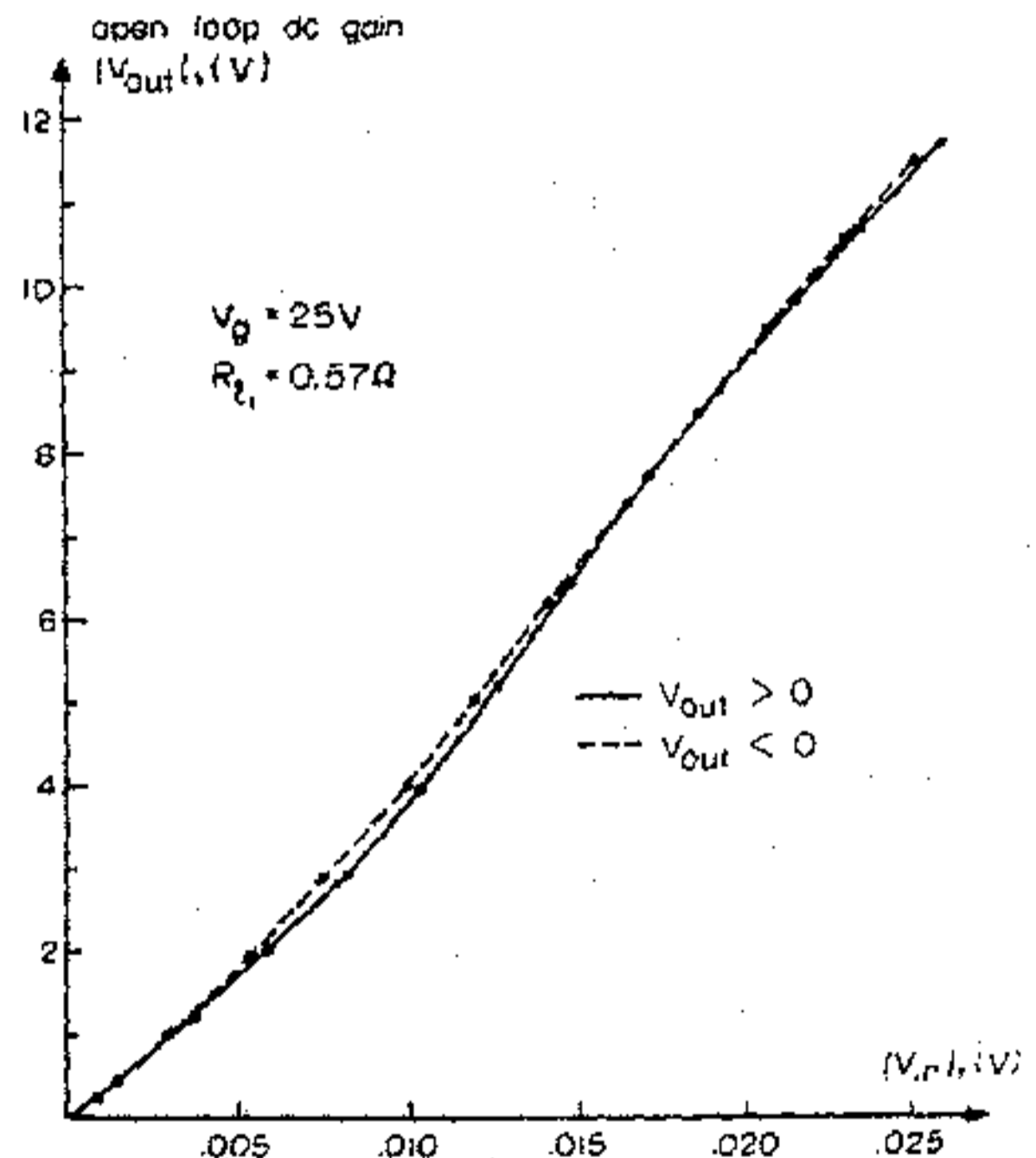


Fig. 24. Open-loop dc gain characteristic accounting for all circuit nonlinearities.

The measurement of the dynamic (ac) small signal frequency response (loop-gain) at the steady-state (dc) operating point  $D = 0.5$  was undertaken next. Although a more sophisticated and general injection method for loop gain measurement without breaking the feedback loop [10] could have been used, the relatively low value of the dc loop-gain designed (28 db) and negligible loading effect of feedback network at power stage output (22 k  $\Omega$  input resistance of 741 op-amp compared to 8  $\Omega$  load



resistance in Fig. 30), permitted breaking the feedback loop at the output. The loop-gain  $T$  was then measured by injecting an ac signal at the input of the 741 op-amp in Fig. 30, and measuring the ac output differential voltage of the power stage.

For the first measurement, the externally added resistances  $R_i = 0.53 \Omega$  have been removed (shorted). The measured loop-gain frequency response shown by dotted lines in Fig. 25 agreed very well with the theoretically predicted one given by (34), (35) and (36). Note from the corresponding minimum phase response in Fig. 25 that even with just the small inherent parasitic resistances of the inductors, the real zero (37) was indeed in left-half plane. When the same measurement was repeated with optimum values of input resistances (26), the frequency response shown in heavy line in Fig. 25 is measured. Again, this frequency response is as predicted theoretically. Namely, for  $R_{i1} = 0.58 \Omega$ , (37) leads to a calculated real zero  $f_z = 933 \text{ Hz}$ . Since the complex poles are not appreciably affected by inclusion of the parasitic resistances (26), they are approximately at  $f_p = 500 \text{ Hz}$ . Therefore, a near cancellation of one pole and this zero results, and effectively a single-pole frequency response as predicted earlier in Section 6, was measured (Fig. 25). Note that the high-frequency pole  $f_p = 34 \text{ kHz}$  is close to  $f_z/2$  (40 kHz) and has negligible effect upon the frequency response.

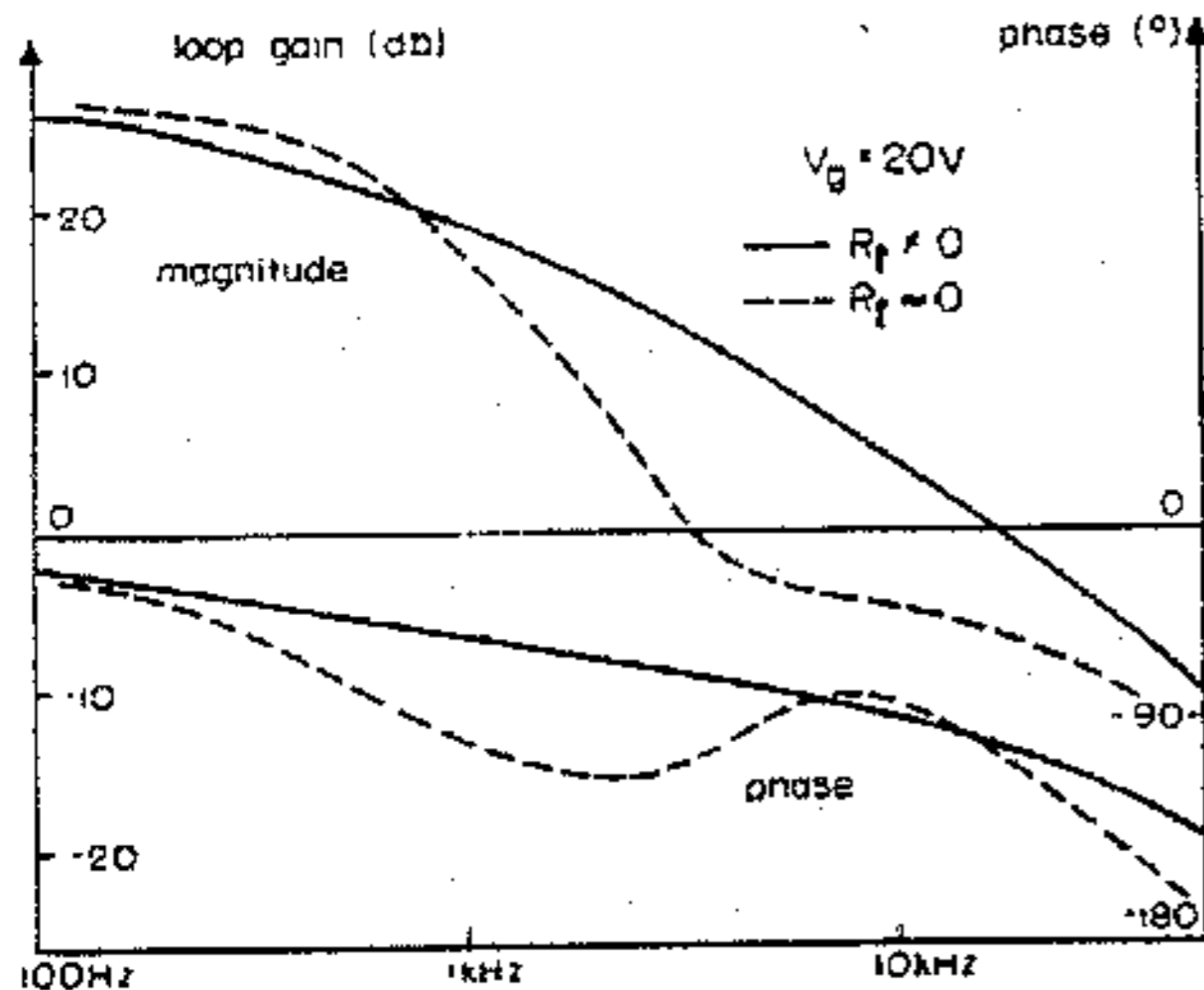


Fig. 25. Effect of the input resistances upon the loop-gain frequency response.

Comparison of the frequency response characteristic in Fig. 25 demonstrates in a very convincing way the stabilizing effect of even very small input resistances, and the excellent dynamic response obtained for their optimal values. As seen in Fig. 25, good stability and a phase margin of  $80^\circ$  is achieved.

When finally the input voltage  $V$  was increased to  $V = 25 \text{ V}$  again, a slight increase<sup>8</sup> of the dc loop gain<sup>8</sup> resulted. The measured loop-gain shown in Fig. 26 had a 0 db crossover at exactly 20 kHz. Thus, when the feedback-loop was closed, the closed-loop gain of 20 kHz bandwidth was measured as shown in Fig. 27. Note from Fig. 30 that the feedback loop is closed without any compensation, and yet a high stability and phase margin of  $73^\circ$  is achieved. The closed-loop gain roll-off at low frequencies (20 Hz) was due to a  $1 \mu\text{F}$  coupling capacitor at the audio signal input in Fig. 30.

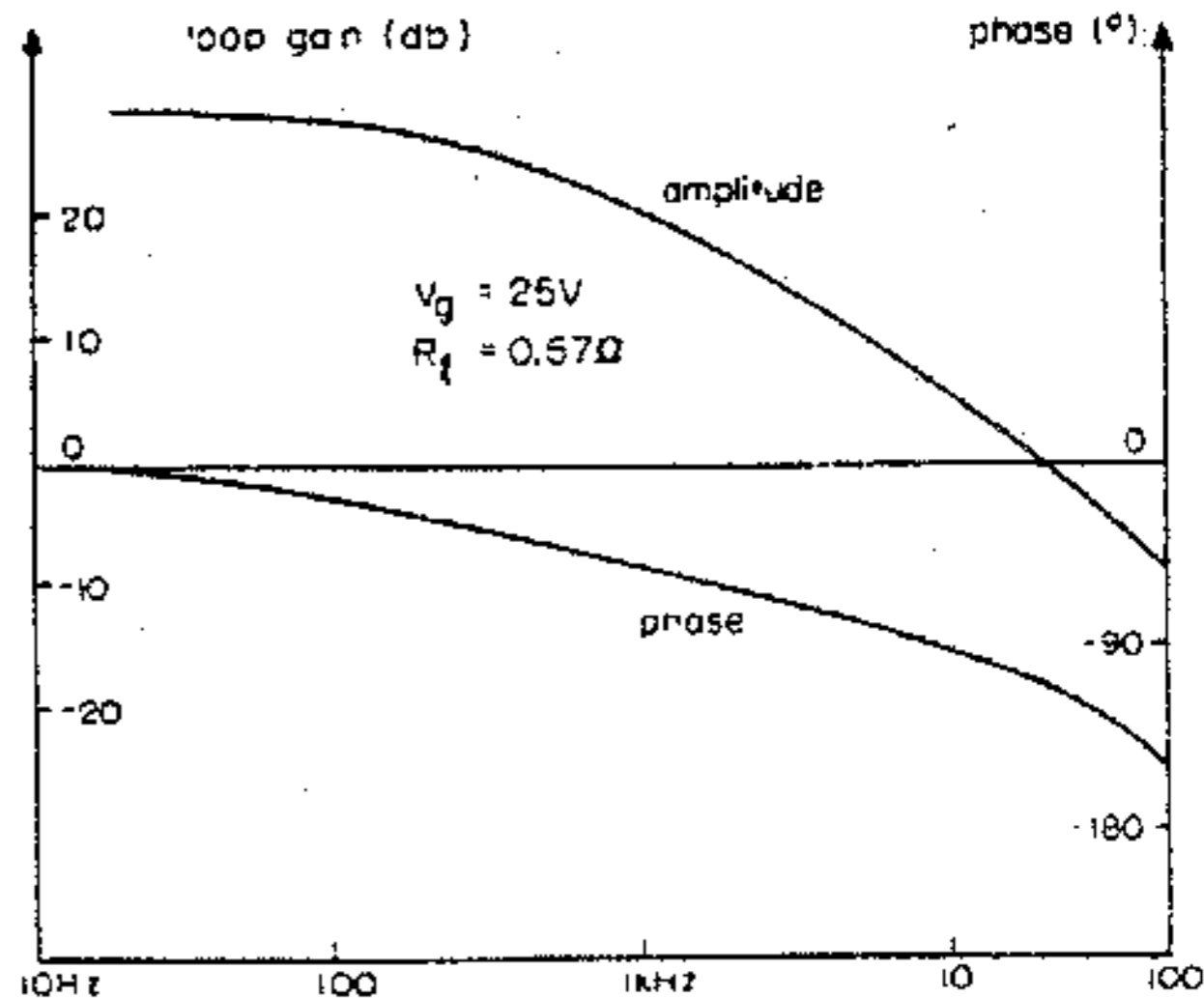


Fig. 26. Experimental loop-gain of the new push-pull switching power amplifier of Fig. 30.

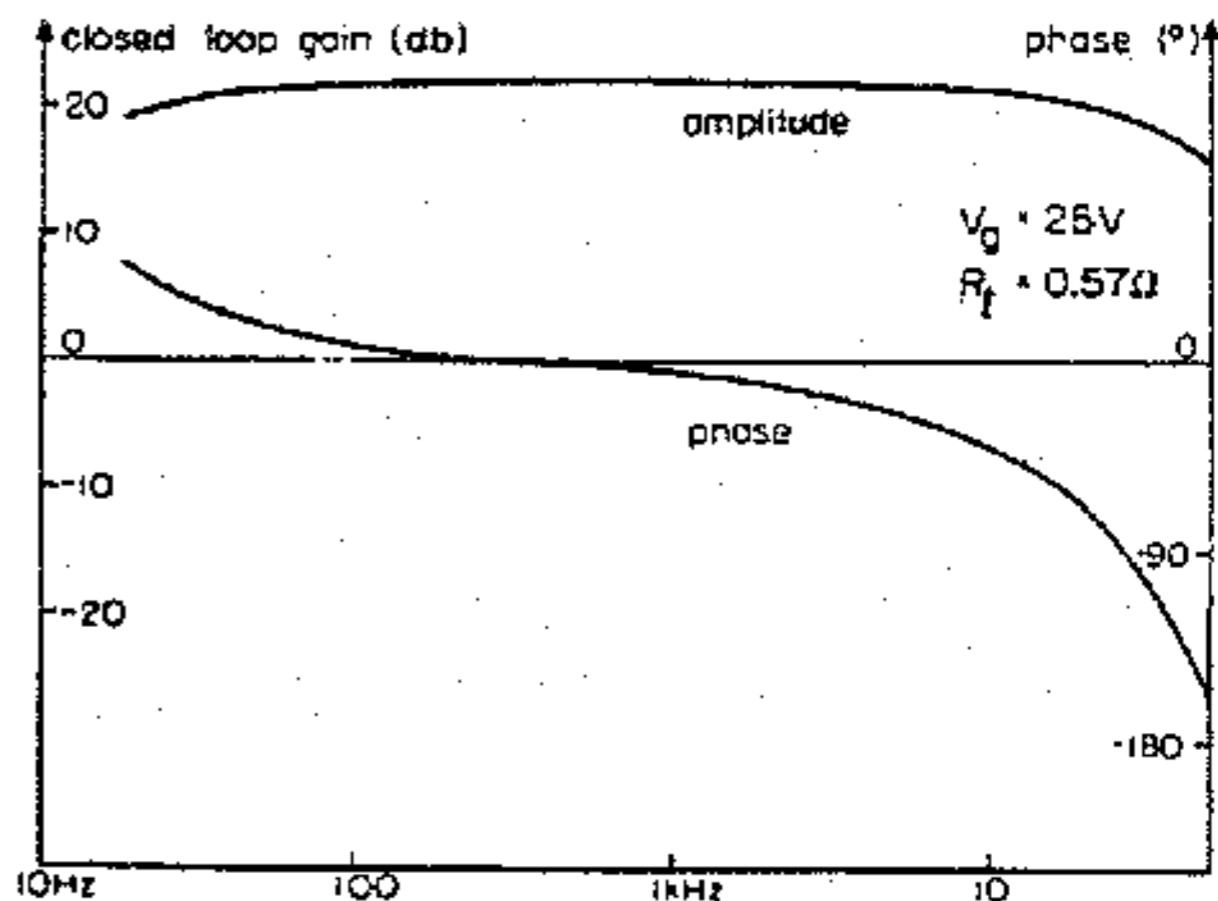


Fig. 27. Closed-loop gain of the new push-pull switching power amplifier in Fig. 30.

Finally, the modest loop-gain of 26 dB was sufficient to obtain very linear overall dc gain characteristic as shown in Fig. 28. The measurements were obtained by injecting a dc signal  $V_{in}$  past the coupling capacitance at audio input, with the feedback loop closed.

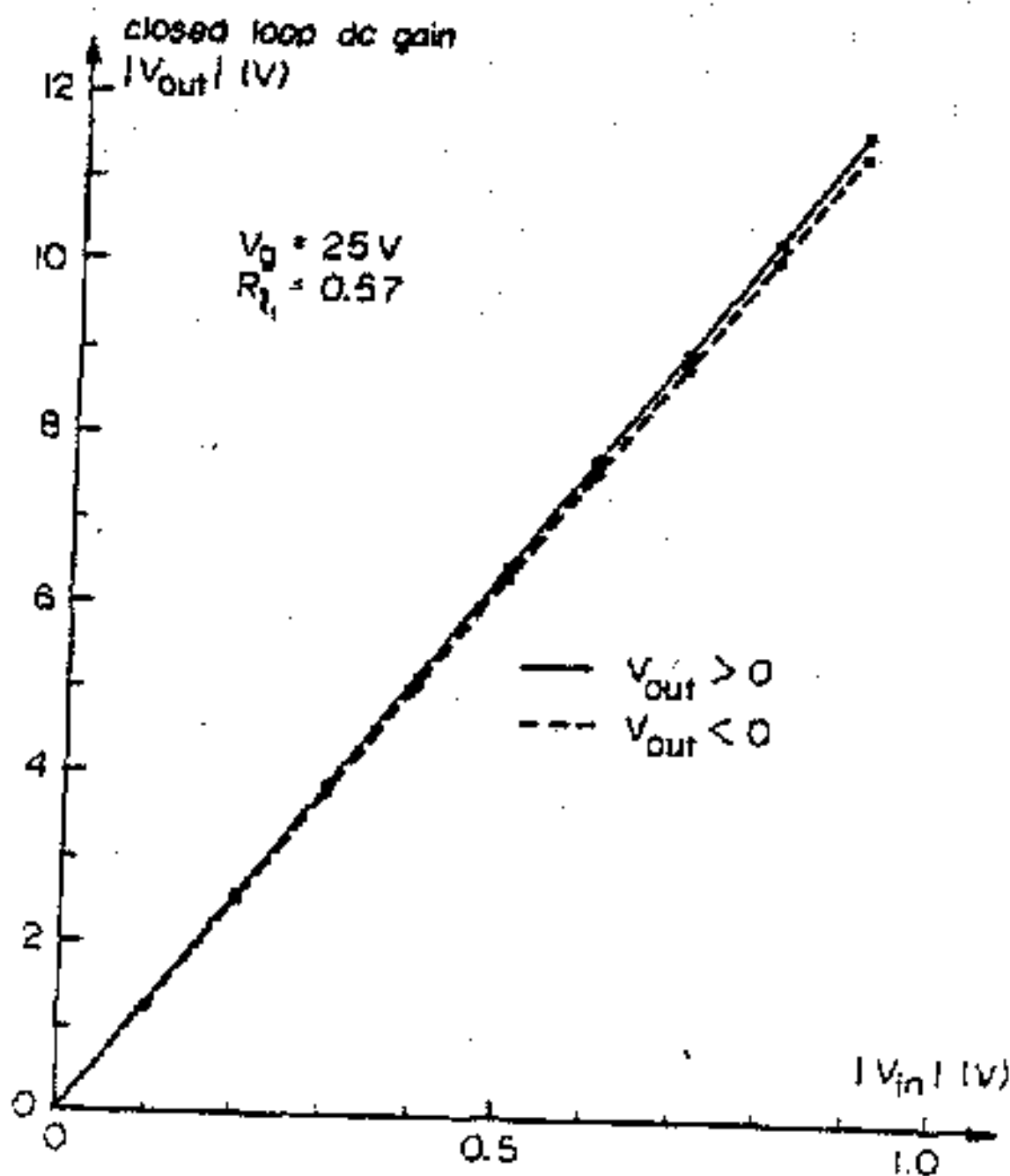


Fig. 28. Closed-loop dc gain measurements.

### 7.2 Comparison of the new and conventional switching audio amplifier design

A switching audio power amplifier based on the buck power stage was designed [16], whose detailed schematic is shown in Fig. 29. To obtain a low switching ripple of 20-30 mV, a switching frequency of  $f_s = 330$  kHz, and a relatively large size of output inductor  $L_1 = 0.63$  mH and output capacitors  $C_1 - C_4$  (40  $\mu$ F) were used. Even larger size input filters  $L_2 = 1.3$  mH, and capacitors (400  $\mu$ F, 47  $\mu$ F) were needed, designed by use of [12], for each of the two power supplies. Use of the VMOS power transistors VMP-1 from Siliconix [18] considerably simplified the driving scheme compared to an earlier version with bipolar transistors, but still required two isolated voltage drives, and additional transformers as shown in Fig. 29. A quite complex feedback compensation network was devised and after several iterations of analytical design and experimental measurements resulted in a satisfactory frequency response.

A considerably simpler and "cleaner" design based on the new converter is shown in Fig. 30. A switching regulator integrated circuit SG 3524 from Silicon General was used [17] in the feedback loop to generate a PWM signal with an 80 kHz switching

frequency. Logic gates connected as a flip-flop (7400 NAND gate) produced two out of phase input signals for the DS 0026 drivers. Diodes (1N914) were used in a modification of the Baker clamp to improve the transistor switching times, while still retaining the feature of automatically preventing the overlap of transistor on times. Inductors as small as 170  $\mu$ H were used in the power stage. Coupling of the inductors resulted in a 10:1 reduction of output current ripple, which was judged satisfactory, although a 100:1 reduction is entirely feasible. A single power supply was used, and input filters were unnecessary. Damping resistors of 0.53  $\Omega$  increased the total "parasitic" resistance  $R_{\Sigma}$  to the near-optimal value of 0.57  $\Omega$  providing improved DC linearity and excellent frequency response at a slight loss in efficiency. No feedback compensation was used; the feedback path consisted entirely of a differential amplifier (741) with flat frequency response. In fact, the overall feedback scheme used in Fig. 30 may be put on a single integrated circuit which would functionally replace the three shown in Fig. 30 (SG 3524, 7400 and DS 0026), resulting in an extremely simple, efficient and high performance switching audio power amplifier.

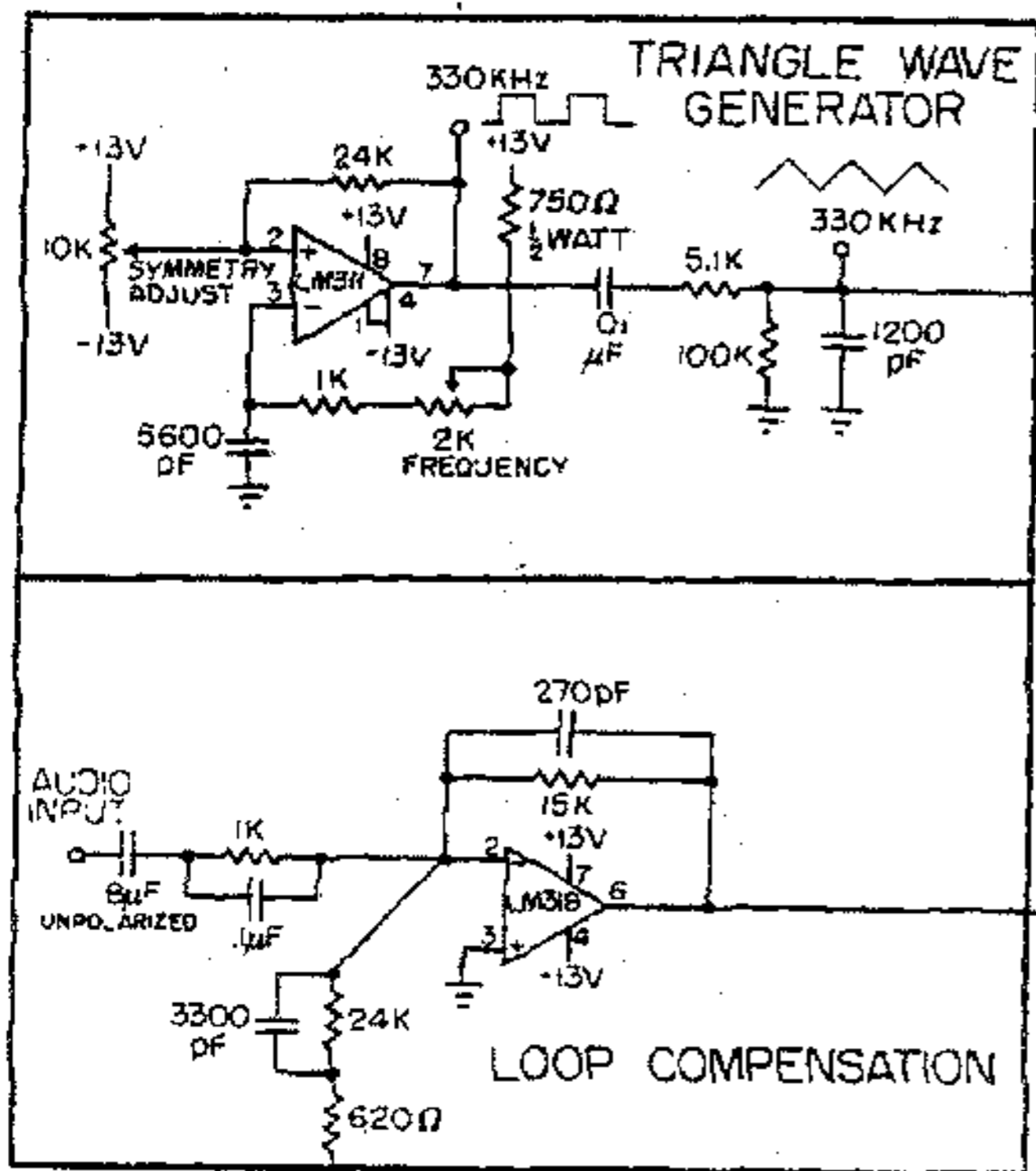
### 8. CONCLUSIONS

Although many results (new modelling techniques as well as new design topologies) have been recently accomplished in the area of switching dc-to-dc converters and regulators, proportionally much less has been done in applying these developed techniques and new converter structures to another useful, and potentially very promising area - the switching power amplifiers.

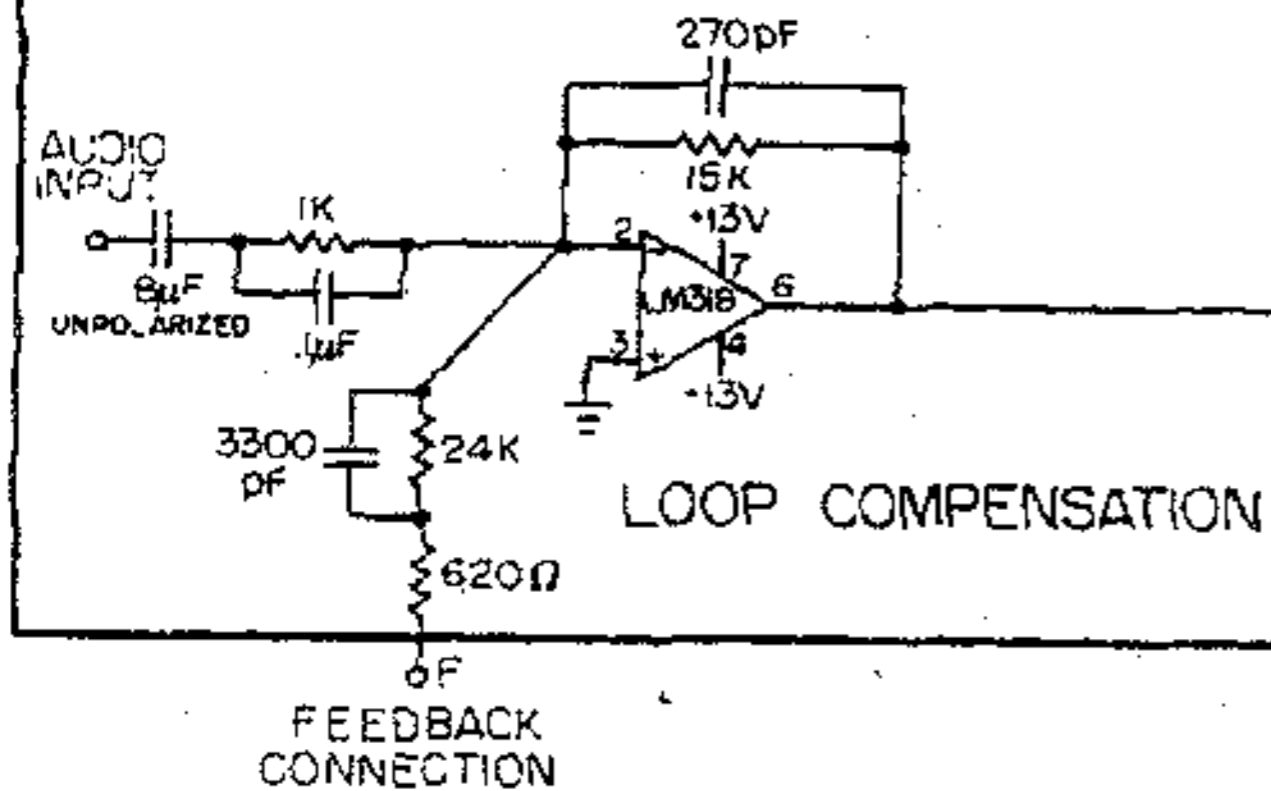
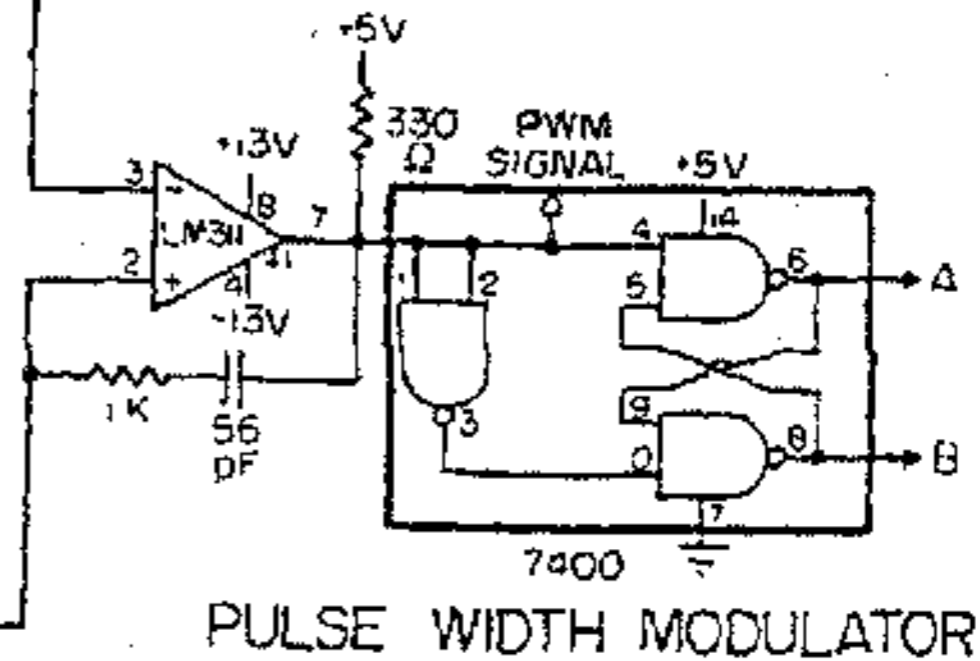
Therefore, the review of switching power amplifier principles in Section 2, showed the necessary requirements that a switching dc-to-dc converter has to fulfill in order to be used as a basic power part of the switching amplifier scheme. The general conclusions arrived at, were then used as the guidelines in modifying other known converters for switching amplifier applications.

After a brief review of the recently introduced new switching dc-to-dc converter and its coupled-inductor extension in Section 3, the general results of Section 2 were applied in Section 4 to the development of the new switching power amplifier based on these new converters. It was demonstrated that the push-pull topology and bidirectional implementation of the switches was the superior solution. In addition to preserving all the good properties and advantages of its constituent converters, some other advantages (such as single power supply, and dc current drawn from it, removal of second order harmonics) resulted from the push-pull connection itself.

The optimal values of input resistances (26) found in Section 5, only slightly degraded efficiency, but tremendously improved the dc gain linearity and resulted in significantly reduced open-loop distortion.



## CONVENTIONAL BUCK-TYPE SWITCHING POWER AMPLIFIER



INDUCTORS ARE  
 L1 - 58 TURNS #20 ON ARNOLD  
 A-930157-2 CORE.  
 L2 - 78 TURNS #20 ON ARNOLD  
 A-930157-2 CORE.

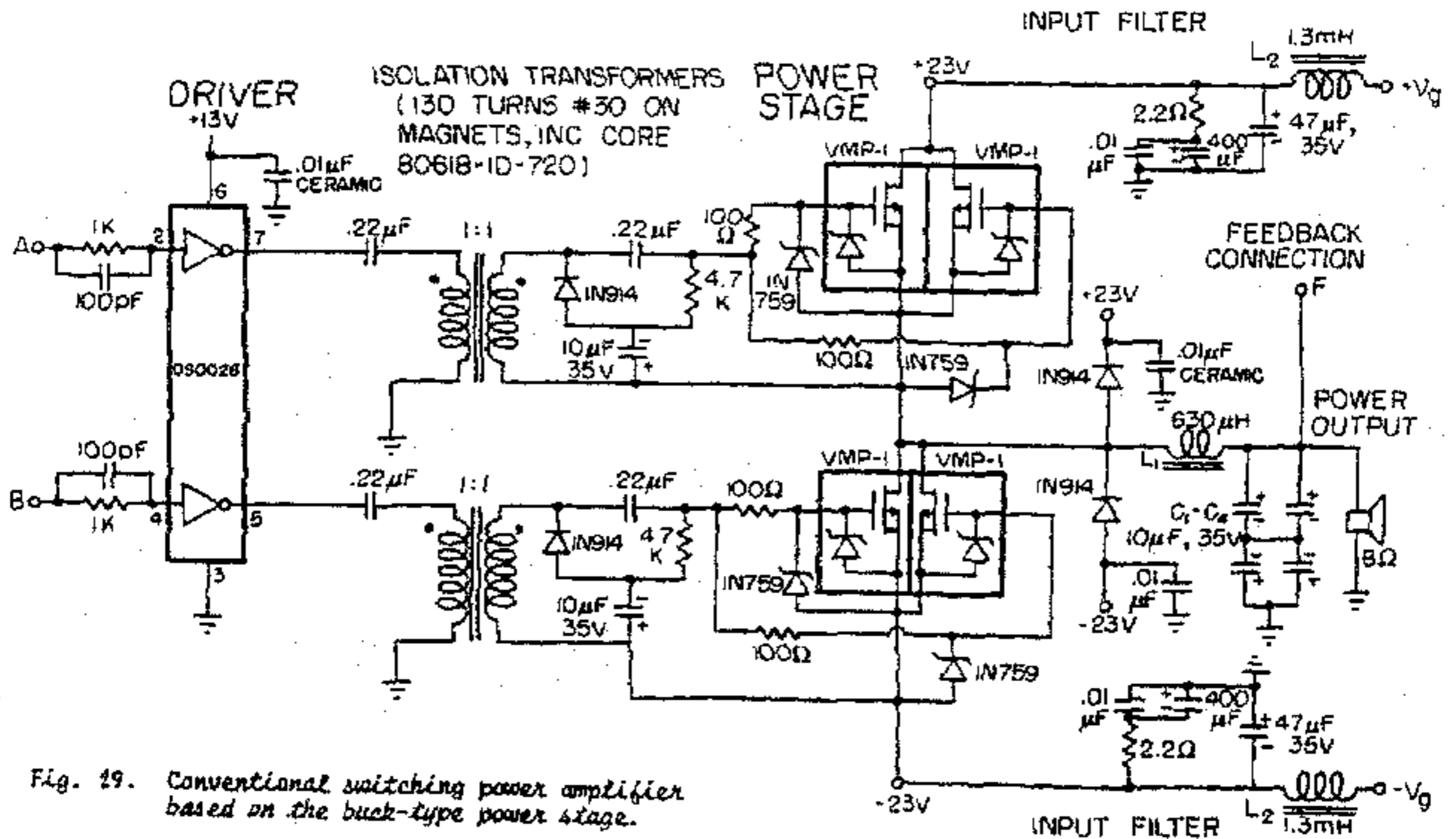
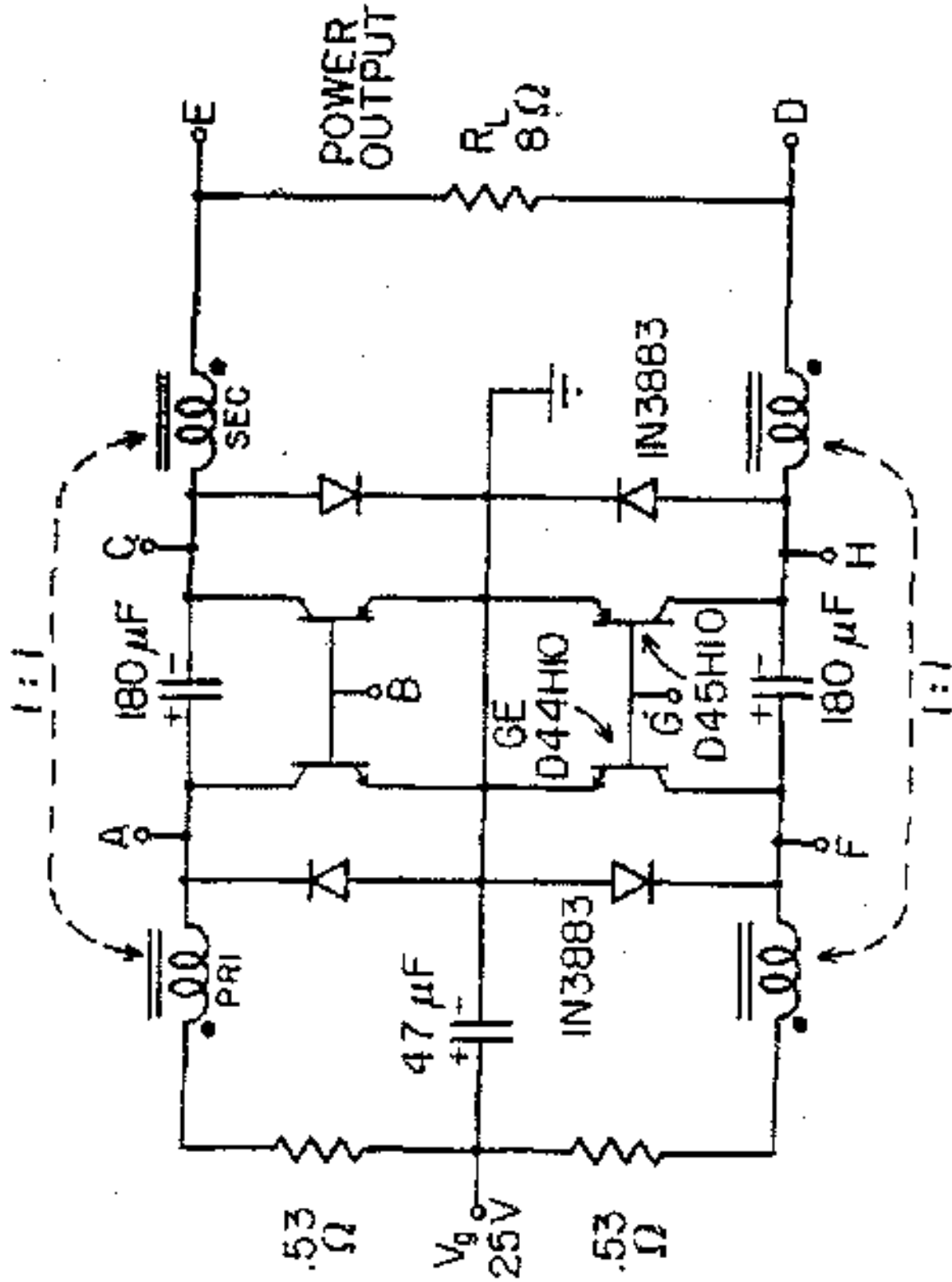


Fig. 19. Conventional switching power amplifier based on the buck-type power stage.

# NEW PUSH-PULL COUPLED- INDUCTOR SWITCHING POWER AMPLIFIER



INDUCTORS ARE  
24 TURNS(PRI) AND  
2 1/2 TURNS(SEC) NO.16  
WIRE ON A FERROXCUBE  
4229-A400-3B7 POT  
CORE.

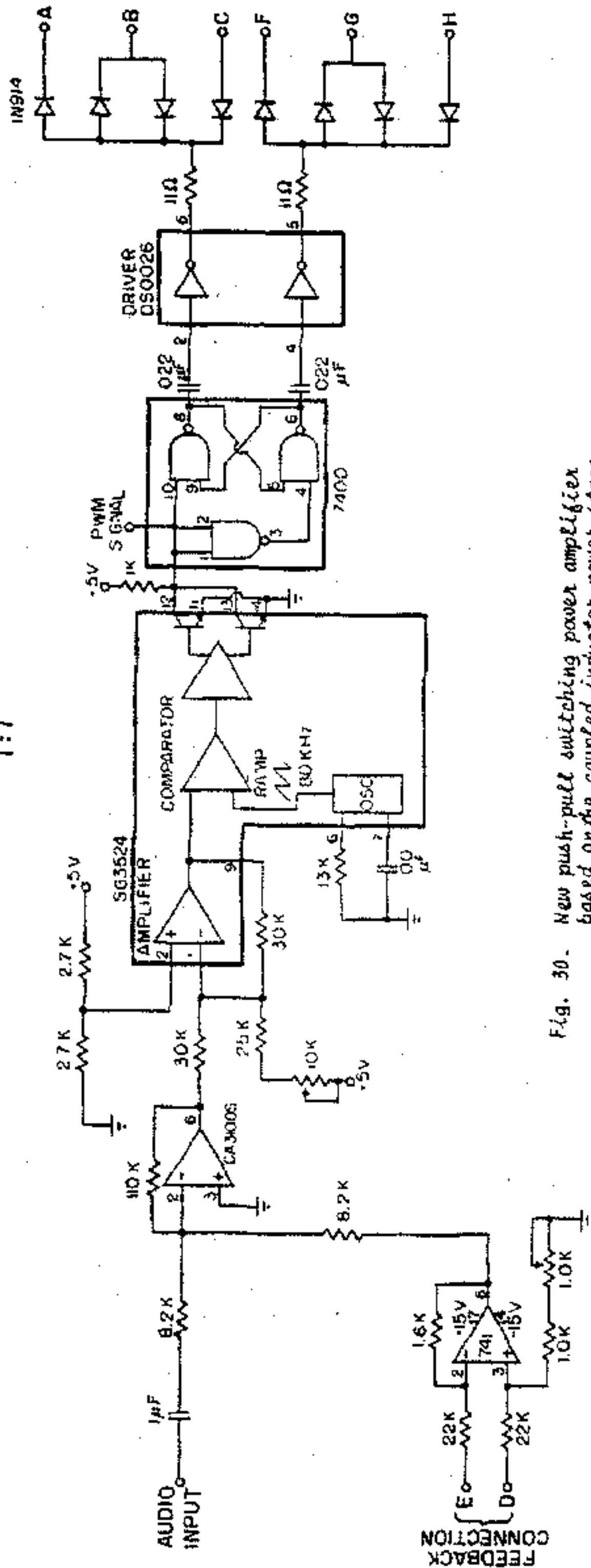


Fig. 30. New push-pull switching power amplifier based on the coupled inductor power stage.

Design-oriented analysis of Section 6 demonstrated how the technique for analysis of switching regulators may lead to the useful design equations for proper design of loop-gain frequency response in switching power amplifiers. Moreover, the optimal resistances of Section 5 were found to result in significantly improved loop-gain dynamics.

In Section 7 the comparative experimental verification of the two circuit breadboards, confirmed the superior properties of the new push-pull switching power amplifier over the conventional design based on the buck-type power stage.

In summary, some of the more important advantages of the new switching power amplifier are:

- 1) There is a need for a single power supply only.
- 2) Wide range of power supply voltages from low (10-15 V) to high (110 V) may be used owing to the basic power stage. Hence, it may be operated from lower power supply voltages than buck-type for the same output power.
- 3) There is no need for an input filter, in fact, the current drawn from the power source is *dc only* (no ripple) for a specified dc reference voltage.
- 4) All the transistors in the push-pull arrangement are *referenced to ground* (grounded emitter), thus permitting the simplest and easiest way to drive them.
- 5) Use of the complementary npn and pnp transistors driven from a single source results in *automatic prevention* of the overlap of transistor on times.
- 6) Very good dc gain linearity (for *optimal* design) results in low open-loop distortion.
- 7) Dc isolation feature although not demonstrated, may be easily introduced, if necessary for certain application, by direct use of [15]

While all these advantages are present with the new converter implementation (Fig. 16), the additional advantages are gained by the coupled-inductor extension (Fig. 19), as follows:

- 1) Low current ripple (and hence low output voltage ripple), when approaching matching condition ( $n = k$ ), completely eliminates the need for the output capacitors, thus further reducing complexity and size and weight of the amplifier. Even zero current ripple may be achieved by use of the results in [13].
- 2) Significantly improved loop-gain frequency response, permits closing the feedback loop directly with no compensation.
- 3) Further reduced complexity by use of coupled inductors on a single core, instead of two cores for two inductors.
- 4) Wide amplifier bandwidth is achieved without excessive requirement on switching frequency  $f$ .

The new push-pull switching power amplifier can, thus, find attractive applications in high efficiency, low cost, small size and weight servo power amplifiers, and also in low cost, high performance audio power amplifiers.

#### ACKNOWLEDGMENTS

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In the derivation of the differential dc voltage gain in presence of parasitics (18) and corresponding differential control transfer function (30) an omission has been made in assuming the same steady-state dc operating point for converters used separately and when they are put in this new push-pull arrangement. Namely, in the push-pull amplifier, at  $D = 0.5$  the load dc current is zero, while in each converter when used separately at the same  $D = 0.5$ , the load current is not zero. Hence, the dc gains used in (18) and ac control transfer function in (29) do not use the proper expressions valid at the same operating point (zero load current at  $D = 0.5$ ). The simplest and most straightforward way to get correct results is to apply the state-space averaging method to push-pull arrangement as a whole without regard to its individual constituent converter dc and ac transfer properties.

The differential dc voltage gain of the push-pull amplifier is, thus,

$$\frac{V}{V_B} = \frac{D - D'}{DD'} \frac{1}{1 + \alpha_1 [(D/D')^2 + (D'/D)^2] + 2\alpha_2} \quad (39)$$

which apparently differs from the previous result given in (18). However, the subsequent optimization procedure (equations (10) through (25)) is not altered and when applied to (39) instead, results in

$$1 + 2\alpha_2 = 14\alpha_1 \quad (40)$$

which is although analytically different, numerically equivalent to (23). For example, the optimum value is

$$\alpha_{1 \text{ opt}} = \frac{1}{14} = 0.0714 \text{ for } \alpha_2 \ll 1 \quad (41)$$

the result which is numerically very close to 0.0718 given by (25). Hence approximately the same optimum resistance  $R_{\text{opt}} = 0.58 \Omega$  still applies.

Note, however, that the dynamic response (control transfer function) is qualitatively changed from the expression (30), because of the absence of any zeros in the push-pull amplifier responses as given by

$$G_d = \frac{\hat{v}}{\hat{d}} = 8V \frac{1}{1 + 4 \frac{L_1}{R/2} s + 4L_1 C_{10} s^2 + 4s^3 \frac{L_1 C_1 L_e}{R/2}} \quad (42)$$

The poles of control transfer function are given by the same analytical expression as in (30) except half of the load resistance ( $R/2$ ) should have been used in (30), because of single-ended versus differential loadings.