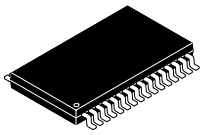


SLES039 – JUNE 2002

TRUE DIGITAL STEREO AUDIO AMPLIFIER WITH PWM STEREO POWER OUTPUT STAGE

FEATURES

- **2 × 15 W High-Quality Digital Amplifier Power Stage**
- **Single-Ended Output**
- **>95-dB Dynamic Range (TDAA System)**
- **THD+N < 0.1% (1 kHz, 1 W to 15 W RMS Into 4 Ω)**
- **Power Efficiency > 90% Into 4-Ω to 8-Ω Load**
- **Low Profile, SMD 32-Pin PowerPAD™ Package Requires No Heat-Sink When Using Recommended Layout**
- **2 × 15-W RMS Continuous Power Into 4 Ω**
- **Self-Protecting Design**
- **3.3-V Digital Interface**
- **EMI Compliant When Used With Recommended System Design**

APPLICATIONS

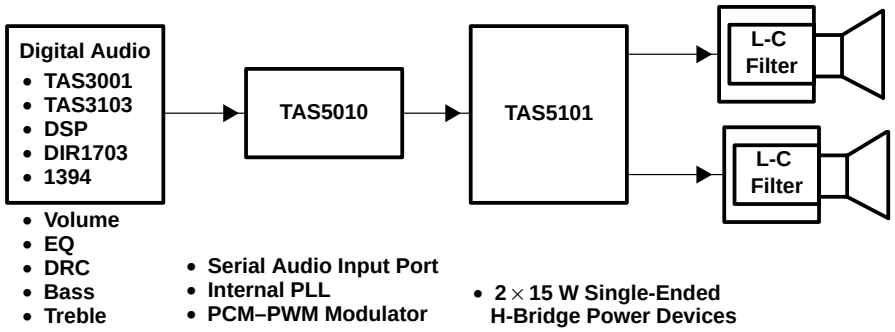
- **Digital TV Audio Amplifier**
- **Car Audio Amplifiers and Head Units**
- **Internet Music Appliance**
- **Mini/Micro Component Systems**

DESCRIPTION

The TAS5101 is a high-performance true digital stereo audio amplifier (TDAA) Power Stage, designed to drive 2 × 15 watts per channel. The TAS5101 incorporates TI's equibit™ technology and is used in conjunction with a Digital Audio PWM processor (TAS50xx) to deliver high-power, true digital audio amplification. The efficiency of this digital amplifier can be greater than 90%, reducing the size of both the power supplies and heat sinks needed. The TAS5101 accepts a stereo PWM 3.3V input and controls the switching of an internal CMOS H-bridge.

When used with the TAS50xx PWM Processor, system performance of less than 0.09% THD is attainable. Over-current protection, over-temperature, and under-voltage protections are built into the TAS5101, safeguarding the H-bridge and speakers against output shorts, over-voltage conditions, and other fault conditions that could damage the system.

TYPICAL TDAA STEREO AUDIO SYSTEM

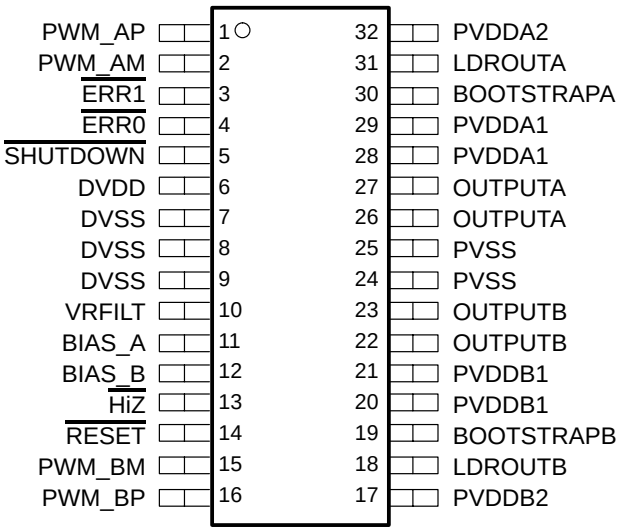


NOTE:
The TAS5000 in **NOT** recommended for use with the TAS5101

terminal assignments

The TAS5101 is offered in a thermally enhanced 32-pin HTSSOP surface-mount package (DAP).

DAP PACKAGE
(TOP VIEW)



ordering information

T_A	PACKAGE	TAPE and Reel
0°C to 70°C	TAS5101DAP	TAS5101DAPR
–40°C to 85°C	TAS5101IDAP	TAS5101IDAPR

references

TAS5010 *Digital Audio PWM Processor* Data Manual – TI Literature Number SLAS328

System Design Considerations for True Digital Audio Power Amplifiers – TI Literature Number SLAA117

Digital Audio Measurements – TI Literature Number SLAA114

PowerPAD Thermally Enhanced Package – TI Literature Number SLMA002

TAS5101SE Evaluation Module User's Guide – TI Literature Number SLEA006

suggested system block diagrams

See application note SLAA117 for more details.

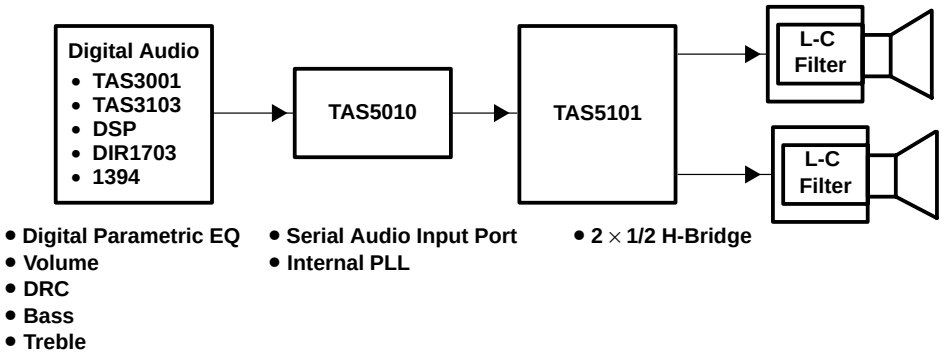
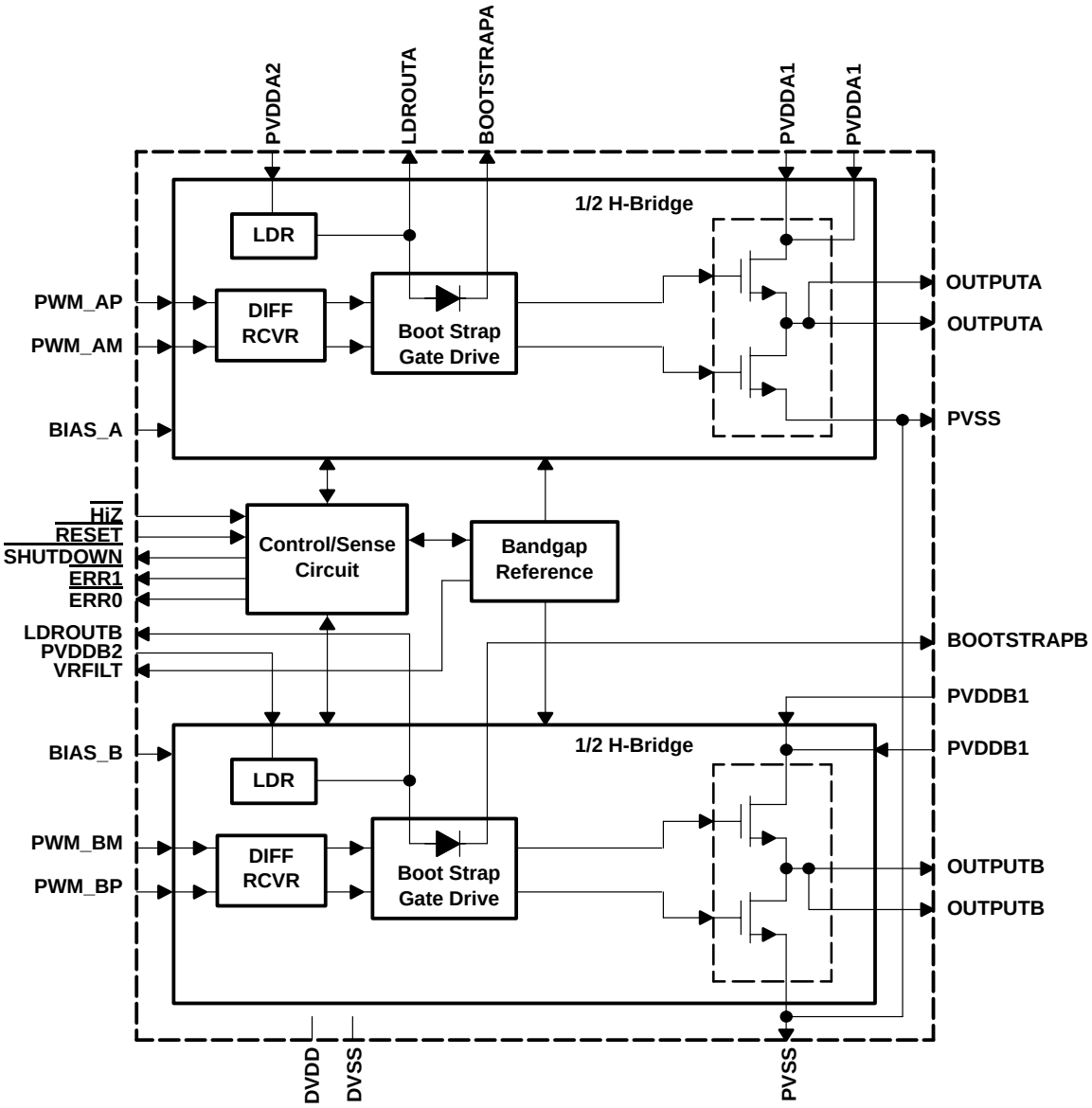


Figure 1. System #1: Stereo Configuration With TAS3001 Digital Audio Processor

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BIAS_A	11	I	Connect external resistor to DVSS. See application note SLAA117
BIAS_B	12	I	Connect external resistor to DVSS. See application note SLAA117
BOOTSTRAPA	30	O	Bootstrap capacitor pin for H-bridge A
BOOTSTRAPB	19	O	Bootstrap capacitor pin for H-bridge B
DVDD	6	I	3.3-V digital voltage supply for logic
DVSS	7, 8, 9	I	Digital ground for logic is internally connected to PVSS. All three pins must be tied together but not connected externally to PVSS. See Figure 5.
$\overline{\text{ERR1}}$	3	O	Error/warning report indicator. This output is open drain with internal pullup resistor.
$\overline{\text{ERR0}}$	4	O	Error/warning report indicator. This output is open drain with internal pullup resistor.
LDROUTA	31	O	Low voltage drop-out regulator output A (not to be used to supply current to external circuitry)
LDROUTB	18	O	Low voltage drop-out regulator output B (not to be used to supply current to external circuitry)
OUTPUTA	26, 27	O	H-bridge output A
OUTPUTB	22, 23	O	H-bridge output B
PVDDA1	28, 29	I	High voltage power supply, H-bridge A
PVDDA2	32	I	High voltage power supply for low-dropout voltage regulator A-side
PVDDB1	20, 21	I	High voltage power supply, H-bridge B
PVDDB2	17	I	High voltage power supply for low-dropout voltage regulator B-side
PVSS	24, 25	I	High voltage power supply ground
$\overline{\text{HiZ}}$	13	I	HiZ = 0, when asserted, the H-bridge output is set to high-impedance mode
PWM_AP	1	I	PWM input A(+)
PWM_AM	2	I	PWM input A(–)
PWM_BP	16	I	PWM input B(+)
PWM_BM	15	I	PWM input B(–)
$\overline{\text{RESET}}$	14	I	Reset and mute mode = 0, normal mode = 1, when in reset mode, H-bridge MOSFETs are in low-low output state. Asserting the $\overline{\text{RESET}}$ signal low causes all fault conditions to be cleared.
$\overline{\text{SHUTDOWN}}$	5	O	Device is in shutdown due to fault condition, normal mode = 1, shutdown = 0. The shutdown condition can be cleared by asserting the $\overline{\text{RESET}}$ signal. This output is open drain with internal pullup resistor.
VRFILT	10	O	A filter capacitor should be added between VRFILT and DVSS pins.

NOTE: The four PWM inputs: PWM_AP, PWM_AM, PWM_BP, and PWM_BM must always be connected to the TAS5010 output pins, and never left floating. Floating PWM input pins will cause an illegal PWM input state signal to be asserted.

Dual pins: OUTPUTA, OUTPUTB, PVDDA1 and PVDDB1 must have both pins connected externally to the same point on the circuit board, respectively. Both PVSS pins must also be connected together externally. These multiple pins are for the high current DMOS output devices. Failure to connect all the multiple pins to the same respective node will result in excessive current flow in the internal bond wires and can cause the device to fail. All electrical characteristics are specified and measured with all of the multiple pins connected to the same node, respectively.

functional description

PWM H-bridge state control

The digital interface control signals consists of PWM_AP, PWM_AM, PWM_BP, and PWM_BM. These signals are a complementary differential signal format for the A-side H-bridge and the B-side H-bridge.

bootstrapped gate drive

The TAS5101 includes 2 dedicated bootstrapped power supplies. A bootstrap capacitor is connected between the individual bootstrap pin and the associated output as described in the application note SLAA117. For example, a capacitor will be connected between the BOOTSTRAPA pin and OUTPUTA pin, and another capacitor will be connected between the BOOTSTRAPB pin and the OUTPUTB pin. The bootstrap power supply minimizes the number of high voltage power supply levels externally supplied to the system while providing a low noise supply level for driving the high-side N-channel DMOS transistors. See application note SLAA117 for details.

low-dropout voltage regulator

Two on-chip low-dropout voltage regulators (LDO) are provided to minimize the number of external power supplies needed for the system. These voltage regulators are for internal circuits only and cannot be used for external circuitry. Each LDO is dedicated to an H-bridge and its gate driver. An LDO output capacitor is connected between the individual LDO output pin and the associated output return as described in the application note SLAA117. For example, a capacitor will be connected between the LDROUTA pin and PVSS pin, and another capacitor will be connected between the LDROUTB pin and PVSS pin. This capacitor is usually 0.1 μF.

high-current H-bridge output stage

The positive outputs of the H-bridge are the two OUTPUTA pins. The negative outputs of the H-bridge are the two OUTPUTB pins. The logic for the input command to H-bridge outputs is described in the H-bridge output mapping section below. When the TAS5101 is in the normal mode, as seen in the H-bridge output mapping tables, the outputs are decoded from the inputs. However, the TAS5101 is immediately shut down if any of the following error conditions occur: over-current, over-temperature, low regulator output voltage, or an illegal PWM input state is applied. For these conditions, the outputs are set to the appropriate disabled state as specified in the H-bridge output mapping section, and the $\overline{\text{SHUTDOWN}}$ pin is set low.

H-bridge output mapping

The A-side and B-side H-bridge output is designed to the following truth table:

INPUTS				OUTPUTS		DESCRIPTION
$\overline{\text{RESET}}$	$\overline{\text{HiZ}}$	PWM_AP/BP	PWM_AM/BM	$\overline{\text{SHUTDOWN}}$	OUTPUTA/B	
X	X	X	X	0	0 or Hi-Z†	Shutdown
X	0	X	X	1	Hi-Z	High Impedance
0	1	X	X	1	0	Low
1	1	0	0	0	0	Low
1	1	0	1	1	0	Normal
1	1	1	0	1	1	Normal
1	1	1	1	0	0	Low

† Output is 0 for low voltage, over temperature, and illegal input. Hi-Z is for over current.

control/sense circuitry

The control/sense circuitry consists of the following 3.3-V logic level pins: $\overline{\text{HiZ}}$, $\overline{\text{RESET}}$, $\overline{\text{ERR0}}$, $\overline{\text{ERR1}}$, and $\overline{\text{SHUTDOWN}}$. The active-low $\overline{\text{HiZ}}$ input pin powers down all internal circuitry and forces the H-bridge outputs to the Hi-Z state. When the $\overline{\text{HiZ}}$ pin is low, the open drain $\overline{\text{ERR0}}$, $\overline{\text{ERR1}}$, and $\overline{\text{SHUTDOWN}}$ pins are also disabled so that their outputs can be pulled high. The active-low $\overline{\text{RESET}}$ input pin forces the H-bridge outputs to the low-low state and resets the over-current shutdown latch. The $\overline{\text{HiZ}}$ pin overrides the $\overline{\text{RESET}}$ pin. The $\overline{\text{ERR0}}$, $\overline{\text{ERR1}}$, and $\overline{\text{SHUTDOWN}}$ outputs indicate the following conditions in the TAS5101 as shown in the table below. These three outputs are open-drain connections with internal pullup resistors so that wire-ORed connections can be made by the user with other external control devices. The short circuit protect error condition will latch the TAS5101 in this shutdown state and force the H-bridge outputs to the Hi-Z state until the device is reset by means of the $\overline{\text{RESET}}$ pin. The illegal PWM input state, over-temperature, and low regulator voltage error conditions will not latch the device in the shutdown condition. Instead the H-bridge outputs are forced to the low-low state and the TAS5101 will return to normal operation as soon as the error condition ends. Loss of clocking PWM signal is also considered an illegal PWM input state.

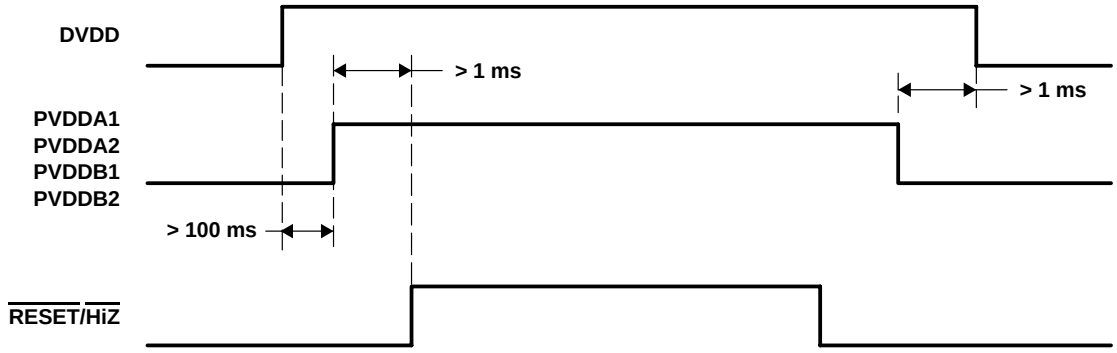
$\overline{\text{SHUTDOWN}}$	$\overline{\text{ERR1}}$	$\overline{\text{ERR0}}$	FUNCTION	OUTPUTA	OUTPUTB
0	0	0	Illegal PWM input state	Low	Low
0	0	1	Short circuit protect (latch)	Hi-Z	Hi-Z
0	1	0	Over temperature protect	Low	Low
0	1	1	Low regulator voltage protect	Low	Low
1	0	0	Reserved	—	—
1	0	1	Reserved	—	—
1	1	0	High temperature – warning	Normal	Normal
1	1	1	Normal operation	Normal	Normal

device operation

power sequences

system power-up/power-down sequencing

The recommended power-up/power-down sequence is shown in Figure 3. For proper operation the $\overline{\text{RESET}}$ signal should be kept LOW when both DVDD and output power (PVDDA1, PVDDA2, PVDDB1, and PVDDB2) are being applied. The $\overline{\text{RESET}}$ signal should remain LOW for at least 1 ms after output power is applied.



NOTE: This power-up/power-down sequence will ensure that there are no device reliability issues. However, audio artifacts during power cycling may occur (see TAS5101_SE Application Report (SLEA001) for more information).

Figure 2. Power-Up/Power-Down Sequence

$\overline{\text{RESET}}$ function

The device is put into a reset condition when the (active low) $\overline{\text{RESET}}$ signal is asserted. While in the reset state, the input H-bridge control signals consisting of PWM_AP, PWM_AM, PWM_BP, and PWM_BM are ignored, and the H-bridge MOSFETs are placed in a state where OUTPUTA and OUTPUTB are both low. Asserting the $\overline{\text{RESET}}$ signal low also causes the short circuit protection latch to be reset. The $\overline{\text{RESET}}$ and $\overline{\text{HiZ}}$ signals are normally connected to the VALID signal from the TAS5010, when used in a single-ended configuration.

$\overline{\text{HiZ}}$ function

The $\overline{\text{HiZ}}$ function places the output MOSFETs in a high-impedance state when this function is asserted by placing pin 13 at logic low. This function is usually used in conjunction with the $\overline{\text{RESET}}$ function during power on and off to reduce or eliminate “pops and clicks” associated with powering the amplifier.

reinitialization sequence

Proper initial conditions for this device include asserting the $\overline{\text{RESET}}$ and $\overline{\text{HiZ}}$ signals until the reset operation has completed (1 ms). Additionally, when using this device with the TAS5010 controller, this function can be accomplished by asserting the reset pin on the TAS5010 during the reset sequence (see Figure 3).

audio application considerations

power supply decoupling

Power supply decoupling and layout optimization information should be obtained by following the detailed information in the evaluation module user’s guide, SLEA006.

optimal power transfer for H-bridge

The TAS5101 is a power H-bridge that is designed to deliver 2×15 W/rms into loads of 4 Ω in a single-ended configuration. Rather than requiring the usual heatsink, the package is designed to deliver this wattage by careful layout as described in the application note SLAA117. Careful attention must be given to the value of the high-voltage power supply level for a given load resistance. See recommended operating conditions.

audio application considerations (continued)

reconstruction output filter

An output reconstruction filter is required between the H-bridge outputs and the loudspeaker load. This second order low-pass filter passes the audio information to the loudspeaker, while filtering out the high frequency out-of-band information contained in the H-bridge output PWM pulses. The values of the L and C components selected are dependent on the loudspeaker load impedance. See application note SLAA117.

fault indicator usage

The TAS5101 is a self-protecting device that provides device fault reporting, including over-temperature protect, under-voltage lockout (low-regulator voltage), and short circuit protection. The short circuit protection protects against short circuits that may occur at the loudspeaker load when configured according to the application note SLAA117. The TAS5101 is not recommended for driving loads less than 4 Ω, since the internal current limit protection might be activated.

An under-voltage lockout signal occurs when an insufficient voltage level is present on the LDROUTA or LDROUTB pins. During this condition gate drive levels are not sufficient for driving the power MOSFETs. Normal operation is resumed when the minimum proper LDROUTA or LDROUTB level is obtained, and the low regulator voltage protect signal is de-asserted. See the control/sense circuitry section for error and warning conditions.

A high temperature warning signal is asserted on pin $\overline{\text{ERR0}}$ when the device temperature exceeds 125°C typical.

If the internal device temperature exceeds 150°C typical, the over temperature protect signal is asserted and the TAS5101 is shut down. The device will re-enable once the temperature drops to 125°C typical. See the control/sense circuitry section for error and warning conditions.

Detection of an illegal PWM input state or the loss of a clocking PWM input signal will cause an illegal PWM input state signal to be asserted on the $\overline{\text{ERR1}}$and $\overline{\text{ERR0}}$ pins and will set the $\overline{\text{SHUTDOWN}}$ pin to the low state.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

DC supply voltage range: DVDD to DVSS	–0.3 V to 5.5 V
$\overline{\text{PWM\_AP}}$, $\overline{\text{PWM\_AM}}$, $\overline{\text{PWM\_BP}}$, $\overline{\text{PWM\_BM}}$	–0.3 V to DVDD + 0.3 V
$\overline{\text{RESET}}$, $\overline{\text{HiZ}}$	–0.3 V to DVDD + 0.3 V
PVDDA1 to PVSS, PVDDB1 to PVSS	–0.3 V to 28 V
PVDDA2 to PVSS, PVDDB2 to PVSS	–0.3 V to 28 V
Output DMOS drain-to-source breakdown voltage	28 V
Operating junction temperature range, T_J	–40°C to 150°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds)	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (nominal output power = 2 × 15 W (RMS), T_A = 25°C)

thermal data†

PARAMETER		MIN	NOM	MAX	UNIT
Shutdown junction temperature, $T_{J(SD)}$			150		°C
Warning junction temperature, $T_{J(W)}$			125		°C
Operating ambient temperature, T_A	Commercial	0	25	70	°C
	Industrial	–40	25	85	
Thermal resistance junction-to-ambient, θ_{ja}	2 oz. trace and copper pad with solder		23.5		°C/W
Thermal resistance junction-to-case, θ_{jc}	2 oz. trace and copper pad without solder		0.32		°C/W
Thermal resistance junction-to-ambient, θ_{ja}	2 oz. trace and copper pad without solder		44.3		°C/W

† One of the most influential components on the thermal performance of a package is board design. In order to take full advantage of the heat dissipating abilities of the PowerPAD packages, a board must be used that acts similar to a heat sink and allows for the use of the exposed (and solderable), deep downset pad. See Appendix A of the *PowerPAD Thermally Enhanced Package* application note, TI literature number SLMA002 and the *Thermal Design of the PowerPad PCB Layout* section of the *System Design Considerations for True Digital Audio Power Amplifiers* application note, TI literature number SLAA117.

R_L = 4 Ω to 8 Ω

PARAMETER			MIN	NOM	MAX	UNIT
Supply voltage	Digital	DVDD to DVSS	3	3.3	3.6	V
	Regulator	PVDDA2 to PVSS	16.5	26.5	28	V
		PVDDB2 to PVSS	16.5	26.5	28	
		PVDDA2 to PVSS‡	10.5		16.5	
		PVDDB2 to PVSS‡	10.5		16.5	

† If PVDD is greater than 26.5 V, 15 Watts per channel is still the maximum specified continuous output power.

‡ If using a PVVD power supply less than 16.5 V, connect LDROUTA to PVDDA2 and connect LDROUTB to PVDDB2. Under this condition H-Bridge forward on-state resistance is increased. This will increase internal power dissipation. Maximum output power may need to be reduced to meet thermal conditions.

maximum available power at common load impedance for DAP package unclipped (0 dB) level

LOAD IMPEDANCE (Ω)	PVDAA1/PVDDB1 (VDC)	APPROXIMATE MAX OUTPUT POWER (W)	THD+N AT MAX POWER AND 1 kHz INPUT†
4	26.5	15	< 0.1%
6	27	12.85	< 0.09%
8	27	9.64	< 0.09%

† Dependent on board design and component selection.

static digital specifications

$\overline{\text{RESET}}$, $\overline{\text{HiZ}}$, PWM_AP, PWM_AM, PWM_BP, PWM_BM, T_A = 25°C, DVDD = 3.3 V

PARAMETERS	MIN	MAX	UNIT
High-level input voltage, V_{IH}	2		V
Low-level input voltage, V_{IL}		0.8	V
Input leakage current	–10	10	μA

$\overline{\text{ERR0}}$, $\overline{\text{ERR1}}$, $\overline{\text{SHUTDOWN}}$, (open drain with internal pullup resistor) T_A = 25°C, DVDD = 3.3 V)

PARAMETERS	MIN	MAX	UNIT
Internal pullup resistors from $\overline{\text{SHUTDOWN}}$, $\overline{\text{ERR0}}$, $\overline{\text{ERR1}}$ to DVDD	15		kΩ
Low-level output voltage (I_O = 4 mA), V_{OL}		0.4	V

TAS5010/TAS5101 system performance measured at the speaker terminals

See the TI Literature Number SLAA117 for TAS5010/TAS5101 system performance.

electrical characteristics

supply, T_A = 25°C ($F_{switching}$ = 384 kHz, OUTPUTA and OUTPUTB not connected, DVDD = 3.3 V, PVDDA1 = 26.5 V, PVDDB1 = 26.5 V, PVDDA2 = 26.5 V, PVDDB2 = 26.5 V, 50% input duty cycle)

PARAMETER			TYP	MAX	UNIT
Supply current	DVDD	Operating	2		mA
	PVDDA1+PVDDB1+ PVDDA2+PVDDB2	Operating†	20		mA

† 13-kΩ resistor from BIAS_A (pin 11) to DVSS and 13-kΩ resistor from BIAS_B (pin 12) to DVSS.

H-Bridge transistors, PVDDA2 = PVDDB2 = 22 V, DVDD = 3.3 V, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Drain-to-source breakdown voltage	I_D = 1 mA, $\overline{\text{HiZ}}$ = 0, Hi-Z state	28			V
Forward on-state resistance, low-side drivers OUTPUTA and OUTPUTB to PVSS	I_{SINK} = 2.5 A, See Notes 2, 3, and 4, PWM_AP = PWM_BP = 0, PWM_AM = PWM_BM = 1		0.2		Ω
Forward on-state resistance, high-side drivers PVDDA1 to OUTPUTA, PVDDB1 to OUTPUTB	I_{SOURCE} = 2.5 A, See Notes 2, 3, and 5, PWM_AP = PWM_BP = 1, PWM_AM = PWM_BM = 0		0.2		Ω
On-state resistance matching low side			98%		
On-state resistance matching high side			98%		

NOTES: 1. Test time should be < 1 ms to avoid temperature change.
2. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
3. Connect PVDDA2 and PVDDB2 to 26.5-V power supply with respect to PVSS. LDROUTA, LDROUTB, BOOTSTRAPA, and BOOTSTRAPB pins open.
4. Connect PVDDA2 to 26.5-V power supply with respect to PVSS. LDROUTA, LDROUTB, BOOTSTRAPA and BOOTSTRAPB capacitors are connected respectively. Clock PWM inputs to allow bootstrap capacitors to charge. 93–99% modulation must be used on PWM_AP, PWM_AM, PWM_BP, and PWM_BM inputs to prevent the activity detector from shutting down the device during this measurement. Note that $F_{switching}$ = 384 kHz.

electrical characteristics, voltage regulator, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage (LDROUTA, LDROUTB)	I_O = 5 mA, See Note 6, PVDDA2 = PVDDB2 = 18 V to 28 V, DVDD = 3.3 V	14.5	15.3	16	V

NOTE 5: These voltage regulators are for internal gate drive circuits only and are not to be used under any circumstances to supply current to external circuity.

THERMAL INFORMATION

The thermally enhanced DAP package is based on the 32-pin HTSSOP, but includes a thermal pad (see Figure 4) to provide an effective thermal contact between the IC and the PWB.

Traditionally, surface mount and power have been mutually exclusive terms. A variety of scaled-down TO-220 type packages have leads formed as gull wings to make them applicable for surface-mount applications. These packages, however, have two shortcomings: they do not address the very low profile requirements (<2 mm) of many of today's advanced systems, and they do not offer a terminal-count high enough to accommodate increasing integration. On the other hand, traditional low-power surface-mount packages require power-dissipation derating that severely limits the usable range of many high-performance analog circuits.

The PowerPAD package (thermally enhanced HTSSOP) combines fine-pitch surface-mount technology with thermal performance comparable to much larger power packages.

The PowerPAD package is designed to optimize the heat transfer to the PWB. Because of the very small size and limited mass of a HTSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a patented lead-frame design and manufacturing technique to provide a direct connection to the heat-generating IC. When this pad is soldered or otherwise thermally coupled to an external heat dissipater, high power dissipation in the ultrathin, fine-pitch, surface-mount package can be reliably achieved.

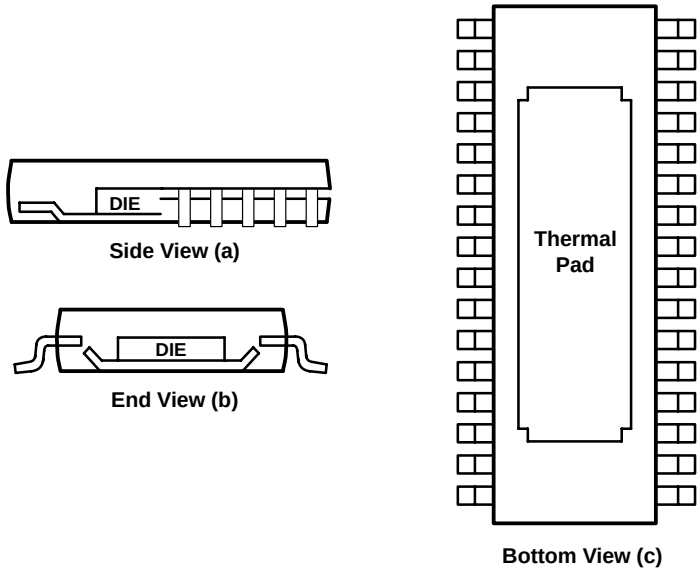
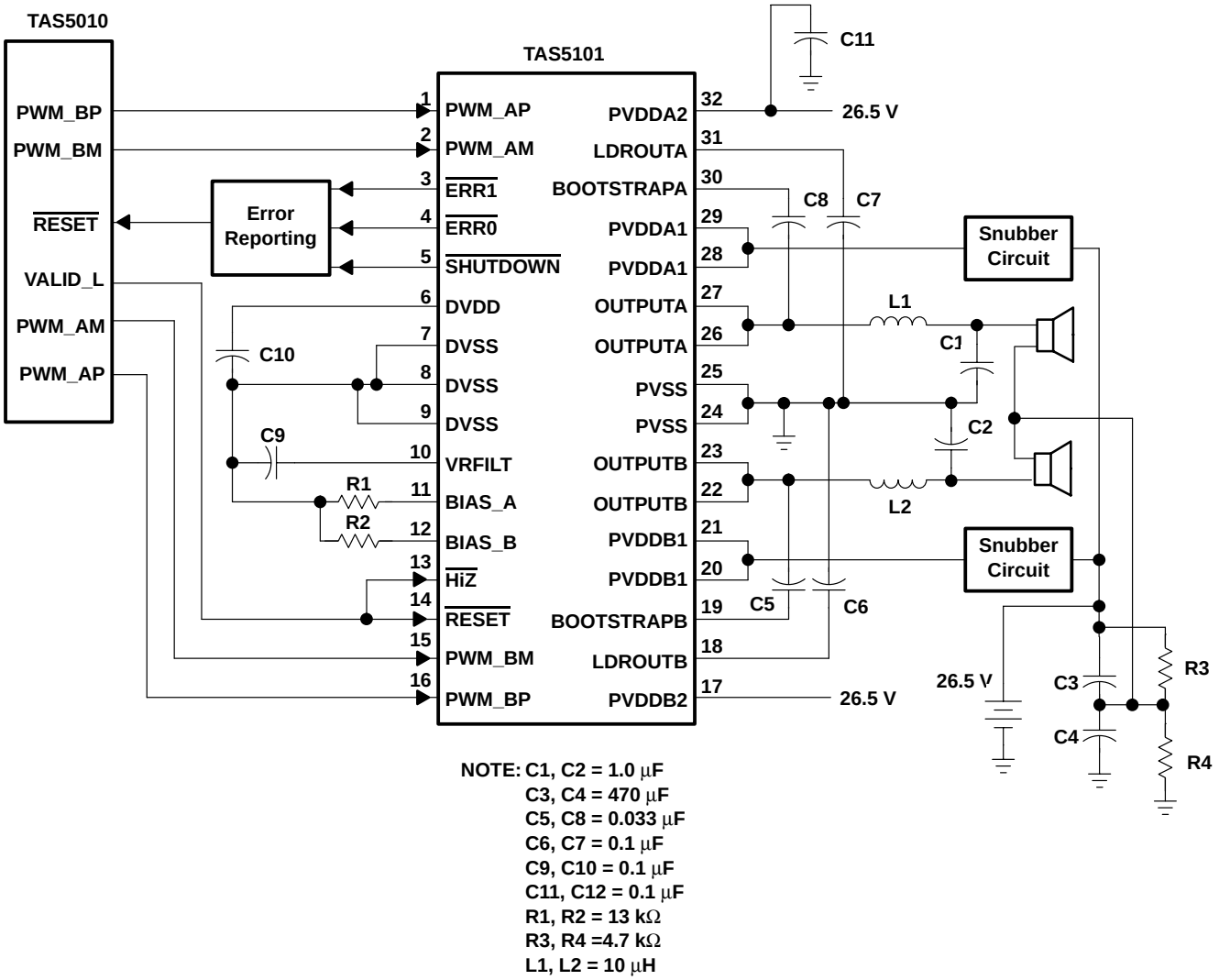


Figure 3. Views of Thermally Enhanced DAP Package

APPLICATION INFORMATION



NOTE: C1, C2 = 1.0 μF
C3, C4 = 470 μF
C5, C8 = 0.033 μF
C6, C7 = 0.1 μF
C9, C10 = 0.1 μF
C11, C12 = 0.1 μF
R1, R2 = 13 kΩ
R3, R4 =4.7 kΩ
L1, L2 = 10 μH

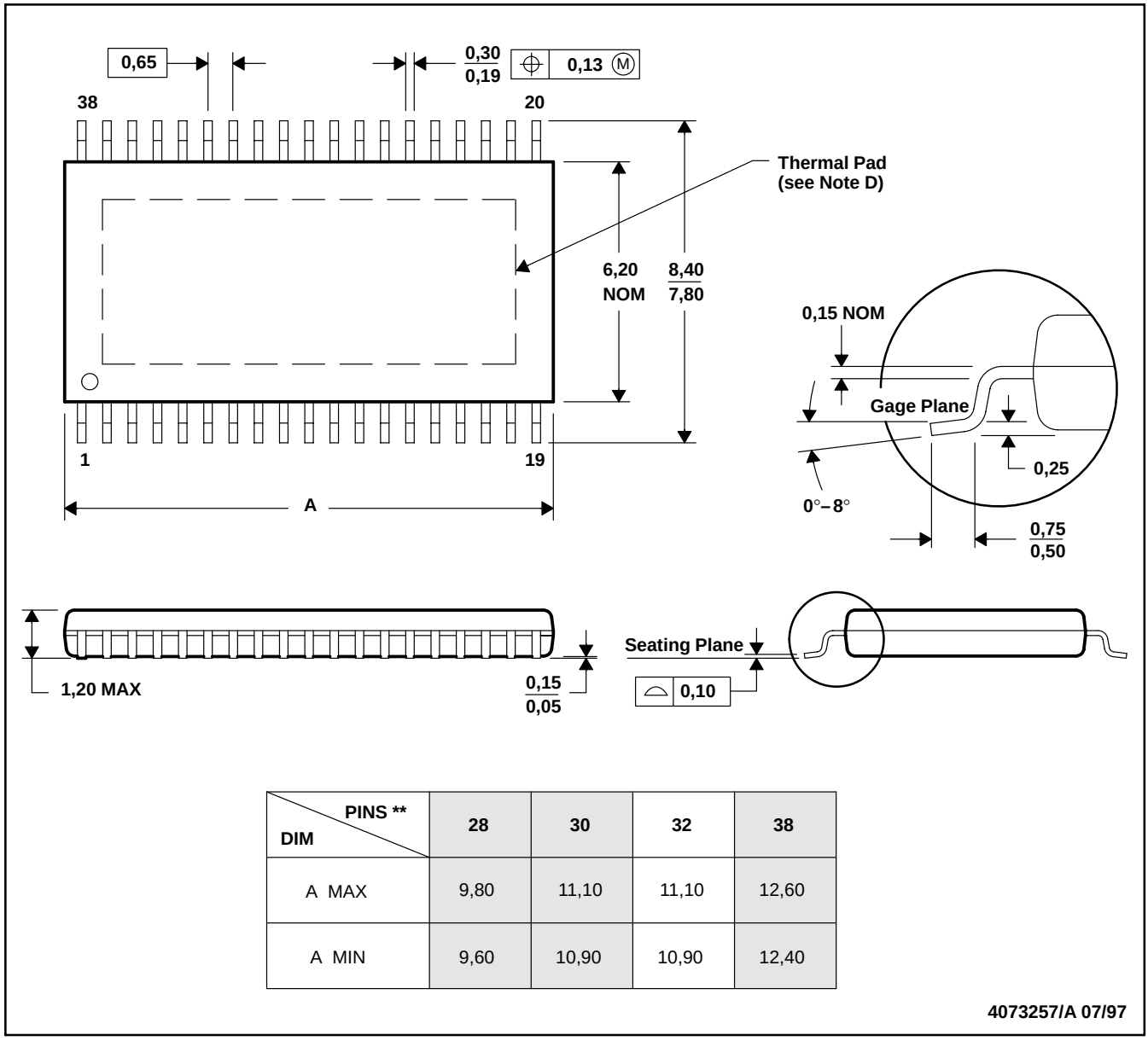
Figure 4. Typical TAS5101 Application (One Channel Shown)

See the evaluation module user's guide, TI literature number SLEA006 for detailed application information.

MECHANICAL DATA

DAP (R-PDSO-G**) PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE

38 PINS SHOWN



DIM \ PINS **	28	30	32	38
A MAX	9,80	11,10	11,10	12,60
A MIN	9,60	10,90	10,90	12,40

4073257/A 07/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads. Thermal pad size is 3,86 mm X 3,91 mm for the 32-pin TAS5101 device.
E. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

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