DESIGN OF CLASS-D AUDIO POWER AMPLIFIERS IN SOI TECHNOLOGY

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Abstract

The design of integrated class-D audio power amplifiers is discussed. The amplifiers are realized in an SOI based BCD-technology that is inherently free from latch-up. The core of a class-D amplifier is the switching output stage. Accurate control of the switch timing is essential for good audio performance. In order to achieve this, detailed knowledge of the transient dynamics is necessary. Robustness is the crucial thread throughout the design. Robustness is complicated by high voltages and the switching of large currents in the output stage. Further the output stage needs to be robust against all sorts of fault conditions such as short circuits and electro-static discharge.

1. Introduction

The operating principles of class-D amplifiers have been known for a long time, but only recently semiconductor manufacturers are able to produce reliable integrated class-D amplifiers of sufficient quality [1]. The audio performance of modern class-D amplifiers equals or even exceeds that of conventional class-AB amplifiers. The distinguishing feature of class-D amplifiers is the high efficiency which allows for smaller heatsinks or higher output power before running into thermal limitations. This is especially advantageous in multi-channel systems such as DVD receivers. The main drawback of class-D amplifiers is that the switching at the output is a source of electro-magnetic interference (EMI). A careful optimization of the application is crucial. Also, class-D amplifiers require an external lowpass filter that contains at least one inductor which adds to the cost.

2. Operating Principle

The core of a class-D amplifier is the switching output stage. A block diagram is shown in figure 1. The switching output stage consists of two large switches S_H and S_L and a *switch control* block. The function of the output stage is a

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simple one: switching the output node V_{out} up and down between the supply rails V_{ssP} and V_{ddP}. This results in a square wave signal with a frequency that generally lies between 200kHz and 800kHz. The audio signal is embedded in the output signal using some form of pulse-width modulation (PWM). Many forms of PWM exist [2], all having their specific advantages and disadvantages. However, a discussion on PWM is beyond the scope of this paper.

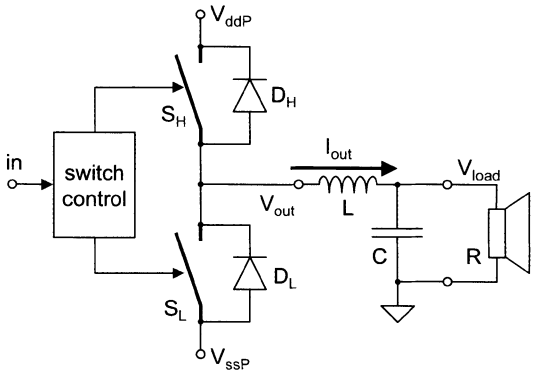

Figure 1. Class-D output stage

Ultimately both the audio performance and EMI are largely determined by the switching output stage. Accurate control of the switch timing is essential to reproduce the PWM signal with sufficient fidelity. Usually, the switch control includes a break-before-make arrangement that prevents the power switches $S_{L,H}$ from conducting simultaneously. This results in a period of time where control of the output voltage is lost which is appropriately called the *dead time*. During the dead time the output current I_{out} flows through one of the fly-back diodes $D_{L,H}$. Dead time is one of the dominant sources of distortion in class-D amplifiers [3].

3. SOI Technology

Design starts with the selection of an appropriate technology. For class-D audio amplifiers a BCD (Bipolar, CMOS, DMOS) processes is an almost inevitable choice. The bipolar transistors are indispensable for analog circuits where noise and offset are important. The CMOS allows for integration of modest size logic circuits for interfacing and control functions. Finally, DMOS transistors are almost perfect power switches featuring high breakdown voltage and low on-resistance plus the ability to conduct current in both directions.
A process that is particularly suitable for switching applications is A-BCD [4] which is an SOI based BCD technology. The dielectric isolation between the

integrated components makes designs in A-BCD inherently free from latch-up phenomena. Consequently, the backgate diodes of the DMOS power transistors in the switching power stage can be exploited as fly-back diodes without the need for external schottky diodes. In conventional bulk technologies external diodes are often necessary to prevent injection of minority carriers into the substrate which can lead to latch-up.

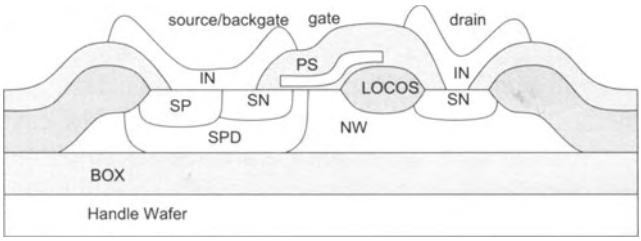

Figure 2. Cross-section of a 60V N-DMOS in A-BCD

The A-BCD process includes DMOS transistors with breakdown voltages ranging from 12V to 120V. Further, a range of resistors, capacitors and (zener-) diodes is available. A cross-section of a 60V DMOS transistor in A-BCD is shown in figure 2.

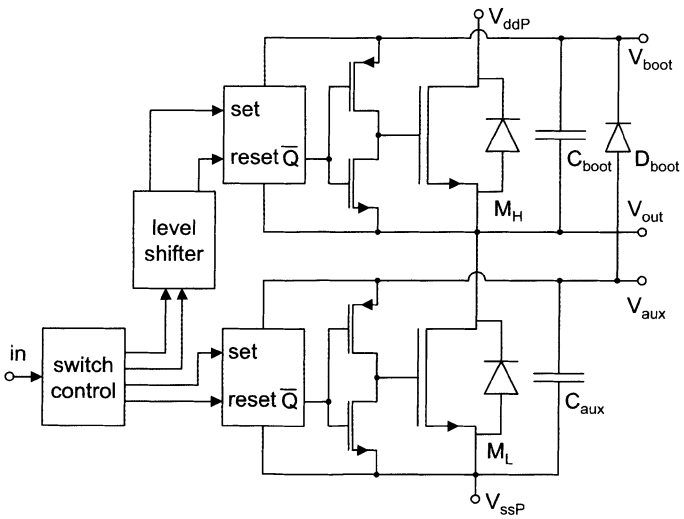

Figure 3. Class-D output stage with nDMOS power transistors

A particularly advantageous feature of A-BCD is the remarkably small reverse recovery charge associated with the backgate diodes of the DMOS transistors.

The reverse recovery charge is almost an order of magnitude smaller than that of comparable DMOS transistors in bulk technology. The small reverse recovery charge makes A-BCD especially suited for switching applications since reverse recovery is one of the major sources of EMI.
In integrated circuits n-channel DMOS transistors are often preferred over p-channel because of their lower R_{on}*$Area$ product. A switching output stage with nDMOS switches is shown in figure 3. A separate low voltage power supply V_{aux} is used for the driver of the lowside power transistor M_L. An external bootstrap capacitor C_{boot} serves as a floating power supply for the driver of the highside power transistor M_H. This configuration enables the gate of the highside power transistor M_H to be driven with a voltage higher than the power supply voltage V_{ddP}. Each time the output V_{out} switches to the lowside, bootstrap capacitor C_{boot} is (re)charged through bootstrap diode D_{boot}. In order to guarantee that the gate drive of the power transistors is not disturbed by steep voltage transients at the output node V_{out}, a latch is included in the drivers. The latches are *set* and *reset* by a *switch control* unit. The highside latch switches up and down with the output node V_{out}. This means that a *levelshifter* is needed to enable the communication between the switch logic and the highside latch. The levelshifter has to be insensitive to the voltage transients at the output node V_{out}.

4. Robustness in High Voltage Circuit Design

Robustness is a general requirement for any (integrated) circuit. Three domains can be distinguished: normal operation, electrostatic discharge (ESD) and fault conditions.

4.1. Normal Operation

A circuit should be inherently robust under normal operating conditions. Although this may seem obvious this is not a trivial matter in high voltage electronics. Usually only a small selection of the available components is capable of handling the entire supply voltage. Especially the gate-oxides of (D)MOS transistors are vulnerable and precautions have to be taken in order to protect them from damage. For this reason the driver of the lowside power transistor M_L uses a separate low voltage supply V_{aux}. The voltage swing at the output node can be 60V or more while the gate-source voltage of M_L is limited to 12V. Since the bootstrap capacitor C_{boot} is charged from V_{aux} the gate-source voltage of the highside power transistor M_H is automatically also limited to 12V.
Cascodes are widely applied throughout high voltage circuits. The 5V NMOS transistors tend to have better noise and matching characteristics than the high voltage DMOS transistors. Therefore, current mirrors are often realized in NMOS with DMOS cascodes as shown in figure 4(a). Another typical circuit structure is the cascoded bipolar differential pair shown in figure 4(b). The

breakdown voltage of the NPN transistors in A-BCD is limited to about 18V so a DMOS cascode is sometimes required to limit the collector voltage.
Special attention is needed to avoid floating nodes. Consider the circuit shown in figure 4(c). Suppose the gate of DMOS transistor M_1 is connected to 12V and the drain to 60V. As long as the switch is closed, resistor R_1 pulls down the source of M_1 to at least one threshold below the gate voltage. But when the switch is opened the source of M_1 becomes floating. The leakage current through the backgate diode of M_1 pulls the source up towards the drain resulting in an increasing voltage across the gate-oxide that eventually leads to destruction of the device. This is prevented by the clamp diode D_1 that limits the reverse gate-source voltage. Alternatively, a very small standby current can be drawn from the source to prevent the source voltage from floating.

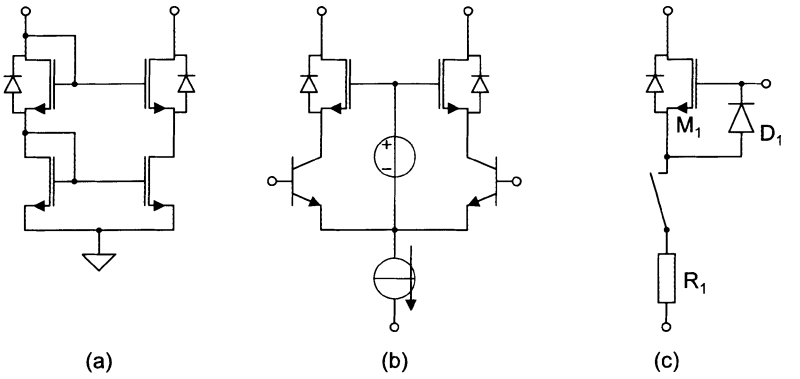

Figure 4. High voltage circuit techniques (a) currentmirror cascode (b) differential pair cascode (c) gate-source clamp

A robustness issue directly related to class-D is caused by the switching of large currents at the output. Unfortunately, DMOS transistors have a rather effective bipolar parasite that causes the device to snap back to a highly conductive bipolar mode when the breakdown current exceeds a critical level. A typical breakdown characteristic of a DMOS transistor is shown as the solid line in figure 5(a). The hold voltage V_{hold} usually lies well below the supply voltage. In this mode the current capability is very limited and the device can easily be destroyed.
Consider the situation shown in figure 5(b) where the highside power transistor M_H is conducting and a substantial current I_{out} flows from the positive supply V_{ddP} towards the output V_{out}. This current also flows through the series inductor L_h that accounts for the parasitic inductance of the bondwires and leadfingers. When the highside power transistor M_H is switched off the current through inductor L_h decreases rapidly which causes the voltage at the drain of M_H to rise.

At the same time the continuing output current I_{out} pulls down the voltage at the source of M_H. The resulting drain-source voltage can easily exceed the breakdown voltage BV_{ds} of M_H. If M_H snaps back this would destroy the output stage. A similar situation can happen with the lowside power transistor M_L.

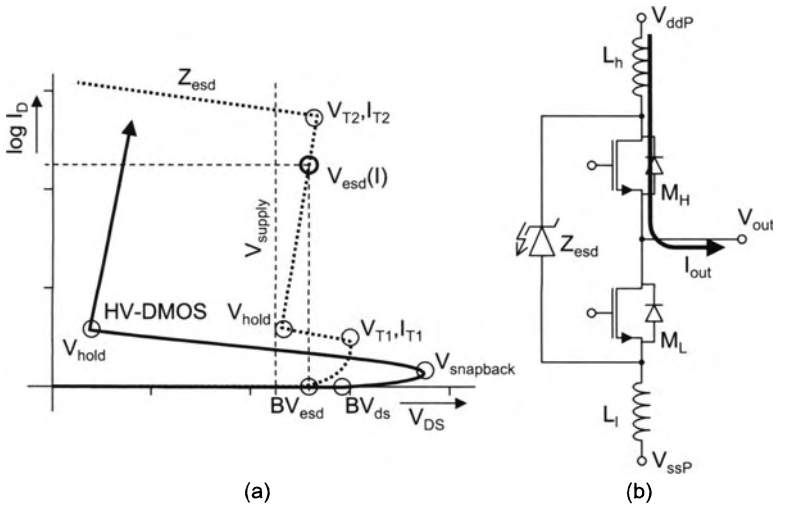

Figure 5. High current switching (a) breakdown characteristics (b) parasitic inductance.

The voltage overshoot caused by the series inductors can be limited effectively using an ESD diode Z_{esd} as shown in figure 5(b) When the supply voltage overshoots, the protection triggers and clamps the drain-source voltages of the power transistors to a safe value. The dissipation in the diode Z_{esd} during high current switching is a few orders of magnitude smaller than that of an ESD discharge since the parasitic inductors are very small and so is the amount of stored energy. Of course, the ESD diode Z_{esd} also protects the output stage against actual ESD zaps.

4.2. Electrostatic Discharge

Robustness against ESD is in general achieved by adding dedicated protection devices to a circuit. The purpose of these ESD protections is to divert the discharge current and prevent it from flowing through the circuit itself. Under normal operating conditions the ESD protections should be inactive. The breakdown behaviour of Z_{esd} in figure 5(b) is shown as the dashed line in figure 5(a). The reverse breakdown behavior of the device is characterized by the following parameters:

BV_{esd}
Breakdown voltage. Below this voltage the protection does not conduct.

V_{T1},I_{T1}
Trigger voltage/current for bipolar turn-on. Above this current the protection snaps back to a state of high conductivity.

V_{hold}
Hold voltage. Below this voltage, the protection shuts down again.

$V_{ESD}(I)$
Clamp voltage at a given discharge current I. This voltage depends on the width of the device and determines the ESD level that can be reached.

V_{T2},I_{T2}
Fail voltage/current. Above this current the protection is destroyed.

In contrast to the DMOS transistor breakdown, the ESD protection can conduct substantial current after snapping back without being destroyed. Also the difference between the trigger voltage V_{T1} and hold voltage V_{hold} is much smaller. Clearly, the ESD protection devices should be applied so that they do not hamper normal operation of the circuit that they are supposed to protect. Thus during normal operation, the voltage across the device should remain below the hold voltage V_{hold}. This is especially important for protections that are connected between supply rails. In the A-BCD process, three protection devices are available with hold voltages of about 5V, 8V and 12V. For higher supply voltages these device can be stacked. For example, a 32V protection can be realized by making a stack of two 12V protections and one 8V protection. The parameters of the stack can be estimated by simply adding the parameters of the components. In this manner a whole range of ESD protection circuits can be tailored for many different situations.
The ESD protections should be placed such that the discharge current of an ESD pulse applied between two arbitrary pins of an IC always flows through one or more protection devices and not through the circuit. An exception is made for very large components in the circuit such as the backgate diodes of the power transistors or the bootstrap diode. These devices are capable of handling large currents without being damaged. It is not practical to insert an ESD protection between each pair of pins of an IC. A 24-pin IC would require 552 protections. The goal is to use a minimal number of protections while maintaining a path through one or more ESD protections between any pair of pins. A complicating factor in power amplifiers is that usually separate power supplies are used for small signal analog, digital and power circuits. Further each channel often also has its own power supply. This can lead to intricate discharge current paths. Consider for example the circuit shown in figure 6. Here the class-D switching output stage shown earlier in figure 2 has been extended with ESD protections.
Two antiseries 12V protections Z_{ssP} connect the relatively quiet digital ground V_{ssD} to the noisy power ground V_{ssP}. The highside and lowside drivers are each

protected by a single 12V protection Z_{boot} and Z_{aux}. The switch control block has a separate positive digital supply V_{ddD} and is protected by Z_{ddD}. The protection Z_{esd} across the output stage is a stack of five 12V protections yielding a 60V protection. Now suppose an ESD pulse is applied between the bootstrap pin V_{boot} and the positive digital supply V_{ddD}. The discharge path then goes through Z_{boot}, the backgate diode of M_H, Z_{esd}, Z_{ssP} and Z_{ddD} yielding a total of seven reverse and three forward voltage drops which amount to at least 85V.

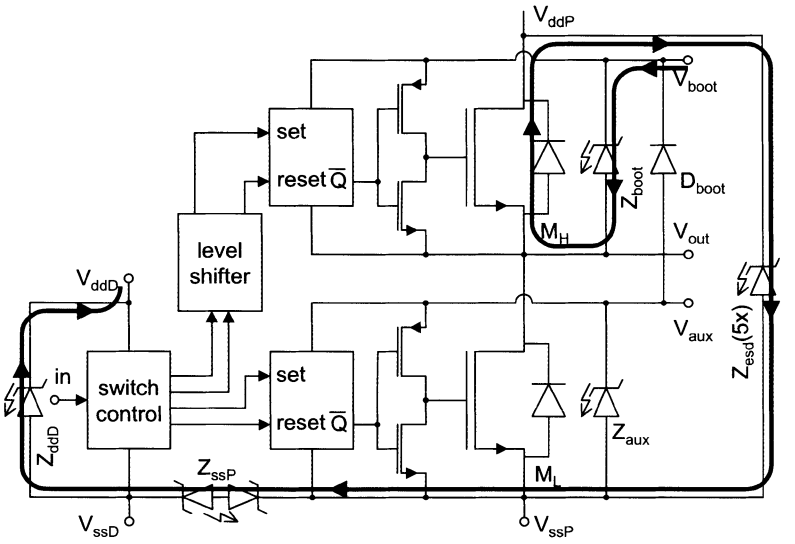

Figure 6. ESD current path example

As is illustrated by this example, the voltages that appear across the components in the circuit during a electro-static discharge can be quite different from the voltages during normal operation. In this case a careful inspection of the levelshifter circuit is required since this circuit is connected to both V_{boot} and V_{ddD}. Sometimes, special measures have to be taken to make a circuit more robust against ESD. This can be achieved by strategically adding diodes and resistors to the circuit. Consider the configuration shown in figure 7(a). Here transistor M_1 can be a current source connected to the negative supply rail V_{ssA} and M_2 the input diode of a current mirror connected to the positive supply rail V_{ddA}. Both transistors have their source and backgate connected. A stack of three ESD protections Z_1 is connected between the supply rails. The diode D_1 serves to block the reverse current path through the backgate diodes of M_1 and M_2. A discharge current flowing from V_{ssA} to V_{ddA} would otherwise flow through the two backgate diodes in the circuit instead of the three diodes in the ESD stack. Sometimes it is not practical to add an additional ESD protection to protect a

single component in a circuit. In that case it is also possible to add series resistance in the circuit in order to limit the current when the component breaks down.

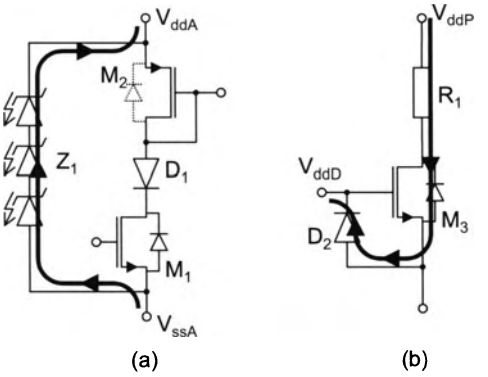

Figure 7. ESD measures (a) blocking reverse current paths (b) limit breakdown currents

For example, in the circuit shown in figure 7(b). the voltage that occurs between gate and drain of transistor M_3 may exceed the breakdown voltage of the device. As was explained earlier the diode D_2 protects the gate-oxide from being damaged. Now if M_3 goes into breakdown the resistor R_1 limits the current through the device, thus avoiding snapback. Clearly, for the output power transistors, adding series resistance is not a viable option.

4.3. Fault Conditions

Robustness against a number of fault conditions can be required. In most consumer applications the output terminals of audio power amplifiers are directly connected to the loadspeaker connectors. Therefore audio power amplifiers should be robust against accidental short circuits that can be made between the output(s) and supply lines. Short circuits come in many forms. During robustness testing shorts are applied with short and long wires, variable resistors (strangle) and inductors between the outputs and supply lines with the output signal varying from mute to clipping. In one particularly nasty test a contact probe is dragged along a coarse file to emulate an intermittent short. A full short circuit protection usually consists of at least an overtemperature protection (OTP) and an overcurrent protection (OCP) [5,6]. Overcurrent detection can be done efficiently using scaled replica transistors biased at a small reference current as shown in figure 8. For the lowside the drain voltage of the output power transistor M_L is compared to the drain voltage of replica M_{reflow} as shown in figure 8(a). The comparison is only valid if M_L is switched fully on

in which case $V_{gatelow}$ equals V_{aux}. When M_L is switched off the comparator is decoupled from the output node by switch S_1.

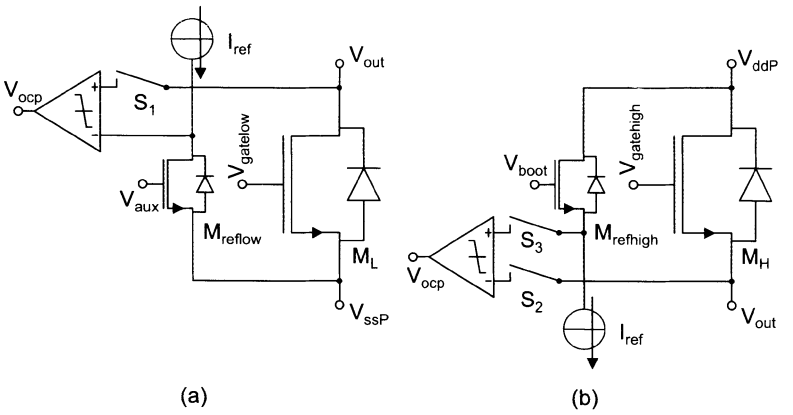

Figure 8. Overcurrent detection (a) lowside (b)highside

At the highside the source voltages of the highside power transistor M_H and replica $M_{refhigh}$ are compared as shown in figure 8(b). If M_H is switched on then $V_{gatehigh}$ equals V_{boot}. Because V_{boot} is coupled to V_{out}, both comparator inputs are decoupled by switches $S_{2,3}$ when M_H is switched off.

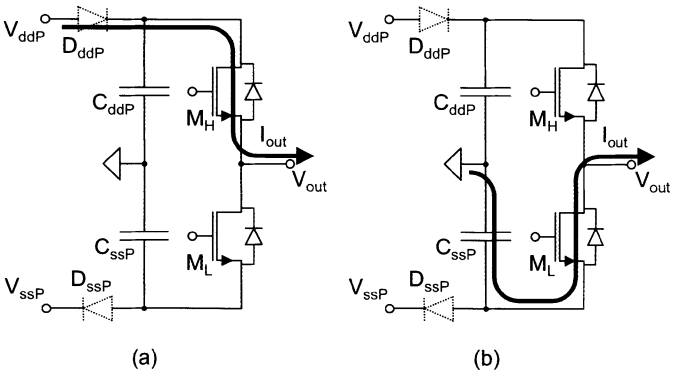

Figure 9. Supply pumping (a) sourcing current from positive supply (b) charging decoupling capacitor negative supply

A different fault condition can be caused by the class-D amplifier itself. Most power supplies are only capable of sourcing current. In figure 9 this is illustrated by means of series diodes D_{ssP} and D_{ddP} in the supply rails. Consider the case where a current I_{out} is flowing out of the amplifier towards the load. When the

highside power transistor M_H is switched on the current can be sourced by the positive power supply V_{ddP} as shown in figure 9(a). However, when the lowside power transistor M_L is switched on, the current can not be sunk by the negative power supply V_{ssP} and has to flow throught the decoupling capacitor C_{ssP} as shown in figure 9(b). This causes the voltage across C_{ssP} to increase, which unbalances the supply voltage. This mechanism is called *supply pumping* and can lead to destruction of the amplifier if the output current I_{out} does not change direction. An *overvoltage protection* prevents the supply voltage to be pumped up to unsafe values by shutting down the amplifier. Also an *unbalance protection* can be desired which limits the amount of unbalance between the positive and negative supply voltages. Note that supply pumping does not occur in bridge-tied-load (BTL) configuration.

5. Design of Class-D Output Stages

As mentioned earlier, one of the dominant sources of distortion in class-D amplifiers is dead time. Therefore, minimal dead time is an important issue in class-D output stage design. To this end, a thorough understanding of the switching dynamics is essential.

5.1. Switching Dynamics

The switching dynamics of a class-D output stage can be analyzed with the simplified schematic shown in figure 10. The input signals in_{high} and in_{low} refer to the output voltage V_{out} and negative supply V_{ssP} respectively. The switching dynamics at the output V_{out} depend on the size of the power transistors M_L and M_H, driver transistors M_{ph}, M_{nh}, M_{pl} and M_{nl} and on the output current I_{out}. At first, the output current I_{out} is assumed to be zero. Now suppose that the lowside power transistor M_L is conducting and so the output V_{out} is low. When switching the output V_{out} from lowside to highside the following sequence of events occurs. First, signal in_{low} goes high and M_L is switched off by discharging the gate through lowside pull-down transistor M_{nl}. The output V_{out} remains low but shows a small step caused by capacitive feedthrough. This situation remains unchanged during the dead time. After the dead time signal in_{high} goes low and highside pull-up transistor M_{ph} starts to charge the gate of the highside power transistor M_H. As soon as the highside gate-source voltage V_{gsh} exceeds the threshold voltage V_T, highside power transistor M_H starts conducting and the output V_{out} starts to rise rapidly. During the transient of the output voltage V_{out} the highside gate-source voltage V_{gsh} stalls because all available current I_{ph} from highside pull-up transistor M_{ph} is now used to discharge the highside gate-drain capacitance C_{gdh}. The highside gate-drain capacitance C_{gdh} appears much larger due to the well-known Miller-effect. The slewrate of the output voltage is thus determined by:

$$\frac{dV_{out}}{dt} = \frac{I_{ph}}{C_{gdh}} \tag{1}$$

Note that at the same time, this same slewrate appears across the lowside gate-drain capacitance C_{gdl}. Since both power transistors are identical, the current through C_{gdl} equals the current through C_{gdh}. This current I_{nl} flows through lowside pull-down transistor M_{nl} and causes the lowside gate-source voltage V_{gsl} to rise. The size of M_{nl} should be made such that this voltage remains below the threshold voltage V_T to avoid cross conduction.

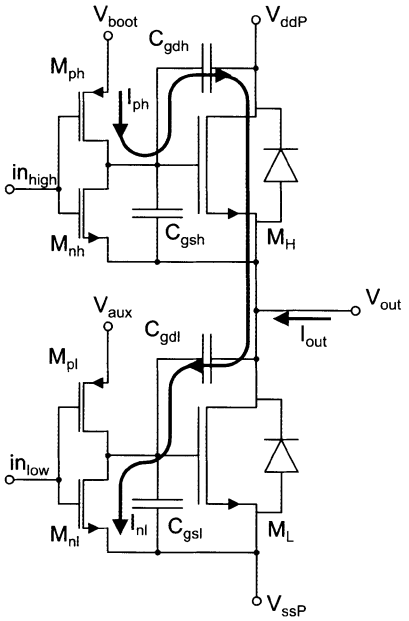

Figure 10. Simplified Class-D Powerstage

In other words, the ratio of the on-resistance R_{ph} and R_{nl} of highside pull-up transistor M_{ph} and lowside pull-down transistor M_{nl} should be such that:

$$\frac{R_{nl}}{R_{nl} + R_{ph}} < \frac{V_T}{V_{boot} - V_{out}} \tag{2}$$

After the transition of the output V_{out} has finished, the highside gate-source voltage V_{gsh} continues to rise until the gate of highside power transistor M_H is fully charged while the gate of lowside power transistor M_L is (again) fully

discharged. The gate-source voltages V_{gsl} and V_{gsh} and the output voltage V_{out} for this transition are shown in figure 11.

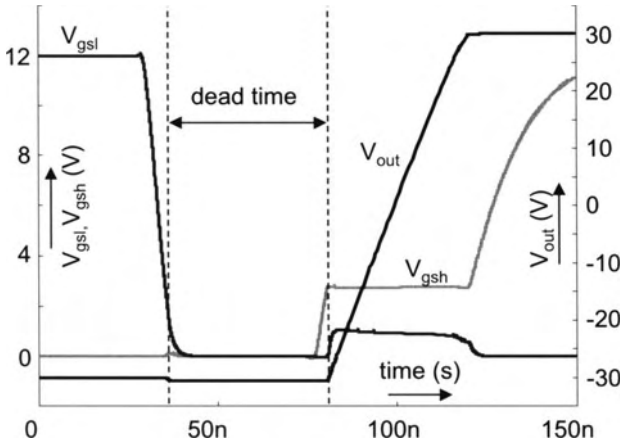

Figure 11. Voltage transients with I_{out}=0

If the output current I_{out} is not equal to zero the situation changes. Consider the case where a small current I_{out} of about 100mA is flowing *into* the amplifier. The corresponding voltage transients are shown in figure 12.

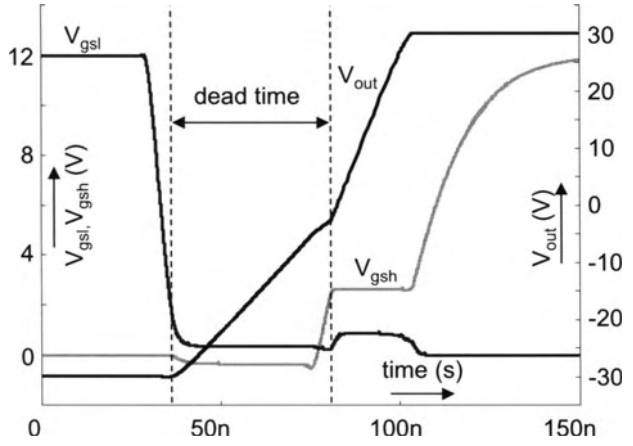

Figure 12. Voltage transients with I_{out}=100mA

As can be seen, the gate-source voltages V_{gsl} and V_{gsh} are similar to the case where I_{out} is zero. The output voltage V_{out} however looks quite different. This time, as soon as the lowside power transistor M_L is switched off, the output current starts charging the output V_{out}. The slewrate is determined by the output

current I_{out} and the capacitance at the output node V_{out}. After the dead time the highside power transistor M_H is switched on and slewrate is now again determined by equation (1). This results in a characteristic dual slope output voltage from which the dead time can easily be determined.

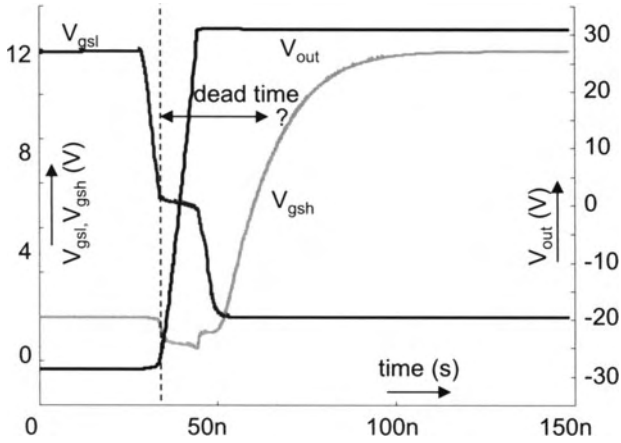

Figure 13. Voltage transients with I_{out}=10A

As the output current I_{out} increases, so does the slewrate of the output voltage V_{out} during the dead time until is exceeds the slewrate determined by equation (1). Consider again the previous example but with a large current I_{out} of about 10A flowing *into* the amplifier. As soon as the lowside power transistor M_L switches off the output current I_{out} starts to charge the output node V_{out}, pulling it towards the highside. In this case the slew rate is limited by the following mechanism. Due to the increased slewrate at the output V_{out} the current that is forced through the gate-drain capacitance C_{gdl} is also larger than in the previous case. This current I_{nl} flows through lowside pull-down transistor M_{nl}. which results in a voltage drop that now prevents the lowside transistor from switching off. The lowside gate-source voltage V_{gsl} stalls at a value above the threshold voltage V_T. In this case the slewrate of the output voltage is determined by:

$$\frac{dV_{out}}{dt} = \frac{I_{nl}}{C_{gdl}} \tag{3}$$

At the same time the highside power transistor M_H is prevented from switching on because the highside pull-up transistor M_{ph} is too small to deliver the necessary current. Only after the transition of the output V_{out} has finished the highside power transistor M_H can be switched on. The corresponding voltage transients are shown in figure 13.

If the direction of the output current I_{out} is reversed the switching dynamics and voltage transients as shown in figure 11 remain largely unchanged. The only difference is that during the dead time, the output current I_{out} flows through the backgate diode of lowside power transistor M_L. Now as soon as the highside power transistor M_H is switched on, the backgate diode of lowside power transistor M_L is reverse biased instantly. This causes a short but high reverse recovery current that flows between the supply lines. Reverse recovery current is one of the main sources of EMI in class-D. When switching the output V_{out} from highside to lowside, the same sequence of events occurs with the role of lowside and highside interchanged. Now the slewrate is determined by:

$$\frac{dV_{out}}{dt} = -\frac{I_{pl}}{C_{gdl}} \tag{4}$$

while the ratio between the on-resistance R_{pl} and R_{nh} of lowside pull-up transistor M_{pl} and highside pull-down transistor M_{nh} should be such that:

$$\frac{R_{nh}}{R_{nh}+R_{pl}} < \frac{V_T}{V_{aux}-V_{ssP}} \tag{5}$$

In practice the drivers of the highside and lowside are made identical. This can be done because the highside and lowside driver have about the same supply voltage since the bootstrap capacitor C_{boot} is charged to V_{aux} when the output V_{out} is low.

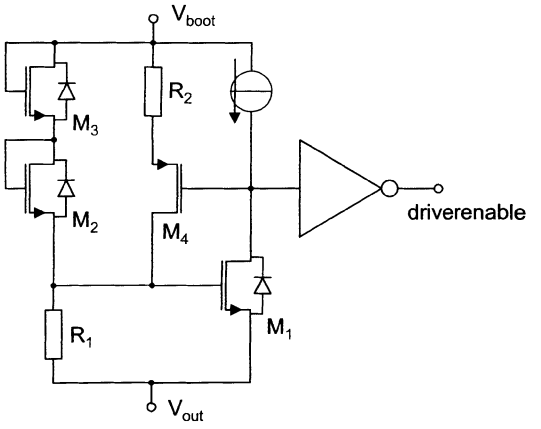

Figure 14. Highside driver undervoltage protection

When the output V_{out} is high the highside driver is supplied by the bootstrap capacitor C_{boot} and is essentially floating which poses a potential problem for the

class-D output stage. If the voltage V_{boot} decreases too much the pull-down transistor M_{nh} is not low-ohmic enough to keep the highside power transistor M_H switched off during a falling edge of the output V_{out}. In this case both power transistors would be conducting simultaneously which could destroy the class-D output stage. To avoid this, the highside driver is equiped with an *undervoltage protection* as shown in figure 14. Resistor R_1 pulls down the gate of M_1 until the voltage V_{boot}-V_{out} becomes higher than three threshold voltages which is enough for proper operation. A hysteresis window around the undervoltage level is realized by transistor M_4 and resistor R_2.

5.2. Zero Dead Time

In figures 11, 12 and 13 can be seen that the name dead time has indeed been chosen appropriately. During the dead time nothing happens. In case the output current is small or zero the dead time is merely a waiting state. In case the output current is large all events take place immediately after the lowside power transistor M_L is switched off, regardless of the dead time. Consequently, the dead time can be made shorter without influencing the switching dynamics as described before. Consider what happens in the previous examples if the dead time would be reduced to zero [7]. In the starting situation lowside power transistor M_L is switched on and highside power transistor M_H is switched off. Now signal in_{low} goes high and simultaneously signal in_{high} goes low.

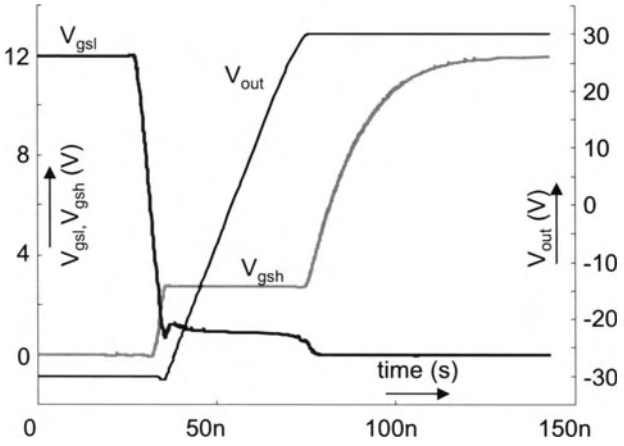

Figure 15. Zero dead time voltage transients

Consequently, the gate of lowside power transistor M_L is discharged through lowside pull-down transistor M_{nl} while at the same time the gate of highside power transistor M_H is charged through highside pull-up transistor M_{ph}. Because of the ratio of the driver transistors the discharge of the gate of lowside power

transistor M_L goes faster than the charge of the gate of highside power transistor M_H, the gate-source voltages of M_L and M_H reach the threshold level V_T at about the same time. At this time the output voltage V_{out} starts to increase according to equation (1) and the behaviour is further identical to that described previously The gate-source voltages V_{gsl} and V_{gsh} and the output voltage V_{out} for this zero dead time case are shown in figure 15. As can be seen in figure 15, the gate-source voltage transients are more or less identical to those in figure 11 except for the absence of dead time. Apparently, dead time is not necessary for correct operation. When the driver transistors have the correct ratio the transitions at the output are self-regulating.

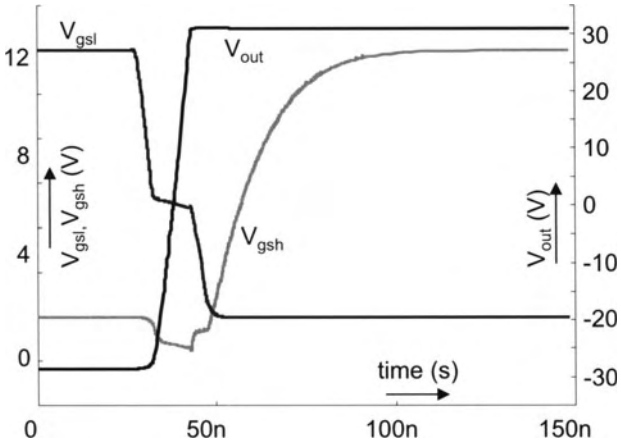

Figure 16. Zero dead time voltage transients with Iout=10A

This is also true in case the output current I_{out} is not zero. For small output currents the voltage transients remain similar to those shown in figure 15. The voltage transients for a large output current I_{out} of about 10A are shown in figure 16. As can be seen the voltage transients are virtually identical to those in figure 13. Consequently, it can be concluded that a class-D output stage with zero dead time is possible provided that the driver transistors are properly dimensioned and the input signals of the drivers are each others inverse. Obviously this latter is the most difficult part. What is needed is a means to set and reset the latches in the highside and lowside drivers simultaneously, i.e. the *set* and *reset* signals should have equal delays. For this purpose a fast levelshifter is required.

5.3. Levelshifters

A fast and robust levelshifter is necessary to transfer the *set* and *reset* signals to the latch in the highside driver. The latch is implemented by two inverters connected in a loop as shown in figure 17(a). The latch can be set and reset by

PMOS pull-up transistors $M_{s,r}$. Note that for proper operation, the signals s and r are not allowed to overlap by being pulled down simultaneously. The signal delay in the levelshifter should not depend on the voltage difference that needs to be shifted since the highside driver can be at both highside and lowside voltage level. A simple but current-hungry implementation is shown in figure 17(b). The signals s_a and r_a are meant to be the levelshifted inverse of the *set* and *reset* signals and are used as inputs for the driver latch. The pull-down transistors $M_{1,2}$ have to be dimensioned such that their drain currents cause the appropriate voltage drop across the pull-up resistors $R_{1,2}$. For low current consumption the resistors need to be high-ohmic which conflicts with the speed requirement.

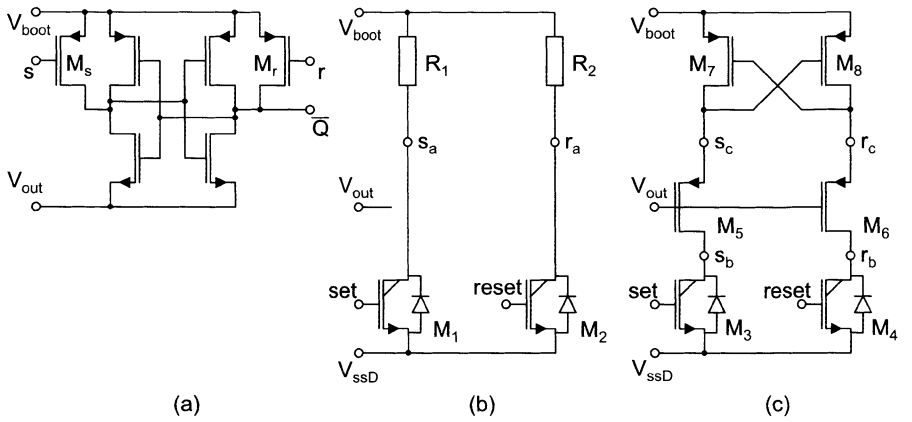

Figure 17. Levelshifting (a) latch (b) simple levelshifter (c) current efficient levelshifter

A more current efficient solution is shown in figure 17(c). The latch formed by transistors $M_{7,8}$ can be toggled by pull-down transistors $M_{3,4}$. Transistors $M_{5,6}$ serve to limit the voltage on the nodes s_b and r_b. Suppose the *reset* signal is high and the *set* signal is low. In this case node r_c is pulled down through M_6 to a level that is one threshold voltage higher than V_{out} while node r_b is pulled down towards V_{ssD}. On the other side node s_c is pulled up towards V_{boot} by M_7. and s_b is pulled up to s_c through M_5. In this situation no current flows. As *reset* goes low the voltages remain the same but now nodes r_b and r_c have become floating.
Now as *set* goes high nodes s_b and s_c are pulled down instantly. However, since M_7 is still switched on, node s_c is not pulled down completely but stalls at a level determined by the dimensions of M_5 and M_7. In this situation a substantial current flows through the branch M_3, M_5, M_7. On the other side M_8 is switched on partially and starts pulling up node r_c and r_b. If the dimensions of $M_{6,8}$ and $M_{5,7}$ are the same, node r_c stalls at the same level as s_c. This situation continues

until node r_b is pulled up to the level of r_c. Then r_b and r_c are pulled up to V_{boot}, M_7 shuts down and s_c is pulled down to one threshold above V_{out}. These voltage transients are shown in figure 18.

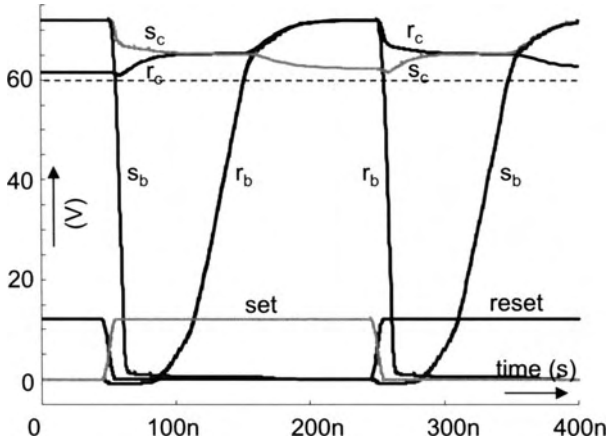

Figure 18. Voltage transients in level shifter

The signals s_c and r_c are meant to be the inverse of the *set* and *reset* signals. However, as can be seen in figure 18 the signals s_c and r_c are distorted and overlap for a significant time which translates to a delay at the latch output Q. This delay depends on the voltage level that needs to be shifted and occurs because M_7 and M_3 are conducting at the same time, counteracting each other.

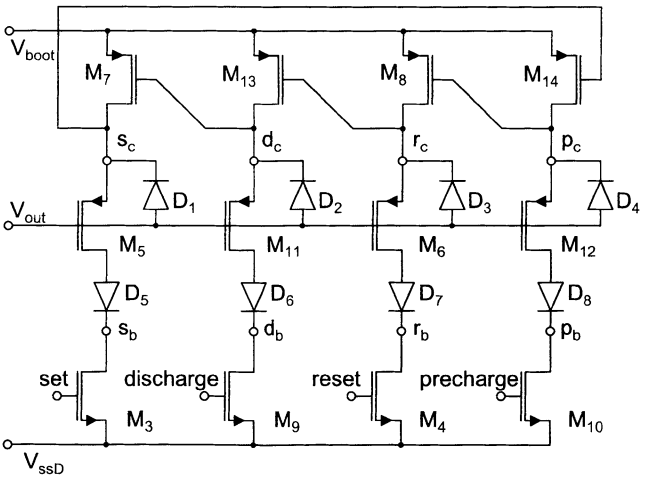

Figure 19. Fourstroke levelshifter

Note that after the *set* signal goes high the node s_c is pulled down *instantly* while after the *reset* signal goes high the node r_c is pulled down *instantly*. This property is exploited by the circuit shown in figure 19. Two signals, *precharge* and *discharge*, are inserted between the *set* and *reset* signals. The four signals are subsequently high one at a time in a fixed cyclic sequence. Suppose the *reset* signal is high and the others are low. In that case nodes r_b and r_c are at V_{ssD} and one threshold above V_{out} respectively and all other nodes are at V_{boot}. In this case only nodes d_b and d_c are pulled up actively by M_{13} while the others are floating. Now as *reset* goes low, *precharge* goes high, nodes p_b and p_c are pulled down unhindered since M_{14} is off. Consequently, M_8 is switched on fully and nodes r_b and r_c are pulled up fast. Next *precharge* goes low and *set* goes high and the events are repeated with the corresponding components and nodes. In this manner it is avoided that pull-up and pull-down transistors counteract each other. This arrangement is called the fourstroke levelshifter [8]. The resulting transfer delay is extremely small and almost independent of the voltage level that needs to be shifted.

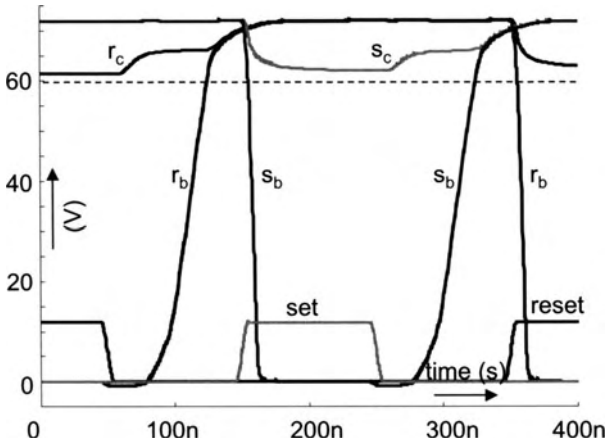

Figure 20. Voltage transients in fourstroke

The corresponding voltage transients are shown in figure 20. As can be seen as soon as the *set* signal goes high, the node s_c is pulled down instantly without stalling. The same holds for *reset* and node r_c. Not shown in figure 20 are the *precharge* and *discharge* signals which are high in between of the *set* and *reset* signals. The *precharge* signal pulls up node r_b before the *set* signal goes high. Consequently, the stalling problem explained earlier is avoided. The *discharge* signal does the same with node s_b. In this manner the delay between the rising edge of the *set* (*reset*) signal and the falling edge of the $s_c(r_c)$ signal has become very small and almost independent of the voltage level that is shifted. For robustness, the diodes $D_{1\text{-}8}$ have been added to the circuit shown in figure 19.

Diodes $D_{1\text{-}4}$ serve to protect the gateoxide of transistors $M_{5,6,11,12}$ when their sources are floating. Diodes $D_{5\text{-}8}$ block the reverse current through the backgate diodes during an ESD discharge from V_{ssD} to V_{boot}.

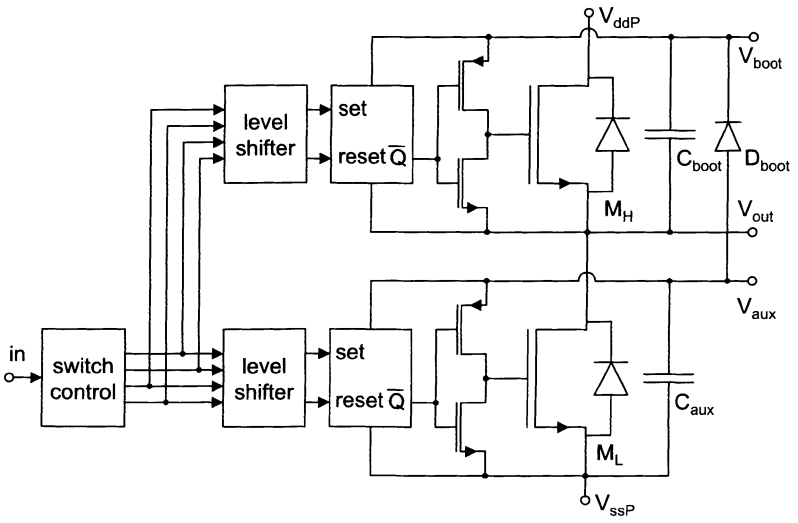

Figure 21. Delay matching highside and lowside

The fourstroke levelshifter is used for both highside and lowside drivers in order to match the signal delays of the *set* and *reset* signals as shown in figure 21.

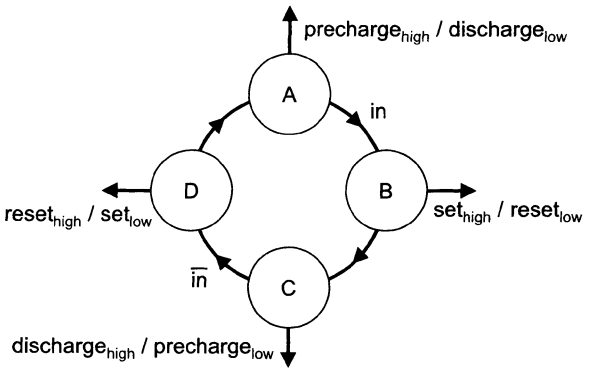

Figure 22. State Machine

The four signals needed for the fourstroke levelshift can readily be generated by a simple state machine as shown in figure 22. The state machine runs through a cyclic pattern of states thus generating the appropriate driving signals for the

fourstroke levelshifters. The highside and lowside are connected such that the *set* signal for the highside is used as *reset* for the lowside and vice versa.

Measurements

The zero dead time arrangement presented previously has been implemented in the output stage of an integrated class-D amplifier. In figure 23 the rising edge of the output signal V_{out} is shown. For comparison, also the rising edge of a class-D output stage with dead time is shown. As can be seen in figure 23, this dead time is approximately 75ns which can readily be determined by the characteristic dual slope. The zero dead time version does not show a dual slope which means there is no measurable dead time anymore. For this measurement a supply voltage of 60V was used.

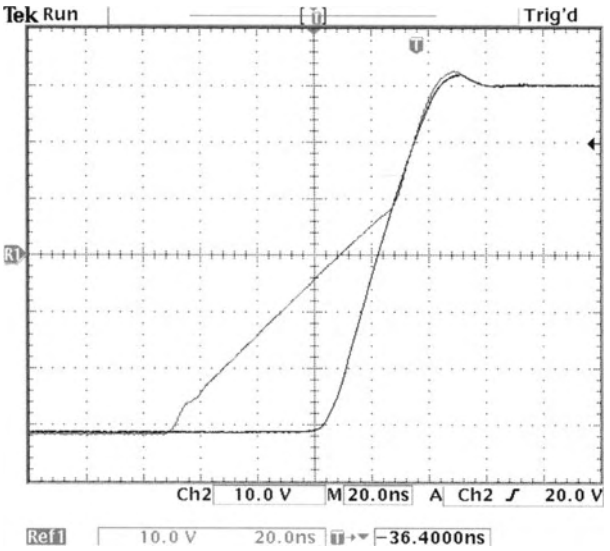

Figure 23. Rising edge with and without dead time

Figure 24 shows the THD+N of a full-bridge zero dead time class-D output stage in an open loop configuration. A supply voltage of 30V was used with a 6Ω BTL load. The measurement was done with a 1kHz audio signal but distortion does not appear to depend on signal frequency. The PWM input signal is generated by a digital PWM modulator and has a carrier frequency of 352.8Khz ($8f_s$). For comparison the THD+N of an almost identical class-D amplifier with 75ns dead time is also shown. As can be seen the difference in performance is large. The zero dead time distortion stays comfortably below 0.1% up to the point of clipping making this class-D output stage suitable for open loop class-D audio amplifiers.

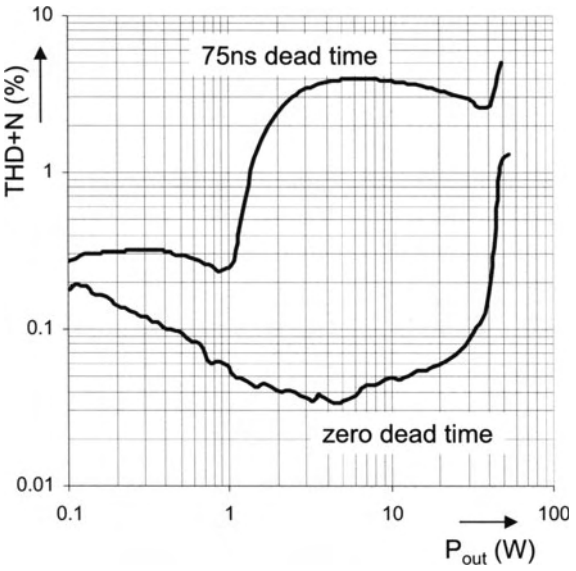

Figure 24. THD+N zero dead time vs. 75ns dead time

10. Conclusions

Design of class-D output stages in an SOI-based BCD process has been presented. Special attention was given to the various robustness aspects involved in the design. A study of the switching dynamics in the class-D output stage under various load conditions showed that dead time can be eliminated provided that the timing difference of the signals that drive the power transistors can be made small enough. A fast levelshifter topology was presented with a delay that is independent on the voltage difference that needs to be traversed. Measurements show a significant improvement in performance.

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