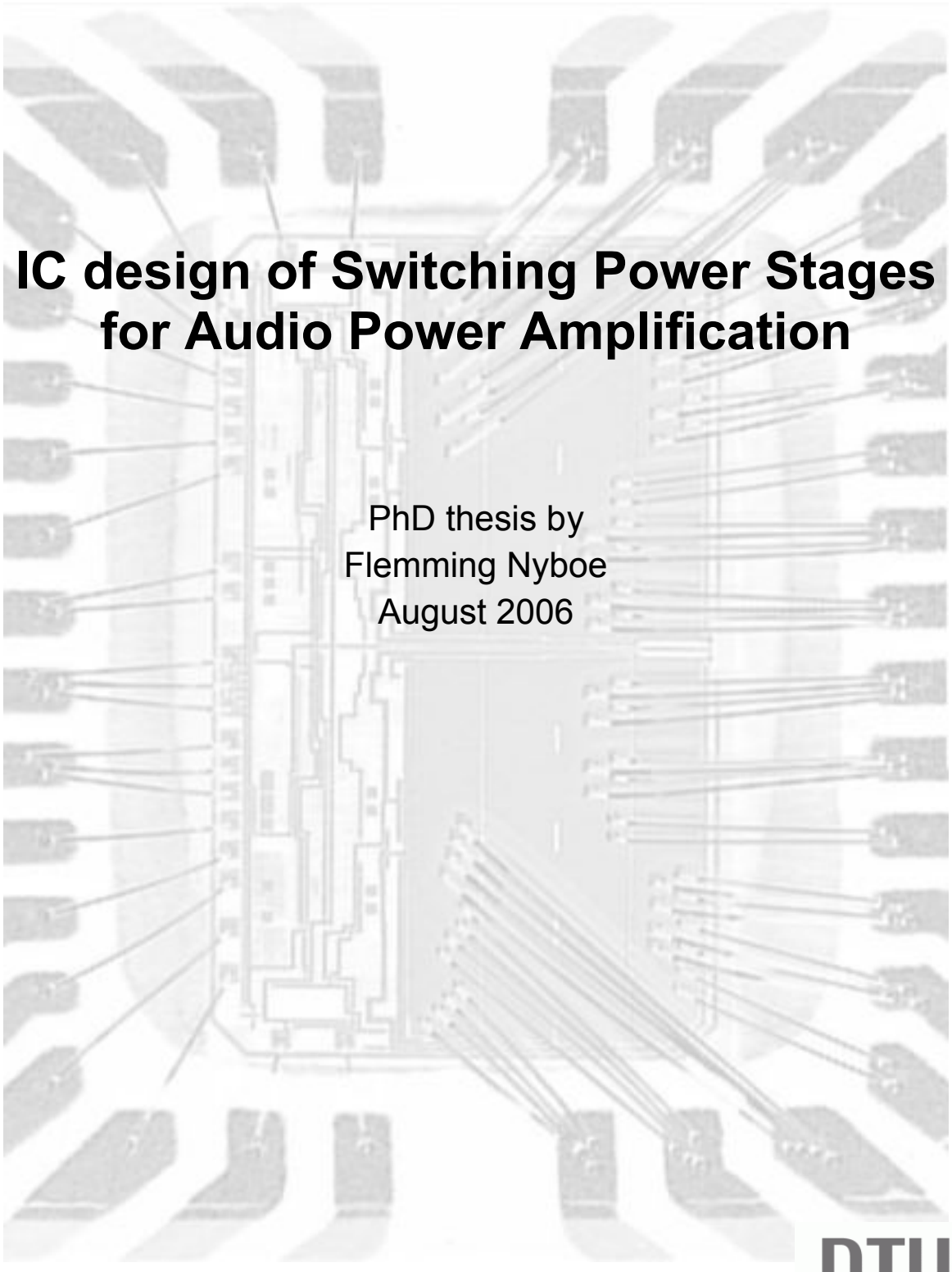

IC design of Switching Power Stages for Audio Power Amplification

PhD thesis by
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August 2006

Ørsted•DTU

To Henrik,
for pushing me.

Preface

This thesis concludes a PhD project carried out in collaboration between the Ørsted•DTU institute at the Technical University of Denmark (DTU) and Texas Instruments (TI).

The project ran from August 2003 thru July 2006, under the Industrial PhD initiative[1], and was supervised by Lars Risbo from TI and Professor Pietro Andreani from Ørsted•DTU.

This version is an update from February 2007. Figure 0-6 is changed, and minor corrections have made to the text.

Abstract

Research in Class D audio amplifiers stems back to the sixties[2], and practical use has increased mainly since the nineties, facilitated by advances in transistor technology. Most publications from this era focus on implementations with analog audio input and discrete output transistors. Since then, monolithic implementations have arrived, and these are the main focus of this thesis. Following the introduction in chapter 0, three chapters discuss each of three performance metrics by which Class D amplifiers are commonly assessed.

Power losses in the output stage are analyzed in chapter 1. This topic is well covered in existing literature on switching power converters, but mostly under assumptions that can not be made for audio amplifiers. This analysis specifically addresses power losses in a switching output stage for audio signal reproduction.

The analysis initially assumes an ideal power supply for the output stage, and subsequently includes the effects of parasitic inductances around the output stage. It is shown that the inclusion of parasitic inductance in the analysis causes fundamental changes in circuit behavior, and that the achieved results do not converge towards the results for an ideal power supply when the values of parasitic inductances go towards zero. Further, it is shown that conduction overlap between the output switches, which is typically prevented by use of switching dead time, is unavoidable when parasitic inductance is considered.

Chapter 2 is an analysis of parameters influencing the maximum output power of a Class D amplifier. It includes a comparison of the die area of equivalent solutions in different topologies, and an analysis of the maximum output currents needed to drive loudspeakers.

Distortion in a Class D amplifier system is mainly caused by the switching output stage, and is covered in chapter 3. This topic is especially relevant because most audio signal sources are digital (CD, DVD, digital media players, etc.), causing an increasing demand for low cost Class D amplifiers accepting a digital audio input. Feedback can not easily be implemented in such amplifiers, so low open-loop distortion is essential. The primary source of distortion is nonlinearities related to the switching transitions, and it is shown that when the influence of output current on switching transition waveforms is considered, the optimum amount of dead time for minimum distortion is not zero, but finite.

The overall performance of the amplifier is shown to depend heavily on properties of the gate driver circuits, and a summary of relations between gate driver properties and performance is given in chapter 4, along with a presentation of a design example; a monolithic power stage from the Texas Instruments portfolio.

Finally, modeling and simulation techniques specifically suited for Class D amplifiers are presented in chapter 5.

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[1] see www.erhvervsphd.dk

[2] e.g. Norman H. Crowhurst "Two-State Power Amplifier with Transitional Feedback", US patent #3,336,538

0 Introduction

This chapter defines the scope of this document, explains general assumptions, and defines some circuit and signal names used in the analyses in the chapters following.

0.1 Scope, the Buck-topology output stage

While it is possible to base class-D amplifiers on different power converter topologies, the two-switch Buck topology is by far the most widely used, due to its linear transfer characteristic from switching duty cycle to output voltage.

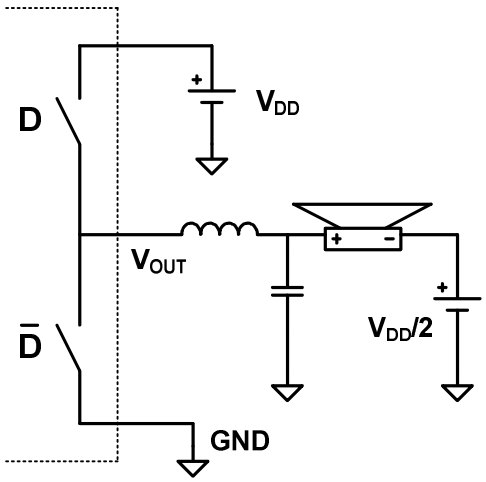


Figure 0-1: Single ended (SE) buck output stage

A single-ended (SE) buck output stage is shown in Figure 0-1. The two switches alternately connect the V_{OUT} node to V_{DD} and GND, at a frequency much higher than the cutoff frequency of the LC filter. The switching duty cycle is D, meaning V_{OUT} is connected to V_{DD} for D•100% of the time. This produces an output voltage of $(D-½)•V_{DD}$ across the loudspeaker, and the desired output signal is then produced by varying D over time. Note that both signs of output voltage can be produced, and that for D=½, no voltage is present across the loudspeaker, since the average value of V_{OUT} is $V_{DD}/2$.

As an alternative to the $V_{DD}/2$ voltage source, the negative loudspeaker terminal can be connected to GND via a capacitor large enough to provide an acceptable lower cutoff frequency with a loudspeaker load (1000µF gives a 40Hz -3dB corner with 4Ω).

A differential output stage configuration is shown in Figure 0-2. It uses four switches and has the following advantages

- Output voltage is $2•(D-½)•V_{DD}$, i.e. twice that of the SE configuration, providing four times higher output power
- The $V_{DD}/2$ voltage rail (or a series capacitor) is not needed
- Lower distortion (see section 3.2.2)

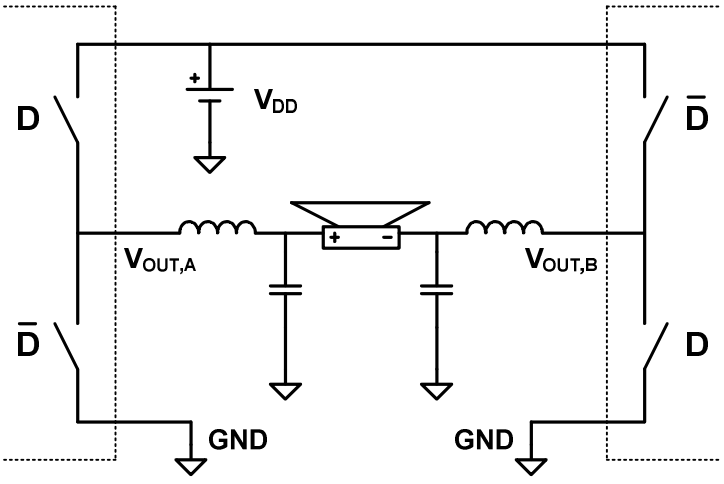


Figure 0-2: Differential (BTL) buck output stage

The differential output stage configuration is sometimes referred to as a Bridge Tied Load (BTL) configuration, or an H-bridge output stage, due to the "H" shape formed by the switches and the load. Similarly, the two switches in a SE output stage are called a half-bridge.

Most of the analyses presented in this document treat only one half bridge, since that with appropriate symmetry considerations, the results can also be applied to H-bridge stages.

The analyses of power losses and device stress have significant relevance for two-switch Buck power supplies also.

Class D amplifier output stages can be monolithic, or discrete transistors can be used for output switches. This document focuses mainly on monolithic solutions, where the all output stage switches are implemented on one chip, so the dotted lines in Figure 0-1 and Figure 0-2 represent the chip boundary. However, most results are relevant for discrete solutions as well.

0.2 Outside of scope

The input signal for the output stage is assumed to be a pulse width modulated (PWM) audio signal with fixed carrier frequency. The impact of using variable-frequency or pulse density modulation will not be covered.

PWM can be generated using different modulation schemes (single-sided, double-sided, etc.), but these will not be discussed since the choice of scheme should not directly affect the performance of the output stage itself. An exception to this is the impact of output stage nonlinearities on output noise when noise shaping is used in the modulation, and this will be discussed briefly.

Conversely, device noise in a Class D amplifier output stage will typically not cause any discernable amount of noise at the loudspeaker load, and is not discussed.

Design of over-current protection systems for the output stage will not be covered, but an analysis of current requirements for driving loudspeaker loads is included in Appendix II.

The design and optimization of feedback loops will not be covered, and the chapter on distortion analyzes only the open-loop distortion of an output stage. Though this is mostly important for open-loop output stage configurations, any open-loop distortion improvement will also benefit an amplifier with feedback.

0.3 Circuit definitions

0.3.1 Half bridge with bootstrap gate driver supply

This document will focus on output stages where both half-bridge switches are N-type MOSFETs, as shown in Figure 0-3. The circuits that control the output switches are called gate drivers, drawn here as buffer amplifiers.

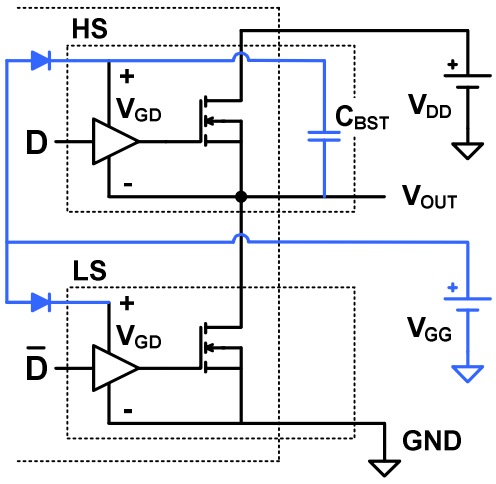


Figure 0-3: Half bridge with N-type MOSFET switches, gate drivers and bootstrap gate driver supply.

The complete switch circuit connecting the V_{OUT} node to V_{DD} (output FET and gate driver) is termed the *high-side* (HS) circuit, and the circuit connecting to GND similarly the *low-side* (LS) circuit. Throughout this document, the HS and LS circuits are considered identical.

The supply circuit for the gate drivers is highlighted in blue. An external decoupling capacitor C_{BST} is connected to the supply rail of the HS gate driver through a separate pin. This capacitor maintains a DC supply for the HS gate driver, relative to the HS output FET source terminal, and is charged through an integrated diode when the V_{OUT} node is at GND potential. This approach is called *bootstrap supply*, and C_{BST} the *bootstrap capacitor*. Since C_{BST} is an external component, its capacitance can

be selected large enough to provide an insignificant voltage ripple. The diode in the low-side gate driver supply could be omitted, but is included here to obtain equal supply voltages for the HS and LS gate drivers: V_{GD} equal to V_{GG} minus the forward drop of the diodes.

0.3.2 Gate driver implementation

Each gate driver (GD) has two states: ON (Q3 on, Q2 off) and OFF (Q3 off, Q2 on). Between switching transitions, the gate driver output voltage V_{GS} is either 0 or V_{GD}, depending on state, and the driver output current I_{GD} is zero.

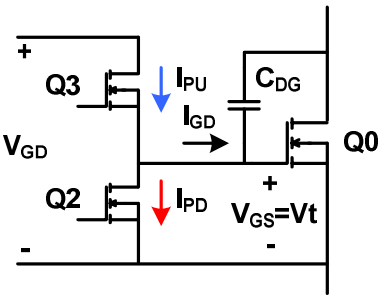


Figure 0-4: An output FET and its Gate driver. HS and LS circuits are identical.

During switching transitions, the voltage change across the output FET causes a current flow in its drain-gate capacitance C_{DG}. This current loads the gate driver output, and effectively limits the rate at which the voltage across the output FET can change. This mechanism is important in output stage analysis, because the output voltage slew rates during switching transitions affect the performance of the amplifier in several ways.

Two different limits apply, depending on the state of the gate driver: When the gate driver is in its OFF state (Q2 on), the voltage across the output FET can increase only as fast as:

$$\frac{dV_{DS,Q0}}{dt} \le \frac{I_{PD}}{C_{DG}} \qquad \text{Gate driver in its OFF state} \qquad \textbf{Eq. 0-1}$$

where I_{PD} is the drain current of Q2 at $V_{DS,Q2}$=Vt, and the transconductance of the output FET is assumed infinite. When the gate driver is in its ON state (Q3 on), the voltage across the output FET decreases at least as fast as:

$$\frac{dV_{DS,Q0}}{dt} \le -\frac{I_{PU}}{C_{DG}} \qquad \text{Gate driver in its ON state} \qquad \textbf{Eq. 0-2}$$

Where I_{PU} is the drain current of Q3 at $V_{DS,Q3}$=V_{GD}-Vt. Equality in Eq. 0-2 occurs when the voltage slope across the output FET is controlled solely by the gate driver turning on the output FET. However, $V_{DS,Q0}$ can decrease faster than this if aided by an external current. In this case, inequality in Eq. 0-2 occurs, and the output current from the gate driver becomes the sum of I_{PU} and additional current flowing in the source-drain diode of Q2. Both limits apply to both output FETs.

A gate driver is characterized fully by two I/V output characteristics for pull-up and pull-down respectively. For a GD where both the pull-up and pull-down devices are N-type MOSFETs as shown in Figure 0-4, Q2 will be in the linear region as long as the GD output voltage V_{GS} is not close to V_{GD}. This results in a linear pull-down I/V curve as shown in red in Figure 0-5. Since Q3 has equal gate and drain potentials when turned on, it will be in the active region, and the drain current will have a parabolic dependency on output voltage as shown in blue in Figure 0-5.

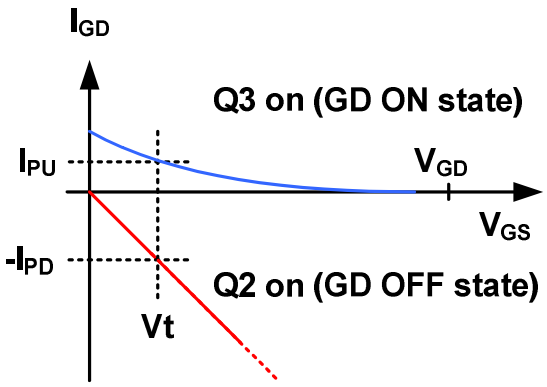


Figure 0-5: Gate driver I/V characteristics

Output stage switching is mostly affected by the values of the pull-up and pull-down I/V curves at V_{GS}=Vt (I_{PU} and I_{PD}) as described by Eq. 0-1 and Eq. 0-2. The rest of the I/V curves only affect the speed of charge or discharge of output FET V_{GS} during the conduction states where V_{OUT} is constant at GND or V_{DD}.

0.3.3 Dead time

If the two switches in a half bridge were turned on simultaneously, they would short circuit the power supply and immediately damage the output stage. To ensure this is avoided, one switch is always turned off slightly before the other is turned on, so both switches are off for a brief interval during each switching transition. This interval is referred to as *dead time* (t_{DT}). Dead time is a key parameter in class D amplifiers, but several different definitions of its exact meaning are seen. In this document, dead time is defined as the duration of the interval in Figure 0-6 where both gate driver outputs are in the OFF state, and assumed equal for falling- and rising-edge switching transitions. When the output state of a gate driver changes, this change is considered instantaneous, i.e. an abrupt switch between the blue and red output characteristics in Figure 0-5. It should be noted that from the time where a gate driver output enters its OFF state, it takes a finite duration before the corresponding output FET reaches the OFF state. Similarly, when a gate driver enters its ON state, it takes finite time before the corresponding output FET enters its ON state, and it may take additional time for the V_{OUT} transition to complete. As a result, V_{OUT} is undefined from the time where one gate driver enters its OFF state, until some time after the other enters its ON state, as indicated by the dashed areas in Figure 0-6. The V_{OUT} waveform in this interval depends on I_{OUT} and properties of the output stage, and will be analyzed in the following chapters.

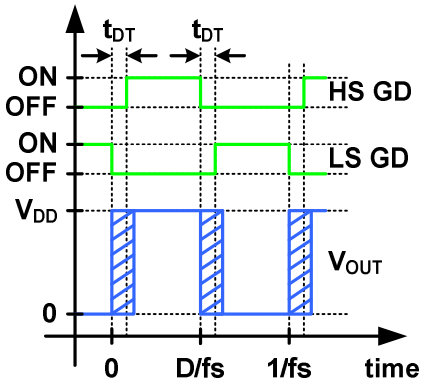


Figure 0-6: Gate driver waveforms. t_{DT} is dead time, shown longer than actual for clarity.

0.3.4 Output FETs

For non-portable audio amplifiers, typical V_{DD} supply voltages are in the range of 12 to 50V depending on application, and loudspeakers typically present a 4 to 8Ω load impedance. This results in output current levels ranging from a few A up to more than 10A for high-power devices. These levels of current cause significant power losses in the output FETs. In order to dissipate the heat, monolithic output stages are packaged in thermally enhanced packages, as shown in Figure 0-7. The die is upside down inside the package, and mounted on a metal heat slug, which protrudes through the plastic mould, for direct attachment to a heat sink.

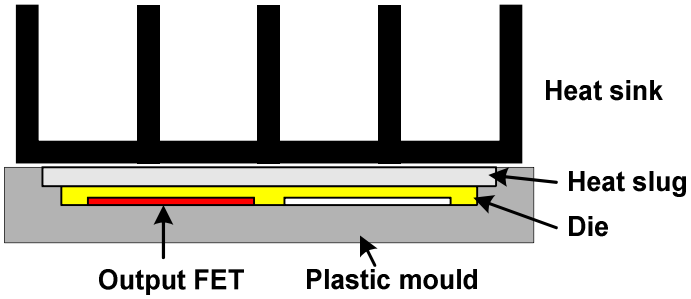


Figure 0-7: Thermally enhanced chip package

In order to handle the current, the output switches are very large and take up a large fraction of the total die area (30-50%). This means that for cost reasons alone, it is desirable to make the output switches as small as possible, where the minimum size is set by thermal limitations; each output FET must be large enough to conduct the maximum needed output current without overheating. Increasing output FET size causes a twofold reduction in its operating temperature: The maximum power loss decreases due to reduced $R_{DS(ON)}$ and the thermal resistance from the FET to the heat sink is reduced (see Figure 0-7). When an output stage is designed to deliver a given output power into a given load impedance, maximum output current is given, and the needed output FET size can be determined. Due to the HS-LS symmetry assumption, all output FETs in an output stage are assumed to be of equal type and size, and the size is considered given in the analyses in this document.

0.3.5 Output filter and ripple current

In most amplifier designs, the PWM output signal from the half bridge is lowpass filtered by an external 2nd order LC filter. Ideally, the cutoff frequency should be just above the upper limit of the audio frequency band (20kHz) to pass through audio frequencies while providing maximum suppression of the PWM switching carrier. Some systems use higher cutoff frequencies to make the gain at 20kHz more independent of load resistance, or simply to reduce the cost of the inductor. The ratio between L and C is determined by the need to obtain reasonable damping with loudspeaker loads in the range of 4 to 8Ω. Note that in a BTL configuration, there are two identical output filters, each loaded by only half the loudspeaker impedance. For a given cutoff frequency and damping requirement, there are no degrees of freedom left in the design of the output filter, and it is considered fixed throughout this document. Example component values are L=10µH and C=1µF for f_0=50kHz and Q=0.63 (Q=1.23) with 4Ω (8Ω) BTL load.

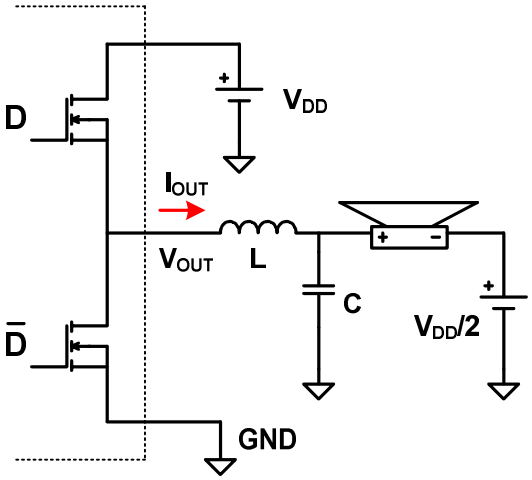


Figure 0-8: Half bridge with output LC filter

Like in switch mode power supplies, the square PWM waveform causes a triangular ripple current waveform in the output filter. Figure 0-9 shows the waveforms at 50% duty cycle, i.e. no output signal, also referred to as *idle (operation)*. Note that at idle, I_{OUT} changes sign between each switching transition. Throughout the document, I_{OUT} is defined positive flowing out of the half bridge, see Figure 0-8.

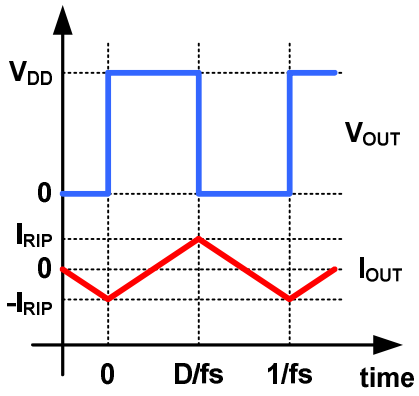


Figure 0-9: Waveforms at idle

0.4 Analytical domains

Three domains of circuit analysis have been used in this work: Measurements, simulations, and calculation. While this is almost obvious for this type of work, I find it particularly important to distinguish between the 3 approaches, understand the strengths and weaknesses of each one, and to use all 3.

What is meant by calculation is the derivation of analytical expressions for circuit behavior, and the use of these expressions for circuit modeling.

	Measurement	**Simulation**	**Calculation**
Included effects	All	Some	Selected set
Execution time	(Medium)	Medium	Fast
Cycle time	Slow	Fast	Fast

The final assessment of circuit performance is of course measurement. It shows the combined effects of all circuit behavior, including known and unknown mechanisms. While this shows the true circuit performance, the all-inclusiveness can also be a disadvantage, when using measurements in development and optimization. For example, the overall power consumption of a chip can be measured, but not always broken down into individual subcircuits, let alone individual transistors. Another limitation is the cycle time from a measurement, through redesign, and to the measurement on the redesigned circuit. In IC design, such a cycle takes months and is expensive. Though measurements are sometimes conceived as ultimately accurate performance assessments, they are in fact not. While simple quantities like DC voltage or current can easily be measured with very large accuracy, more complex measurements based e.g. on high sampling rate oscilloscope waveforms are subject to significant errors, both due to the instrument and to its interface to the circuit. Another limitation of measurements relates to control of external variables. Temperature can be controlled to some extent, but when making measurements on a prototype IC, it represents a random sample of the process variations, shifting results in a most often unknown direction relative to typical performance.

Some disadvantages of measurements are overcome in simulation. All circuit variables are available, and since the circuit can be changed instantly, the cycle time is as fast as the simulation itself. The cost is loss of accuracy. Simulation has a number of error sources, including:

- Lack of temperature awareness. All devices are typically assumed to have equal and constant temperature while in practice, devices will self-heat depending on their individual power losses, resulting in different temperatures

- Device substrate modeling. The simplest substrate models are just a single net covering the whole chip, with no account for the physical placement of devices. In practice, substrates have finite resistivity, resulting in localized interaction between devices.
- Numerical errors (often a trade-off with execution time)
- Device model inaccuracies. While devices models have become fairly complex, it is still a challenge to make them fit over all regions of operation, sizing and temperature.
- Package/peripheral model inaccuracies. A large effort is put into pin and bond wire models (especially driven by RF designs), but models are not equally mature for all technologies. Further, device performance often depends on surrounding components and PCB layout, for which no ready-made models exist.

Process variations can be simulated by Monte Carlo runs with random process variations, and this is a major strength of simulation. Doing something similar in measurements would not only require a large measurement effort, but also a selection of devices with a perturbation of process parameters which is representative of the long-term process variation, and this is not easily obtainable.

A note on simulation speed: There is no such thing as "fast enough". Assuming that the distortion of a circuit can be simulated in 5 seconds, simulating it vs. temperature (5 steps) and one supply voltage (5 steps) then takes 625 seconds. Including process variation (50 Monte Carlo runs) then becomes an overnight simulation (on a single CPU), and gives one iterative step a day for circuit optimization. If the simulation instead took 1 second, it could run for 5 different sizes of a given device to find its optimum size, or if it was 0.2 seconds, it could do this for two devices in a night. There is no upper limit for useful simulation speed. Moore's law [1] is on our side, but will it outgrow the circuits we simulate, using increasingly complex device models?

A faster alternative to simulation is to calculate circuit behavior based on known analytical expressions. The derivation of such expressions is typically the most fruitful part of this process. Determining dependencies and finding which ones are logarithmic, square root, linear, quadratic, exponential or nonexistent, is the key to understanding of circuits or, as Richard W. Hamming put it: *The purpose of computing is insight, not numbers*. If circuit performance is the cake, these equations are the recipe. A unique feature of calculating performance is that the set of contributions (to power losses, distortion etc.) is well defined, and each individual contribution can be gauged, included or excluded from the results as desired. Comparing calculated results to measured (or simulated) can reveal whether or not certain known mechanisms can or can not account for the observed performance. In this perspective, the derivation of mathematical models can be useful even if the results do not match actual circuit performance well. When they do, straightforward calculation becomes the fastest possible modeling tool.

0.5 Abbreviations and Terms

Abbreviation	Meaning	Comments
C_{DG}	Drain-Gate capacitance of output FETs	
C_{OUT}	Output LC filter capacitance	
D	PWM duty cycle	Range 0 to 1
ESL	Equivalent Series Inductance	Parasitic component in e.g. discrete capacitors

Abbreviation	Meaning	Comments
ESR	Equivalent Series Resistance	Parasitic component in e.g. discrete capacitors and inductors
FET	Field Effect Transistor.	Also used for LDMOS.
fs	PWM switching frequency	
GD	Gate Drive circuit	
GND	Electrical ground	Exact definition varies with context. Note that GND is often defined as ground on the PCB outside the chip
HS	High-Side output stage switch circuit	
I_{OUT}	Half bridge output current (waveform) Positive out of the half bridge	Flows in the output filter inductor $I_{OUT} = I_{SPK}+I_{RIP}$
I_{PD}	Gate drive pull-down current	At GD output voltage = Vt Always positive, see Figure 0-4
I_{PU}	Gate drive pull-up current	At GD output voltage = Vt Always positive, see Figure 0-4
I_{RIP}	Ripple current (waveform)	Flows in output filter capacitor
$I_{RIP,P}$	Ripple current amplitude (scalar)	
I_{SPK}	Speaker current (waveform)	
KCL	Kirchoff's current law	
KVL	Kirchoff's voltage law	
LDMOS	Lateral double-diffused MOSFET	
L_{OUT}	Output LC filter inductance	
LS	Low-Side output stage switch circuit	
MI	Modulation Index (for PWM)	Amplitude of Duty cycle variation. Range [0..1]
OC	Over Current (in case of amplifier output short circuit or overload)	
PCB	Printed Circuit Board	
PVT	Process / Voltage / Temperature (variations)	
PWM	Pulse Width Modulation	
R_{SP}	Specific resistance. The on-resistance of a transistor of unit area.	
t_{DT}	Dead time	Defined as the duration of the interval where both gate drivers are in the off state
V_{DD}	Output stage positive supply rail	Typically 12-50V
V_{GD}	Effective Gate driver supply voltage	V_{GG} minus a forward diode drop
V_{GG}	Gate drive supply rail	Typically 12V
Vt	FET Gate-source threshold voltage	

Active region: For MOSFETs, the region where $V_{DS} > V_{GS}$-Vt, commonly known as the *Saturation region*, but this term is avoided here to avoid confusion with the saturated region for bipolar transistors, as suggested in [2].

Transfer characteristic: The time-domain ratio of output to input signal, not to be confused with frequency-domain transfer function.

0.6 References

[1] Gordon E. Moore: *Cramming more components onto integrated circuits.* Electronics Magazine 19, April 1965

[2] David A. Johns, Ken Martin: *Analog Integrated Circuit Design*. ISBN 0-471-14448-7

1 Power losses

High power efficiency is one of the main advantages of class D audio amplifiers over traditional class AB designs. Lower power losses for the same output power allows the use of smaller heat sinks, allowing smaller form factor end products. Even with the inherent efficiency advantage of class D there is still a strong interest in minimizing losses, to gain the most from the technology. This chapter presents an analysis of output stage power losses, and how they depend on design variables.

1.1 Introduction

1.1.1 Ripple current

The output current from the half bridge I_{OUT} is the sum of the audio signal current in the speaker load I_{SPK} and the ripple current caused by the output filter, see Figure 1-1. The ripple current itself is triangular-shaped, has mean value 0 and a peak amplitude of:

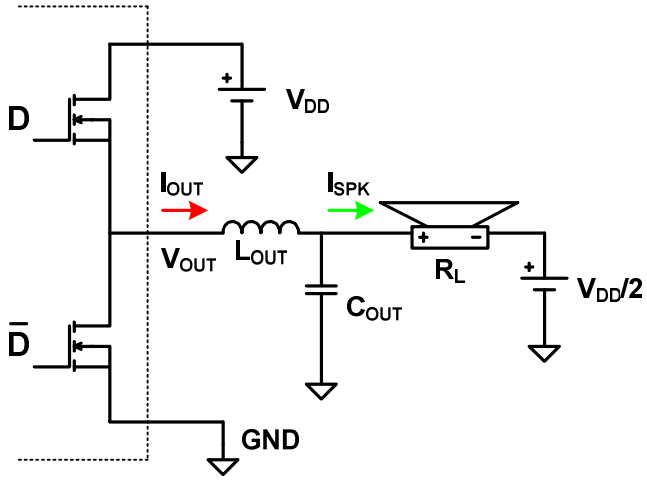


Figure 1-1: Definition of I_{OUT} vs. I_{SPK}

$$I_{RIP,P} = \frac{V_{DD}}{2 \cdot L_{OUT} \cdot fs}\left(D - D^2\right) \qquad \textbf{Eq. 1-1}$$

when V_{OUT} is assumed to be a perfect square wave, which is reasonable since the rising- and falling edge transitions have short durations compared to the PWM period. Maximum ripple current amplitude occurs at idle (D=½):

$$I_{RIP,P,IDLE} = \frac{V_{DD}}{8 \cdot L_{OUT} \cdot fs} \qquad \textbf{Eq. 1-2}$$

Figure 1-2 shows output and ripple current waveforms for an output stage operating at a fixed duty cycle D=60%. I_{SPK} is the output current delivered to the load, and has the value

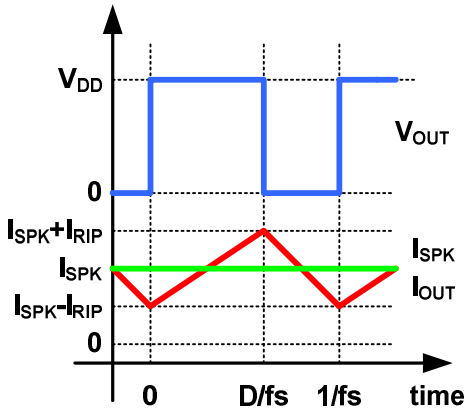


Figure 1-2: Waveforms for a DC output signal, D=60%.

$$I_{SPK} = \frac{V_{DD}}{R_L} \cdot \left(D - \frac{1}{2}\right) \qquad \textbf{Eq. 1-3}$$

The relation between duty cycle, I_{SPK} and I_{OUT} is shown in Figure 1-3. Note that while I_{SPK} depends on R_L, I_{RIP} depends only on D (for given V_{DD}, fs and L_{OUT})

I_{OUT} is the current flowing in the output transistors, and thus responsible for output stage power losses. Consequently, the I_{OUT} waveform plays a central role in power loss analysis; it can be approximated by the following piecewise linear waveform:

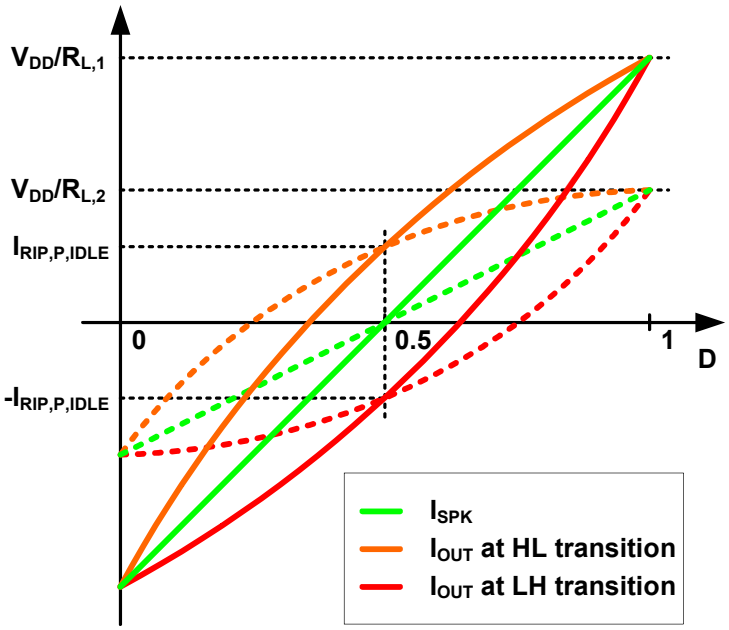


Figure 1-3: I_{SPK} and I_{OUT} peak values vs. Duty cycle, for two different load resistances $R_{L,1} < R_{L,2}$.

$$I_{OUT} = \begin{cases} \text{Linear increase from } I_{SPK} - I_{RIP,P} \text{ to } I_{SPK} + I_{RIP,P} & \text{HS FET on (PWM high)} \\ \text{Linear decrease from } I_{SPK} + I_{RIP,P} \text{ to } I_{SPK} - I_{RIP,P} & \text{LS FET on (PWM low)} \end{cases} \quad \text{Eq. 1-4}$$

where I_{SPK} and $I_{RIP,P}$ are given by Eq. 1-3 and Eq. 1-1.

1.1.2 Output switch energy losses at a fixed duty cycle D

At a fixed duty cycle (Figure 1-2) the energy loss during one period of the PWM signal consists of 4 subsequent contributions:

Loss mechanism	Function	I_{OUT} value
Switching loss during the LH transition of V_{OUT}	$E_{SW,RISE}$	$I_{OUT} = I_{SPK}-I_{RIP,P}$
Conduction loss in the HS FET while V_{OUT} is high	$E_{COND,HS}$	I_{OUT} going from $I_{SPK}-I_{RIP,P}$ to $I_{SPK}+I_{RIP,P}$
Switching loss during the HL transition of V_{OUT}	$E_{SW,FALL}$	$I_{OUT} = I_{SPK}+I_{RIP,P}$
Conduction loss in the LS FET while V_{OUT} is low	$E_{COND,LS}$	I_{OUT} going from $I_{SPK}+I_{RIP,P}$ to $I_{SPK}-I_{RIP,P}$

Table 1: The four output stage power loss events that occur once per PWM period.

While the two functions for transition losses E_{SW} are most easily expressed by I_{OUT} at the time of the transition, each of the two loss functions for conduction E_{COND} depend on the respective I_{OUT} waveform segment as given by Eq. 1-4. For given values of V_{DD} and R_L, all four loss functions can be expressed in D by using Eq. 1-1, Eq. 1-3 and Eq. 1-4, and then added to find the total loss during one period of the PWM signal:

$$E_{PER}(D) = E_{SW,RISE}(D) + E_{COND,HS}(D) + E_{SW,FALL}(D) + E_{COND,LS}(D) \quad \text{Eq. 1-5}$$

1.1.3 Output switch power losses when playing a signal

The average power loss for a fixed switching duty cycle D are

$$P_{TOT}(D) = fs \cdot E_{PER}(D) \qquad \textbf{Eq. 1-6}$$

This expression can be used to find the power loss for any output signal, for example the idle power loss is $P_{TOT}(0.5)$, and the average power loss for any periodic input signal is

$$P_{PER,AVG} = \frac{1}{T}\int_0^T P_{TOT}(D(t))dt \qquad \textbf{Eq. 1-7}$$

Where D(t) is the duty cycle variation that defines the signal, and T is the period length. When playing a pure sine wave audio signal, the duty cycle D will vary with time as:

$$D(t) = \frac{\mathbf{1}}{\mathbf{2}} + \frac{\mathbf{1}}{\mathbf{2}} \cdot MI \cdot \sin(\mathbf{2\pi} \cdot fa \cdot t) \qquad \mathbf{0} \le MI \le \mathbf{1} \qquad \textbf{Eq. 1-8}$$

where MI is the amplitude of the duty cycle variation, called the *modulation index*. MI=0 corresponds to idle operation, MI=1 to maximum output power. Inserting Eq. 1-8 into Eq. 1-7 and integrating over one period of the audio sine wave gives the average power dissipation for sine wave playback:

$$P_{SINE,AVG}(MI) = fa\int_0^{1/fa} P_{TOT}(D(t))dt = \int_0^{2\pi} P_{TOT}\left(\frac{1}{2} + \frac{1}{2} \cdot MI \cdot \sin(x)\right)dx \qquad \textbf{Eq. 1-9}$$

Figure 1-4 shows I_{SPK} and I_{OUT} when playing a large amplitude sine wave (MI=0.96). The output filter causes a small phase lag between I_{SPK} and I_{OUT} which is ignored in Eq. 1-4, and has negligible effect on power losses averaged over a full sine wave period.

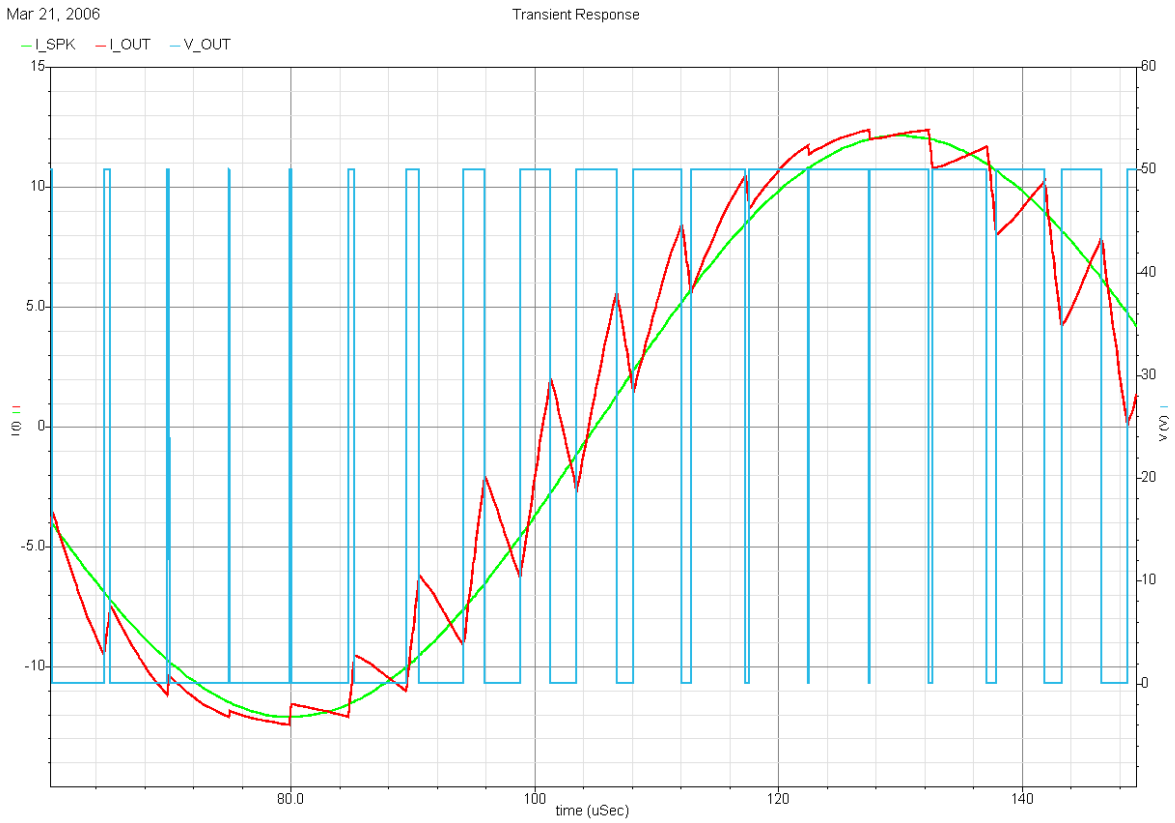


Figure 1-4: Output stage waveforms while playing a sine wave at MI=0.96, fa=10kHz, with fs=200kHz, V_{DD}=50V, L=10µH, 4Ω resistive load (BTL). I_{SPK} and I_{OUT} (left Y axis) and V_{OUT} (right Y axis).

1.1.4 End product implications

During practical use, the power loss in an audio amplifier depends on the music played, the volume, and the loudspeaker. Lacking a standardized music signal and loudspeaker, power losses are typically analyzed for a sine wave audio signal and a resistor as load. Two specific operating conditions have particular impact on end product design, and are often evaluated: The maximum possible power loss, and the power loss at idle operation.

Maximum power loss represents the worst-case condition for cooling requirements. The heat sink must be large enough to dissipate this loss as heat, while keeping the output transistors below their maximum junction temperature. Since power loss generally increases with output power, maximum power losses are caused by maximum output power, and can be found from Eq. 1-9 as:

$$P_{SINE,AVG(MAX)} = P_{SINE,AVG}(1) \qquad \textbf{Eq. 1-10}$$

and depends on load resistance.

In more conservative designs, an overdriven (clipped) sine wave signal is used as worst case input, since overdrive increases power losses further. As overdrive is increased, the power loss goes towards the power loss for a full-amplitude square wave signal, corresponding to a sine wave with infinite overdrive. Eq. 1-7 can then readily be used.

In small form factor end products, an air fan is sometimes used to provide forced cooling when playing at high output powers, to reduce the heat sink size necessary to dissipate the maximum power loss. However when playing at low volumes, the noise of the air fan can typically not be tolerated, and this imposes a different heat sink requirement: The heat sink,

though aided by forced air at high output power, must be large enough to dissipate the idle power loss even with the fan turned off. Depending on product design, heat sink size may be determined by this requirement, and this causes a special interest in the idle power loss. It should be noted that from a thermal point of view, there is only a negligible difference between idle operation and playing music at background listening levels. Due to the logarithmic nature of volume perception, everyday music playback typically requires less than 1W of output power, which for a powerful amplifier will not cause any significant difference in output stage power loss compared to idle operation, since I_{OUT} will be heavily dominated by the ripple current. Using Eq. 1-9, the idle power loss can be found as

$$P_{IDLE,AVG} = P_{SINE,AVG}(0) \qquad \textbf{Eq. 1-11}$$

Since there is no output signal, the idle loss is independent of load resistance.

Through the equations given above, output stage power losses for any input signal can be found from the four energy loss functions in Table 1. In the following two sections, expressions will be derived for the conduction losses $E_{COND,HS}$ and $E_{COND,LS}$, and for the switching losses $E_{SW,RISE}$ and $E_{SW,FALL}$.

1.2 Conduction power losses

During each PWM period, the half bridge output current I_{OUT} flows in the high side output FET for a duration of:

$$t_{COND,HS} = \frac{D}{fs} - t_{DT} - t_{ON} + t_{OFF} \qquad \textbf{Eq. 1-12}$$

Where t_{DT} is dead time, t_{ON} is the time from the end of dead time until the FET is turned on, and t_{OFF} is the time it takes the gate drive to turn off the FET at the end of its conduction state. Similarly, the low side FET is conducting I_{OUT} for a duration of:

$$t_{COND,LS} = \frac{1-D}{fs} - t_{DT} - t_{ON} + t_{OFF} \qquad \textbf{Eq. 1-13}$$

For typical values of dead time and switching speed, the first term in Eq. 1-12 and Eq. 1-13 is much larger than the sum of the 3 last terms, which can then be ignored with an error of less than 1%. With this assumption, the sum of the HS and LS conduction periods is

$$t_{COND,HS} + t_{COND,LS} \approx \frac{D}{fs} + \frac{1-D}{fs} = \frac{1}{fs} \qquad \textbf{Eq. 1-14}$$

which corresponds to assuming that at any point in time, I_{OUT} flows in one of the switches, and the durations of the two switching transitions are ignored. The mean-squared value of I_{OUT} over one PWM period is

$$I^2_{OUT,RMS} = I^2_{SPK} + \tfrac{1}{3} I^2_{RIP,P} \qquad \textbf{Eq. 1-15}$$

The current paths are shown in Figure 1-5, and the waveforms in Figure 1-6. Due to the triangular shape of I_{OUT}, it can be shown that the mean-squared currents in each output switch are simply:

$$I_{HS,RMS}^2 = D \cdot I_{OUT,RMS}^2 \qquad \text{Eq. 1-16}$$

$$I_{LS,RMS}^2 = (1-D) \cdot I_{OUT,RMS}^2 \qquad \text{Eq. 1-17}$$

And hence the conduction energy losses per PWM period in each device become:

Eq. 1-18

$$E_{COND,HS} = \frac{D}{fs} \cdot R_{DS,ON} \cdot \left(I_{SPK}^2 + \tfrac{1}{3} I_{RIP,P}^2 \right)$$

Eq. 1-19

$$E_{COND,LS} = \frac{1-D}{fs} \cdot R_{DS,ON} \cdot \left(I_{SPK}^2 + \tfrac{1}{3} I_{RIP,P}^2 \right)$$

And the total conduction power loss in the output devices is the sum of the two, multiplied by fs:

Eq. 1-20

$$P_{COND,TOT} = R_{DS,ON} \cdot \left(I_{SPK}^2 + \tfrac{1}{3} I_{RIP,P}^2 \right)$$

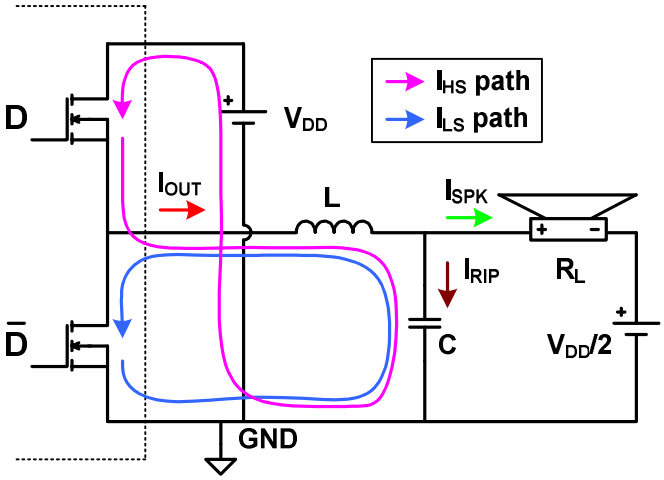


Figure 1-5: High side and Low side current paths

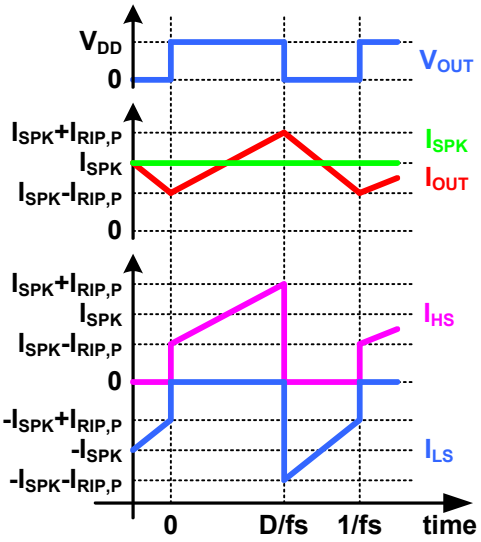


Figure 1-6: High side and Low side current waveforms

where $R_{DS(ON)}$ is the channel resistance of Q0 and Q1. Using Eq. 1-1 and Eq. 1-3, I_{SPK} and $I_{RIP,P}$ can be expressed in the duty cycle D (for a given R_L and V_{DD}) to give the conduction power loss as a function of duty cycle, which can then be inserted in Eq. 1-7 to find the conduction power loss for any periodic input signal.

1.2.1 Conduction losses outside the chip

While Eq. 1-20 accounts only for the power losses in the output FETs, there are also power losses in the external components. The system impact of these losses is different, since they do not influence heat sink requirements (except by increasing air temperature inside an enclosure).

As shown in Figure 1-5, the ripple current flows in the output filter capacitor, thus causing a power loss of

$$P_{COUT} = ESR_{COUT} \cdot \frac{1}{3} I_{RIP,P}^2 \quad \textbf{Eq. 1-21}$$

where ESR_{COUT} is the parasitic series resistance of the capacitor. This power loss is largest at idle, and will typically not exceed 50mW.

The output inductor carries I_{OUT}, i.e. the sum of I_{SPK} and I_{RIP}. The spectrum of I_{OUT} spans both audio frequencies, the switching frequency fs and its harmonics, and the series resistance of the inductor varies over this frequency range. At the upper limit of the audio band (20kHz), skin depth is 0.47mm, and for a reasonable thickness of copper wire in the output inductor, it is accurate to assume that the current is uniformly distributed across the wire cross section. At a switching frequency of 384kHz, skin depth is 0.1mm, so the fundamental frequency of the triangular ripple current waveform flows only in the surface of the wire, increasing effective series resistance and hence power losses. At idle (D=½) the ripple current has its maximum amplitude, and can be expressed as:

$$I_{RIP}(t) = I_{RIP,P} \sum_{n=1}^{\infty} b_n \cdot \sin(n \cdot 2\pi \cdot fs \cdot t) \qquad b_n = \frac{8}{(\pi \cdot n)^2} \sin(\frac{\pi \cdot n}{2}) \quad \textbf{Eq. 1-22}$$

which means it causes a power loss in the inductor series resistance of

$$P_{LOUT,IDLE} = \frac{1}{2} I_{RIP,P}^2 \sum_{n=1}^{\infty} b_n^2 \cdot R_{LOUT}(n \cdot fs) \qquad b_n = \frac{8}{(\pi \cdot n)^2} \sin(\frac{\pi \cdot n}{2}) \quad \textbf{Eq. 1-23}$$

Where $R_{LOUT}(f)$ is the parasitic series resistance of the inductor at frequency f. Since b_n^2 decreases as n^{-4}, the sum in Eq. 1-23 converges quickly even though $R_{LOUT}(f)$ increases somewhat with frequency. While the impact of skin effect on $R_{LOUT}(f)$ is easily described theoretically, the impact of proximity effect (current in neighbor windings) is not, so in practice $R_{LOUT}(f)$ is most conveniently measured using an impedance analyzer. Depending on inductor design, $R_{LOUT}(f)$ can reach several Ω at frequencies of fs and above, and thus easily becomes larger than $R_{DS(ON)}$ of the output transistors. This means that conduction losses at idle will generally be concentrated in the output inductor, and depending on output stage design, this loss can be larger than the switching losses, and thus dominate idle losses overall.

Finally, as shown in Figure 1-5, I_{HS} also flows in the V_{DD} supply, where in practice the high frequency components flow only in the closest decoupling capacitor. This also causes a power loss, but like the loss in the output capacitor, this should not contribute significantly to overall losses.

1.3 Switching power losses, ideal power supply model

This section analyzes transient losses in the output FETs during switching transitions. The losses are most conveniently expressed in I_{OUT} at the time of the transition, but can be expressed in other variables using the equations from section 1.1.

1.3.1 Circuit simplifications

Initially, the analysis of switching losses is based on the circuit shown in Figure 1-7.

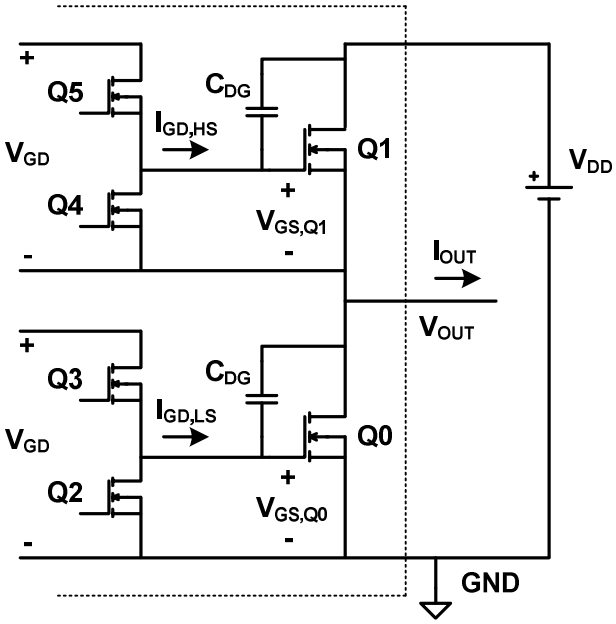


Figure 1-7: Circuit for switching loss analysis

- High-side / low-side symmetry is assumed, i.e. Q0=Q1, Q2=Q4 and Q3=Q5.
- Bulk is tied to source on all transistors, meaning that these N-type devices have a body diode which can conduct current in the source to drain direction.
- C_{DG} is the only parasitic capacitor included in the analysis, and its capacitance is considered fixed (voltage dependency ignored). In practice, it is voltage dependent, and the effects of this nonlinearity are discussed qualitatively after the analysis, as is the influence of the other parasitic capacitors in the output transistors.
- The transconductance gm of the output transistors is considered large, so the transistors can conduct an arbitrary current with V_{GS} in the vicinity of Vt. This means the slope of V_{OUT} during switching transitions is bounded by the limits described by Eq. 0-1 and Eq. 0-2.
- Only the losses in the output transistors Q0 and Q1 are considered, since these are the relevant figures for the thermal considerations from which output transistor size is determined (see section 0.3.4)
- I_{OUT} is considered constant during the switching transition. This is a good approximation as long as no other components than the output inductor are connected to the V_{OUT} node (RC snubbers, clamps, etc), since the output inductor will then prevent any significant change in I_{OUT} within the time frame of a switching transition.

1.3.2 Switching transition Scenarios and Phases

Consider a rising edge switching transition in this circuit. Initially the LS GD switches to its OFF state, i.e. Q2 turns on and a discharge of $V_{GS,Q0}$ begins. Assuming large transconductance for Q0, there is no change in V_{OUT} until $V_{GS,Q0}$ reaches the vicinity of Vt, so the Q0 conduction state continues until t_1 in Figure 1-8.

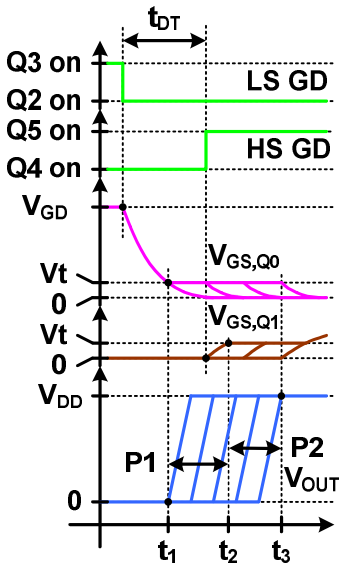


Figure 1-8: Rising edge transition timeline. P1 and P2 indicate time Phases 1 and 2.

t_1: $V_{GS,Q0}$ reaches Vt, and this is the time where the LS GD OFF state can affect the output stage at the earliest. From this point, voltage and current waveforms in the output stage depend on the sign and magnitude of I_{OUT}, and different scenarios occur, depending on whether I_{OUT} is smaller or larger than certain system dependant values. The following power loss analysis will be divided into sections that treat each scenario.

After the dead time interval, the HS GD switches to its ON state (Q5 turns on), and again waveforms depend on scenario, as determined by I_{OUT}. $V_{GS,Q1}$ may or may not reach Vt shortly after the onset of the HS GD ON state.

t_2: is defined as the time where $V_{GS,Q1}$ can reach Vt at the earliest, i.e. the time it takes Q5 to charge $V_{GS,Q1}$ to Vt in the absence of external currents in the $C_{DG,Q1}$ capacitor. This is the time at which the HS GD ON state can affect the output stage at the earliest.

t_3: is defined as the time where HS output FET voltage $V_{DS,Q1}$ reaches 0.

The green traces in Figure 1-8 show when the two gate drivers change their states, but since these changes never affect the output stage before t_1 and t_2 respectively, only t_1 and t_2 appear in the analysis. t_2-t_1 is the duration of time where both $V_{GS,Q1}$ and $V_{GS,Q0}$ would be below Vt in the absence of external currents in the C_{DG} capacitors, and is assumed positive in the analysis.

The loss analysis is divided into two time phases; before and after t_2:

- Time Phase 1 (P1): t_1...t_2, initiated by the LS GD switching to its OFF state prior to t_1.
- Time Phase 2 (P2): t_2...t_3, initiated by the HS GD switching to its ON stage prior to t_2.

For large negative values of I_{OUT}, V_{OUT} may reach V_{DD} already during Phase 1, in which case $t_3 < t_2$ and Phase 2 vanishes.

During each of the two time phases, dV_{OUT}/dt is considered constant, as is V_{GS} of each output transistor Q0 and Q1, which means no current flows in C_{GS}, which is why it is ignored. The phases are thus considered individual dynamic steady states, and the transitions between LS conduction, P1, P2 and HS conduction are ignored. At the cost of accuracy, this approximation allows for analytical expressions simple enough to clearly reveal relations between design parameters and power losses (see section 0.4).

What differentiates the two time phases is that different limits apply to dV_{OUT}/dt. Since $dV_{OUT}/dt = dV_{DS,Q0}/dt$, Eq. 0-1 can be rewritten to

$$\frac{dV_{OUT}}{dt} \le \frac{I_{PD}}{C_{DG}} \qquad \text{rising edge transition, } t > t_1 \text{ (P1 and P2)} \qquad \textbf{Eq. 1-24}$$

and similarly, since $dV_{OUT}/dt = -dV_{DS,Q1}/dt$, Eq. 0-2 can be rewritten to

$$\frac{dV_{OUT}}{dt} \geq \frac{I_{PU}}{C_{DG}} \qquad \text{rising edge transition, } t > t_2 \text{ (P2 only)} \qquad \textbf{Eq. 1-25}$$

In order to fulfill both Eq. 1-24 and Eq. 1-25 during P2, the system must be designed so that

$$I_{PD} \geq I_{PU} \qquad \textbf{Eq. 1-26}$$

which has also been shown earlier [6]. This corresponds to requiring that when Q1 is on, it must not pull V_{OUT} towards V_{DD} at a higher rate than Q0 can tolerate without parasitic turn-on (see section 0.3.2). If not obeyed, simultaneous conduction through the two output transistors will occur, resulting in large power losses.

As mentioned, the sign and magnitude of I_{OUT} influences the output stage waveforms during both time phases, and the analysis is divided into four different scenarios (ranges of I_{OUT}), labeled A thru D as illustrated in Figure 1-9.

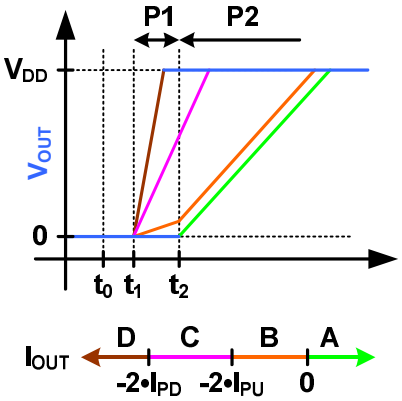


Figure 1-9: Four rising edge transition scenarios A thru D depending on I_{OUT}. Two time phases P1 and P2 determined by the gate driver states as shown in Figure 1-8.

For large negative values of I_{OUT}, Q0 will limit dV_{OUT}/dt of the transition as given by Eq. 1-24, resulting in a power loss in Q0 (scenario D). For positive I_{OUT}, Q1 will drive the transition at the minimum rate given by Eq. 1-25, resulting in a power loss in Q1 (scenario A). In between these two cases are two intermediate steps where the V_{OUT} transition is driven by I_{OUT}, either entirely (scenario C), or aided by Q1 (scenario B). The energy loss functions for each of the four scenarios are found in the analysis below.

In summary, the following analysis is divided into four different scenarios, depending on the value of I_{OUT} at the time of the switching transition, and each scenario is then subdivided into two time phases P1 and P2 determined by the gate driver states.

1.3.3 Scenario A ($0 \leq I_{OUT}$)

Phase 1:

In scenario A ($I_{OUT} \geq 0$), $V_{GS,Q0}$ drops below Vt at t_1, and I_{OUT} continues flowing in source-drain diode of the LS FET during Phase 1, while both output FETs are off (Figure 1-10). The power loss in Q0 during Phase 1 is:

$$E_{SW,AP1} = I_{OUT} \cdot V_F \cdot (t_2 - t_1) \qquad \textbf{Eq. 1-27}$$

where V_F is the forward voltage drop across the diode. This loss is very small compared to other switching losses, where the voltage drops across the FETs are much larger, and it is ignored in the switching loss analysis.

Phase 2:

When the HS GD switches to its ON state, i.e. Q5 turns on and sources a current I_{PU} into the gate of Q1 (Figure 1-11). $V_{GS,Q1}$ increases until Q1 has taken over the flow of I_{OUT} from Q0, at which point V_{OUT} starts to increase. Since the voltage derivatives across the two C_{DG} capacitors are equal and opposite during the transition, they conduct equal currents. The current in Q1 thus becomes $I_{OUT}+2\bullet I_{PU}$, and remains constant while V_{OUT} increases from 0 to V_{DD} at a rate of I_{PU}/C_{DG}. The energy loss in scenario A, Phase 2 can then be found as

$$E_{SW,AP2} = (I_{OUT} + 2\cdot I_{PU})\cdot V_{DS,Q1,AVG}\cdot(t_3 - t_2)$$
$$= (I_{OUT} + 2\cdot I_{PU})\cdot \frac{V_{DD}}{2}\cdot \frac{V_{DD}\cdot C_{DG}}{I_{PU}} \quad \text{for} \quad I_{OUT} \geq 0 \qquad \textbf{Eq. 1-28}$$

Note that for $I_{OUT}=0$, $E_{SW,AP2}$ is independent of I_{PU}, and equals $V_{DD}^2\bullet C_{DG}$, known as the energy loss in a current source charging $2\bullet C_{DG}$ to V_{DD} volts.

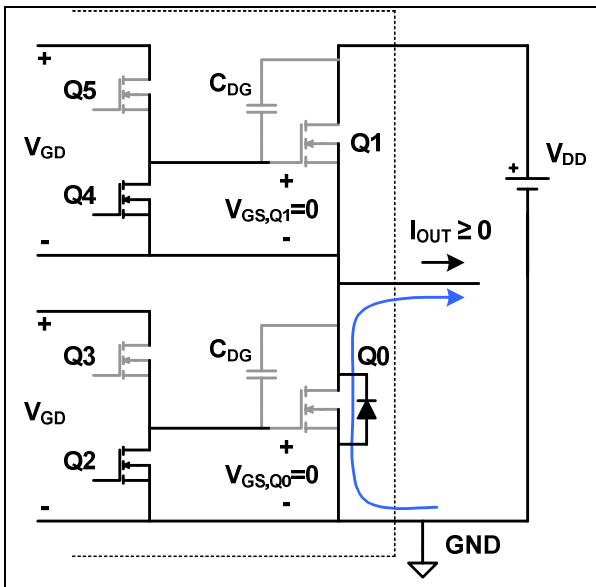


Figure 1-10: Scenario A, Phase 1

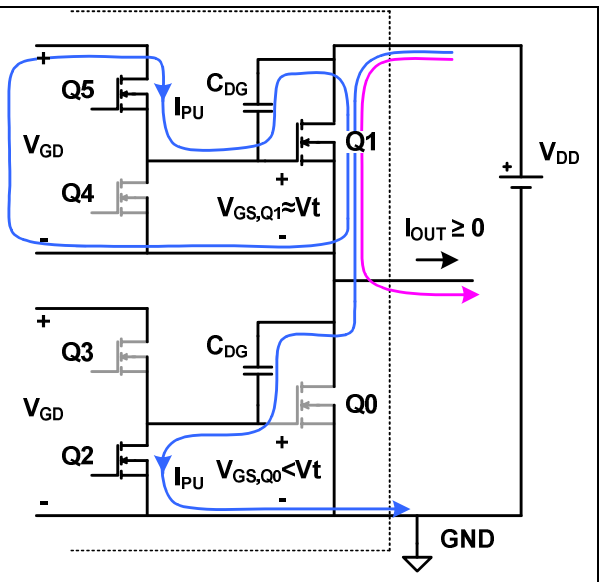


Figure 1-11: Scenario A, Phase 2

1.3.4 Scenario B ($-2\bullet I_{PU} \leq I_{OUT} < 0$)

Phase 1:

When I_{OUT} is negative (i.e. physically flowing into the half bridge), it will charge V_{OUT} towards V_{DD} during Phase 1 (Figure 1-12). The current flows through Q2 and Q4 into the two C_{DG} capacitors, while both output FETs are in the off state. Since the currents in the C_{GD} capacitors must be equal, the current in each path is $I_{OUT}/2$, and causes $V_{GS,Q1}$ to become negative, and $V_{GS,Q0}$ positive. Q0 does not turn on as long as $I_{OUT}/2\bullet R_{DS,Q2(ON)} < Vt$, corresponding to $-2\bullet I_{PD} < I_{OUT}$. Neither output FET then conducts current so Phase 1 is lossless (ignoring losses in the gate driver transistors Q2 and Q4). The output inductor current is merely charging the C_{DG} capacitors, like a small fraction of an LC tank oscillation.

Phase 2:

Phase 2 exists if $V_{DS,Q1}$ has not reached 0 already in Phase 1. Circuit behavior in Phase 2 is identical to scenario A, Phase 2, even though the sign of I_{OUT} has changed. Applying Kirchoff's current law at the V_{OUT} node (Figure 1-13) shows that $I_{D,Q1}$ is $2\bullet I_{PU}+I_{OUT}$, i.e. going to 0 as I_{OUT} goes towards $-2\bullet I_{PU}$, which becomes the limiting current for scenario B.

Note that $-2 \cdot I_{PU} \leq I_{OUT} < 0$ implies $-2 \cdot I_{PD} < I_{OUT} < 0$ (since $I_{PU} < I_{PD}$), so the requirement for avoiding that Q0 turns on is also fulfilled. The current paths in this phase are identical to Scenario A, Phase 2, but the energy loss is smaller due to the fact that V_{OUT} has already reached a positive voltage before the onset of Phase 2 (see Figure 1-9, orange trace). The losses in Phase 2 are found by first finding V_{OUT} at the end of Phase 1:

$$V_{OUT}(t_2) = \frac{-I_{OUT}}{2 \cdot C_{DG}} \cdot (t_2 - t_1) \qquad \text{(up to } V_{DD}\text{)} \qquad \textbf{Eq. 1-29}$$

And the loss is then given by an expression similar to Eq. 1-28:

$$E_{SW,B} = (I_{OUT} + 2 \cdot I_{PU}) \cdot \frac{V_{DD} - V_{OUT}(t_2)}{2} \cdot \frac{V_{DD} \cdot C_{DG}}{I_{PU}} \quad \text{for} \quad -2 \cdot I_{PU} \leq I_{OUT} < 0 \qquad \textbf{Eq. 1-30}$$

The loss depends on $V_{OUT}(t_2)$, which depends on t_2-t_1, and hence on dead time. Larger dead thus time reduces losses in scenario B by increasing $V_{OUT}(t_2)$. The loss vanishes as I_{OUT} approaches $-2 \cdot I_{PU}$, since the current in Q1 reaches 0. It also vanishes if $V_{OUT}(t_2)$ reaches V_{DD}, where the duration of Phase 2 reaches 0. From Eq. 1-29 it is seen that this happens for

$$V_{OUT}(t_2) = V_{DD} \quad \Leftarrow \quad I_{OUT} \leq -\frac{2 \cdot C_{DG} \cdot V_{DD}}{t_2 - t_1} \equiv I_{LIM} \qquad \text{rising edge transition} \qquad \textbf{Eq. 1-31}$$

Since scenario B is confined by $-2 \cdot I_{PU} \leq I_{OUT} < 0$, this requirement can only be fulfilled in systems where $-2 \cdot I_{PU} < I_{LIM}$, since otherwise $I_{OUT} \leq I_{LIM}$ does not occur in scenario B.

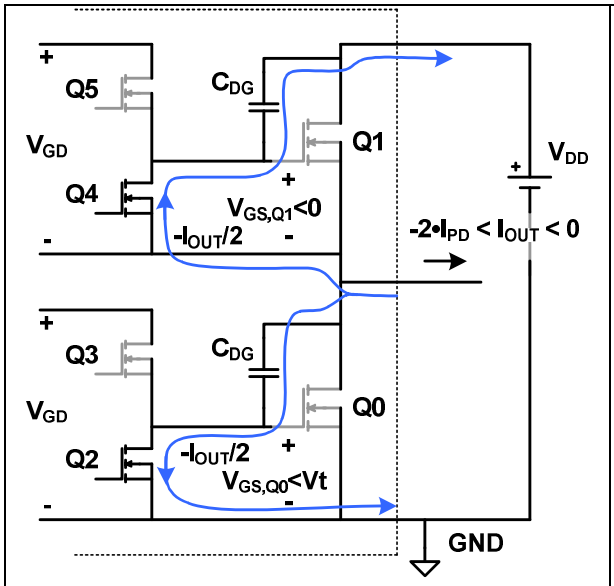


Figure 1-12: Scenario B, Phase 1

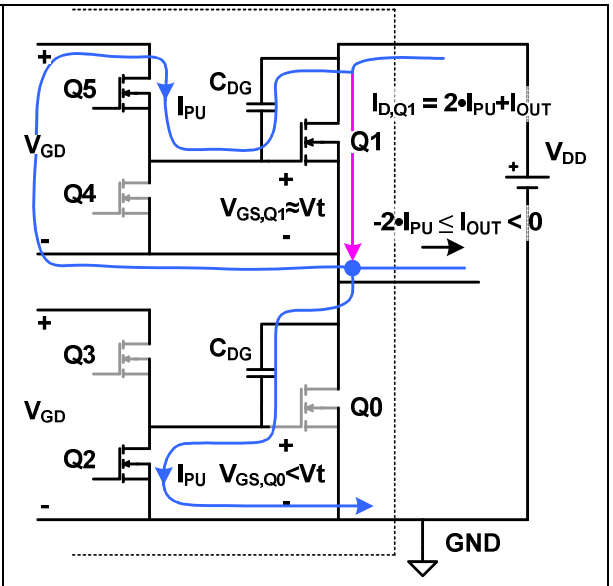


Figure 1-13: Scenario B, Phase 2

1.3.5 Scenario C ($-2 \cdot I_{PD} \leq I_{OUT} < -2 \cdot I_{PU}$)

Phase 1:

Since the analysis of scenario B, Phase 2 required that $-2 \cdot I_{PU} < I_{OUT}$, scenario C starts from $I_{OUT} = -2 \cdot I_{PU}$ and going towards more negative values. However, since the scenario B, Phase 1 analysis was valid for $-2 \cdot I_{PD} \leq I_{OUT} < 0$, it can be reused for $-2 \cdot I_{PD} \leq I_{OUT} < -2 \cdot I_{PU}$, which becomes the interval for scenario C.

Phase 2:

The difference from scenario B is in Phase 2. Since now $I_{OUT} < -2 \cdot I_{PU}$, Q5 will not be able to pull $V_{GS,Q1}$ up to Vt during Phase 2. Even though Q5 in on, $V_{GS,Q1}$ will remain below Vt, so Q1 will remain off until $V_{DS,Q1}$ reaches 0, where the external current in $C_{DG,Q1}$ stops. If I_{OUT} is negative enough, $V_{GS,Q1}$ will become negative, and the source-drain diode of Q4 will conduct part of the HS GD output current. The ON state of the HS GD has no effect on the current in the C_{DG} capacitors, and since both output FETs remain off, the power losses remain zero (ignoring the loss in Q5).

$$E_{SW,C} = 0 \quad \text{for} \quad -2 \cdot I_{PD} \leq I_{OUT} < -2 \cdot I_{PU} \qquad \textbf{Eq. 1-32}$$

Same as scenario B, Phase 1

Figure 1-14: Scenario C, Phase 1

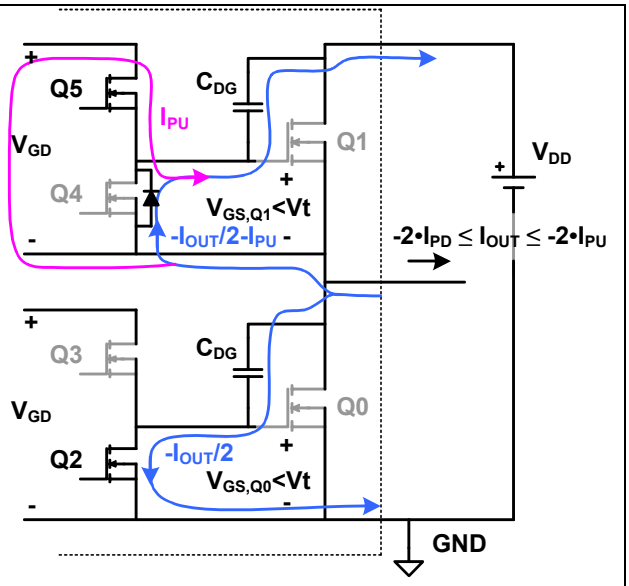


Figure 1-15: Scenario C, Phase 2

1.3.6 Scenario D ($I_{OUT} < -2 \cdot I_{PD}$)

Phase 1:

The final rising edge switching scenario occurs for $I_{OUT} < -2 \cdot I_{PD}$. Based on the analysis of Phase 1 from scenarios B and C, I_{OUT} would split evenly between two paths flowing through Q2 and Q4. However, since the current in each path is then larger than I_{PD}, Q2 can not keep $V_{GS,Q0}$ below Vt and prevent Q0 for turning on, and this is the characteristic of scenario D. When $V_{GS,Q0}$ reaches Vt, Q0 turns on and conducts the amount of current by which $-I_{OUT}$ exceeds $2 \cdot I_{PD}$ (Figure 1-16). Any negative increment of I_{OUT}, will flow in the channel of Q0, while the current in each gate driver is I_{PD}, causing V_{OUT} to increase at a rate of I_{PD}/C_{DG}.

Phase 2:

This phase exists if and only if V_{OUT} has not already reached V_{DD} during Phase 1 (as in the example shown in Figure 1-9). If Phase 2 does exist, part of the HS GD output current will be sourced from Q5, rather than Q4 (see Figure 1-17). However, since Q5 can only source I_{PU}, which is smaller than I_{PD}, $V_{GS,Q1}$ will not reach Vt, and Q1 remains off until $V_{DS,Q1}$ reaches 0, where the current in C_{DG} stops. This means the HS GD does not influence waveforms or power losses, and ignoring losses in the gate drivers, the loss mechanisms in Phase 1 and 2 are identical, and the total loss in Q0 including both phases is given by:

$$E_{SW,D} = \left(-I_{OUT} - 2 \cdot I_{PD}\right) \cdot V_{DS,Q0,AVG} \cdot \left(t_3 - t_1\right)$$
$$= \left(-I_{OUT} - 2 \cdot I_{PD}\right) \cdot \frac{V_{DD}}{2} \cdot \frac{V_{DD} \cdot C_{DG}}{I_{PD}} \quad \text{for} \quad I_{OUT} < -2 \cdot I_{PD} \qquad \textbf{Eq. 1-33}$$

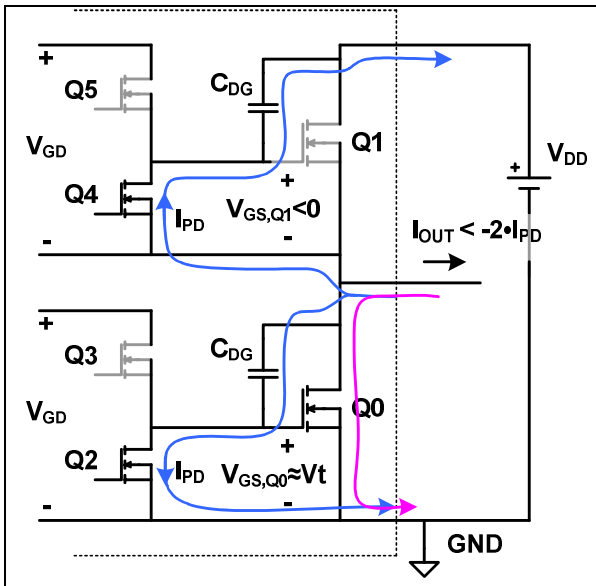


Figure 1-16: Scenario D, Phase 1

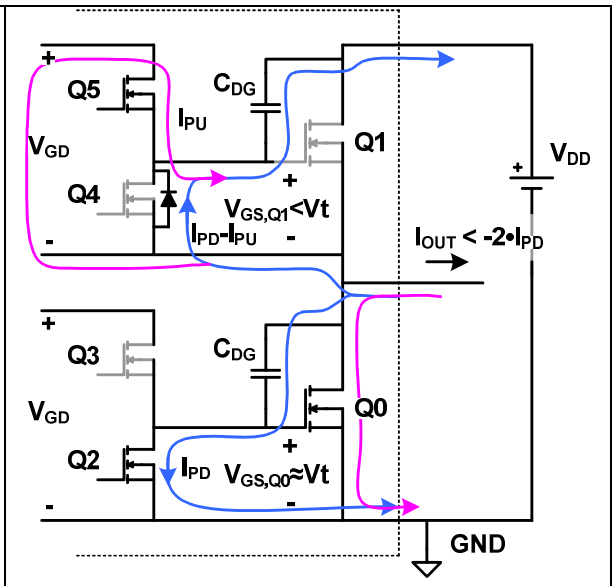


Figure 1-17: Scenario D, Phase 2

1.3.7 Summary of Scenarios ABCD, Rising edge transition

	I_{OUT} *	Time Phase 1	Time Phase 2
A	$0 < I_{OUT}$	Positive I_{OUT} flows in source-drain diode of Q0, and keeps V_{OUT} at GND potential. $dV_{OUT}/dt = 0$, no loss	Q1 forces $V_{DS,Q1}$ towards 0 $dV_{OUT}/dt = I_{PU}/C_{DG}$, loss in Q1
B	$-2 \cdot I_{PU} \leq I_{OUT} \leq 0$	Negative I_{OUT} charges V_{OUT} towards V_{DD}, but is too small to turn on Q0.	If $V_{DS,Q1}$ has not reached 0, Q1 forces it the rest of the way. $dV_{OUT}/dt = I_{PU}/C_{DG}$, loss in Q1
C	$-2 \cdot I_{PD} < I_{OUT} < -2 \cdot I_{PU}$	$dV_{OUT}/dt = I_{OUT}/2 \cdot C_{DG}$, no loss	Q5 is on but Q1 remains off until $V_{DS,Q1}$ reaches 0, i.e. no change from Phase 1: $dV_{OUT}/dt = I_{OUT}/(2 \cdot C_{DG})$, no loss

	I_{OUT} *	Time Phase 1	Time Phase 2
D	$I_{OUT} \leq -2 \bullet I_{PD}$	Negative I_{OUT} charges V_{OUT} towards V_{DD}, and turns on Q0. $dV_{OUT}/dt = I_{PD}/C_{DG}$, loss in Q0	Q5 is on but Q1 remains off until $V_{DS,Q1}$ reaches 0, i.e. no change from Phase 1: $dV_{OUT}/dt = I_{PD}/C_{DG}$, loss in Q0

*) The total power loss is a continuous function of I_{OUT}, so the use of "<" vs. "≤" is arbitrary.

Table 2: Switching loss scenario descriptions

Scenario D and C transitions are called *auto-commutation* transitions because V_{OUT} commutates from GND to V_{DD} automatically, i.e. driven by I_{OUT} rather than by the output transistors.

Scenario A transitions are called *forced-commutation* transitions, since the V_{OUT} change is forced by Q1, acting against the direction of I_{OUT}.

Scenario B transitions fall between these two categories. To be specific, Phase 1 is autocommutation and Phase 2 is forced commutation.

1.3.8 Example losses in Scenarios ABCD, Rising edge transition

During amplifier operation, I_{OUT} varies continually, and the loss energy associated with each rising edge switching transition is then found by evaluating I_{OUT} at the time of the transition, determining the scenario (A,B,C, or D) from its value, and using the appropriate loss equation derived above. The rising edge transition energy loss in an example system is plotted as a function of I_{OUT} in Figure 1-18. Each scenario covers a section of the horizontal axis, D to the left thru A to the right.

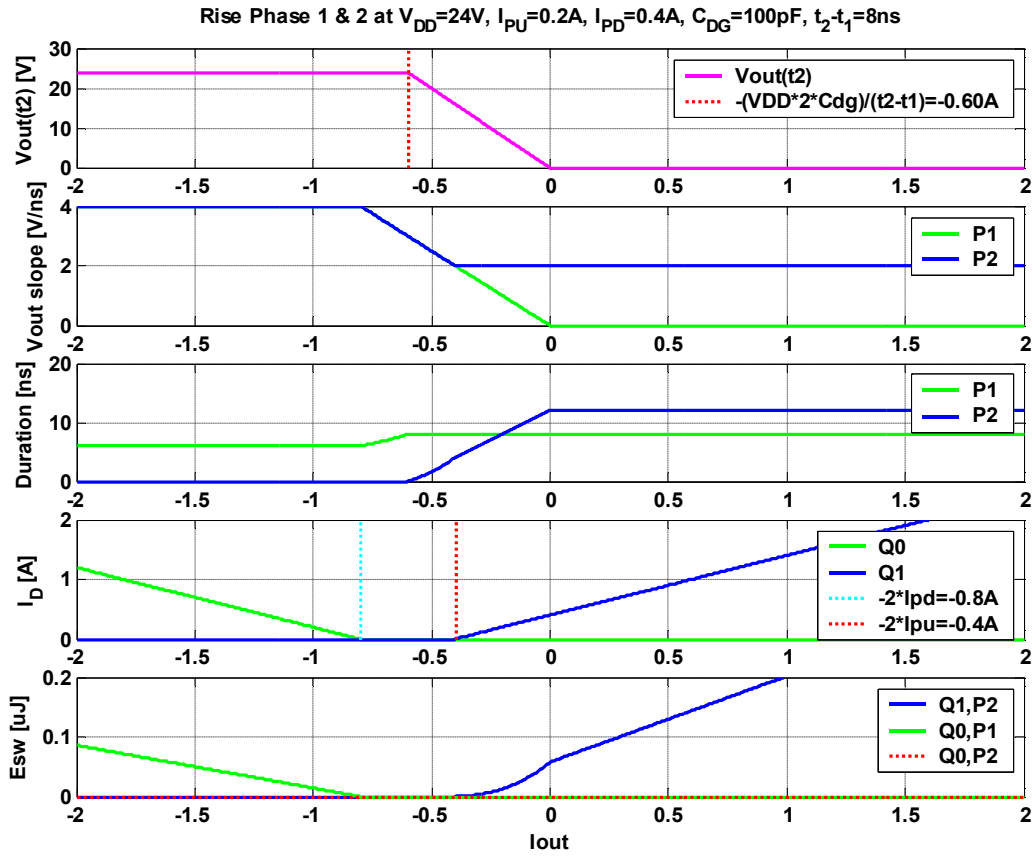


Figure 1-18: Rising edge switching energy loss vs. I_{OUT}. Scenarios D,C,B and A (left to right). $I_{LIM} < -2 \bullet I_{PU}$, so scenario B, Phase 2 always exists and causes a power loss in Q1 in scenario B.

Strip 1 shows V_{OUT} at the end of Phase 1. V_{OUT} reaches V_{DD} before the end of Phase 1 if $dV_{OUT}/dt > 3V/ns$. This happens for $I_{OUT} \leq I_{LIM}$ (-0.6A).

Strip 2 shows dV_{OUT}/dt during phases 1 and 2. The upper limit of 4V/ns (Eq. 1-24) applies in both phases. In Phase 2 the HS GD is in its ON state so Eq. 1-26 applies, causing a minimum of 2V/ns.

Strip 3 shows the duration of each phase. Phase 1 has a maximum duration of t_2-t_1=8ns. However, for $dV_{OUT}/dt > 3V/ns$, it is terminated when V_{OUT} reaches V_{DD}. The minimum duration occurs in scenario D, when dV_{OUT}/dt is at the 4V/ns maximum. Phase 2 exists for $I_{OUT} > I_{LIM}$ (-0.6A), and its duration increases up until I_{OUT}=0, from where it equals the time it takes V_{OUT} to reach V_{DD} at the minimum Phase 2 slope of 2V/ns.

Strip 4 shows the drain current for each device when it is on, whether in Phase 1 or 2. The vertical dotted bars indicate the borders between scenarios D, C and B. Scenario A is to the right of I_{OUT}=0.

Strip 5 shows the switching energy losses for each transistor and phase, as a function of I_{OUT}. In scenario D, $I_{OUT} < -2 \bullet I_{PD}$ (-0.8A), a loss occurs in Q0 during P1. Since P1 duration is fixed, this loss increases linearly towards more negative I_{OUT}.

In scenario B, when I_{OUT} goes from -0.4A towards 0A, the loss in Q1 during P2 increases as the product of 3 effects: The initial drain-source voltage V_{DD}-$V_{OUT}(t_2)$ increases (Strip 1), P2 duration then increases (Strip 3) and Q1 current increases (Strip 4). In scenario A ($I_{OUT} > 0$), only the last effect continues, and the loss increases linearly with current. Note that the

loss increases at a steeper slope towards positive then negative I_{OUT}. This is always the case, as a consequence of Eq. 1-26.

As shown in section 1.3.4, the switching loss in scenario B depends on $V_{OUT}(t_2)$, and becomes zero for $I_{OUT} \leq I_{LIM}$ (see Eq. 1-31). However, this is not possible in this system since $I_{LIM} < -2 \bullet I_{PU}$, so $I_{OUT} \leq I_{LIM}$ does not occur in scenario B, but in C and D. Losses in scenarios C and D are independent of $V_{OUT}(t_2)$, so in this system the power losses are not affected in any way by whether I_{OUT} is smaller than I_{LIM} or not.

If dead time in increased, t_2-t_1 increases by the same amount and I_{LIM} becomes less negative (see Eq. 1-31). Figure 1-19 shows the same analysis on the same system, except t_2-t_1 has been increased, changing I_{LIM} to -0.3A.

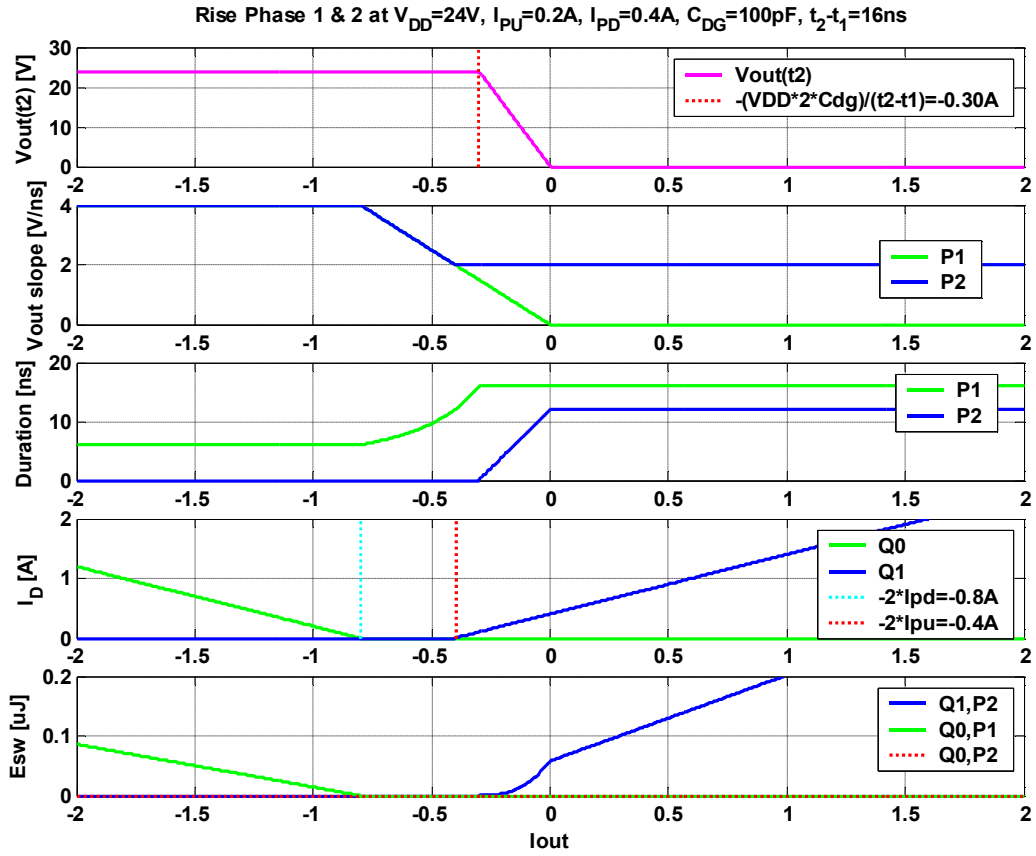


Figure 1-19: Rising edge switching energy loss vs. I_{OUT}. Scenarios D,C,B and A (left to right). $-2 \bullet I_{PU} < I_{LIM}$, and Phase 2 vanishes for $I_{OUT} < I_{LIM}$ in scenario B.

Strip 1 shows that $V_{OUT}(t_2)$ now reaches V_{DD} in scenario B, causing Phase 2 to vanish (Strip 3), which in turn causes lossless scenario B transitions for $-2 \bullet I_{PU} < I_{OUT} < I_{LIM}$ (-0.3A) (Strip 5). scenario C is always lossless, so the total I_{OUT} interval for lossless transitions has expanded from [-0.8...-0.4]A, to [-0.8...-0.3]A (see section 1.3.4).

1.3.9 Influence of transistor sizes

The size of the output transistors Q0 and Q1 only influence switching losses through the value of C_{DG}. For a given gate driver, larger C_{DG} causes slower switching, which increases losses as shown in Figure 1-20. scenario D and A losses are proportional to C_{DG}. Note that the lossless interval remains unchanged.

Figure 1-21 shows the effects of reducing the size of the gate driver pull-up transistors Q3 and Q5. The result is increased losses for $I_{OUT} > 0$ as given by Eq. 1-28. It also widens the lossless interval (scenario C).

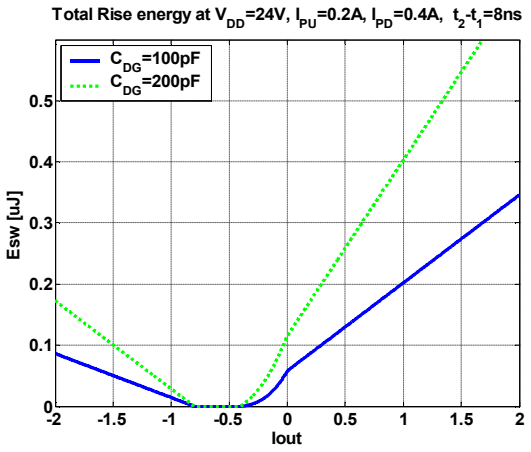


Figure 1-20: Effects of changing output transistor size

Similarly, the effects of reducing the size of the gate driver pull-down transistors Q2 and Q4 are shown in Figure 1-22. The lossless interval narrows, and scenario D losses increase as given by Eq. 1-33.

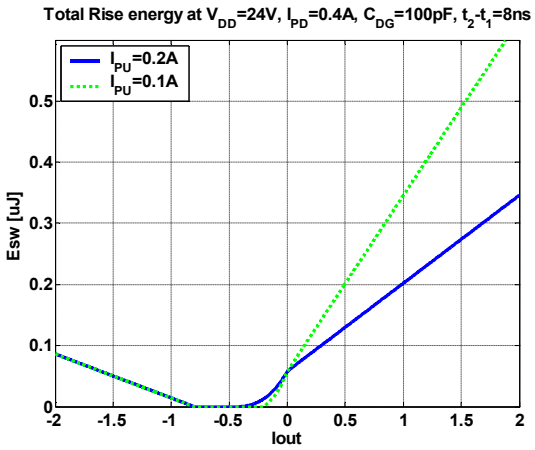


Figure 1-21: Effects of changing gate drive pull-up transistor size

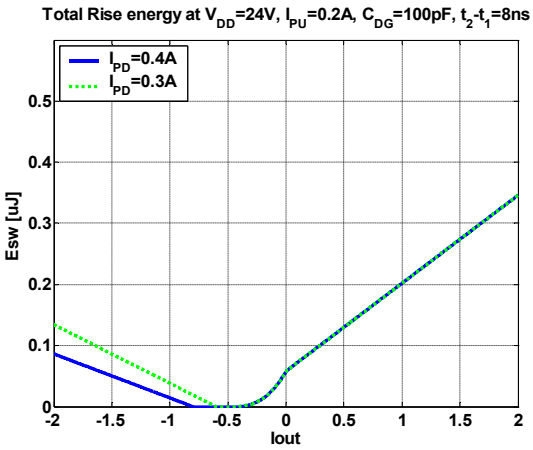


Figure 1-22: Effects of changing gate drive pull-down transistor size

1.3.10 Falling edge transitions

The above analysis discusses only rising edge switching transitions, but can be applied to falling edge transitions also. Considering each output switch including its gate driver as a self-contained floating switch circuit, the output stage can be represented as shown in Figure 1-23 A, with V_{OUT} going from GND to V_{DD} during a rising edge transition. Now, since the HS switch circuit is connected in series with the V_{DD} voltage source, their order can be switched without affecting power losses in the circuit. Further, since there is only one GND connection, and power losses are independent of absolute potentials, the GND connection can be moved, resulting in the reorganized circuit shown in Figure 1-23 B. Note that when the LS switch turns OFF and the HS switch turns ON (causing a rising edge V_{OUT} transition in circuit A), it will cause the bottom node in circuit B to switch from V_{DD} to GND. Figure 1-23 C is obtained by simply redrawing circuit B without change.

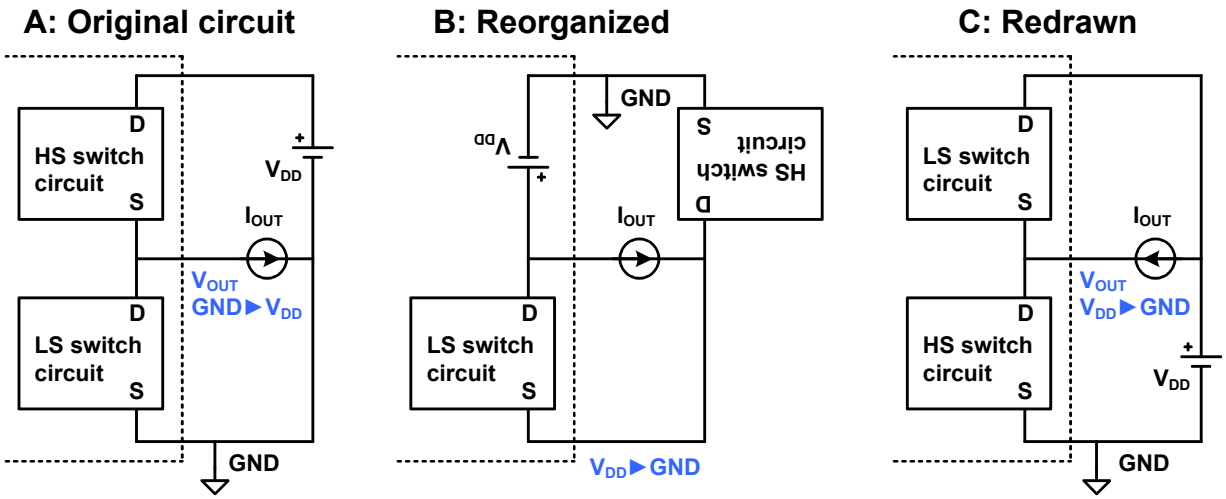


Figure 1-23: Reorganization of rising-edge circuit to falling-edge circuit with reversed I_{OUT} direction.

Since the switch circuits are assumed identical, and power losses in the switches are unaffected by which side of the V_{DD} source the I_{OUT} source connects to, the following relation is shown:

$$E_{SW,FALL}(I_{OUT}) = E_{SW,RISE}(-I_{OUT}) \qquad \text{Eq. 1-34}$$

Consequently, the analysis of rising edge switching losses applies to falling edge switching losses as well, if only the sign of I_{OUT} is reversed.

Falling edge transitions with $I_{OUT}<0$ and rising edge transitions with $I_{OUT}>0$ are forced commutation transitions. Falling edge transitions with $I_{OUT} > 2 \bullet I_{PU}$ and rising edge transitions with $I_{OUT} < -2 \bullet I_{PU}$ are autocommutation transitions.

1.3.11 Minimizing losses at idle

As described in section 1.1.4 the power loss in idle operation is particularly important for some designs. At idle, I_{OUT} has the value $-I_{RIP,P,IDLE}$ (Eq. 1-2) at every rising edge transition, and $I_{RIP,P,IDLE}$ at every falling edge transition. Using Eq. 1-34, the losses in rising- and falling edge transitions are then equal. Figure 1-24 shows the total idle switching loss per PWM period (both transitions) plus the output transistor conduction loss (assuming $R_{DS(ON)}$=80mΩ), vs. the amplitude of the triangular ripple current. Minimum idle losses are achieved for $-I_{RIP,P,IDLE}$=-0.4A, which equals $-2 \bullet I_{PU}$. This value of ripple current amplitude would result in minimum power losses in a given system, but since ripple current is system dependent and often predetermined by other

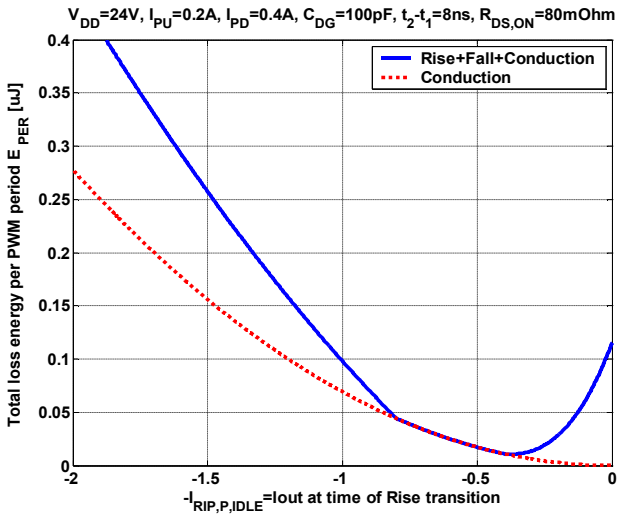


Figure 1-24: Idle power loss vs. Ripple current amplitude

considerations (see section 0.3.5), minimum losses for a given ripple current are typically achieved by selecting I_{PU} and I_{PD} to fulfill:

$$I_{PU} < \frac{V_{DD}}{16 \cdot L_{OUT} \cdot fs} < I_{PD} \quad \text{for minimum idle power losses} \qquad \textbf{Eq. 1-35}$$

(using Eq. 1-2) which ensures that switching losses are zero at idle, and only conduction losses occur.

1.3.12 Influence of output transistor C_{DS} capacitance

The drain-source capacitance of the output transistors has been ignored in the above analysis, and its effect is analyzed here. In the dynamic steady state (see section 1.3.1) V_{GS} is constant, so $dV_{DG}/dt = dV_{DS}/dt$, and the gate driver output current I_{GD} is always accompanied by $C_{DS}/C_{DG} \bullet I_{GD}$ flowing in C_{DS}, as shown in Figure 1-25 A. Note that the limits for V_{OUT} slope given by are Eq. 0-1 and Eq. 0-2 are unchanged. Adding C_{DS} and observing the entire switch circuit from the outside, it is indistinguishable from the one in Figure 1-25 B during the dynamic steady state. The C_{DS} current now flows in the gate driver, but when transistors Q2 and Q3 are increased in size by a factor of kc (defined in Figure 1-25 B), V_{GS} of the output transistor remains unchanged under all conditions, compared to circuit A.

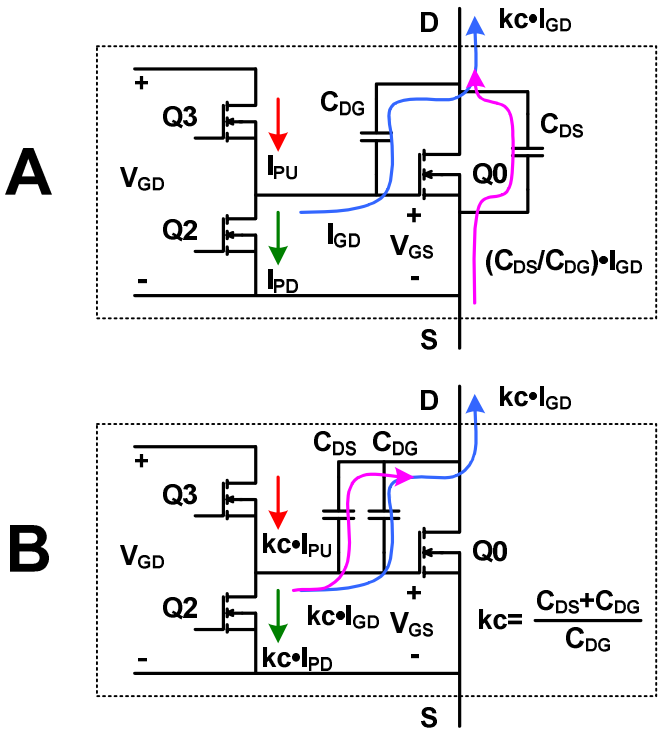


Figure 1-25: C_{DS} current path

This leads to the observation that adding C_{DS} capacitances to the power loss analysis has exactly the same effect as increasing C_{DG} by C_{DS} while scaling the gate driver transistors by a factor of kc. The switching power losses in the physical circuit in Figure 1-25 A can thus be found by applying equations Eq. 1-28 thru Eq. 1-33 to the equivalent circuit in Figure 1-25 B. This results in the following set of loss equations:

	Iout *	**Rising edge transition energy loss, accounting for C_{DS}**
A	$0 < I_{OUT}$	$E_{SW,A} = (I_{OUT} + 2 \cdot kc \cdot I_{PU}) \cdot \frac{V_{DD}}{2} \cdot \frac{V_{DD} \cdot C_{DG}}{I_{PU}}$
B	$-2 \bullet kc \bullet I_{PU} \le I_{OUT} \le 0$	$E_{SW,B} = (I_{OUT} + 2 \cdot kc \cdot I_{PU}) \cdot \frac{V_{DD} - V_{OUT}(t_2)}{2} \cdot \frac{V_{DD} \cdot C_{DG}}{I_{PU}}$
C	$-2 \bullet kc \bullet I_{PD} \le I_{OUT} < -2 \bullet kc \bullet I_{PU}$	$E_{SW,C} = 0$

	Iout *	Rising edge transition energy loss, accounting for C_{DS}
D	$I_{OUT} < -2 \bullet kc \bullet I_{PD}$	$E_{SW,D} = \left(-I_{OUT} - 2 \cdot kc \cdot I_{PD}\right) \cdot \frac{V_{DD}}{2} \cdot \frac{V_{DD} \cdot C_{DG}}{I_{PD}}$

*) The total power loss is a continuous function of I_{OUT}, so the use of "<" vs. "≤" is arbitrary.

Table 3: Switching losses, accounting for C_{DS}

Where $V_{OUT}(t_2)$ is now given by

$$V_{OUT}(t_2) = \frac{-I_{OUT}}{2 \cdot kc \cdot C_{DG}} \cdot (t_2 - t_1) \qquad \text{(up to } V_{DD}\text{)} \qquad \textbf{Eq. 1-36}$$

Note that for C_{DS}=0, kc is 1, and the equations take their original form.

The influence of C_{DS} on switching power losses is shown in Figure 1-26. With the addition of C_{DS}=100pF kc equals 2. The losses in scenario D decrease because the drain current in Q0 decreases, and similarly the losses scenario A increase because Q1 drain current increases (see Table 3).

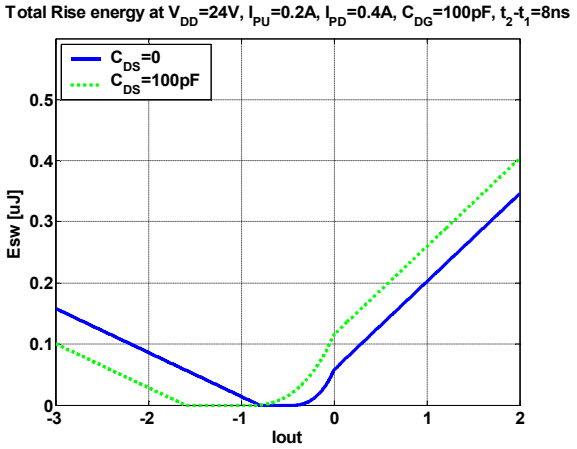


Figure 1-26: Influence of C_{DS} on switching power loss.

It should be noted that simply adding an external capacitor C_{OUT} from the V_{OUT} node to GND has the same effect as increasing C_{DS} by $C_{OUT}/2$, and this can be particularly useful for reducing idle loss in small output stages where I_{PU} is too small to satisfy Eq. 1-35. Adding output capacitance moves the lossless scenario C towards more negative I_{OUT} values. This technique is similar to resonance tuning in zero-voltage-switching power converters, but it should be noted that dead time is not required to be larger than the duration of the switching transitions, since scenario C is lossless for any positive t_2-t_1 (see Figure 1-9).

When the chip substrate is connected to GND, the bulk-substrate capacitance of the HS FET will effectively connect from V_{OUT} to GND, and thus have the same influence as C_{OUT}, except for the substrate resistance.

1.3.13 Gate driver power losses

Power losses in the gate driver transistors Q2..Q5 occur only during switching transitions, since the gate current for the output transistors is zero during the high and low conduction states. The losses during switching transitions depend on I_{OUT}, and can be found using a similar approach as used for output transistor losses (section 1.3.3 and on). When this is done for rising edge transitions, the results also apply to falling edge transitions as described in section 1.3.10.

The losses in the gate drivers are generally smaller than the output transistor losses, and not a dominant contributor to overall device losses. Only an analysis of the maximum possible gate driver losses will be given here, since this is sufficient to find the required power handling for the gate driver transistors Q2..Q5.

During the entire rising edge switching transition, Q2 discharges $V_{GS,Q0}$ to 0. Depending on I_{OUT}, the last part of the discharge from Vt to 0 may occur after the switching transition, but either way, the total loss in Q2 is:

$$E_{Q2,discharge} = \frac{1}{2} V_{GD}^2 \cdot (C_{DG} + C_{GS}) \quad \text{any } I_{OUT} \qquad \textbf{Eq. 1-37}$$

While V_{OUT} increases from GND to V_{DD}, whether driven by negative I_{OUT} or Q1 turning on, $C_{DG,Q0}$ will be charged to V_{DD}, and its charge flows through Q2. This also causes a loss in Q2 which increases with C_{DG} current. Since $V_{DS,Q0}$ is limited to Vt (scenario D), the maximum possible Q2 loss during this period is:

$$E_{Q2,transition} = V_{DD} \cdot C_{DG} \cdot Vt \quad \text{maximum value, occurs for } I_{OUT} < -2 \cdot I_{PD} \qquad \textbf{Eq. 1-38}$$

During the transition, $C_{DG,Q1}$ discharges and its charge flows in the HS gate driver, while either Q4 or Q5 is on. Since the HS gate driver output voltage $V_{GS,Q1}$ is at most Vt during the transition and $Vt << V_{GD}$, the loss in the driver is larger if the C_{DG} charge flows through Q5 than Q4. This means worst case HS gate driver losses occur in scenario A, where Q5 delivers the total C_{DG} charge, causing a loss of:

$$E_{Q5,transition} = V_{DD} \cdot C_{DG} \cdot (V_{GD} - Vt) \quad \text{maximum value, occurs for } I_{OUT} > 0 \qquad \textbf{Eq. 1-39}$$

During the entire rising edge switching transition, Q5 charges $V_{GS,Q1}$ to V_{GD}. Depending on I_{OUT}, the first part of the discharge from 0 to Vt may occur before the switching transition, but either way, the total loss in Q5 is:

$$E_{Q5,charge} = \frac{1}{2} \cdot V_{GD}^2 \cdot (C_{DG} + C_{GS}) \quad \text{any } I_{OUT} \qquad \textbf{Eq. 1-40}$$

Adding the four loss equations sets an upper limit for the total loss in Q2 and Q5 for a rising edge transition:

$$E_{SW,GD} < V_{GD}^2 \cdot (C_{DG} + C_{GS}) + V_{GD} \cdot V_{DD} \cdot C_{DG} \quad \text{any } I_{OUT} \qquad \textbf{Eq. 1-41}$$

This result also applies to falling edge transitions, where the loss occurs in Q4 and Q3. It is pessimistic since conditions for Eq. 1-38 and Eq. 1-39 cannot be fulfilled simultaneously.

For the example system with output transistor switching losses shown in Figure 1-26, with C_{GS}=200pF and V_{GD}=11V, Eq. 1-41 amounts to 63nJ, and the gate driver loss can possibly exceed the output transistor losses for a certain range of I_{OUT}. Since this upper limit applies for any value of I_{OUT}, the output transistor losses will always dominate at large output currents, especially when adding the conduction loss. At idle, in a loss optimized system, the output transistors only have conduction loss, and gate driver losses can dominate on-chip losses (compare to Figure 1-24).

Comparing Eq. 1-38 to Eq. 1-39 shows that the gate driver pull-up transistors Q5 and Q3 have larger power losses than the pull-down transistors Q4 and Q2. At the same time, the pull-up transistors must be smaller than the pull down transistors, in order to fulfill Eq. 1-26 despite the larger drain-source voltage across the pull-ups. Consequently, the largest average power density in the gate drivers occur in the pull-up transistors Q5 and Q3.

Note that since the worst case power dissipation in the gate drivers (Eq. 1-41) depends only on the size of the output transistors, a reduction in gate driver transistor size will increase its power density.

1.4 Switching losses, inductive power supply model

Any output stage half bridge has parasitic inductances caused mainly by package pins, bond wires and PCB traces. These have been ignored in the switching power loss analysis above, but their influence on losses will be discussed here. A full set of power loss equations will not be derived due to complexity, but a few expressions which show the basic influence of parasitic inductance are shown.

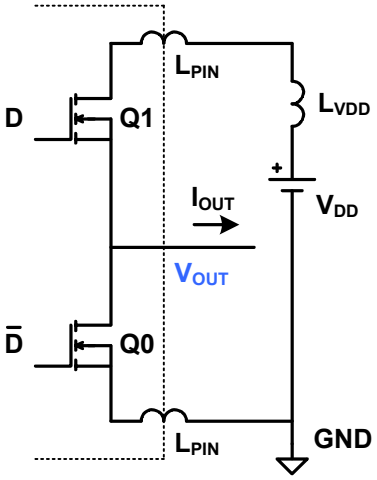


Figure 1-27: Parasitic inductances in a half bridge

The major parasitic inductances in a half bridge circuit are shown in Figure 1-27. L_{PIN} is the total inductance of pins and bond wires (possibly more in parallel) for each package terminal. On the output pin inductance is ignored because the output inductor, which is many orders of magnitude larger, will prevent any significant voltage drop across it. L_{VDD} is the inductance of the V_{DD} supply rail, as seen from the chip pins, which in practice is determined mostly by the ESL of the innermost decoupling capacitor. The inductance between Q0 and Q1 is also ignored, since the physical distance is very small in monolithic solutions.

Considering each switch with its gate driver as a floating circuit, the power losses in the output stage will not depend on the selection of GND node (see section 1.3.10), and the circuit can be redrawn as shown in Figure 1-28, where all parasitic inductance is lumped in to one component L, representing the total inductance of the loop going from GND, through the V_{DD} supply, the V_{DD} package pin, Q1, Q0, out through the GND package pin and back to GND.

Note that since the currents in and out of the HS switch circuit (including gate driver) must be equal, we have

$$I_{D,Q0} = I_{VDD} - I_{OUT} \qquad \text{Eq. 1-42}$$

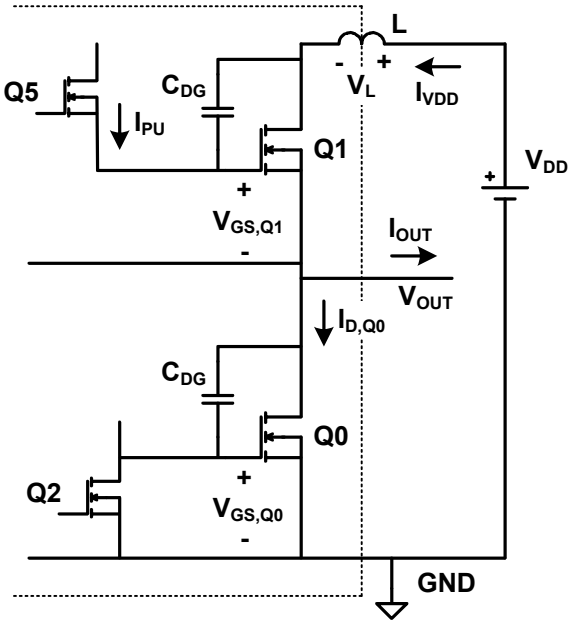


Figure 1-28: Circuit for power loss analysis with parasitic inductance

1.4.1 Forced commutation transition

Consider a rising edge switching transition for $I_{OUT}>0$: Initially Q2 turns on and discharges $V_{GS,Q0}$ below Vt. V_{OUT} stays at GND potential (ignoring the forward voltage drop of the Q0

source-drain diode), because I_{OUT} is positive. Up until t_2, circuit behavior is similar to scenario A for the ideal power supply model (see section 1.3.3). The difference occurs from t_2 because I_{VDD} cannot increase instantaneously. When Phase 2 starts at t_2, Q5 charges $C_{DG,Q1}$ and forces $V_{DS,Q1}$ to decrease at a rate of

$$\frac{dV_{DS,Q1}}{dt} = -\frac{I_{PU}}{C_{DG}} \qquad \begin{cases} t > t_2 \\ V_{DS,Q1} > 0 \end{cases} \qquad \textbf{Eq. 1-43}$$

(see Figure 1-29). This is similar to Eq. 0-2, where equality applies because I_{OUT} is positive.

Since V_{OUT} is at GND, Eq. 1-43 causes a linear increase in V_L, which in turn causes I_{VDD} to increase from 0 as time squared. V_{OUT} stays at GND potential as long as $I_{D,Q0}$ is negative, i.e. until I_{VDD} reaches I_{OUT} at t_{2a}.

At t_{2a}, $I_{D,Q0}$ intersects 0 and becomes positive, causing V_{OUT} to start increasing. $V_{DS,Q1}$ continues to decrease, resulting in a linear increase in voltage, now across the series connection of L and $C_{DG,Q0}$. The circuit thus responds as a series LC branch driven by a ramp voltage, with the initial conditions $V_{CDG,Q0}$=0 and I_{VDD}=I_{OUT} at time t_{2a}. The waveforms are then governed by the following equation for $I_{D,Q0}(t)$, derived in Appendix I.

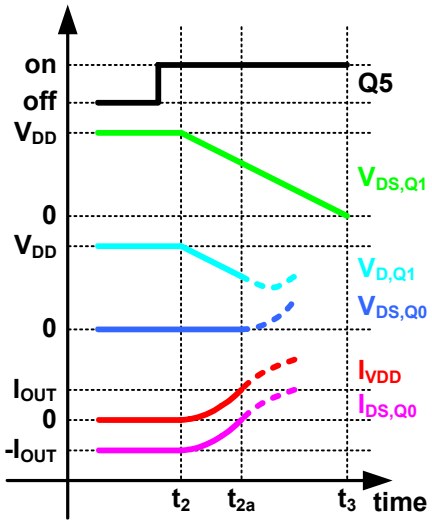


Figure 1-29: Rising edge transition waveforms, inductive model

$$I_{D,Q0}(t) = \sqrt{2 \cdot I_{PU} \cdot I_{OUT}} \cdot \sin(\omega(t - t_{2a})) - I_{PU} \cdot \cos(\omega(t - t_{2a})) + I_{PU}, \begin{cases} t_{2a} < t < t_3 \\ I_{D,Q0} < I_{PD} \\ I_{OUT} > 0 \end{cases} \qquad \textbf{Eq. 1-44}$$

This solution is only valid as long as the ramp source is active, i.e. until $V_{DS,Q1}$ reaches 0 at t_3. Further, it is only valid if Q0 does not turn on, i.e. as long as $I_{D,Q0} < I_{PD}$, causing the LS switch circuit to behave simply as a capacitance being charged by $I_{D,Q0}$.

The solution for I_{OUT}=2A is shown in Figure 1-30, and is to be inserted in Figure 1-29 from t_{2a} to t_3. The LC oscillations are sustained because damping is ignored in the solution in Eq. 1-44. In practice, they decay because of damping e.g. from the channel resistance of Q2. The most important observation in this solution is the large peak value of $I_{D,Q0}$, reaching 1.12A. This behavior is inherent to the presence of inductance in the system. A voltage drop V_L is required for I_{VDD} to reach I_{OUT}, and when it does so at t_{2a}, this voltage cannot disappear instantaneously, since L is in a series loop with capacitors and voltage sources. Consequently, I_{VDD} continues to increase above I_{OUT}, and the excess current flows in Q0 (see Eq. 1-42). To avoid that $V_{GS,Q0}$ exceeds Vt, turning on Q0, I_{PD} must be larger than the peak $I_{D,Q0}$ current. This value is derived in Appendix I, and is

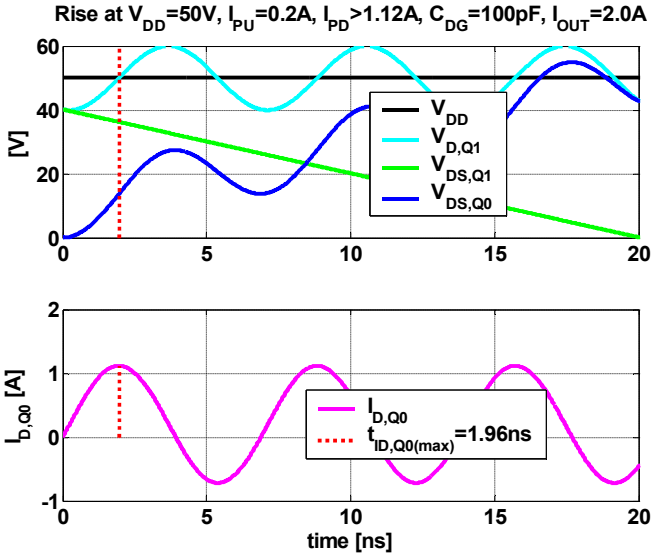


Figure 1-30: Solution to Eq. 1-44 for L=12nH at I_{OUT}=2A, assuming that I_{PD} is larger than $I_{D,Q0(max)}$, which is much larger than I_{PU}. Oscillation is sustained because Eq. 1-44 ignores damping.

$$I_{D,Q0,max} = \sqrt{2 \cdot I_{PU} \cdot I_{OUT} + I_{PU}^2} + I_{PU} \quad \text{for} \quad \begin{cases} t_{2a} < t < t_3 \\ I_{OUT} > 0 \end{cases} \qquad \textbf{Eq. 1-45}$$

Comparing to Eq. 1-26, which was the similar requirement when parasitic inductance was ignored, this requirement is much more severe, with a minimum value of 2•I_{PU}, and increasing further with positive I_{OUT}. Note that Eq. 1-45 is independent of L, so the requirement is the same for any amount of parasitic inductance, and thus applies to any actual half bridge circuit.

If an external capacitor is added from V_{OUT} to GND, it will conduct a given fraction of $I_{D,Q0}$, and thus correspond to an increasing I_{PD} by the kc factor as described in section 1.3.12.

For the limiting case of I_{OUT}=0, the time segment t_{2a}-t_2 in Figure 1-29 vanishes, and the solution given by Eq. 1-44 applies immediately when Phase 2 starts at t_2. This solution is shown in Figure 1-31. Note that $V_{D,Q1}$ now starts at V_{DD}, and the peak value of $I_{D,Q0}$ is exactly 2•I_{PU}.

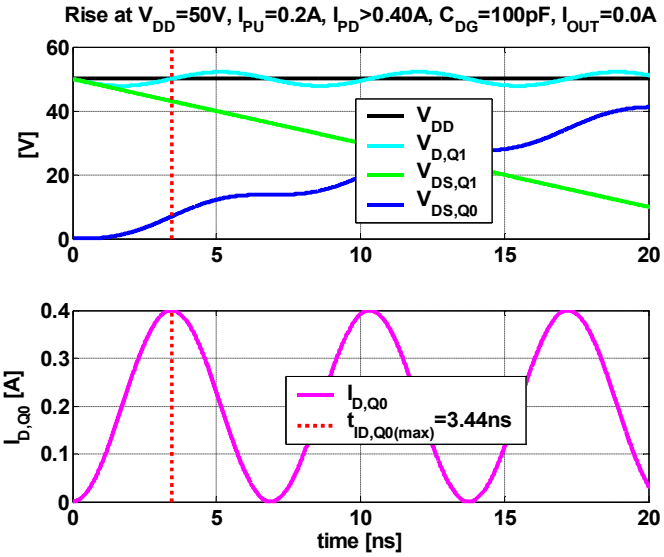


Figure 1-31: Solution to Eq. 1-44 for L=12nH at I_{OUT}=0A, where $I_{D,Q0(max)}$ assumes its minimum of 2•I_{PU}. Oscillation is sustained because Eq. 1-44 ignores damping.

There is a theoretical possibility that the peak value of $I_{D,Q0}$ could be avoided, since if $V_{DS,Q1}$ reached 0 before the peak occurred, i.e. $t_3 < t_{ID,Q0(max)}$, it would never occur. It can be shown that $t_{ID,Q0(max)}$ reaches its maximum value for I_{OUT}=0, where it equals half an oscillation period for L and C_{DG} (see Appendix I). The peak thus never occurs later than illustrated in Figure 1-31, and for realistic circuit parameters this will be before t_3.

In conclusion, it is observed that:

When any amount of power supply inductance is included in the analysis, the gate driver pull-down current I_{PD} needed to avoid simultaneous conduction in the output transistors Q0 and Q1 is at least 2•I_{PU}, and increases further with positive I_{OUT}. For large positive I_{OUT}, simultaneous conduction is unavoidable.

The damping of the LC oscillation has been disregarded in this analysis, but this does not affect the peak $I_{D,Q0}$ current significantly, since the peak occurs after a half oscillation period at the latest.

For large I_{OUT}, where $I_{D,Q0(max)}$ exceeds I_{PD}, there will be a power loss in Q0 during a rising edge transition. The stages of such a transition are shown in Figure 1-32, referring to the circuit in Figure 1-28.

t2: Phase 2 starts and $V_{DS,Q1}$ decreases as given by Eq. 1-43. $I_{D,Q0}$ equals $-I_{OUT}$ at t_2, and $V_{DS,Q0}$ (equal to V_{OUT}) stays at GND potential as long as $I_{D,Q0}$ is negative.

t2a: $I_{D,Q0}$ reaches 0 and changes sign, causing $V_{DS,Q0}$ to start increasing. As long as $I_{D,Q0}$ is less than I_{PD}, Q0 simply acts like a capacitor being charged. $I_{D,Q0}$ is given by Eq. 1-44.

t2b: $I_{D,Q0}$ reaches I_{PD}, and Q0 enters the active region. Eq. 1-44 no longer applies, and instead $dV_{DS,Q0}/dt=I_{PD}/C_{DG}$ applies since the current in $C_{DG,Q0}$ equals I_{PD}. The remainder $I_{D,Q0}$-I_{PD} flows in the Q0 channel, causing a power loss. $dV_{D,Q1}/dt$ equals $(I_{PD}-I_{PU})/C_{DG}$, and since $I_{PD}>I_{PU}$, $V_{D,Q1}$ increases in this time segment, continuing as long as $V_{DS,Q1}>0$

t3: $V_{DS,Q1}$ reaches 0, i.e. $V_{D,Q1}=V_{DS,Q0}$. This may happen before or after $V_{D,Q1}$ has reached V_{DD}. $I_{D,Q0}$ peaks when $V_{D,Q1}$ intercepts V_{DD}, and then starts decreasing as V_L becomes negative.

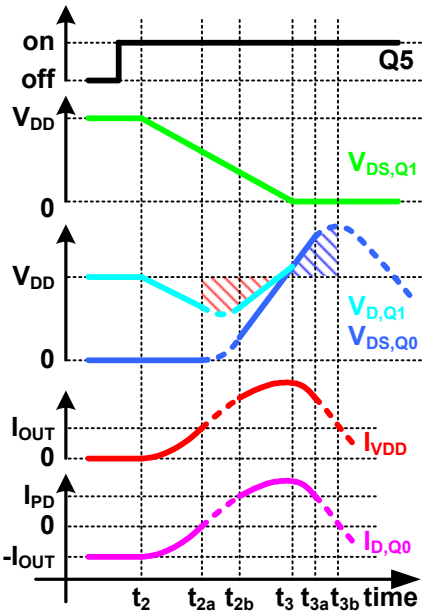


Figure 1-32: Forced commutation transition where $I_{D,Q0(max)} > I_{PD}$. Dashed curve segments are governed by Eq. 1-44. Power loss occurs in Q1 from t_2 to t_3, and in Q0 from t_{2b} to t_{3a}.

t3a: $I_{D,Q0}$ has decreased to I_{PD}, so Q0 leaves the active region and once again acts like a capacitor. Since $I_{D,Q0}$ is still positive, $V_{D,Q1}$ ($=V_{DS,Q0}$) still increases. $I_{D,Q0}$ is now controlled by the homogenous part of Eq. 1-44 (since $V_{DS,Q1}$ is 0), and from this point the waveforms oscillate, $V_{D,Q1}$ around V_{DD}, I_{VDD} around I_{OUT}, and $I_{D,Q0}$ around 0.

t3b: $V_{D,Q1}$ peaks when $I_{D,Q0}$ reaches 0, i.e. when $I_{VDD}=I_{OUT}$. The blue and red dashed areas illustrate the volts-second product across L, and since I_{VDD} also equaled I_{OUT} at t_{2a}, these areas are equal.

In conclusion:

When including power supply inductance in the analysis of a high-current forced commutation transition, an excess current flow from V_{DD} to GND through both transistors will appear, in addition to I_{OUT} flowing in the transistor turning on. The excess current increases energy loss, and causes the voltage across the transistor turning off to exceed V_{DD} immediately after the transition.

Observing the dashed areas in Figure 1-32, the ratio of excess current to I_{OUT} depends only on the switching waveforms, which means it is mostly determined by I_{PU} and I_{PD}. The duration of current flow (both I_{OUT} and the excess current) depends on L.

Note 1: From t_{3a}, none of the output transistors are in active region, so the only remaining power loss is the energy stored in the LC branch at t_{3a}, which is dissipated as the oscillation decays, e.g. in $R_{DS,Q2(ON)}$. Note that this damping is ignored in Eq. 1-44.

Note 2: It is possible that Q0 turns on again when $I_{D,Q0}$ peaks again after one oscillation period, and this can happen one or several times. A practical symptom of this is that the

first cycles of the oscillating voltage waveforms become more triangular shaped than sinusoidal, due to the slew rate limit of I_{PD}/C_{DG}.

1.4.2 Autocommutation transition

For the autocommutation transition case, a rising edge transition at $I_{OUT} < -3 \cdot I_{PD}$ is analyzed. Referring to Figure 1-33:

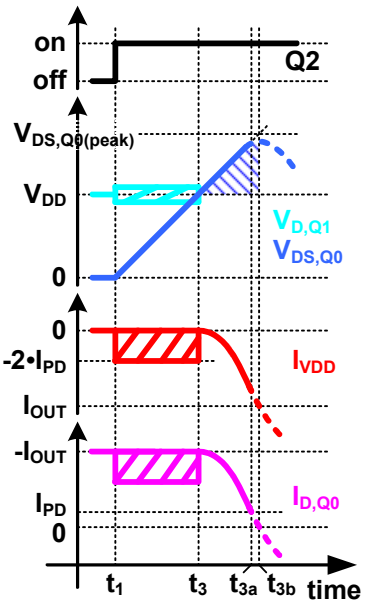


Figure 1-33: Autocommutation transition for $I_{OUT} < -2 \cdot I_{PD}$. Dashed curve segments are governed by Eq. 1-44. Power loss occurs in Q0 from t_1 to t_{3b}.

t_1: Phase 1 starts and I_{OUT} charges $V_{DS,Q0}$ towards V_{DD} at a rate of I_{PD}/C_{DG}. This situation is similar to scenario D for the ideal power supply model. The only difference is that the parasitic inductance of the V_{DD} rail L now forms an LC tank with $C_{DG,Q1}$ and this tank is excited by a decreasing ramp voltage, causing a voltage oscillation on $V_{D,Q1}$. The corresponding current oscillation appears on I_{VDD}, and thus on $I_{D,Q0}$ (see Eq. 1-42). This oscillating current is given by an expression similar to Eq. 1-44, and given the initial conditions of $I_{VDD}(t_1)=0$ and $dI_{VDD}(t_1)/dt=0$, it can be shown that I_{VDD} oscillates between 0 and $-2 \cdot I_{PD}$. Hence it is never positive during this oscillation, so regardless of amplitude, it can not cause a positive $V_{GS,Q1}$ voltage and turn Q1 on.

In order for $V_{DS,Q0}$ to keep increasing linearly, $I_{D,Q0}$ must remain larger than I_{PD} (bottom curve in Figure 1-33). Given the oscillation amplitude of $2 \cdot I_{PD}$, the requirement for this solution thus becomes $I_{OUT} < -3 \cdot I_{PD}$.

t_3: $V_{DS,Q1}$ reaches 0, and the path of I_{OUT} gradually starts moving from Q0 to Q1. This happens even if Q1 has not yet turned on, since the current can flow in its source-drain diode. I_{OUT} still causes $V_{DS,Q0}$ to increase at an unchanged rate of I_{PD}/C_{DG}, but now pulls $V_{D,Q1}$ above V_{DD} at the same rate. This causes I_{VDD} to increase in the negative direction as time squared, while $I_{D,Q0}$ decreases correspondingly.

t_{3a}: $I_{D,Q0}$ has decreased to I_{PD}, so $V_{GS,Q0}$ drops below Vt, and from this point, Q0 acts simply like a capacitor. The rest of the solution is an oscillation governed by Eq. 1-44. Like in the case of positive I_{OUT}, there is a possibility that $I_{D,Q0}$ exceeds I_{PD} again after one or more oscillation periods, temporarily turning on Q0.

t_{3b}: $V_{DS,Q0}$ peaks when $I_{D,Q0}$ reaches 0, i.e. when I_{VDD} reaches I_{OUT}.

Assuming $I_{VDD}(t_3)=0$ (ignoring the current from the LC tank oscillation), the dashed blue area in Figure 1-33 equals $-L \cdot I_{OUT}$. Further assuming that this area is triangular, corresponding to a linear extension of the $V_{DS,Q0}$ waveform to t_{3b}, $V_{DS,Q0(peak)}$ can be found as:

$$V_{DS,Q0(peak)} \approx V_{DD} + \sqrt{-2 \cdot I_{OUT} \cdot I_{PD} \cdot \frac{L}{C_{DG}}} \qquad I_{OUT} < -3 \cdot I_{PD} \qquad \textbf{Eq. 1-46}$$

Note 1: The duration of the linear increase of V_{OUT} from t_1 to t_3 is $V_{DD} \cdot C_{DG}/I_{PD}$. In systems where t_2-t_1 is smaller than this value, Phase 2 will start before t_3, i.e. before $V_{DS,Q1}$ has reached 0. In the ideal power supply model (scenario D) this would never cause Q1 to turn on, since Q5 is not able to pull $V_{GS,Q1}$ above Vt against the direction of I_{PD} flowing the

$C_{DG,Q1}$. However, this situation is different when parasitic inductance is considered. Since the current in $C_{DG,Q1}$ (equal to $-I_{VDD}$) now oscillates between 0 and $2 \cdot I_{PD}$ from t_1 to t_3, it is not always larger than I_{PU} and cannot prevent $V_{GS,Q1}$ from exceeding Vt temporarily, causing Q1 to conduct current. This causes an excess current to build up in L prior to t_3, and hence increases the dashed blue area in Figure 1-33, that must be covered before $V_{D,Q1}$ peaks.

In conclusion:

When including power supply inductance in the analysis of a high-current autocommutation transition, the transistor turning off will be exposed to a voltage $V_{DS(peak)}$ larger than V_{DD} immediately after the transition.

As opposed to forced commutation transitions there is not necessarily an excess current, flowing through both output transistors. However, it can occur in systems with dead time small enough to satisfy $t_2-t_1 < V_{DD} \cdot C_{DG}/I_{PD}$, depending on the exact timing of the turn-on in relation to the phase of the LC oscillation that occurs between t_1 and t_3.

If excess current does occur, it increases both the energy loss and the peak voltage $V_{DS(peak)}$.

1.5 Assessment of higher-order effects

1.5.1 C_{DG} voltage nonlinearity

In the above analysis (with and without parasitic inductance), the C_{DG} capacitors are considered linear capacitances. In practice, C_{DG} decreases with increasing V_{DG}, because the gate capacitance of the device becomes more associated with the source terminal as the channel becomes pinched off at the drain end. Mainly drain-gate overlap capacitance remains at larger V_{DG}. This voltage dependency causes the assumption of equal currents in the C_{DG} capacitors of Q0 and Q1 to fall.

Figure 1-34 illustrates the actual currents, as for example in a rising edge transition for positive I_{OUT}, i.e. a transition is driven by the HS gate driver turning on, forcing a current of I_{PU} in $C_{DG,Q1}$. Initially, V_{OUT} is at GND potential, so $V_{DG,Q0}$ is 0, and $C_{DG,Q0}$ is larger than $C_{DG,Q1}$. Since the voltage derivatives across the two C_{DG} capacitors are equal and opposite, this means more current will flow in $C_{DG,Q0}$. At $V_{OUT}=V_{DD}/2$, the capacitances are equal, and so are the currents. For V_{OUT} close to V_{DD}, $C_{DG,Q1}$ becomes larger, causing the switching transition to slow down, and $I_{CDG,Q0}$ to decrease below I_{PU}.

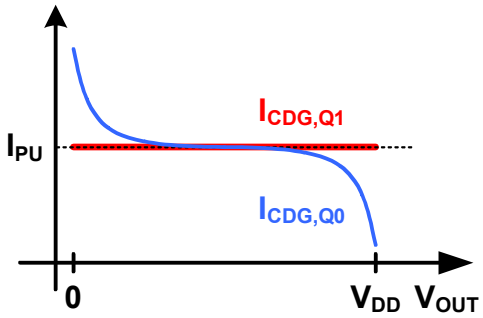


Figure 1-34: Output transistor Drain-Gate capacitor currents for a rising edge forced commutation transition.

As illustrated by this example, Q0 will turn on momentarily at the beginning of the transition, unless I_{PD} is much larger than I_{PU}.

This observation, combined with the results of the parasitic inductance analysis, shows that although simultaneous conduction of the two output transistors can be reduced by increasing the I_{PD}/I_{PU} ratio, it may not be realistic to prevent it completely.

1.5.2 Diode conduction and Reverse recovery

For sufficiently large positive I_{OUT}, the Q0 source-drain diode will conduct part of the output current during the Q0 conduction state (see Figure 1-10). Consequently, there will be a minority carrier charge that needs to be swept out of this diode before the following rising

edge switching transition, where the diode becomes reverse biased. This is referred to as the reverse recovery charge, Qrr.

When $I_{D,Q0}$ becomes positive at t_{2a} (see Figure 1-32), V_{OUT} will remain close to GND potential and $I_{D,Q0}$ continue increasing until the reverse recovery charge has been removed. This causes an increase in the switching power loss.

Conversely, since the diode conduction reduces the voltage drop across Q0 during the conduction state, it reduces conduction power losses. The net effect of reverse recovery on total power losses thus depends on switching frequency, since the switching power loss increase is proportional to fs while the conduction loss decrease is independent of fs.

Due to the direction of the FET diodes, reverse recovery only occurs in forced commutation transitions, i.e. as described above in rising edge transitions, or at large negative I_{OUT} in falling edge transitions.

1.6 References

Analysis of switching power losses has been covered in several papers, including:

[3] Jerry Waite, Thomas G. Wilson, Jr. (Zytec Corporation): *Use Of Simulation To Understand And Predict Switching Losses In A Two-Stage Power Factor Corrected AC-To-DC Converter* IEEE 1996

[4] Alan Elbanhawy (Fairchild Semiconductor): AN-7019 *Limiting Cross-Conduction Current in Synchronous Buck Converter Designs*. www.fairchildsemi.com 2005

[5] Yuancheng Ren, Ming Xu, Jinghai Zhou, and Fred C. Lee *Analytical Loss Model of Power MOSFET*. IEEE Transactions on Power Electronics, Vol. 21, No. 2, March 2006.

Some of the reasons for conducting an additional analysis are:

Like most papers concerning this topic, the ones listed here actually focus on switch mode power supplies rather than Class D output stages. Positive output current is thus assumed (except [4], where analysis is based on a pulse voltage source), since it is reasonable to assume positive output power from a power supply. Comparing to the present analysis, this corresponds to assuming that all rising edge transitions are scenario A and all falling edge transitions are scenario D. In Class-D output stages, I_{OUT} assumes both signs, so all scenarios must be taken into consideration.

The present analysis has shown that gate driver output current impacts switching losses, and notably that the influences of I_{PU} and I_{PD} are distinctly different. The papers listed above model the gate driver output as a voltage source with output resistance. This binds the ratio of I_{PU}/I_{PD}, and since $Vt << V_{GD}$, it also implies that I_{PU} is several times larger than I_{PD}. Such a gate driver does not satisfy Eq. 1-26, and would thus cause large excess switching currents in practice.

[6] Marco Berkhout: *A Class D Output Stage with Zero Dead Time*. International Solid State Circuits Conference (ISSCC) 2003.

1.7 Conclusions

- Switching power losses depend on the half bridge output current at the time of the switching transition. Depending on its sign and magnitude, 4 different loss scenarios occur, depending on whether current can flow in the channels of each output transistor.
- As long as dead time is large enough so $t_2 > t_1$ (see) it will only influence output transistor switching losses in one of the four scenarios (B).

- One of the scenarios (C) is lossless, and this can be exploited to minimize idle power losses.
- A falling edge switching transition possesses the same loss mechanisms as a rising edge transition at the opposite sign of output current.
- Assuming an ideal V_{DD} power supply, simultaneous conduction in the two output transistors is avoided if $I_{PU} < I_{PD}$. When taking parasitic inductance into consideration, it is unavoidable, but the amount increases with I_{PU}/I_{PD}.
- Comparing to the switching power loss analysis for ideal power supply, the inclusion of parasitic inductance is shown to increase switching power losses significantly, by exposing output transistors to excess current and voltages larger than V_{DD}. Consequently, it is to be expected that the analytical loss expressions from the ideal power supply model (1.3) show lower losses than actual. However, the inclusion of parasitic inductance also precludes simple analytical loss expressions, especially because circuit behavior forks into even more different scenarios, particularly in forced commutation transitions (Figure 1-32). In conslusion, circuit analysis provides insight in power loss optimization, but has limited use for qualitative modeling of switching losses, compared to simulation.
- Conduction power losses are simpler to model, and reliable analytical results can be found, provided that the resistance of the output current paths (see Figure 1-5) is known up to frequencies including the first few harmonics of the ripple current. Skin depth at 400kHz is around 0.1mm, so especially the output filter inductor can be expected to have significantly higher resistance at the switching frequency than at audio frequencies. A measurement is the preferred way to determine the inductor ESR vs. frequency, since wire proximity effect is not easily modeled.

2 Output power

Maximum output power in a given load resistance is largely determined by V_{DD}, which in turn is limited by the voltage handling capability of the output transistors. As shown in section 1.4, the output transistors will be exposed to drain-source voltages which exceed V_{DD} when peaking immediately after switching transitions. This further reduces the V_{DD} voltage that can safely be used, and hence the achievable output power with a given choice of output transistors is related to the voltage peak amplitude.

In autocommutation transitions, the voltage peak is caused by the output current building up in L after the transition, and the peak voltage can be approximated by Eq. 1-46. In forced commutation transitions, the voltage peak is caused by excess current that decays in L after the transition. The peak voltage thus depends on excess current (see section 1.4.1), including the effect of eventual reverse recovery charge, but is usually smaller than the peak voltage in autocommutation at the same current magnitude.

The following relation can be observed from Figure 1-23 in section 1.3.10:

$$V_{DS,Q0(peak)}(I_{OUT}) = V_{DS,Q1(peak)}(-I_{OUT}) \qquad \textbf{Eq. 2-1}$$

meaning that over a symmetric range of I_{OUT}, the HS and LS output transistors will be exposed to equal peak voltages.

2.1 Output transistor peak voltages with Loudspeaker loads

For any given output transistor type, $V_{DS(peak)}$ must be kept below a certain limit to ensure device reliability, and in order to evaluate $V_{DS(peak)}$, the parameters on the right hand side of Eq. 1-46 must be found. L is typically determined by package and PCB geometries, and C_{DG} is given by the type and size of output transistors, which leaves V_{DD}, I_{PD} and the maximum possible value of I_{OUT} to be determined. Though Eq. 1-46 is only valid for negative I_{OUT}, the actual range of I_{OUT} variation can be considered symmetrical, since music signals have zero DC value. Hence, the determination of maximum I_{OUT} only needs to concern its numerical value.

When an amplifier is designed for a specific output power into a given nominal load resistance R_L (e.g. 200W unclipped sine wave into 4Ω), the maximum output voltage is then given, and the V_{DD} voltage necessary to provide it can be found by accounting for $R_{DS(ON)}$ and the maximum modulation index (MI).

$V_{DS(peak)}$ decreases when decreasing I_{PD}, but this has the disadvantage of increasing switching power losses, and thus presents a tradeoff.

In order to determine the maximum output current $I_{OUT(peak)}$, the maximum speaker current $I_{SPK(peak)}$ must be found (currents defined in Figure 1-1). However, this is not as simple as dividing the maximum output voltage by R_L, since an actual loudspeaker presents a complex and frequency dependent load impedance. It is common for loudspeakers to have a minimum impedance lower than the nominal specification R_L, and more importantly, the output current is not limited to the maximum output voltage divided by the minimum impedance either, since that number is only the maximum current that can occur for a sine wave audio signal. The maximum possible output current for an arbitrary audio signal, limited to $\pm V_{DD}$, can be found using methods similar to how overflow in digital filters is tested. This is done in "Determination of Overcurrent Protection Thresholds for Class D Audio Amplifiers" in Appendix II. The major conclusions are:

- For a given loudspeaker, there is a certain waveform that will produce the maximum possible output current $I_{OUT(peak,ARBwfm)}$ for an arbitrary voltage limited signal.
- For some loudspeakers this current is very large, and it is not feasible to design for.
- When playing music at maximum unclipped volume, I_{OUT} will typically remain significantly below $I_{OUT(peak,ARBwfm)}$, but this is a statistical consideration that relies on lack of correlation between the music signal and the maximum current excitation signal mentioned above.
- When playing music with overdrive (gained beyond clipping), the peak value of I_{OUT} increases.
- For amplifiers that are not sold bundled with (or built into) loudspeakers, the loudspeaker is unknown, and consequently so is $I_{OUT(peak,ARBwfm)}$.

In order to ensure reliability, most amplifiers have built-in overcurrent protection circuitry which shuts down the amplifier (often temporarily) if I_{OUT} exceeds a certain threshold I_{OCP}. Such a system is necessary to prevent permanent damage to the amplifier in case of an output short circuit. Setting I_{OCP} to $I_{OUT(peak,ARBwfm)}$ for a given loudspeaker would allow playing any signal on it, but given the conclusions above, I_{OCP} can be set somewhat lower and still provide a very small probability of interrupting the music during normal use of the amplifier.

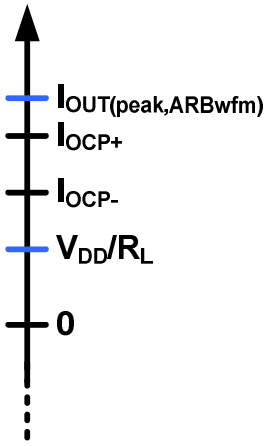


Figure 2-1: Output current values and limits (BTL configuration). Same values apply for negative I_{OUT}.

For any protection system implementation, the I_{OCP} threshold will vary somewhat depending on timing and circuit conditions as well as PVT (process, voltage and temperature) variations. Rather than a fixed threshold, the amplifier thus shuts down when I_{OUT} is somewhere in a range I_{OCP-} to I_{OCP+}, depending on conditions.

An example of an output current budget is illustrated in Figure 2-1. V_{DD}/R_L is approximately the maximum current that could flow in a resistive load with the same value as the nominal loudspeaker impedance R_L. $I_{OUT(peak,ARBwfm)}$ is loudspeaker dependent, and typically several times larger than V_{DD}/R_L. I_{OCP} can be set somewhere between these two values, depending on the acceptable probability of interrupting a music signal being played (see Appendix II for details). Considering the inevitable variation of I_{OCP}, the maximum possible value of I_{OUT} before shutdown is then I_{OCP+}, so $-I_{OCP+}$ this is the negative value that should be inserted in Eq. 1-46 to find the maximum $V_{DS(peak)}$ voltage.

With this knowledge, an output transistor type with adequate drain-source voltage rating can be selected, and its size subsequently determined by thermal considerations as described in section 0.3.4. This in turn determines C_{DG}, influencing $V_{DS(peak)}$, so results must rechecked.

2.2 SE versus BTL topology

While the procedure described in the previous section can be used to choose an output transistor type for a given output power and output stage topology, the choice of topology (Single Ended or Bridge Tied Load, see section 0.1) will be discussed here.

At a glance, the SE topology has the advantage of needing only two output transistors and one output inductor per amplifier channel, i.e. half that of BTL. However, in order to produce the same output voltage swing across the load, the SE output stage must be supplied by twice the voltage, and hence the output transistors must switch twice the voltage of the BTL output transistors. However, since I_{OUT} flows in only one transistor at

the time, vs. two in BTL, each output transistor can have twice the $R_{DS(ON)}$ for equal conduction power losses.

This relationship is illustrated in Figure 2-2. Theoretically, a BTL output stage can be reorganized to an SE output stage with equal output power, by connecting the same output transistors in pairs of two in series to form each switch, thus providing twice the voltage rating and twice the $R_{DS(ON)}$ for each switch. Note that since each individual output transistor switches the same current at the same voltage as in BTL configuration, both switching and conduction losses remain unchanged, and since the total output transistor area is also unchanged, so is the thermal design.

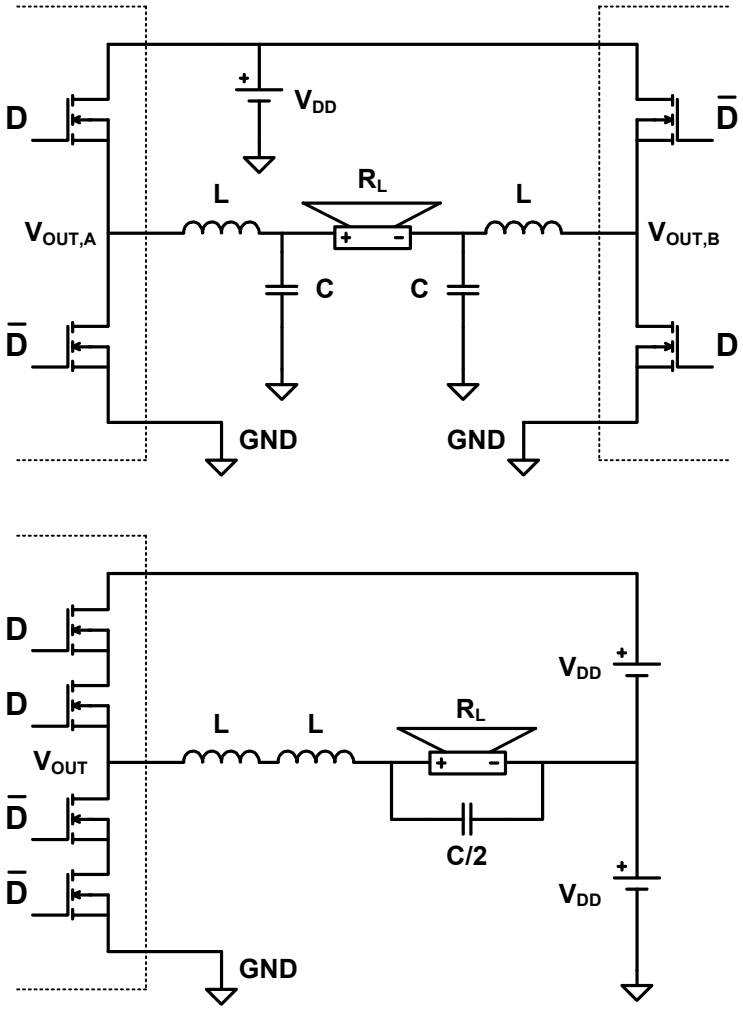


Figure 2-2: BTL output stage vs. equivalent SE output stage.

Each branch of the BTL output filter is effectively loaded by $R_L/2$, while the SE output filter is loaded by R_L. In order to provide equal frequency response, the SE output filter thus needs twice the inductance and half the capacitance compared to each of the BTL filter branches. Figure 2-2 illustrates this by placing the two inductors in series. Actual implementations obviously use a single inductor with twice inductance, but the illustration is meaningful because such an inductor needs to store twice the energy (double inductance, same peak current), requiring twice the core volume to avoid saturation. Note that with twice the inductance at twice the supply voltage, the two systems shown have equal ripple current amplitude.

The single SE capacitor is a real benefit, with only half the capacitance of the BTL filter capacitor, and since suitable capacitor types are typically bipolar anyway, the voltage swing of $\pm V_{DD}$ vs. $0\text{-}V_{DD}$ for BTL does not present an additional constraint.

Actual SE implementations do not have series connected switches like shown in Figure 2-2, since it would require unrealistic matching to ensure an even voltage distribution between two switches during fast switching transients. Instead, single output transistors with twice the voltage rating are needed. Since die area is a main determinant of device cost, this raises a question about the size of one device with twice the voltage rating and twice the $R_{DS(ON)}$, vs. the equivalent two series-connected devices. An approximate rule for high voltage semiconductors is that the specific resistance, i.e. $R_{DS(ON)}$ of a device with unit area, varies with its drain-source breakdown voltage as:

$$R_{SP} \propto \left(V_{DS(breakdown)}\right)^{2.5} \qquad \textbf{Eq. 2-2}$$

(see e.g. [7]) and using this, the ratio of total output transistor area between equivalent SE and BTL output stages can be found:

$$\frac{A_{SE}}{A_{BTL}} \approx \frac{2^{2.5}}{2 \cdot 2} = 1.4 \qquad \textbf{Eq. 2-3}$$

where 2 in the nominator is the increase in $V_{DS(breakdown)}$, first 2 in the denominator is because twice the $R_{DS(ON)}$ is allowed, and second 2 in the denominator is because only 2 (vs. 4) devices are needed. Consequently, the 2 transistors needed for an SE output stage appear to occupy a larger die area than the 4 needed for an equivalent BTL output stage. However, there are some additional factors to consider:

- When taking into account voltage peaks (Eq. 1-46), V_{DD} will be twice as large for the SE output stage, but the excess voltage (square root term) may remain almost unchanged, depending mainly on C_{DG} of the SE transistors and the chosen I_{PD}. Maximum I_{OUT} should be unchanged for equal output power, and since L is simply geometry dependent, it may not change significantly either. Consequently, though V_{DD} doubles, $V_{DS(peak)}$ does not.
- With half the number of switches, the die area for control circuitry (gate drivers, overcurrent protection circuitry, etc.) is reduced, though not likely halved, since these circuits must also operate at twice the supply voltage in SE. This consideration is most relevant for lower power output stages, where a larger fraction of the total die area is occupied by control circuitry, since output transistors are small.
- When considering SE vs. BTL for a given design, the candidate solutions will often be in two different IC processes, due to the difference in supply voltage. The specific resistances of the suitable output transistors for each solution may adhere more or less closely to Eq. 2-2, for the benefit of either solution.
- SE requires less package pins per amplifier channel.
- BTL provides for some modulation schemes which are not possible in SE, utilizing that the two half bridges in BTL do not necessarily have to be simply inverted.

2.3 Measurement caveats

When making measurements on an amplifier, internal nodes in the chip are often not accessible, and the closest available nodes to the output transistor terminals are the outside ends of the package pins. This can cause significant errors when measuring peak voltages.

Figure 2-3 shows a half bridge where the parasitic inductance L is divided into its physical contributions associated with pins and power supply. Since the output inductor (not shown) prevents I_{OUT} from changing significantly within the timeframe of a switching transition, dI/dt is practically equal for the 3 parasitic inductors, and the voltages across them are thus proportional to their respective inductances:

$$\frac{V_{LPIN,VDD}(t)}{L_{PIN,VDD}} = \frac{V_{LPIN,GND}(t)}{L_{PIN,GND}} = \frac{V_{LVDD}(t)}{L_{VDD}} \qquad \textbf{Eq. 2-4}$$

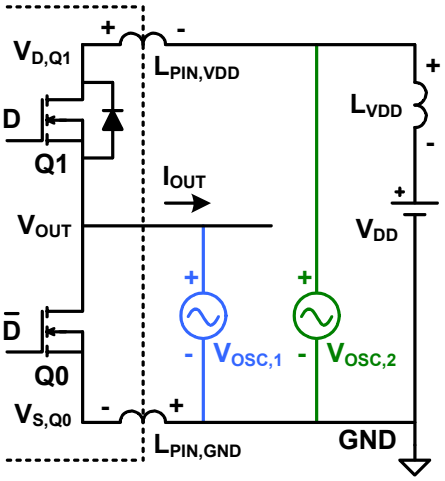


Figure 2-3: Measuring device V_{DS} voltage with instruments attached outside the chip package.

Now consider a measurement of $V_{DS,Q0(peak)}$ after a rising edge switching transition for large negative I_{OUT}. The voltage drop across Q1 at this time is small because current flows in the forward direction of its source-drain diode (see Figure 1-33 at $t=t_{3b}$). Attempting to measure $V_{DS,Q0}$, an oscilloscope probe is mounted as shown by $V_{OSC,1}$, but because of the parasitic inductances, it actually measures:

$$V_{OSC,1} = V_{DD} + \frac{L_{PIN,VDD} + L_{VDD}}{L_{GND,VDD} + L_{PIN,VDD} + L_{VDD}} \cdot \left(V_{DS,Q0} - V_{DD}\right) \qquad \begin{cases} \text{rise transition} \\ t > t_{3a} \\ V_{DS,Q1} = 0 \end{cases} \qquad \textbf{Eq. 2-5}$$

where the forward voltage drop of the Q1 source-drain diode has been ignored, assuming $V_{OUT}=V_{D,Q1}$. In other words, the excess voltage ($V_{DS,Q0}$-V_{DD}) is divided between the 3 inductors, and this measurement misses the fraction present across $L_{PIN,GND}$, showing lower voltage than actual. Basically the error corresponds to assuming $V_{S,Q0}=0$.

If the same voltage probe is used to determine $V_{DS,Q1}$ by subtracting V_{OUT} from V_{DD} after the equivalent (autocommutation) falling edge transition for large positive I_{OUT}, the measurement only shows the fraction of excess voltage present across $L_{PIN,GND}$. This error is typically larger, and can lead to the incorrect conclusion that the maximum peak voltage across the HS output transistor is smaller than that occurring across the LS device.

Getting back to the rising edge transition, and adding an additional oscilloscope probe $V_{OSC,2}$, we measure:

$$V_{OSC,2} = V_{DD} + \frac{L_{VDD}}{L_{GND,VDD} + L_{PIN,VDD} + L_{VDD}} \cdot \left(V_{DS,Q0} - V_{DD}\right) \qquad \begin{cases} \text{rise transition} \\ t > t_{3a} \\ V_{DS,Q1} = 0 \end{cases} \qquad \textbf{Eq. 2-6}$$

In devices where the V_{DD} and GND package terminals have pins and bond wires of similar geometries, it is reasonable to assume that $L_{PIN,VDD} \approx L_{PIN,GND}$, and using Eq. 1-35 and Eq. 1-36 we get:

$$V_{DS,Q0} \approx V_{OSC,1} + \left(V_{OSC,1} - V_{OSC,2}\right) = 2 \cdot V_{OSC,1} - V_{OSC,2} \qquad \begin{cases} \text{rise transition} \\ t > t_{3a} \\ V_{DS,Q1} = 0 \end{cases} \qquad \textbf{Eq. 2-7}$$

which is an approximate method of determining the actual peak voltage across the terminals of an output transistor inside the package, from a measurement outside the package.

The bandwidth limits of the oscilloscope input, the voltage probe, and the way this probe is mounted to the output stage can reduce the measured peak voltage significantly, so it must be verified that measurement bandwidth is sufficient.

The voltage accuracy of the oscilloscope should also be taken into consideration. An oscilloscope with 7 equivalent bits of voltage accuracy (6 bits for positive voltages) can cause errors of 3-4% when evaluating Eq. 2-7.

2.4 References

[7] Bruce Carsten: *The Bipolar Transistor is Dead, Long live the Bipolar Transistor!* PCIM conference in 1993.

[8] Marco Berkhout: *An Integrated 200-W Class-D Audio Amplifier*. IEEE Journal of solid-state circuits, Vol. 38, No. 7, July 2003

[9] Marco Berkhout: *Integrated Overcurrent Protection for Class D Power Stages.* IEEE 2003.

[8] discusses output transistor peak voltages and reliability (and much more), and [9] presents an implementation of an overcurrent protection system (not covered here).

3 Distortion

Total Harmonic Distortion (THD) is the quantity typically used to assess the audio performance of an amplifier. If the PWM waveform reproduced by a Class-D output stage was a perfectly square waveform, alternating between V_{DD} and GND with the exact timing dictated by the input signal, the output stage would be distortion free. In practice, the PWM waveform deviates from ideal during the conduction states due to voltage drops across the output transistors, and during the switching transitions due to the switching waveform variations discussed in chapter 1. These deviations can cause distortion, and are analyzed in this chapter.

3.1 Transfer characteristic analysis

A method for analysis of PWM waveform errors and their contributions to THD is given in "Time Domain Analysis of Open Loop Distortion in Class-D Amplifier Output Stages" in Appendix III. The paper includes examples of the most common types of errors. A few introductory notes on the paper, especially concerning how the analysis differs from the power loss analysis in chapter 1 are given here.

3.1.1 Introduction to the paper

The treatment of switching transition waveforms assumes an ideal power supply, and is more simplified than the one in the on power losses. Switching transitions are divided into 3 scenarios, but due to differences in definitions, these are not directly comparable to the scenarios in chapter 1 above.

The analysis in chapter 1 shows that for a given I_{PU}, a forced commutation transition waveform is independent of I_{OUT} (scenario A, equality applies in Eq. 1-25). This is a consequence of the assumption of infinite transconductance and in practice, finite transconductance causes the waveform to depend slightly on I_{OUT}. As I_{OUT} increases V_{GS} during the transition must increase, which in turn causes a slight decrease in actual I_{PU}, due to the finite output impedance of the gate driver. Consequently as I_{OUT} increases, a forced commutation transition waveform changes in two ways:

- It is slightly delayed because V_{GS} must be charged to a larger voltage before the transition starts
- Its slew rate decreases slightly, since I_{PU} is effectively decreased by the V_{GS} increase and the finite output impedance of the gate driver.

A first-order expression for this compliance of the waveform to I_{OUT} is the equivalent delay of the switching waveform per additional ampere of I_{OUT} (ns/A), and this number influences THD. When I_{PU} is reduced by decreasing the width of the gate driver pull-up transistors, the output impedance of the gate drivers in the ON state increases proportionally (if a curve in Figure 0-5 is multiplied by a given factor, its slope changes by the same factor). Consequently, when finite output transistor transconductance and gate driver output impedance is considered, the influence of an I_{PU} decrease on forced commutation transition waveforms is twofold:

- The transition slew rate decreases as shown earlier (Eq. 1-25)
- The transition becomes more compliant to increasing I_{OUT} (more ns/A), as described above.

While the first effect increases power losses, only the latter influences THD. When the paper discusses how THD is influenced by that adjusting "turn-on speed", it is actually not

the slew rate itself, but the accompanying change in compliance (ns/A) that makes the difference.

This observation is general to distortion analysis. Since the voltage at the speaker terminal represents an averaging of the PWM waveform, only the waveform average influences THD. Any fixed switching delay, slew rate, voltage overshoot, or other artifact will only contribute a DC error at the speaker terminal. However, if these artifacts depend on output current this causes distortion, if and only if the change in the average of the PWM waveform is a nonlinear function of speaker current I_{SPK} (or of D, which is proportional to I_{SPK} for a resistive load). The concept in the paper is thus to analyze the transfer characteristic from D to the average of the PWM waveform.

The definition of I_{LIM} in the paper (Figure 5) is equivalent to Eq. 1-31, since that the two C_{DG} capacitors are the only output stage capacitors considered in section 1.3.

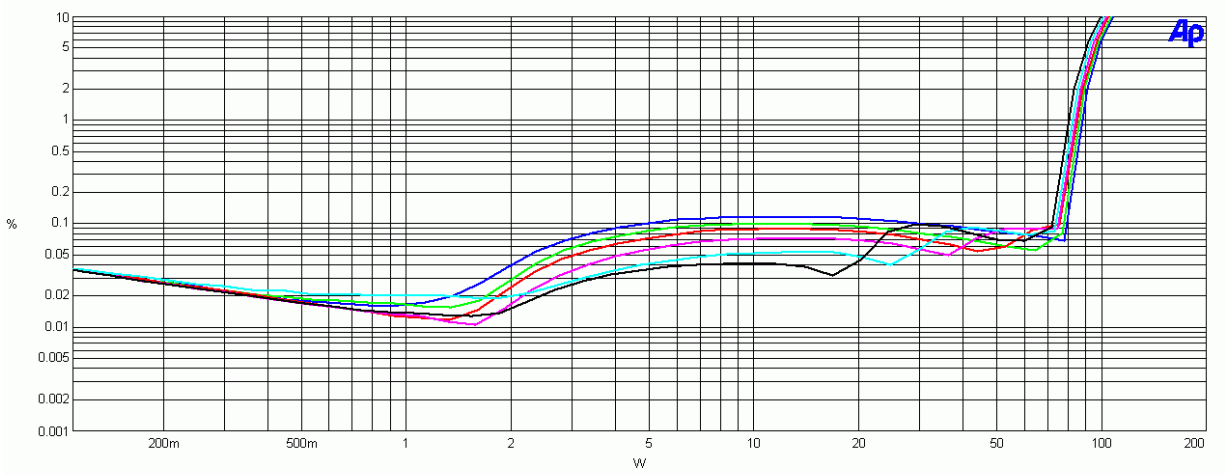
One of the errors described in the paper results from source-drain diode conduction (Figure 4). A complementary consequence of diode conduction is that the charge stored in this diode must be swept out during the following switching transition. In addition to causing a power loss (see section 1.5.2), this separately influences PWM waveform area and hence THD, but this effect is not easily quantified theoretically.

3.1.2 Modeling example

In this section, a calculation of THD based on some of the nonlinearities described in the paper is compared to a measurement. Some of the parameters needed for the THD calculation are unknown, so performance can not be predicted directly by calculation. Instead, the calculation is repeated several times, while iteratively changing input parameters, trying to obtain a match between the calculation result and the measurement.

While this approach does not predict THD of an output stage, it can be used to verify that certain known nonlinearities can cause THD as measured, and to find the unknown parameter values.

The measurement is shown in Figure 3-1 below:



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Blue	Solid	2	Anlr.THD+N Ratio	Left	0 degC
2	1	Green	Solid	2	Anlr.THD+N Ratio	Left	25 degC
3	1	Red	Solid	2	Anlr.THD+N Ratio	Left	50 degC
4	1	Magenta	Solid	2	Anlr.THD+N Ratio	Left	75 degC
5	1	Cyan	Solid	2	Anlr.THD+N Ratio	Left	100 degC
6	1	Black	Solid	2	Anlr.THD+N Ratio	Left	125degC

Figure 3-1: THD+N vs. RMS output power in 4Ω, measured on a monolithic BTL output stage at temperatures from 0°C to 125°C

The measurement is THD+Noise, i.e. the instrument does not distinguish random noise from distortion power, so at low power, the THD+N level is determined by the amplifier noisefloor. Noise power is thus $(0.035\%)^2 \bullet 100mW = 12.25nW$, or -98dB compared to the 80W maximum output power.

When output power exceeds about 1.5W, the variation in I_{OUT} begins to excite several different switching scenarios (paper Figure 5). This increases distortion since the voltage average of the switching waveform is not generally a linear function of I_{OUT}, and even less so across different scenarios. This switching transition related distortion dominates in the range 2-20W, and the decrease in distortion with temperature in this range can be attributed to decreasing dead time.

Above 20W I_{OUT} becomes large enough for diode conduction to occur, and larger $R_{DS(ON)}$ at higher temperatures causes the diode related distortion to onset at lower power.

The steep increase to the right is signal overdrive (the amplifier is clipping).

The following parameters are known from the measurement setup or from other measurements:

- Switching frequency fs = 384kHz
- Supply voltage V_{DD} = 29V
- Total capacitance from V_{OUT} at node ($C_{DG,Q1}+C_{DS,Q1}+C_{DB,Q1}+C_{DG,Q0}+C_{DS,Q0}$) ≈ 200pF
- Output transistor $R_{DS(ON)}$ vs. temperature = 0.110Ω at 0°C to 0.185Ω at 125°C
- Background noise level = -98dB (seen from the THD+N graphs as explained above)

These parameters are then used for the THD calculation, which includes the following selection of nonlinearities:

- Background noise (a fixed noise power added to mimic the measured noisefloor)
- Switching transition nonlinearity is modeled as illustrated in Figure 5 in the paper. Finite turn-on speed is not included, i.e. when the HS GD turns on, V_{OUT} immediately equals V_{DD}. This corresponds to assuming infinite I_{PU}, and I_{PD} is also assumed infinite. Under these assumptions, t_2-t_1 simply equals dead time.
- Source-drain diode conduction. The diode model is purely exponential, and its I/V characteristic is defined by a “knee voltage” Vknee, where the dynamic resistance of the diode equals $R_{DS(ON)}$, i.e. Vknee is the output transistor source-drain voltage at whitch an infinitesimal current increment will split evenly between the source-drain diode and the transistor channel.
- The impact of source-drain diode reverse recovery on switching transitions. While difficult to quantify theoretically, it is modeled here simply by a switching transition delay proportional to the diode current prior to the switching transition.

The calculation assumes an ideal power supply and the signal level is not increased beyond clipping.

The result is shown in Figure 3-2

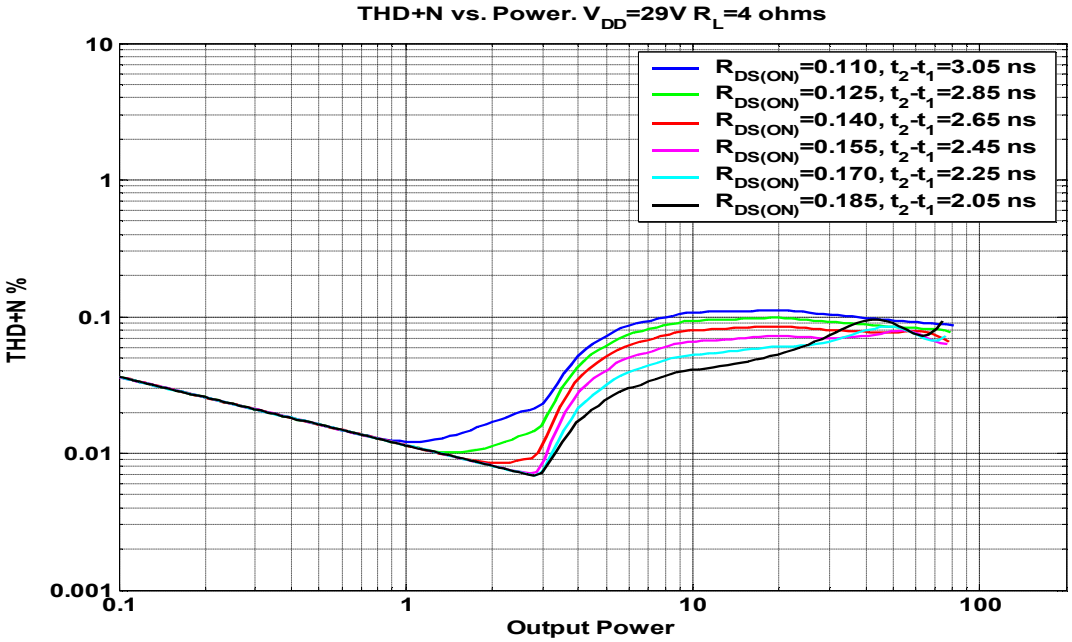


Figure 3-2: THD+N vs. output power in 4Ω, calculated from theoretical nonlinearities, for temperatures from 0°C (blue) to 125°C (black). t_2-t_1 is the interval labeled "Dead time" in Figure 5 of the paper.

Some necessary parameters for the calculation are unknown, and are adjusted for best match with the measurement:

- t_2-t_1 and its temperature dependence. The V_{GS} charging/discharging waveforms shown in Figure 1-8 delay both t_1 and t_2 with increasing temperature, as the gate driver transistors become weaker because mobility decreases. Since Vt<<V_{GD}, the discharge from V_{GD} to Vt during turn-off typically has longer duration, and larger absolute temperature variation, than the charging from 0 to Vt during turn-on. The net effect is thus a decrease in t_2-t_1 with temperature, and best match of the calculated dead time related distortion occurs for t_2-t_1=3.05ns at 0°C to 2.05ns at 125°C (linear decrease assumed).
- Vknee (V). Best match of diode conduction related distortion occurs for a value of 0.8V.
- Reverse recovery transition delay per A of diode current (ns/A). This effect only influences THD at very high power, where it can partly cancel the distortion from diode conduction, causing e.g. the 125°C THD+N trace (black) to decrease slightly from 40W to 60W. Best match is obtained for a transition delay of approximately 1.4ns per A of current in the source-drain diode prior to the transition.

While the match between modeling and measurement is not perfect, this exercise does prove that the measured THD+N can be attributed to the nonlinearities included in this relatively simple calculation. A few comments on the calculated THD curves:

- When output power exceeds 3W, I_{SPK} starts exceeding the ripple current amplitude, so forced commutation transitions start to occur. This causes an increase in distortion, which is steepest for large t_2-t_1 values, since these cause the sharpest kinks in the transfer characteristics (Figure 6 in the paper).
- Another observation is that for dead time values larger than 2.5ns, distortion starts to increase below 3W. This occurs because the sum of I_{SPK} and the ripple current starts exceeding ±I_{LIM}, causing transitions to occur on the parabolic parts of the transfer

characteristics in Figure 6 in the paper. Larger t_2-t_1 reduces I_{LIM} (defined in Figure 5 in the paper, where $t_{DT} = t_2$-t_1), causing this to occur at lower output power.

Similar trends are visible in the measurement though not as clearly, since the actual switching transitions are influenced by several additional mechanisms which are ignored in the calculation model.

3.2 System level distortion considerations

Besides nonlinearities in the output stage itself, the distortion of a Class D amplifier depends heavily on the surrounding system components and architecture. Some of these influences are discussed in this section.

3.2.1 Power supply impedance

While the analysis in the paper concerns only nonlinearities in the output stage itself, the finite impedance of the V_{DD} power supply also causes distortion. Consider the BTL output stage shown in Figure 3-3, where a resistor R_{VDD} has been inserted in the V_{DD} supply rail, outside the decoupling capacitor. Playing a sinusoidal signal, the voltage across the loudspeaker load is

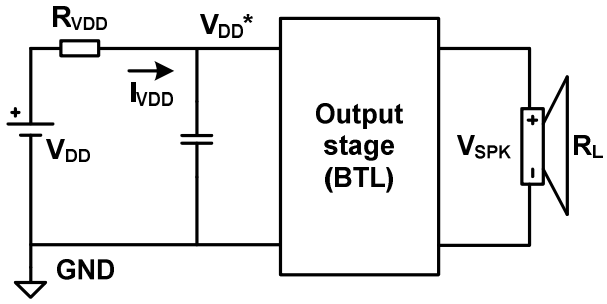


Figure 3-3: BTL output stage supplied by a V_{DD} source with finite output impedance.

$$V_{SPK}(t) = MI \cdot V_{DD}{}^* \cdot \sin(\omega t) \approx MI \cdot V_{DD} \cdot \sin(\omega t) \qquad \textbf{Eq. 3-1}$$

where MI is the modulation index, and the last approximation is valid for small R_{VDD}. Assuming that the ripple current flows in the V_{DD} decoupling capacitor (not in R_{VDD}), and disregarding all power losses in the system, the output power is equal to the input power at all times:

$$\frac{1}{R_L} V_{SPK}'^2(t) = V_{DD}{}^*(t) \cdot I_{VDD}(t) \approx V_{DD} \cdot I_{VDD}(t) \qquad \textbf{Eq. 3-2}$$

again the last approximation assumes that R_{VDD} is small. $I_{VDD}(t)$ can be found by inserting Eq. 3-1 into Eq. 3-2:

$$I_{VDD}(t) = \frac{1}{V_{DD} \cdot R_L} \cdot MI^2 V_{DD}^2 \cdot \sin^2(\omega t) = \frac{MI^2}{R_L} \cdot V_{DD} \cdot \left[\tfrac{1}{2} - \tfrac{1}{2}\cos(2\omega t)\right] \qquad \textbf{Eq. 3-3}$$

And since

$$V_{DD}{}^*(t) = V_{DD} - R_{VDD} \cdot I_{VDD}(t) \qquad \textbf{Eq. 3-4}$$

we find

$$V_{DD}^{*}(t) = V_{DD}\left(1 - R_{VDD}\frac{MI^2}{R_L}\cdot\left[\tfrac{1}{2} - \tfrac{1}{2}\cos(2\omega t)\right]\right) \qquad \text{Eq. 3-5}$$

Inserting this back into Eq. 3-1, one of the terms appearing in $V_{SPK}(t)$ is:

$$V_{DD}\cdot R_{VDD}\frac{MI^3}{2\cdot R_L}\cos(2\omega t)\cdot\sin(\omega t) = V_{DD}\cdot MI^3\frac{R_{VDD}}{4\cdot R_L}\left[\sin(3\omega t) - \sin(\omega t)\right] \qquad \text{Eq. 3-6}$$

i.e. a third order distortion product proportional to R_{VDD} occurs. On a plot of THD vs. signal level, it will increase as MI^2 (since the output signal fundamental increases as MI), and amount to approximately $R_{VDD}/4{\cdot}R_L$ for one amplifier channel at full power (MI=1).

Contrary to the output stage related distortion discussed in section 3.1, the distortion caused by R_{VDD} is typically dependent on signal frequency, because so is R_{VDD}. A typical power supply for an open-loop Class-D amplifier is a regulated switch mode power supply with electrolytic capacitors on its output. At low frequencies, the capacitors have a large impedance, but low output impedance is easily achieved by the control loop of the power supply. As frequency increases, the control loop gain will have to decrease, causing the output impedance of the native supply to increase, while the impedance of the electrolytic capacitors decreases. At some frequency in the audio band, the impedance of the capacitors seizes to decrease, and becomes limited by their series resistance (ESR). The sum of these effects determines the variation of R_{VDD} vs. frequency, and thus the frequency variation of the resulting THD.

Note that since the V_{DD} supply current has twice the frequency of the output signal Eq. 3-3, it is $R_{VDD}(2{\bullet}f)$ which influences THD at signal frequency f.

3.2.2 BTL vs. SE distortion

In general, an SE output stage will produce distortion components of both even and odd order. When connecting two identical SE output stages to form the two branches A and B of a BTL output stage, their even ordered harmonic distortion components will cancel. This is illustrated for 2nd and 3rd order in Figure 3-4. The top part shows one period of the output fundamental sine wave from branch A (red) and B (blue dashed). Note that the second order distortion signal from branch A (shown also in red) is identical for the positive and negative swing of the fundamental. Since the branches are identical, branch B also produces this distortion waveform, whether it swings positive or negative. Consequently, when branch A and B swing in opposite directions, the 2nd order harmonic waveforms are identical, and when the loudspeaker load is connected differentially, they cancel. The same is true for any even ordered distortion product.

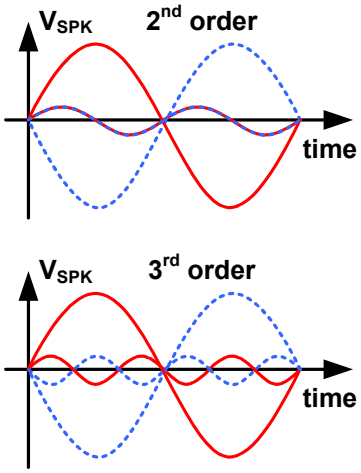


Figure 3-4: Even and odd ordered distortion from the two branches of a BTL output stage. Red traces are branch A, blue are branch B, operating in opposite phase.

Note that identical DC offsets from the two branches will also cancel, and this can be described theoretically as 0^{th} order distortion.

At the bottom of Figure 3-4, a 3^{rd} order distortion product is shown. Contrary to 2^{nd} order, the distortion waveform is not identical, but inverted for negative voltage swing. The same is true for all odd-ordered distortion products and consequently, odd ordered distortion at the BTL output will be identical to the odd-ordered distortion of each individual SE branch.

3.2.3 Output inductor core hysteresis

The output inductor is typically wound on a magnetic core. The hysteresis of the magnetization curve causes the inductor to deviate slightly from the ideal $V_L=L \bullet dI_L/dt$ behavior, and this causes distortion. Using low hysteresis core materials to reduce this effect serves the additional purpose of minimizing power losses in the inductor core.

3.2.4 Noise

Though noise is not distortion, it is included here for completeness. Digital-input PWM modulators typically use noise shaping, and the PWM signal then contains considerable noise power at frequencies above the audio band, even in idle operation (zero input signal). Noise shaping relies on output stage linearity, since if the shaped noise gets distorted, the distortion components will appear as noise in the audio band. This is especially critical at idle, where background noise is most audible in the absence of music. When noise shaping is used, it is thus particularly important that the output stage is linear in the vicinity of $I_{SPK}=0$ (D=½), since audio band noise increases otherwise. A necessary requirement for achieving this linearity is the $I_{LIM} > I_{RIP,P}$ requirement explained at the end of section 2.2 in the paper (Appendix III). I_{LIM} can be increased either by decreasing dead time or by adding capacitance from V_{OUT} to GND.

3.2.5 Feedback

Distortion can be reduced by the addition of a feedback loop, but since a straightforward implementation requires an analog summation point at the amplifier input, it can only be implemented if the input signal to the PWM modulator is analog. When designing a feedback loop there are a number of issues to consider, some of which are specific to Class D:

- When the amplifier is powered up, its output DC offset will appear as a step function at the output, and this step must be small enough to avoid an audible pop when applied to a loudspeaker. A 10mV step can be audible [10], depending on the exact waveform and on the loudspeaker. When using feedback, the DC offset of the amplifier is determined by the input offset of the feedback branch. If the loudspeaker terminals are referenced to GND (split-rail power supply) it is easy to obtain an offset of a few mV when using operational amplifiers. However, in a BTL configuration with only one power supply rail, the $V_{DD}/2$ DC voltage at the speaker terminals will necessitate a non-trivial solution like a high voltage operational amplifier, or a voltage divider with very high precision resistors.
- A high performance feedback loop for audio frequencies requires large capacitors (by on-chip standards) which must also be linear. Integrated feedback solutions thus require a significant die area.
- Feedback provides power supply rejection, i.e. the supply related distortion discussed in section 3.2.1 is suppressed, as are volume changes that occur for larger variations in supply voltage. This relaxes power supply requirements, but the output stage must still be designed to be reliable at the highest V_{DD} voltage it is exposed to. If nominal supply

voltage is significantly below this maximum, the output stage is effectively over-designed for the output power it can deliver. Consequently, while feedback can suppress the impact of supply voltage variations on the amplifier output, the only way to consistently get the maximum power for which an output stage is designed is to use a well regulated power supply.

Solutions for implementing an analog feedback loop on a digital-input amplifier (without simply adding a DA converter at the input) do exist, but since the feedback branch still essentially operates at audio frequencies, these solutions are still subject to the above considerations, including the need for large linear capacitors.

In conclusion, while distortion can be reduced by the use of feedback, the solutions can add significantly to die area, and a well regulated power supply is still needed to consistently exploit the power capability of the output stage. Hence it remains an advantage if the required THD level can be achieved without feedback.

Open loop output stages require a low-impedance power supply, but since one V_{DD} power supply can drive multiple output stages, the overall advantage of open loop increases with the number of amplifier channels sharing a the power supply.

3.3 References

[10] Tomas B. Sørensen: *Click and Pop Measurement Technique*.
Texas Instruments Application Report SLEA044.

Please also see the references in the paper in Appendix III.

4 Summary for design optimization

Different aspects of Class-D amplifier performance have been analyzed in chapters 1 thru 3. With output stage topology and output transistor type given by the considerations discussed in section 2.2, and output transistor size by the thermal limits discussed in 0.3.4, the most important remaining design variables are gate driver output currents I_{PU} and I_{PD}, and the amount of dead time. Power losses, output transistor peak voltages and THD are all mainly determined by these variables in combination, and the optimum depends on performance priorities.

This chapter presents a summary of the influences of design parameters on the various performance metrics, and an example of a practical design.

4.1 Performance vs. design variables

Conduction power losses	
$R_{DS(ON)}$ V_{GD}	For a given output signal, the conduction power losses inside the chip depend solely on $R_{DS(ON)}$ of the output transistors, which in turn depends somewhat on V_{GD}. Significant conduction losses can occur outside the chip. Specifically, the ripple current can cause significant losses in the output inductor wire if it has a large series resistance at and above the switching frequency. Since the ripple current has maximum amplitude at idle, this can become the dominant contribution to overall idle power loss.

Switching power losses	
I_{PU}	At large output currents, switching losses are dominated by forced commutation transition losses, which depend on I_{PU}. Increasing I_{PU} decreases forced commutation transition losses by decreasing the duration of the transitions (see Figure 1-21). Assuming an ideal power supply, this is the only effect. When considering parasitic inductance, an excess current will start flowing through both output transistors during forced commutation transitions if I_{PU} is increased enough for $I_{D,Q0,max}$ to exceed I_{PD} (Eq. 1-45), and this increases power losses. At the optimum I_{PU} value for minimum power losses, the power loss reduction from an infinitesimal I_{PU} increment, caused by reduced switching time, will equal the power loss increment caused by additional excess current. Note that since Eq. 1-45 depends on I_{OUT}, this balance also depends on the output signal. Increasing I_{PU} also increases the probability of excess current in autocommutation transitions that can occur in systems with low dead time (see below).

I_{PD}	Increasing I_{PD} reduces switching power losses through decreased duration of autocommutation transitions (see Figure 1-22). When considering parasitic inductance, it further reduces forced commutation transition switching losses by reducing excess current in transitions. Increasing I_{PD} also decreases the probability of excess current in autocommutation transitions that can occur in systems with low dead time (see below).
Dead time	Assuming an ideal power supply, increasing dead time decreases losses in scenario B, possibly to 0, thus widening the range of I_{OUT} with no switching losses (see section 1.3.8). Power losses in other scenarios are unaffected as long as $t_2 > t_1$. When considering parasitic inductance, excess current can occur in autocommutation transitions in systems where dead time is small enough to satisfy $t_2-t_1 < V_{DD} \bullet C_{DG}/I_{PD}$. The probability of excess current then increases with decreasing dead time (section 1.4.2 Note 1).

Switching power losses, specifically at idle operation: $I_{OUT} = \pm I_{RIP,P}$ (Eq. 1-2).	
I_{PU} and I_{PD}	Assuming an ideal power supply, if these values are selected to satisfy Eq. 1-35 (an upper limit for I_{PU} and a lower limit for I_{PD}), there will be zero switching losses at idle (see Figure 1-24).
Dead time	Assuming an ideal power supply, dead time only influences switching losses in scenario B. Hence idle losses decrease with dead time if $I_{RIP,P}$ is in scenario B, and are otherwise independent of dead time as long as t_2-t_1 is positive.
The loss analysis with parasitic inductance only concerns autocommutation transitions with $I_{OUT} < -3 \bullet I_{PD}$ (rising edge, see section 1.4.2), and hence does not cover idle operation unless $I_{RIP,P}$ is very large. However, by arguments similar to section 1.4.2 Note 1, it can be shown that • $I_{PD} > I_{RIP,P}$ (twice that required by Eq. 1-35) is a necessary condition for lossless switching transitions at idle. • Excess current can occur at idle even for small $I_{RIP,P}$, and the probability of this increases with decreasing dead time.	

Maximum output transistor voltage $V_{DS(peak)}$	
I_{PD}	The largest V_{DS} voltages typically occur after autocommutation transitions with large current, and increase with I_{PD} is given by Eq. 1-46
I_{PU} and Dead time	The probability that excess current occurs in autocommutation transitions increases with I_{PU} and decreases with dead time (see section 1.4.2 Note 1). If excess current occurs, it increases $V_{DS(peak)}$

THD	
Dead time I_{PU} and I_{PD}	I_{PU} must be smaller than I_{PD} to avoid large power losses. A side effect of this is that forced commutation transitions are apt to be more compliant to I_{OUT} than autocommutation transitions*, and this causes a kink in the input-output transfer characteristic of the output stage. Dead time adds additional compliance to autocommutation transitions, which can partly cancel the kink. Consequently, minimum THD is achieved for a certain finite amount of dead time, which increases with the difference between I_{PD} and I_{PU} (see the paper in Appendix III). Large I_{PD} and I_{PU} generally decrease THD, since the absolute errors caused by various switching transition nonlinearities become smaller as transition durations decrease.

*) This applies to the topology shown in Figure 0-4 (see section 3.1.1). Alternative gate driver topologies may behave differently.

4.2 Design example

As shown in the previous section, improvement of different performance measures causes conflicting requirements to design variables, and the design challenge is to balance these tradeoffs based on given performance priorities.

A Texas Instruments output stage with gate drivers optimized using some of the above theory is presented in "A 240W Monolithic Class D Audio Amplifier Output Stage" in Appendix IV. The theoretical presentation is greatly compacted and simplified compared the one in this document, but the paper serves as an example of an achievable performance point.

A few other notes:

- The gate driver output currents I_{PU} and I_{PD} can be adjusted simply by the widths of the gate driver pull-up and pull-down transistors. The paper discusses these widths rather than the I_{PU} and I_{PD} values.
- I_{OUT} is defined positive into the half bridge, i.e. the opposite sign of this document.
- Since $I_{PD} = V_{GS,Q0}/R_{DS,Q2(ON)} = Vt/R_{DS,Q2(ON)}$ (assuming infinite transconductance):
    - Equation (1) is equivalent to Eq. 1-46.
    - Equation (2) is equivalent to Eq. 1-35, but concerns only I_{PD} which is relevant for the tradeoff with device peak voltage.

5 Simulation techniques

The theoretical models discussed in the previous chapters are generally too simple for predicting performance figures with sufficient accuracy. As stated in section 0.4, simulation is the better option for this purpose, due to the inclusion of a large number of higher order effects. Detailed transistor models are usually available for the chip process, but as shown in chapters 1 and 2, device performance also depends heavily on parasitic components, particularly the inductances of output stage terminals and the power supply. These turn out to influence THD also, and determining parasitic inductances in a system thus becomes a necessity for performance simulation.

This chapter discusses simulation techniques for Class D output stages, and how parasitic inductances of the package and PCB can be modeled.

5.1 Modeling parasitic components in and around the output stage

Though transistor capacitances are included in the transistor models, a minor addition may be needed to account for the capacitance of the large metal interconnects needed to handle the currents in the output transistors.

For verification of the model, the total output capacitance at the V_{OUT} node of an existing device can be measured, by permanently switching off both output transistors at a time where I_{OUT} is small but nonzero. The output capacitance will then oscillate with L_{OUT}, and its value can be determined from the oscillation frequency at $V_{OSC,1}$. The parasitic inductances will have negligible influence on this frequency, since they are several orders of magnitude smaller than L_{OUT}, and so will C_{OUT}, being several orders of magnitude larger than the output capacitance. I_{OUT} must be smaller than I_{PD} to avoid that Q0 or Q1 turn on during the oscillation. Note that the capacitance found includes the parallel capacitance of the output inductor, as well as the capacitance of the oscilloscope probe.

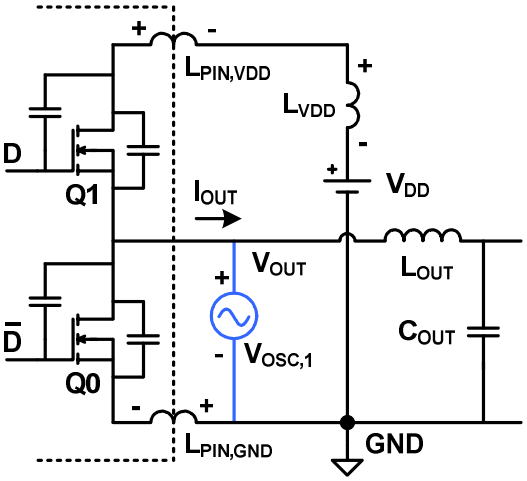


Figure 5-1: Parasitic capacitances and inductances in an output stage.
$L=L_{PIN,GND}+L_{PIN,VDD}+L_{VDD}$.

Once the capacitances are determined, the total loop inductance L can be determined from the frequency of the oscillations that occur at V_{OUT} after switching transitions (Figure 1-33 after t_{3a}). Note that the capacitance in this oscillation is only $C_{DG}+C_{DS}$ of one output transistor, since the other transistor acts as a short circuit.

While output transistor power losses and drain-source voltages are influenced only be the sum of parasitic inductance L, THD can also be influenced separately by the fraction of L contributed by $L_{PIN,GND}$. As explained in section 2.3, the amplitude of the V_{OUT} oscillation measured by $V_{OSC,1}$ after a rising edge transition is only a fraction of the oscillation amplitude across Q0 (Eq. 2-5). Similarly after a falling edge transition, only the fraction $L_{PIN,GND}/L$ of the oscillation amplitude across Q1 appears at V_{OUT}. Since these inductance fractions are generally different, and the average of the oscillation waveforms is not zero,

this asymmetry of parasitic inductances causes asymmetry between the positive and negative output voltage swing of the amplifier.

For an SE output stage this causes distortion, but for a BTL output stage it can be shown that these errors from each output branch cancel (at least if the PWM modulation scheme drives the two branches in simple inversion).

Consequently, THD simulation requires the modeled value of $L_{PIN,GND}$ to be determined separately, at least for SE configuration output stages. This can be done by measuring the relative oscillation amplitudes at V_{OUT} for rising- and falling-edge switching transitions at equal but opposite I_{OUT} (see section 2.3).

5.2 Efficient simulation

Transient simulation on Class-D amplifiers can be rather slow due to the mixture of slow time constants (in the output lowpass filter) and fast switching transitions. An approach for CPU efficient simulations of power losses, device voltage stress and THD is presented in "Efficient Performance Simulation of Class D Amplifier Output Stages" in Appendix V.

6 Acknowledgements

Besides the supervisors, many people have contributed indirectly or directly to this work. Some of the modeling ideas are a continuation of previous work done by my colleagues at TI. The influence of switching node capacitance on THD was initially analyzed by Anker B. Josefsen, and the simulation methods presented in the paper in Appendix V are loosely based on a similar setup made by Claus Neesgaard.

The output stage design presented in the paper in Appendix IV is entirely based on existing Texas Instruments circuitry, and my part was to optimize performance by adjusting design parameters based on the theory presented above. This happened over the winter 2004/2005 where I stayed in Dallas. Design lead was Cetin Kaya, and design manager Dale J. Skelton, TI Fellow.

Thanks to Claus Reckweg (TI), for providing measurement results from TI output stages, including the one in section 3.1.2, and to Thomas Mørch (TI) for reviews of this document.

Finally I wish to thank my TI manager Hans K. Andersen for arranging TI's involvement and support to this project.

Appendix I

Derivation of switching power loss equations with parasitic inductance.

It is readily observed that

$$V_{DS,Q0} + V_{DS,Q1} + V_L = V_{DD} \qquad \textbf{Eq. 0-1}$$

And by differentiation we get

$$\frac{dV_{DS,Q0}}{dt} + \frac{dV_{DS,Q1}}{dt} + \frac{dV_L}{dt} = 0 \qquad \textbf{Eq. 0-2}$$

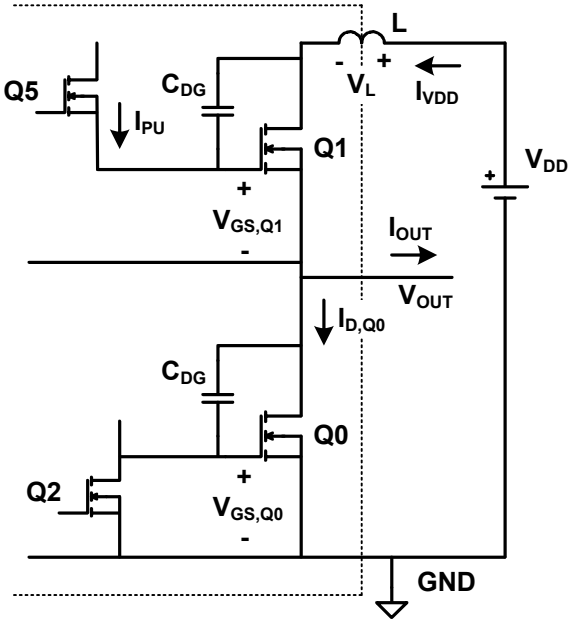


Figure 0-1: Circuit for power loss analysis with parasitic inductance

Now consider a rising edge switching transition, for $I_{OUT}>0$. Initially Q2 turns on and discharges $V_{GS,Q0}$ below Vt. V_{OUT} stays at GND potential (ignoring the forward voltage drop of the Q0 source-drain diode), because I_{OUT} is positive.

When Q5 turns on at t_2 (see Figure 1-29), it will charge $C_{DG,Q1}$ and force $V_{DS,Q1}$ to decrease at a rate of

$$\frac{dV_{DS,Q1}}{dt} = -\frac{I_{PU}}{C_{DG}} \quad t > t_2 \wedge V_{DS,Q1} > 0 \qquad \textbf{Eq. 0-3}$$

(similar to Eq. 0-2, where equality applies because I_{OUT} is positive).

Since the currents in and out of the HS switch circuit (including gate driver) must be equal, we have

$$I_{D,Q0} = I_{VDD} - I_{OUT} \qquad \textbf{Eq. 0-4}$$

V_{OUT} stays at GND potential as long as $I_{D,Q0}$ is negative, i.e. $I_{VDD} < I_{OUT}$, so Eq. 1-43 results in a linear decrease in the drain potential of Q1, i.e. a linear increase of V_L. Since

$$V_L = L\frac{dI_{VDD}}{dt} \qquad \textbf{Eq. 0-5}$$

I_{VDD} will then increase as time squared until it reaches I_{OUT} at t_{2a} in Figure 1-32. At t_{2a}, $I_{D,Q0}$ reaches 0 and changes sign, causing V_{OUT} to start increasing as given by

$$\frac{dV_{OUT}}{dt} = \frac{dV_{DS,Q0}}{dt} = \frac{I_{D,Q0}}{C_{DG}}, \quad t > t_{2a} \wedge I_{D,Q0} < I_{PD} \qquad \textbf{Eq. 0-6}$$

inserting Eq. 0-3, Eq. 0-5 and Eq. 0-6 into Eq. 0-2 gives:

$$\frac{I_{D,Q0}}{C_{DG}} - \frac{I_{PU}}{C_{DG}} + L\frac{d^2 I_{VDD}}{dt^2} = 0, \qquad \begin{cases} t > t_{2a} \\ I_{D,Q0} < I_{PD} \\ V_{DS,Q1} > 0 \end{cases} \qquad \textbf{Eq. 0-7}$$

since I_{OUT} is constant, $dI_{D,Q0}/dt$ equals dI_{VDD}/dt (differentiating Eq. 1-42), so this can be rewritten to

$$I_{D,Q0} + L \cdot C_{DG}\frac{d^2 I_{D,Q0}}{dt^2} = I_{PU}, \qquad \begin{cases} t > t_{2a} \\ I_{D,Q0} < I_{PD} \\ V_{DS,Q1} > 0 \end{cases} \qquad \textbf{Eq. 0-8}$$

which, given the initial conditions:

$$I_{D,Q0} = 0 \quad \text{and} \quad \frac{dI_{D,Q0}}{dt} = \frac{dI_{VDD}}{dt} = \frac{V_L}{L}, \quad t = t_{2a} \qquad \textbf{Eq. 0-9}$$

has the solution:

$$I_{D,Q0}(t) = \sqrt{\frac{C_{DG}}{L}} V_L(t_{2a}) \cdot \sin(\omega(t - t_{2a})) - I_{PU} \cdot \cos(\omega(t - t_{2a})) + I_{PU}, \begin{cases} t > t_{2a} \\ I_{D,Q0} < I_{PD} \\ V_{DS,Q1} > 0 \end{cases} \qquad \textbf{Eq. 0-10}$$

where

$$\omega = \sqrt{\frac{1}{L \cdot C_{DG}}} \qquad \textbf{Eq. 0-11}$$

$V_L(t_{2a})$ can be found by first finding t_{2a}-t_2, then multiplying by the voltage slope I_{PU}/C_{DG}.

$$I_{VDD}(t) = \frac{1}{L}\int_{t_2}^{t} V_L(t) \cdot dt = \frac{1}{L}\int_{t_2}^{t} \frac{I_{PU}}{C_{DG}} \cdot t \cdot dt = \frac{I_{PU}}{2L \cdot C_{DG}} \cdot (t - t_2)^2 \qquad \textbf{Eq. 0-12}$$

and since t_{2a} is the time where $I_{VDD}(t)$ reaches I_{OUT}

$$I_{OUT} = \frac{I_{PU}}{2L \cdot C_{DG}} \cdot (t_{2a} - t_2)^2 \Rightarrow t_{2a} - t_2 = \sqrt{\frac{2L \cdot C_{DG} \cdot I_{OUT}}{I_{PU}}} \qquad \textbf{Eq. 0-13}$$

$V_L(t_{2a})$ can then be found as

$$V_L(t_{2a}) = (t_{2a} - t_2) \cdot \frac{I_{PU}}{C_{DG}} = \sqrt{\frac{2L \cdot I_{PU} \cdot I_{OUT}}{C_{DG}}} \qquad \textbf{Eq. 0-14}$$

and by inserting this into Eq. 0-10 we get:

$$I_{D,Q0}(t) = \sqrt{2 \cdot I_{PU} \cdot I_{OUT}} \cdot \sin(\omega(t - t_{2a})) - I_{PU} \cdot \cos(\omega(t - t_{2a})) + I_{PU}, \begin{cases} t > t_{2a} \\ I_{D,Q0} < I_{PD} \\ V_{DS,Q1} > 0 \end{cases} \qquad \textbf{Eq. 0-15}$$

The maximum of $I_{D,Q0}(t)$ is

$$I_{D,Q0(max)} = \sqrt{\left(\sqrt{2 \cdot I_{PU} \cdot I_{OUT}}\right)^2 + {I_{PU}}^2} + I_{PU} = \sqrt{2 \cdot I_{PU} \cdot I_{OUT} + {I_{PU}}^2} + I_{PU} \qquad \textbf{Eq. 0-16}$$

The time at which this maximum occurs can be found by differentiation of Eq. 0-15:

$$\frac{dI_{D,Q0}(t)}{dt} = 0 \Leftrightarrow \omega t = a\tan\left(\frac{\sqrt{2 \cdot I_{PU} \cdot I_{OUT}}}{-I_{PU}}\right) \pm n \cdot \pi \qquad \textbf{Eq. 0-17}$$

Since the atan argument is never positive, atan evaluates to]–π/2..0], and the first positive t solution occurs for n=1. By differentiating Eq. 0-15 twice, it can be shown that this is always a maximum (not a minimum) for $I_{D,Q0}(t)$, and we get:

$$t_{ID,Q0(max)} = \frac{1}{\omega}\left[a\tan\left(\frac{\sqrt{2 \cdot I_{PU} \cdot I_{OUT}}}{-I_{PU}}\right) + \pi\right] \leq \frac{\pi}{\omega} \qquad \textbf{Eq. 0-18}$$

where the inequality applies because atan evaluates to]–π/2..0]. The latest possible maximum of $I_{D,Q0}(t)$ occurs when equality applies, i.e. for I_{OUT}=0.

Appendix II

Determination of Overcurrent Protection Thresholds for Class D Audio Amplifiers
Presented at the 23rd NORCHIP Conference
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Determination of Overcurrent Protection Thresholds for Class D Audio Amplifiers

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Abstract:

Monolithic Class-D audio amplifiers typically feature built-in overcurrent protection circuitry that shuts down the amplifier in case of a short circuit on the output speaker terminals. To minimize cost, the threshold at which the device shuts down must be set just above the maximum current that can flow in the loudspeaker during normal operation. The current required is determined by the complex loudspeaker impedance and properties of the music signals played. This work presents a statistical analysis of peak output currents when playing music on typical loudspeakers for home entertainment.

1. Introduction

A simplified schematic of a class D audio amplifier system is shown in Figure 1. The audio input signal (analog or digital) is converted to a logic-level pulse width modulated (PWM) signal by a modulator (not shown), and level shifted to produce the gate signals for the switches. The two output stage switches are turned on alternately, reproducing the PWM waveform at the switching node V_{AMP}. The demodulation LC filter then removes the switching frequency components of the PWM signal, leaving only the audio signal on the output node V_{SP}. The overcurrent protection circuit measures the output current I_{AMP} during operation, either by measuring the voltage across the output switch that conducts the current [1], or otherwise.

In a monolithic Class D amplifier design, the output stage switches take up a major fraction of the total die area, and thus the cost of build. Determination of the minimum overcurrent threshold that will not interfere with normal operation, i.e. playing music into the loudspeaker, is necessary to minimize the size of the output switches.

Previous papers have dealt with the topic of finding the maximum possible current in a loudspeaker, caused by any signal limited in magnitude to the supply voltage V_B [3], [4]. These papers are from the Class AB amplifier era, and the output current from the amplifier is considered equal to the current in the loudspeaker. As shown in Figure 1, this is not the case for Class D amplifiers, where amplifier output and loudspeaker are separated by a demodulation LC filter. For accurate results, this must be accounted for in computation. Another difference is that while traditional Class AB amplifiers employ high gain feedback loops, causing very low amplifier output impedance, many low-cost Class D amplifiers operate from purely digital input signals, and feedback cannot easily be applied. This causes significant amplifier output impedance, which must also be accounted for in computation.

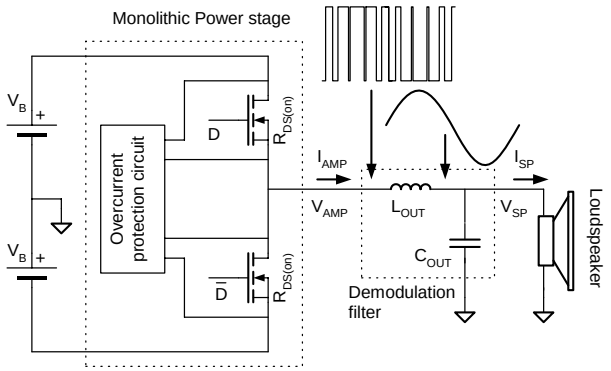

Figure 1: Simplified Class D amplifier system. The input signal is the duty cycle (D) of the gate signals for the switches.

Practical amplifiers can be implemented as shown, or 2 such output stages can be bridge connected to form one Bridge Tied Load (BTL) output stage running from a single V_B supply rail. Either way, the maximum output voltage across the loudspeaker is $\pm V_B$, and the following results apply.

2. Computation of peak current

The maximum possible peak current in a loudspeaker, caused by any signal limited to $\pm V_B$ can be derived from the complex impedance $Z_{SP}(f)$ of the loudspeaker, through the following steps:

1. Measure the complex impedance versus frequency $Z_{SP}(f)$ of the loudspeaker

2. Calculate the complex admittance $Y_{SP}(f) = 1/Z_{SP}(f)$
3. Apply an anti-aliasing filter to band-limit $Y_{SP}(f)$ and avoid discontinuity at the Nyquist frequency [3]
4. Calculate the current impulse response $y(t) = IFFT(Y_{SP}(f))$
5. The maximum current signal is $V_B \cdot sign(y(-t)) * y(t)$

This procedure is described in [2] and [3] and will not be detailed here. An example of y(t) for a loudspeaker is shown below

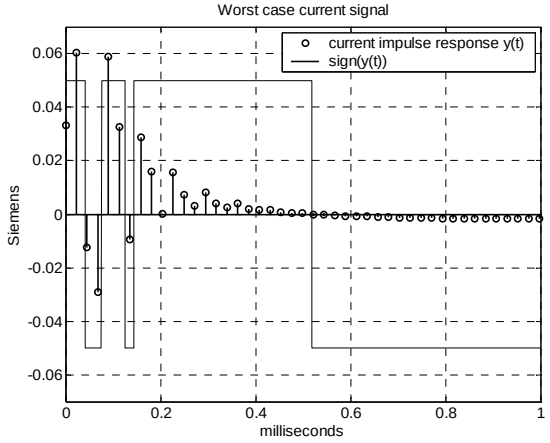

Figure 2: Derivation of the voltage waveform that will produce the maximum possible peak current in a loudspeaker. The amplitude of sign(y(t)) is arbitrarily set to 0.05 to fit in the figure.

y(t) is the current impulse response, i.e. the current waveform the would flow in the loudspeaker in response to an impulse voltage of unit area. The current in the loudspeaker when driven by any voltage waveform v(t) can be found by convolution of v(t) with the current impulse response, i.e.

$$I_{SP}(t) = V_{SP}(t) * y(t) \qquad (1)$$

sign(y(t)) plotted in Figure 2 illustrates why $V_{SP}(t)=V_B \cdot sign(y(-t))$ is the voltage waveform that will produce the maximum possible convolution integral with y(t), and thus the maximum peak current $I_{SP}(t)$, when applied to the loudspeaker. The time inversion in y(-t) occurs because of the time inversion inherent to convolution.

Since an on-chip overcurrent protection system like the one shown in Figure 1 has no access to the actual loudspeaker current $I_{SP}(t)$, the current limit is instead enforced on the amplifier output current $I_{AMP}(t)$. To calculate the maximum possible current $I_{AMP}(t)$, rather than $I_{SP}(t)$, the calculation must be based not just on $Z_{SP}(f)$ alone, but on the total impedance of output filter and loudspeaker, as seen from the switching output terminal V_{AMP} on the amplifier. Referring to the components in Figure 1, the load impedance at this point is given by

$$Z_{AMP}(f) = \frac{Z_{RL} \cdot Z_{SP} + Z_{RL} \cdot Z_C + Z_{SP} \cdot Z_C}{Z_C}$$

where

$$Z_C = \frac{1}{i2\pi \cdot f \cdot C_{OUT}} \qquad (2)$$

$$Z_{RL} = R_{OUT} + i2\pi \cdot f \cdot L_{OUT}$$

$$Z_{SP} = Z_{SP}(f)$$

and R_{OUT} is the total output impedance of the amplifier at the loudspeaker terminals.

Since one of the output stage switches is turned on at any point in time, the on-resistance $R_{DS(on)}$ will act exactly like series resistance in the output inductor L_{OUT} and R_{OUT} is the sum of $R_{DS(on)}$ and the actual inductor series resistance R_{LOUT}. For BTL configurations, each half of the output stage has its own output LC filter and contribution to output resistance. Since the two output filter capacitors, as seen from the loudspeaker terminals, are series connected, we get

$$R_{OUT} = 2 \cdot R_{DS(on)} + 2 \cdot R_{LOUT,BTL}$$

$$L_{OUT} = 2 \cdot L_{OUT,BTL}$$

$$C_{OUT} = \frac{1}{2} C_{OUT,BTL}$$

to be used in equation (2) for a BTL power stage.

3. Calculated vs. Measured maximum currents

As indicated in Figure 2, y(t) is only defined in discrete time, due to the finite frequency range of the impedance measurement $Z_{SP}(f)$, from which it is found. The sampling interval is determined by the frequency range of $Z_{SP}(f)$, and if the measurement frequency limit is set to 22050Hz, the sampling frequency will be 44100Hz, which is the sampling frequency of audio CDs. The worst case current excitation signal sign(y(-t)) can then be written onto an audio CD at maximum signal level, and played on the loudspeaker to verify the worst case current by measurement. This has been done for 4 different loudspeakers, and the results are shown in **Figure 3**.

The loudspeakers selected are not particularly high-end, but represent those typically shipped with medium-powered home theatre solutions, since this is the primary market space for monolithic Class D amplifiers.

The checkered bars are measured peak currents when playing the sign(y(-t)) functions from the CD on each respective loudspeaker. The amplifier used was a BTL Class D amplifier without feedback, and with total R_{OUT} of 0.50 ohms. The measured current has been normalized by the supply voltage V_B.

The calculated maximum currents are found by use of equation (1), where y(t) in the case of the vertically-striped bars is based just on the measured

$Z_{SP}(f)$+0.50ohm, i.e. the amplifier output resistance is accounted for, but the LC output filter is not. These results are seen to be very inaccurate, more that a factor of two in case of the Panasonic Satellite loudspeaker. The non-systematic nature of the errors means the results can not be used even as best- or worst-case estimates. For the horizontally-striped bars, the calculation of y(t) is based on $Z_{AMP}(f)$ as given by equation (2), thereby accounting for both the output resistance and LC filter components. With the exception of the Kenwood loudspeaker, these results are more accurate, illustrating the importance of including the LC filter in the calculations.

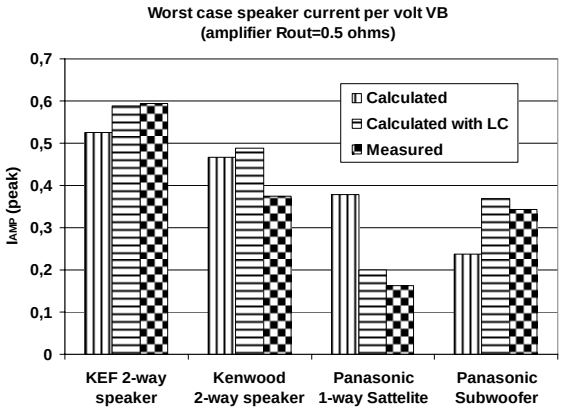

Figure 3: Calculated vs. measured worst case currents for 4 loudspeakers

The remaining inaccuracies are believed to be related to the fact that the calculated results are derived from an $Z_{SP}(f)$, which is in fact only a small signal model of the loudspeaker. During measurement of the worst case currents, the loudspeaker membranes had quite large excursions, even though the amplifier supply voltage was kept at a moderate level of V_B=3V. Using even lower V_B voltages might have resulted in better agreement between calculation and measurement. This deserves a more detailed study, since the final interest obviously is the level of peak currents that occur when amplifiers operate at realistic supply voltages.

4. Statistical analysis with music signals

The currents measured and calculated above are very large compared to the nominal impedances of the loudspeakers. The KEF 2-way speaker (KEF KHT2005.2) is labeled 8 ohms, but its worst case peak current is almost 0.6A per volt V_B.

For low cost audio amplifiers it may not always realistic to design the output stage to deliver the current needed under absolute worst case conditions. Such amplifiers can instead be designed so that in case of an overcurrent detection, they only shut down the output stage briefly, and then restart it, rather than shutting down the amplifier completely. If implemented correctly, the resulting drop-outs can be almost inaudible, given that they are brief and occur rarely.

This calls for an analysis of music signals, to determine how likely it is for a typical music signal to cause a given peak current level in a loudspeaker load. To answer this, a selection of 32 CD music tracks from varied genres has been analyzed. Using y(t) for the KEF 2-way loudspeaker, the entire current waveform $I_{SP}(t)$ resulting from playing each music track at full volume[1] into the loudspeaker has been calculated by use of equation (1). The peak current for each track can then be found from each calculated waveform. The 32 results so obtained had a mean value of μ =0.196A and a standard deviation of σ =0.049A. Based on these numbers, the probability that a randomly selected audio track will produce a peak current that exceeds a current I is given by:

$$P\{I_{SP,PEAK} > I\} = 1 - \Phi\{I\}$$

where Φ(I) is the cumulative normal distribution with mean μ and standard deviation σ.

$P\{I_{SP,PEAK} > I\}$ is graphed in Figure 4. The figure should be read as follows: The curve "Music, gain=0dB" is at 47% for 0.20A. This means that based on the distribution of peak currents from the 32 music tracks analyzed, 47% of randomly selected tracks will produce an output current peak of 0.20A/V_B or more, when played at full volume into the KEF 2-way loudspeaker. The vertical lines show similar results for load resistors of selected values. Here there is no variation in current since for a resistive load R, any output signal with a peak voltage of $\pm V_B$ will produce a peak current of $\pm V_B$/R. Taking R_{OUT} into account, all 32 audio tracks would produce a current of $V_B/(8+0.5)$= 0.12A/V_B into an 8 ohm resistor, as indicated by the line "Nominal imp (8 ohms)". This shows that 94% of randomly selected audio tracks will produce a larger peak current into the KEF 2-way speaker than into an 8 ohm resistor. Similarly, 15% of randomly selected tracks will produce larger peak current than a load resistor with the same value as the minimum impedance of the loudspeaker, which is 3.3 ohms at 350Hz. The "Worst case" line indicates the maximum possible current from Figure 3.

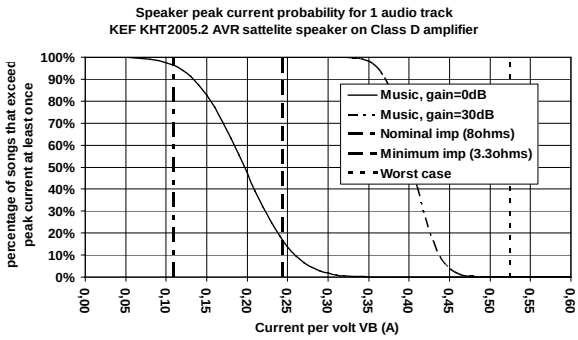

Figure 4: Statistical distribution of loudspeaker peak current, playing one CD track

The results so far are based on playing music at full volume, but without overdrive (clipping). Most amplifier

[1] Full volume is defined such that an all-zero digital code on the CD produces a no-load amplifier output voltage of $-V_B$ V, and an all-one digital code $+V_B$ V.

products have the feature of applying gain to the audio input signal (analog or digital), with signal clipping as a result. In some end user products as much as 30dB gain can be applied to a digital input signal which may already utilize the full digital headroom. Though this results in severe distortion and very low audio fidelity, the situation is technically within normal operation of the amplifier, and must be accounted for in design.

Calculation of peak currents that occur when playing 30dB overdriven audio into the KEF 2-way speaker has been made simply by applying 30dB gain to the 32 audio tracks (still constrained by the range of the digital code), and then convoluting the result by the current impulse response y(t). The resulting distribution of peak currents is shown by the curve "Music, gain=30dB" in Figure 4. The peak currents are now much higher, which is not surprising from the intuitive point of view that a heavily clipped audio signal bears stronger resemblance with the worst-case signal shown in Figure 2, than an unclipped signal does.

For designs where a very low rate of system drop-outs is required, the probability that a given output current will be exceeded at least once per n (rather than 1) audio tracks can be found simply by

$$P_n\left\{I_{SP,PEAK} > I\right\} = 1 - \Phi\left\{I\right\}^n$$

where $\Phi(I)$ is the cumulative normal distribution with mean μ and standard deviation σ.

This probability function is plotted below for n=100 and 0dB vs. 30dB gain, based on the same data as Figure 4.

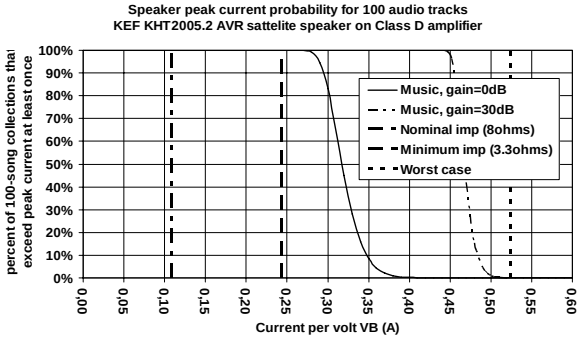

Figure 5: Statistical distribution of peak current, playing 100 CD tracks

It is seen that when playing back 100 audio tracks into this loudspeaker, the probability that current will at some point exceed that of a load resistor with the same value as the minimum loudspeaker impedance (3.3 ohms) driven by the same signal, is almost 1. This contradicts measured results in [4], where this is claimed not to have happened for hundreds of hours of music played on 7 different loudspeakers.

It is also seen that the probability of the output current exceeding $0.4A/V_B$ is very small (unless the signal is clipped). Setting the overcurrent threshold at this level would thus result in very infrequent drop-outs. For a supply voltage of V_B=30V, it corresponds to $30 \cdot 0.4$=12A.

The above analysis can readily be applied to any given amplifier with any given loudspeaker. This is useful for systems where the loudspeakers are sold bundled with the amplifier, as is common for lower-power amplifiers that employ monolithic Class-D output stages. For higher power solutions, where amplifier and loudspeakers are typically sold separately, a number of loudspeakers that represent those typically used with an amplifier can be analyzed. It is worth noting that higher power multi-driver loudspeakers will tend to cause higher peak currents (even for the same nominal impedance) due to the higher complexity of the crossover networks [3].

5. Summary

A method for calculating maximum peak currents for given combinations of amplifiers and loudspeakers has been presented. The basic approach has been described in earlier papers, but the effects of amplifier output resistance and the LC output filters used in Class D amplifiers have been included in calculations here. It has been shown that these additions are necessary to obtain results of useful accuracy for Class D amplifier systems.

Since it is not always realistic to design low cost amplifier systems for the absolute worst case current, a statistical analysis of peak currents during normal music playing has been added. The results for a single loudspeaker chosen for this analysis contradict those of [4], since it is shown that the output current will frequently exceed that of a resistor with the same value as the minimum impedance of the loudspeaker, driven by the same signal.

Finally, it is shown that overdriving the audio signal increases the peak currents significantly.

6. References

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Appendix III

Time Domain Analysis of Open Loop Distortion in Class-D Amplifier Output Stages
Presented at the 27th Audio Engineering Society (AES) Conference,
Hillerød, Denmark, September 2-4 2005

TIME DOMAIN ANALYSIS OF OPEN LOOP DISTORTION IN CLASS D AMPLIFIER OUTPUT STAGES

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During the long history of Class AB amplifiers, many topology improvements have been developed with the aim of reducing open-loop THD. Cascode stages, local feedback loops, and strategically placed linearizing resistors are some of the tricks known to all Class AB designers. As Class D amplifiers become widely used, a new learning of such improvements is needed, since the basic distortion mechanisms are very different from those of Class AB amplifiers. This is even more important with Class D designs because the very high feedback loop gains seen in Class AB designs are not always achievable in Class D designs, and in some cases no feedback is used at all, because it cannot easily be applied to digital input systems at low cost. This paper analyzes the nature of different contributors to THD in Class D output stages: Dead time, Body diode conduction, and the speed of output switch turn-off and turn-on. It is shown how large-signal transfer characteristic analysis can be applied to individual parts of a PWM output signal, to help identify problems and optimize a design for minimum THD.

INTRODUCTION

Amplifier distortion is typically shown as plots of THD versus signal level or frequency. While these may be adequate metrics for overall linearity, they convey little information about the root causes of the distortion shown. Finding the relations between design parameters and the resulting THD graphs can thus be a cumbersome trial and error work process. While FFT plots provide more information by showing the spectral content of the distortion at a given signal level and frequency, this information may still not reveal the root causes.

A conceptually more indicative way of displaying amplifier nonlinearity is the transfer characteristic, output voltage versus input voltage. This allows for straightforward distinction of e.g. zero-crossing distortion from other types of distortion. Since any practical audio amplifier is linear enough that its Vout/Vin transfer characteristic looks perfectly straight to the naked eye, the best-fit straight line can be subtracted from the transfer characteristic, to emphasize the nonlinearity. Using this approach, some of the most fundamental nonlinearities of Class D output stages are discussed in this paper.

A more complete mathematical analysis of these and other nonlinearities is given in [1]. However the effect of switch output capacitance on the switching waveform during the dead time segment is not included, nor is optimization of switching speeds (other than stating that fast switching minimizes errors).

These mechanisms are analyzed in this paper, and is it shown that for a given switch output capacitance, optimum linearity is achieved when a certain relation between dead time, turn-off and turn-on speed is satisfied.

SCOPE

Only distortion that origins from the switching output stage is considered. The input signal to the output stage is assumed to be a Pulse Width Modulated (PWM) digital signal, generated by a modulator, from an analog or digital input audio signal.

There are many possible configurations of Class D output stages, and the one selected for this discussion is a 2-switch buck-converter based (single ended) topology, supplied by a single positive supply rail. The methodology as well as main results applies to other topologies as well. Specifically, it can be shown that a 4-switch Bridge Tied Load (BTL) configuration, where each speaker terminal is driven by a 2-switch output stage like the one analyzed in this paper, has the same odd-ordered distortion components as each of the two outputs, while the even ordered components cancel, because they only present a common mode signal to the

speaker terminals. With this in mind, the analysis applies to both single ended and BTL output stages.
The loudspeaker load is assumed to be purely resistive. While a resistor is in fact a quite poor model of a loudspeaker for this purpose, the THD specifications of interest to the mass market are still commonly measured using only resistive loading.

1 LARGE SIGNAL TIME DOMAIN ANALYSIS

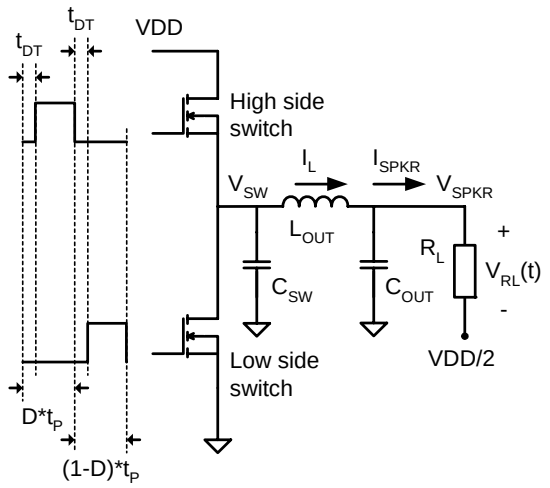

Figure 1: Output stage with demodulation filter L_{OUT} and C_{OUT} and load R_L. For a single ended system, R_L represents the loudspeaker resistance, and the VDD/2 terminal voltage must be provided by a DC blocking capacitor or by the power supply. For a BTL system, the speaker is connected to the outputs of two identical output stages, and R_L represents only half the loudspeaker resistance. $t_P=1/f_s$ is the duration of one PWM period, typically a few microseconds. I_{SPKR} is the output current. I_L is the output inductor current, equal to I_{SPKR} plus the triangular switching ripple current. C_{SW} is the combined output capacitance of the two switches.

Since this paper concerns only the distortion arising from the switching output stage, V_{SPKR} is graphed versus PWM input duty cycle, not input voltage.
Consider the system shown in Figure 1. The switches are controlled by the PWM signal, which at a given time has a duty cycle D. The output stage reproduces this signal at its output V_{SW}, at a voltage amplitude of VDD. To avoid large transient currents during switching, one switch must be turned off before the other is turned on, and in a small time interval t_{DT}, both switches are off. The value of t_{DT} is referred to as *dead time*. A lossless output stage with zero dead time would provide a steady state output voltage of exactly D•VDD at node V_{SPKR}, but any actual output stage has deviations from this, some of which are causing distortion of the audio signal.

An example of such deviations is shown in Figure 2. The actual error voltage has been divided by VDD, to create a normalized value. The intent of this is to make it easy to judge the severity of the errors compared to the maximum output signal. It does not mean that the system would actually produce the shown error voltage if supplied by a VDD voltage of 1V, since not all error mechanisms exhibit such linearity. Since the error voltage at a given duty cycle D also depends on the output current I_{SPKR}, the curve can only represent nonlinearity for given values of VDD and R_L. This is similar to a THD vs. level plot, and in fact there is an injective mapping from the plot shown in Figure 2 to THD versus signal level.

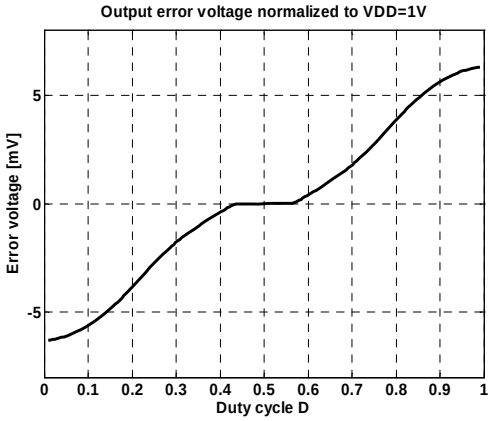

Figure 2: An alternative display of distortion; the normalized output voltage error vs. duty cycle D. A straight line ax+b has been subtracted from the curve to achieve zero value and zero slope at D=0.5, in order to emphasize the nonlinearity

1.1 Time invariance

A graph like the one shown in Figure 2 shows no information about the dependency of distortion on audio signal frequency, though multiple curves on the same plot could be used to display the transfer characteristic at different audio frequencies.
For the purpose of further analysis, the distortion of the output stage is considered to be independent of audio frequency, which is equivalent to assuming a time invariant transfer characteristic from input duty cycle to output voltage.
This assumption can be justified for the switching output stage itself, since its nonlinearities are basically time invariant, when thermal effects are ignored. The phase shift of the output demodulation filter can also be disregarded, because the cutoff frequencies used are typically much higher than maximum audio frequency, for reasons of minimizing inductor cost or, when feedback is used, maximizing loop gain. For high audio frequencies, the output filter will reduce distortion by

attenuating high order harmonic components. This will also be ignored here, considering only the distortion at frequencies too low for this effect to be significant.
In practice, the total open loop THD for Class D amplifiers is indeed frequency dependent, but mostly because of the variation of power supply impedance over the audio band, and because of output filter inductor core losses. Because these errors occur outside the switching output stage, they are outside the scope of this paper.
When the transfer characteristic is considered time invariant, it follows that for any duty cycle D, there is a given voltage V_{SPKR}, and thus a given output current I_{SPKR}, determined by the load resistance.
V_{SPKR} will be equal to the periodic average of the voltage V_{SW}. The series resistance of the output inductor can be ignored for distortion analysis, since it causes only a gain loss. This in turn implies that instead of basing distortion analysis on the transfer characteristic from duty cycle to V_{SPKR}, as shown in Figure 2, the analysis can instead be based on the periodic average voltage on the V_{SW} node, which for a given VDD and load resistance is only a function of duty cycle D. Plotting the periodic average of V_{SW} versus D would indeed produce the same graph as shown in Figure 2.

1.2 Time segmentation

The construction of the PWM output signal can be split into different time segments, each of which has a

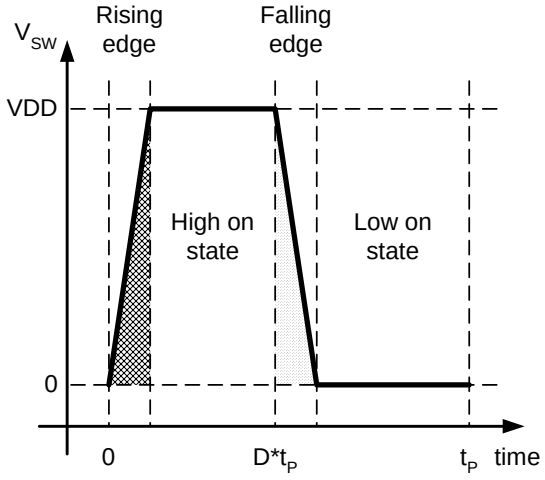

Figure 3: One period of the PWM signal, divided into 4 time segments, rise, high, fall, and low, for individual analysis of associated nonlinearities

specific set of associated nonlinearities. The analysis of distortion based on the periodic average of the V_{SW} voltage provides the possibility of isolating each time segment from the others, thereby analysing distortion from each segment separately. Figure 3 shows a division of one period of a PWM signal into 4 time segments: rise, high, fall, and low. For any given duty cycle D, each segment has its own average voltage, and contributes to the overall periodic average by a share proportional to the duration of the segment. The switching transition segments (shown wider than they are for clarity) make a small relative contribution due to their short duration, but can be very nonlinear, and still produce significant distortion.
In some cases, the nonlinearity of one time segment can cancel that of another. Since the resulting THD is only a function of the time-weighted sum of the average voltages of all time segments, it may not always be optimal to make each isolated segment as linear as possible.

2 NONLINEARITY EXAMPLES

This section shows and explains some typical nonlinearities associated with each of the PWM signal time segments shown in Figure 3.

2.1 The high-on and low-on states

At duty cycles close to 1, I_L is continuously positive, and if MOSFET type switches are used, the body diode of the low side switch can conduct part of the current. The voltage drop across the switch then becomes a nonlinear function of I_L, which causes distortion. As duty cycle goes towards one, the error goes towards 0 as the duration of the low-side on-state diminishes. A similar condition exists for the high side switch at low duty cycle values and negative I_L. An example of such errors is shown in Figure 4, for MOSFETs with channel $R_{DS(ON)}$ of 120mΩ and a body diode with an ideal exponential diode I/V characteristic

$$I_D = Is \cdot \left(e^{\frac{V_D}{Vt}} - 1 \right)$$

Where *Is* is set to $1.97 \cdot 10^{-13}$ A and Vt to 25.3mV.

Diode conduction errors become more pronounced at high temperature, where the body diodes conduct a larger fraction of the output current as $R_{DS(ON)}$ and Is increase with temperature.

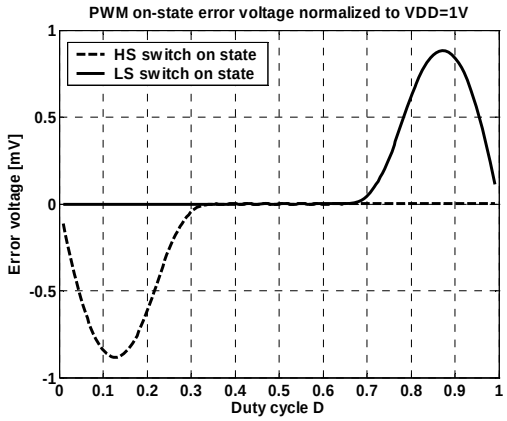

Figure 4: Example of output voltage errors from MOSFET body diode conduction at VDD=50V and R_L=4Ω. A normalized error voltage of 1mV can cause in the order of 0.1% THD

Note that the error is always caused by the switch which is on for the shortest duration, i.e. the low side (LS) error occurs for large duty cycle and vice versa.
Contrary to most distortion contributions, the one from diode conduction is expanding (adds to the output voltage), rather than compressing. This opens the possibility that other compressing distortion components could in part cancel the distortion from diode conduction.

2.2 The rising and falling edge switching transitions

The rising edge switching transition waveform depends on the output inductor current I_L at the time of switching. The average voltage on the switching node in a narrow time window around the transition is a nonlinear function of speaker current, and this causes distortion. Many mechanisms influence the exact switching waveform for a given switching current I_L, and a description of some of them is given below. In practice the switching node capacitance C_{SW} is nonlinear but even though it is assumed linear in the following, its basic impact on distortion can still be shown.
Consider again the system shown in Figure 1, where the on-resistance of the switches is ignored for now. V_{SW} will be at VDD or ground potential if either switch is on. In the dead time intervals, both switches are off, and the V_{SW} waveform is determined by the output inductor current I_L, charging or discharging the switching node capacitance C_{SW}. 3 different scenarios occur, depending on I_L. These are indicated by a), b), and c) in Figure 5.
In scenario a), the output inductor current is positive, and V_{SW} stays at ground potential until the high side switch turns on. In scenario b), the output current is negative, and charges the switching node capacitance Csw. However, its voltage V_{SW} does not reach VDD before the high side switch turns on. In this case, the average voltage in the dead time segment increases linearly as I_L becomes more negative. In scenario c), the output current is negative enough to charge the V_{SW} node to VDD potential before the high side switch turns on. In this case the increase in average voltage is no longer a linear function of I_L. As I_L becomes more negative, the average voltage follows a hyperbolic function, converging towards a boundary voltage as I_L goes towards minus infinity.

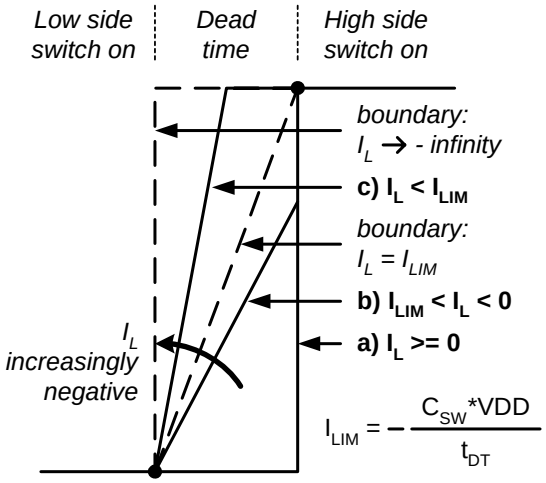

Figure 5: 3 different scenarios of a rising edge transition, depending on I_L at the time of switching.

For one specific value of I_L, the V_{SW} node will be charged and reach VDD exactly as the high side switch turns on. This current is denoted I_{LIM} in Figure 5, and is the boundary current between scenarios b) and c). Symmetrical conditions exist for the falling edge switching transition.
If the switching capacitance C_{SW} was disregarded in the analysis I_{LIM} would become 0, as shown by the equation in Figure 5. This means that scenario b) vanishes, leaving only scenario a) and the boundary condition of scenario c) for $I_L \rightarrow \infty$. Such analysis of dead time distortion have been presented in [2] and [3], and are very reasonable for large values of dead time applicable in closed-loop systems, since large dead time t_{DT} causes actual near-zero I_{LIM} values even in the presence of the switching capacitance C_{SW}. Open-loop systems, on the other hand, typically use much smaller dead time values in order to achieve acceptable THD in the absence of feedback to suppress the nonlinearity. This causes larger I_{LIM} values, and thus a wider scenario b) region that acts as a gradual transition between scenarios a) and c). Consequently, the 3-scenario analysis of dead time nonlinearities presented here is feasible mostly for systems with small dead time.
For a given value of duty cycle D in the range 0 to 1, and ignoring the voltage drop across of the output stage

switches, the inductor current I_L at the time of the switching transition is given by

$$I_L(D) = I_{SPKR}(D) \pm I_{RIP}(D) = \frac{VDD}{R_L} \cdot \left(D - \tfrac{1}{2}\right) \pm \frac{VDD \cdot t_p}{2 \cdot L_{OUT}} \cdot \left(D - D^2\right) \quad \text{Eq. 1}$$

where + corresponds to the falling edge transition and – corresponds to the rising edge transition. Using these values for I_L at the times of switching, and applying the geometry of the switching waveforms shown in Figure 5, the contribution of the switching node voltage during each dead time interval to the average output voltage can be found, and is shown in Figure 6.

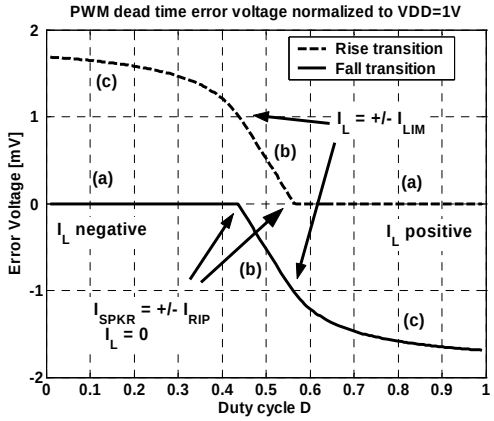

Figure 6: Output voltage errors caused by 5ns dead time at fs=384kHz. The curves are found from the geometry of the curves in Figure 5, and the labels (a), (b) and (c) correspond to the 3 scenarios. The scenario c) error converges towards a boundary value of 5ns•1V•384kHz=1.92mV. I_L is zero during switching at when I_{SPKR} equals the inductor ripple current I_{RIP}. Most of the distortion related to dead time is caused by the sharp kinks in the curves at this point.

For each transition, rising and falling, zero I_L occurs at the duty cycle value where the two terms in Eq. 1 cancel, and this determines the boundary between scenarios a) and b).

The combined effect of the rising and falling edge transitions on the output signal is seen by adding the values of the two curves in Figure 6. Since the parts of the curves that correspond to scenario b) are completely straight lines, the combined error voltage will be 0 in the vicinity of D=0.5 if and only if $I_{LIM} > I_{RIP}$. This reduces THD significantly at low signal levels, and can be achieved in systems with small enough dead time to causing a large enough I_{LIM} value. Since I_{RIP} can be selected by choice of output inductor value L_{OUT}, the requirement can be translated into a minimum inductance for a given system.

2.3 Finite-speed turn-on

The above analysis assumes that the output stage switches turn on in zero time. Consequently, the scenario a) waveform in Figure 5 is considered unchanged for any positive I_L value. In practice, increasing I_L current will delay this rising edge transition, because the drive current of the high-side switch must reach a larger value before the transition starts. This causes a decrease in average V_{SW} voltage as I_L increases, but only for positive I_L values. This decrease is not a linear function of I_L, but for simplicity it is assumed to be so in the following analysis, and important results can still be derived under this assumption. The impact of finite turn-on speed on average V_{SW} voltage in each dead time segment is shown in Figure 7.

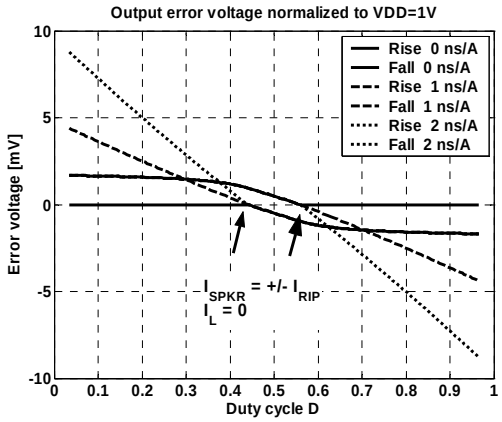

Figure 7: Switching transition errors for different turn-on speeds of the output switches. 0 ns/A curves are identical to Figure 6. Slower turn-on straightens the kink that otherwise occurs when I_L changes sign, with an optimum value of about 1 ns/A.

A slower turn-on tends to straighten the kink that occurs at I_L=0 for both rising and falling edge transition average voltages. If the switch output capacitance C_{SW} was not taken into consideration, the kink would be a right angle, and could not be straightened this way.

2.4 Finite-speed turn-off

The effect of finite-speed switch turn-off is similar to that of finite-speed turn-on, but affects the switching waveform for the opposite sign of I_L, i.e. negative I_L for rising edge transitions and positive I_L for falling edge transitions. A slower turn-off will increase the bending of the kink on the voltage error curves at I_L=0 (see Figure 6). Thus, to straighten the kink, the turn-on must be slow enough to match the combined kink

contributions from the finite turn-off speed and the dead time. Consequently, optimum THD is achieved with a turn-on speed which is slower than the turn-off speed by a certain amount.
An approach has been presented that eliminates dead time altogether [4]. This flattens out regions a), b) and c) in Figure 6 to zero. However, for avoidance of large transient currents, such a design requires that the turn-on speed is much slower than the turn-off speed, and in absence of any kink caused by dead time, this difference in strength will itself cause a kink at I_L=0.
Turn-on and turn-off switching speeds can be controlled by adjusting the pull-up and pull-down strengths of the gate drive circuits that control the output switches.
The lowest overall THD at all signal levels is not necessarily achieved when the kink at I_L=0 is completely straight, since a moderate kink may in part cancel the effect of the bending of the hyperbolic error curve in scenario c), for signal levels large enough to include both errors.

3 EFFECT OF TURN-ON SPEED ON THD CURVES

While the voltage error curves discussed above serve the purpose of depicting individual nonlinearities, the final metric of interest is still low overall THD.
For the output stage shown in Figure 1, the undistorted voltage across the load resistor during sine wave playback is given by

$$V_{RL(IDEAL)}(t) = VDD/2 \cdot M \cdot \cos(\omega \cdot t)$$

Where VDD is the supply voltage, and M is the modulation depth, in the range 0 to 1. The error voltage on the output during the same time is

$$V_{RL(DIST)}(t) = VDD \cdot Ve\left(0.5 \cdot \left(1 + M \cdot \cos(\omega \cdot t)\right)\right)$$

Where Ve(D) is the normalized error voltage as a function of duty cycle D in the range 0 to 1, e.g. like the function graphed in Figure 2.
The total voltage across the load resistor is the sum of the ideal output voltage and the error voltage

$$V_{RL(TOTAL)}(t) = V_{RL(IDEAL)}(t) + V_{RL(DIST)}(t)$$

For any given modulation depth M, the Fourier transform of $V_{RL,TOTAL}(t)$ will show the distortion spectrum and hence the THD value, caused by a given voltage error function Ve(D).
This has been applied to each of the error voltage functions shown in Figure 7, and Figure 8 thus shows the effect of changing turn-on speed on THD versus signal level. Lowest THD is achieved for a turn-on speed of 1 ns/A, which is also the value that visually produces the best straightening of the kinks on the voltage error curves in Figure 7.
Since the error voltage function Ve(D) can be found for different nonlinearities individually, THD vs. level graphs related to individual errors can also be found, keeping in mind that there is no general rule of superposition for the THD contributions. Further, by measuring Ve(D) in an individual time segment, e.g. a narrow time window around the rising edge switching transition, THD vs. level related only to that transition can be calculated and plotted. Care must be taken not to introduce significant measurement errors caused by the limited voltage resolution of oscilloscopes.

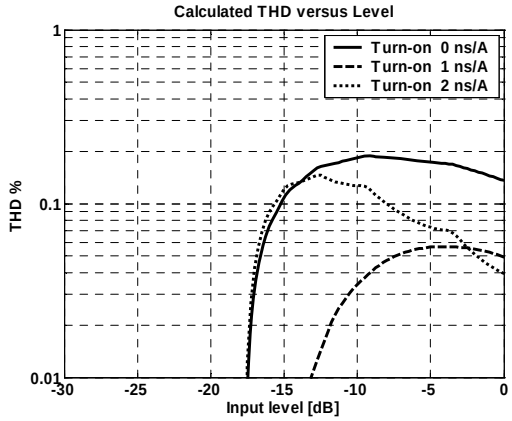

Figure 8: Calculated THD versus signal level, showing the effect of switch turn-on strength. An infinitely fast turn-off is used for this calculation.

4 CONCLUSIONS

This paper has described how time domain analysis of Class D amplifier nonlinearities can be used to quantify root cause distortion mechanisms in much greater detail than THD graphs.
Switching transition delays cause changes in average switching voltage which depend on inductor current I_L in a nonlinear fashion. Fast turn-on and turn-off of the switches minimize the magnitude of these errors, but lowest overall distortion is achieved when the turn-on is slower than the turn-off by a certain amount, since this partly cancels the error caused by dead time. This implies that optimum turn-on speed is finite.
Similarly, it can be shown that for a system with a given turn-off speed and slower turn-on speed, the lowest distortion is achieved for a dead time greater than zero. This is useful for avoidance of transient current problems associated with very low dead time values. The existence of this relation between dead time, turn-off and turn-on speed can only be shown when the capacitance of the switching output node is taken into account.

The output stage nonlinearities discussed here are only a small selection of mechanisms influencing Class D amplifier distortion. The analysis does not attempt to be complete, but to serve as an example of the application of time domain analysis to distortion optimization.
The error voltage graphs shown in this paper are calculated by simple mathematical models of the nonlinearities of concern. In product development, the same methodology can be applied to circuit simulation, including many of the nonlinear effects that are ignored in this presentation. It can also be applied to laboratory optimization, by making time-gated average voltage measurements on actual systems.

ACKNOWLEDGEMENTS

The authors would like to thank Claus Neesgaard, Texas Instruments, for his contributions to the ideas described in this paper.

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[3] Marco Berkhout, *An Integrated 200-W Class-D Audio Amplifier*. IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 38, NO. 7, JULY 2003

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Appendix IV

A 240W Monolithic Class D Audio Amplifier Output Stage
Presented at the 2006 IEEE International Solid-State Circuits Conference (ISSCC)
San Francisco, CA, February 5-9 2006

19.1 A 240W Monolithic Class-D Audio Amplifier Output Stage

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The audio amplifier market continuously demands improved performance at low cost. Apart from reliability, 3 performance criteria are of main interest: output power, idle loss and THD. Low THD should preferably be achieved open-loop, since a feedback loop cannot be easily added if the signal path is fully digital. For an integrated Class-D amplifier as shown in Fig. 19.1.1, all 3 performance criteria are influenced primarily by the timing and electrical characteristics of the gate drives, i.e., the circuits that drive the gates of the output switches. The input is a PWM audio signal, reproduced by the output stage at the V_{OUT} node. The external lowpass filter, L_{OUT} and C_{OUT}, reconstructs the analog audio signal on the loudspeaker terminal. The filter must be close to critically damped with a 4 to 8Ω load and provide maximum attenuation of the PWM carrier. This means that no degrees of freedom are left in its design, and L_{OUT} and C_{OUT} are considered fixed in the following. The influences of the gate drive output characteristics on each of the 3 main performance criteria are discussed below.

The V_{DS} voltage rating of the output LDMOS devices $Q0$ and $Q1$ (Fig. 19.1.2) sets a hard limit on the output power that can be delivered to a given load resistance. The supply voltage V_{DD} must be less than the device V_{DS} voltage rating by an amount large enough to account for the inevitable switching voltage overshoots. The size of the gate drive pull-down devices $Q2$ and $Q4$ influences the switching overshoots, and thus the achievable output power. For a rising-edge transition with a large output current I_{OUT}, the voltage at the output node V_{OUT} exceeds V_{DD} while the current builds up in the parasitic inductance L_{VDD} of the power-supply decoupling network. Neglecting all parasitic capacitances other than C_{GD} (which is acceptable for LDMOS transistors working in the saturation region), it can be shown that the peak drain-source voltage $V_{DS,p,Q0}$ for $Q0$ can be approximated by

$$V_{DS,p,Q0} \cong V_{DD} + \sqrt{I_{OUT} \cdot \frac{2 \cdot L_{VDD}}{C_{GD}} \cdot \frac{V_{GS,Q0}}{R_{DS,Q2}}} \qquad (1)$$

where C_{GD} is the gate-drain capacitance of $Q0$ or $Q1$ (considered identical), $V_{GS,Q0}$ is the gate-source voltage required by $Q0$ to conduct I_{OUT} (neglecting the fraction of I_{OUT} flowing into $C_{GD,Q0}$), and $R_{DS,Q2}$ is the channel resistance of $Q2$. It is clear that the second term in (1) can be reduced by increasing $R_{DS,Q2}$, i.e., by reducing the width of the gate drive pull-down device $Q2$. This allows the use of a higher V_{DD} without exceeding device ratings, which in turn increases the achievable output power. Symmetrical conditions result in the same dependence of $V_{DS,p,Q1}$ on the width of $Q4$. Another important performance parameter for Class-D amplifiers is idle power losses, which must be kept low, since the noise of a cooling air fan cannot be tolerated at low music volume. During idle operation, I_{OUT} equals the switching ripple current (see Fig. 19.1.3). For each rising-edge transition, I_{OUT} will charge the output node V_{OUT} towards V_{DD} right after $Q0$ is turned off. This charging process is referred to as autocommutation, and is almost lossless, since charge is merely moved from $C_{GD,Q1}$ to $C_{GD,Q0}$. However, if the current in $C_{GD,Q0}$ is large enough to cause a voltage drop across $Q2$ which exceeds the $Q0$ threshold voltage V_t, $Q0$ will conduct part of I_{OUT}, and the resulting power dissipation in $Q0$ will increase power losses. It can easily be shown that this loss is avoided if:

$$R_{DS,Q2} < \frac{16 \cdot V_t \cdot f_s \cdot L_{OUT}}{V_{DD}} \qquad (2)$$

(and similarly for $R_{DS,Q4}$ for the falling edge transition). This leads to an important design tradeoff for higher output power: Since a higher-power output stage must operate from a larger V_{DD} voltage, the widths of $Q2$ and $Q4$ must be increased to satisfy (2) and maintain low idle losses. However, this increases the overshoot voltages as given by (1). This effect is further accelerated by a larger I_{OUT}, and causes diminishing returns in terms of the output power achievable from higher voltage process nodes.

Low power losses also require avoiding any overlap between the conduction times for $Q0$ and $Q1$ during transitions. It has been shown that this sets an upper bound on the ratio $R_{DS,Q2}/R_{DS,Q5}$ (and similarly $R_{DS,Q4}/R_{DS,Q3}$) [1], as indicated in Fig.19.1.3. This is not a major constraint, since it can be achieved simply by selecting a sufficiently small width for $Q3$ and $Q5$, a change that does not affect (1) or (2). Since the present design uses N-type devices for $Q3$ and $Q5$, these transistors operate in the saturated region when turning on $Q0$ and $Q1$, and the above requirement on the channel resistances should instead be applied to the ratios of the respective drive currents. Moreover, it can be shown that this ratio bound must be obeyed not only for the zero dead time approach presented in [1], but also to avoid conduction overlap in systems with finite dead time t_{DT}. The requirement causes the switch timing in the output stage to become asymmetrical, since $Q0$ and $Q1$ are now turned on more slowly than they are turned off. Given such an asymmetry, it can be shown that the minimum THD is obtained for a finite value of t_{DT}, contrary to the common assumption that THD always increases with dead time (e.g., see [2]). Through careful optimization of the t_{DT}-versus-$Q2/Q3$ ($Q4/Q5$) ratio, the open-loop THD performance shown in Fig. 19.1.4 has been obtained.

The amplifier was implemented in a 0.4µm/1.8µm P-bulk high-voltage BiCMOS process with 2 Al and 1 Cu metal layers. For each of the 2 half bridges, 3 pins are used for each of the terminals VDD, GND and OUT, and multiple bond wires connect each of these pins to the die, in order to ensure adequate current handling and reduce conduction power losses. The chip contains two half bridges, and when used in bridge tied load (BTL) configuration, the unclipped output power is 244W into 4Ω. To the best of our knowledge, this power level is unprecedented for monolithic output stages. While the output power is conventionally measured on a purely resistive load, a 4Ω loudspeaker is a complex load and requires additional current. To accommodate this need, the amplifier is designed to provide at least ±18A of output current during normal operation (see Fig. 19.1.5). Currents above this level will cause the output stage to automatically invert the PWM state, in order to limit the output current. This feature protects the device against an inadvertent short circuit at the output. During characterization, the speaker output terminals have been short circuited to ground and V_{DD} respectively. A total of 80,000 short circuit events have been applied over a -25 to +125°C temperature range without failure. A summary of the key performance measures is shown in Fig. 19.1.6, and a chip micrograph is shown in Fig. 19.1.7.

Acknowledgements:
The chip was designed by the Digital Audio design team at Texas Instruments, section manager Sreenath Unnikrishnan and design manager Dale J. Skelton, TI Fellow.

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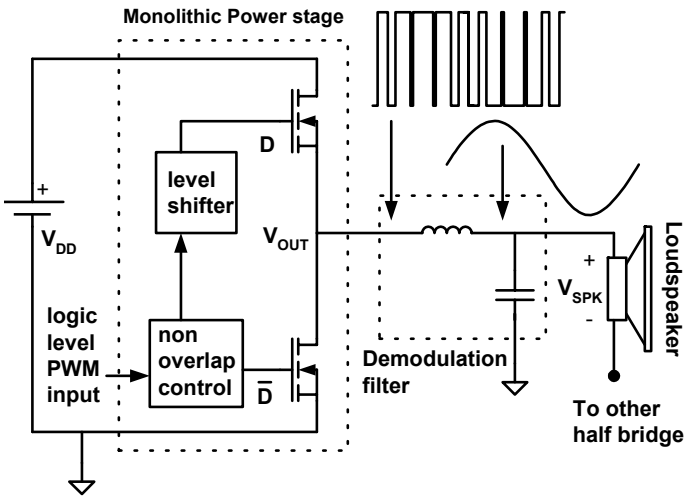

Figure 19.1.1: Single-rail Class-D output stage (one half bridge shown).

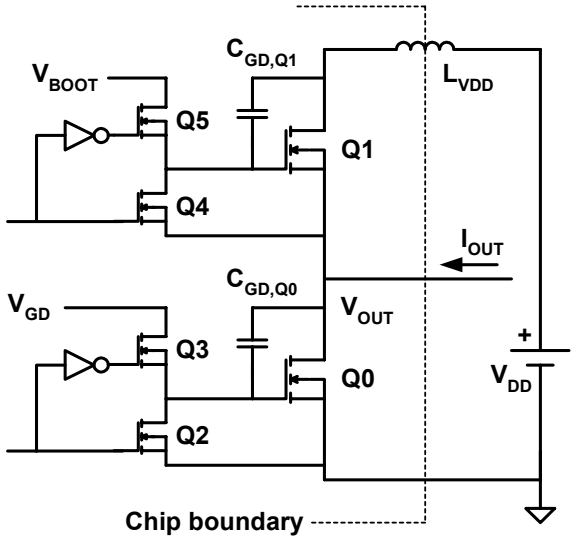

Figure 19.1.2: Half bridge output stage detail.

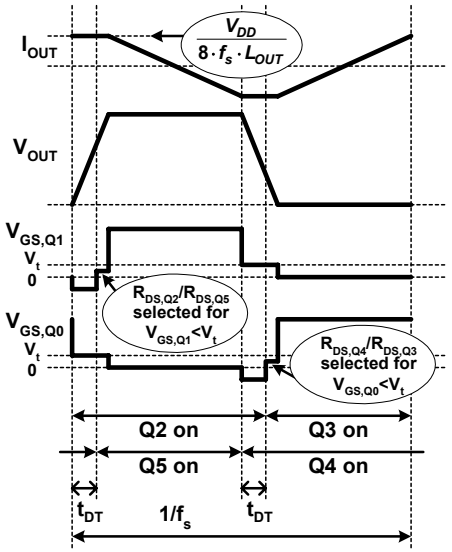

Figure 19.1.3: Switching waveforms during idle operation.

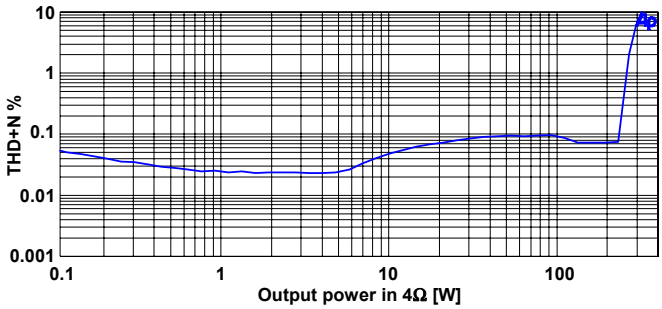

Figure 19.1.4: THD+N measurement.

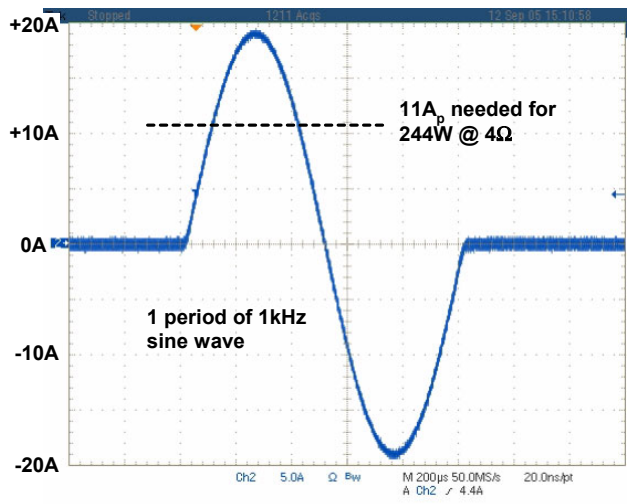

Figure 19.1.5: Output current capability.

Output power V_{DD}=50V	133W	8Ω, unclipped, Tc=75°C
	176W	8Ω, 10% THD, Tc=75°C
	244W	4Ω, unclipped, Tc=75°C
	322W	4Ω, 10% THD, Tc=75°C
V_{DD} idle current	42mA	V_{DD}=50V, f_s=384kHz, L_{OUT}=10µH, Tc=25°C
THD+N	<0.07 %	8Ω
	<0.10 %	4Ω, see Figure 19.1.4
Noise	-110dBA	Not limited by the output stage. -110dB (A-weighted) is achievable with a TI TAS5518 PWM modulator
Output current capability	± 18A	See Figure 19.1.5

Figure 19.1.6: Performance summary.

Continued on Page

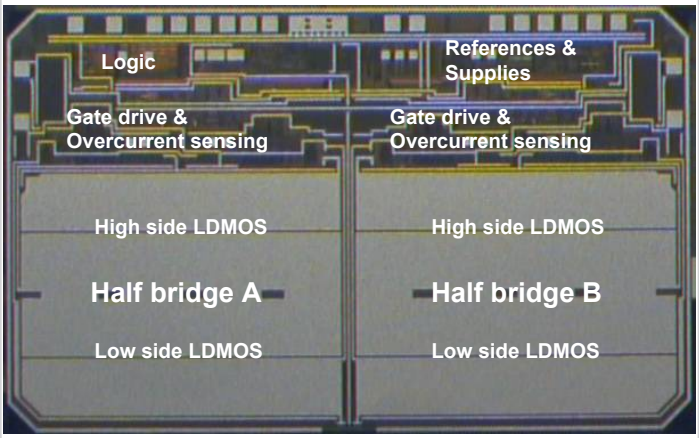

Figure 19.1.7: Die micrograph. The two half bridges form one bridge tied output.

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Appendix V

Efficient Performance Simulation of Class D Amplifier Output Stages
Presented at the 23rd NORCHIP Conference, Oulu Finland, November 21-22 2005

Efficient Performance Simulation of Class D Amplifier Output Stages

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Abstract:

Straightforward simulation of amplifier distortion involves transient simulation of operation on a sine wave input signal, and a subsequent FFT of the output voltage. This approach is very slow on Class D amplifiers, since the switching behavior forces simulation time steps that are many orders of magnitude smaller than the duration of one period of an audio sine wave. This work presents a method of simulating the amplifier transfer characteristic using a minimum amount of simulation time, and then deriving THD from the results.

1. Introduction

A simplified schematic of a class D audio amplifier system is shown in Figure 1. The audio input signal (analog or digital) is converted to a logic-level pulse width modulated (PWM) signal by a modulator (not shown), and level shifted to produce the gate signals for the switches. The two output stage switches are turned on alternately, reproducing the PWM waveform at the switching node V_{SW}. The demodulation LC filter then removes the switching frequency components of the PWM signal, leaving only the audio signal on the output node V_{out}.

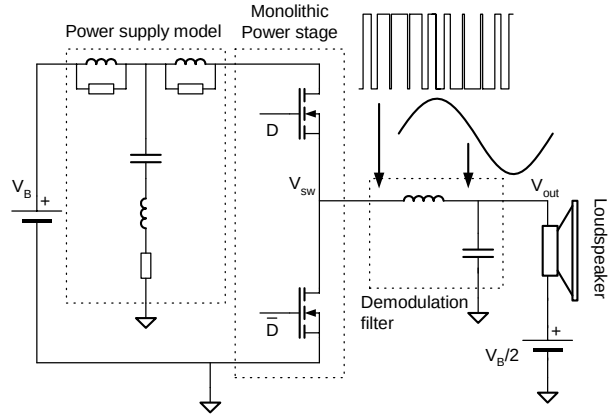

Figure 1: Simple Class D amplifier system. The input signal is the duty cycle (D) of the gate signals for the switches.

Typical switching frequencies are in the range of 300-800kHz. One period of the PWM signal is referred to as a frame. For the case of switching duty cycle D=0.5, the output voltage V_{out} equals $V_B/2$, leaving zero voltage across the loudspeaker. This case is referred to as idle operation.

One of the key performance metrics for audio amplifiers is THD vs. output signal amplitude. Straightforward simulation of THD for the system shown in Figure 1 would involve a transient simulation where the duty cycle D was varied in a purely sinusoidal fashion around D=0.5, at an audio frequency, e.g. 5kHz. THD could then be found from an FFT of the simulated voltage V_{out}. The problem about this approach is runtime. The switching transitions force the use of small time steps in simulation, and since the switching frequency is about two orders of magnitude higher than 5kHz, many PWM frames must be simulated to reproduce a single period of a sine wave audio signal. While similar simulation challenges have been treated in literature, mainly within RF electronics [1], this work focuses on switching power amplifiers.

Using a higher frequency audio signal obviously shortens the needed transient simulation time, but as audio signal frequency is increased, THD contributions will disappear gradually from the simulation result for two reasons: Firstly, the output LC filter will filter out the higher order harmonic components. This problem is easily avoided by deriving THD from an FFT of V_{SW} instead of V_{out}, and then applying a filter with higher cutoff frequency in computation, thereby ignoring frequency components associated with the PWM switching. Secondly, too small a ratio between the switching frequency and the audio frequency corresponds to a coarse sampling of the nonlinearities present in the output stage, hiding some THD contributions from the result, and there is no similar workaround for this problem. For example, to accurately simulate distortion originating from switching dead time, many closely spaced values of PWM duty cycle in the vicinity of D=0.5 are needed [2].

2. Simulation of the Transfer Characteristic

An alternative to the straightforward performance simulation approach described above is to simulate the

input/output transfer characteristic of the amplifier once, and then derive THD vs. signal amplitude from the result. This assumes that the transfer characteristic from duty cycle D to output voltage V_{out} is indeed constant, i.e. not dependant on audio signal frequency. This assumption is valid for the nonlinearities in an open loop Class D output stage, since the switching waveforms depend only on the current in the LC filter inductor at the time of switching.

In practice, Class D amplifier distortion can depend significantly on audio signal frequency. This is partly due to the frequency dependency of the V_B power supply output impedance, and partly to temperature in the output stage varying at the audio frequency. The first effect is not related to the output stage itself, and considered outside the scope of this paper, and the second is not seen in simulation, regardless of approach, as long as the simulator does not incorporate device self heating. Finally, analog-input Class D amplifiers typically use feedback, which will cause distortion to increase with frequency as the feedback loop looses gain. However, amplifiers with feedback can not easily be simulated using the principles described here anyway, since the PSS shooting algorithm (mentioned below) is not likely to converge. If the feedback loop is opened, the simulation approach described here can be applied to the feed-forward path of the amplifier, and still be a useful tool to assess linearity.

For convenience, the amplifier transfer characteristic TC is defined as:

$$VN_{out} = TC(DN) \qquad (1)$$

where (referring to Figure 1)

$$VN_{out} = \frac{2 \cdot V_{out}}{V_B} - 1 \quad \text{and} \quad DN = 2 \cdot (D - 0.5)$$

This means that both DN and VN_{out} will be normalized to the range -1..1, and for an ideal distortion free amplifier, TC would be linear with slope 1, i.e. VN_{out} = DN. Once this normalized transfer characteristic has been determined, the output signal at any amplitude can be calculated (rather than simulated) using the following equation:

$$VN_{out}(t) = TC(10^{\frac{A}{20}} \cdot M \cdot \sin(t)) \quad t = 0 \,..\, 2\pi \qquad (2)$$

and THD vs. signal amplitude can be found from a subsequent FFT of the result. Here A is the audio signal amplitude of interest (in dB), and M is the maximum modulation index. M is typically in the range 0.95 to 0.98 and accounts for the fact that most Class D output stages have a lower bound on PWM pulse width, meaning that the actual duty cycle range at A=0dB is slightly narrower than 0 to 1. Note that for each signal amplitude of interest, THD can be found using equation (2) and an FFT calculation, no extra simulation is needed like the straightforward simulation approach described in the introduction.

3. Selection of D values and Transfer Characteristic Interpolation

In order to determine TC(DN) for a system, a number of duty cycle values DN must be selected, and VN_{out} simulated for each value. In order to use equation (2), TC(DN) must be defined for any DN in the range -1..1, and since it can only be simulated for a finite number of input values DN, interpolation is needed. Figure 2 shows an example of a transfer characteristic that is simulated for 7 values of DN, and then reconstructed using linear or cubic spline interpolation.

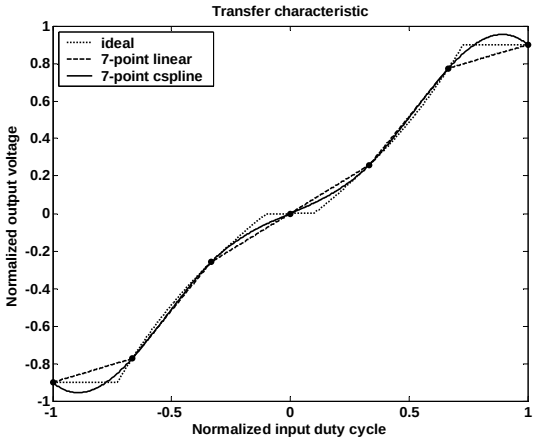

Figure 2: Amplifier transfer characteristic VN=TC(DN), simulated for 7 linearly spaced duty cycle values and recontructed using linear or cubic spline interpolation.

The ideal transfer characteristic shown in Figure 2 is given by

$$TC(DN) = \begin{cases} VN_{out} = d3 \cdot DN^3 & DN \le zc \\ VN_{out} = DN + d3 \cdot DN^3 & DN > zc \end{cases}$$
$$VN_{out} \text{ limited to } \pm VN_{clip} \qquad (3)$$

where d3 is the 3rd order distortion coefficient, zc is the bound for zero-crossing distortion, where gain is reduced for |DN|<zc. VN_{clip} is the output clipping limit.

These properties represent common amplifier nonlinearities[1]. For the curves in Figure 2, d3=0.7, zc=0.1 and VN_{clip}=0.9. The degree of nonlinearity is vastly exaggerated in order to aid visibility in Figure 2. For any reasonable audio amplifier, the actual nonlinearity would not be visible in such a plot.

In the example shown, the 7 DN values at which TC(DN) is simulated are linearly spaced. This poses a problem when equation (2) is used to derive THD at

[1] Though Class D amplifiers do not exhibit zero crossing distortion in a traditional sense, they do have a nonlinearity associated with switching dead time that causes reduced gain at low signal amplitudes. See [2] for a detailed discussion.

small signal amplitudes from the interpolated TC(DN) function. E.g. if THD at A ≤ -10dB is derived from one of the interpolated transfer characteristics in Figure 2, the result will be based almost exclusively on the 3 points at and around DN=0 where TC(DN) has been simulated[2]. Obviously this problem is reduced when more points are used, but even for 201 DN value points a similar problem will occur for A ≤ -40dB.
Improved resolution at small signal amplitude can be achieved by distributing the DN values unevenly, with a higher concentration in the vicinity of DN=0. Instead of a linear spacing, we propose distributing m points as follows:

$$DN = 0, \pm \log_{10}\left(\frac{2k}{m-3} \cdot \frac{lvlmin}{20}\right) \quad k = 0..\frac{m-3}{2}$$

where m must be odd

There is a data point at DN=0, and logarithmically distributed values from *lvlmin* dB towards 0dB in both the positive and negative direction. For example, for m = 7 and *lvlmin* = -40dB we get

$$DN = (-1, -0.1, -0.01, 0, 0.01, 0.1, 1)$$

Since this distribution is logarithmic in nature, but includes zero and both positive and negative values, we will refer to it as *pseudo-logarithmic* here.

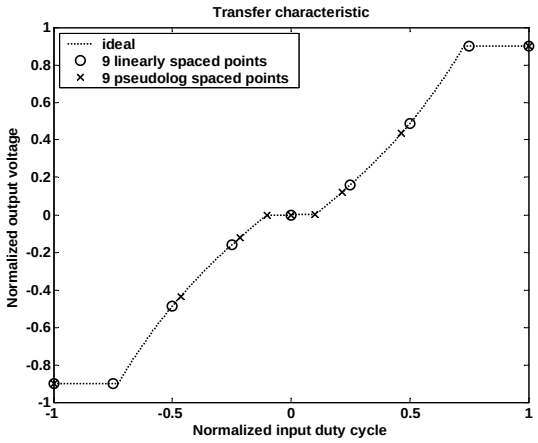

Figure 3: TC(DN) simulated at 9 DN values, with linear versus pseudo-logarithmic distribution

For a given number of DN points, the pseudo-logarithmic distribution greatly increases the accuracy of THD calculations for small signal amplitudes, at the penalty of a decrease in accuracy at large signal amplitudes.

4. THD matching

To test the accuracy of THD simulation using different algorithms for DN value spacing and transfer characteristic interpolation, THD for the nonlinearity described by equation (3) is used as a test case. Rather than using a measured transfer characteristic TC(DN) from an actual Class D amplifier, this has the advantage that due to the symbolic nature of the equation, there is a definite correct answer to the THD vs. amplitude curve. For this purpose, the parameters for equation (3) are set at values that realistically represent an audio amplifier: d3=0.003, zc=$5 \cdot 10^{-5}$, VN_{clip}=0.9

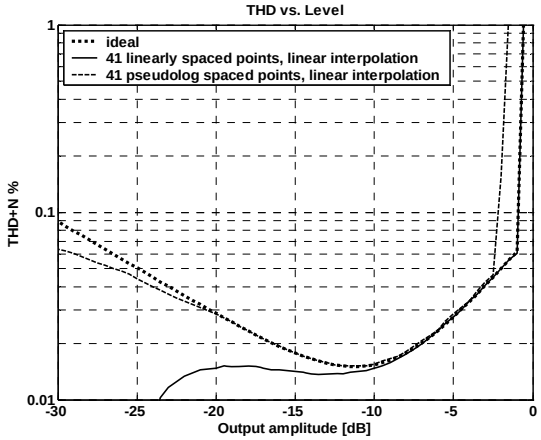

Figure 4: THD reconstruction using 41 simulation points and linear interpolation between them. THD based on all harmonics from an FFT of size 64, M=1 (refer to equation 2).

Figure 4 shows THD calculation results based on 41 simulation points, spaced linearly and pseudo-logarithmically. Linear interpolation between the data points is used in both cases. As expected, the linear distribution results in too small THD numbers at small signal amplitude, because the density of simulated data points TC(DN) is too low to model the zero-crossing distortion. Conversely, the pseudo-logarithmic distribution models the clipping at large signal amplitude inaccurately.

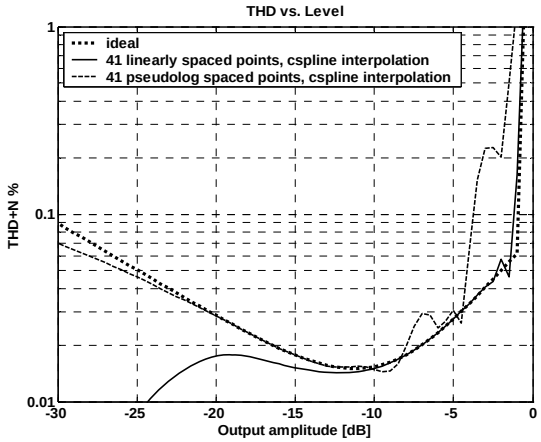

Figure 5: THD reconstruction using 41 simulation points and cubic spline interpolation between them. THD based on all harmonics from an FFT of size 64, M=1 (refer to equation 2).

The clipping sets in too early, because the density of data points is low, and the linear interpolation results in a less

[2] When using cubic spline interpolation, the interpolated TC(DN) function does depend sligthly on data points further from DN.

aggressive clipping between the data points at DN=±1 and their nearest neighbors, which are below the actual clipping level. This phenomenon can also be observed in Figure 2 (linear interpolation).
Figure 5 shows the same THD calculation, except cubic spline interpolation is used between the simulated data points. While cubic spline interpolation may generally be conceived as superior to linear interpolation, it is not the case for this purpose. For small signal amplitudes, the results are about equal to those from linear interpolation, but the cubic spline causes large inaccuracies in the modeling of clipping, especially in combination with the pseudo-logarithmic distribution of data points, again because of its coarse resolution of DN values at large signal amplitudes. This is not surprising, since ideal clipping as described by equation (3) is an abrupt kink in the transfer characteristic, and cubic splines are free of kinks by design.
Cubic spline interpolation may still provide superior accuracy on actual designs that do not have sharp kinks in their transfer characteristic. This can be tested by running one (CPU intensive) simulation with a very large number of data points, and then test which interpolation method that best matches the high-resolution THD result with fewer data points. When a useful resolution, spacing algorithm and interpolation method has been found, it can be used in design optimization, and the final solution verified with another high-resolution simulation.

5. Computational efficiency

For comparison to a straightforward transient simulation of a period of an audio sine wave on V_{out}, consider the following: One sine wave period at 5kHz audio frequency would require 200us transient simulation, plus additional time for the output LC filter to stabilize before the FFT window starts. Assuming another 100us is needed for stabilization, this is 300us of transient simulation per THD vs. amplitude data point. Note that even if THD is derived from V_{SW} rather than V_{out}, the output filter influences linearity by generating switching ripple current, which in turn influences the switching transition waveforms and thus THD. This means that the LC output filter cannot be disregarded in simulation, and it must settle in order to find the periodical output sine wave. Computing the initial conditions for the LC filter components at the start of each transient simulation, with as good accuracy as possible, is obviously crucial for fast settling.
Assuming that a THD vs. amplitude plot is to be generated, for -40dB to 0dB signal amplitude in 1dB steps, a total of 12.3ms transient simulation time is needed. If 41 CPUs are available, the wall clock time is that of simulating 300us.
Using the transfer characteristic approach, the accuracy seen in Figure 4 and Figure 5 can be achieved with 41 data points. For a Class AB amplifier, each data point would be just an operating point simulation, but for a Class D amplifier, it requires a Periodic Steady State (PSS) simulation to find the output voltage Vout (equal to the average of VSW) for a given duty cycle DN. For a description of PSS, refer to [3]. The PSS shooting algorithm typically takes 5 iterations to find the steady state, so at 400kHz PWM switching frequency that means 12.5us transient simulation time per data point. This is 512us total transient simulation time, or just about 4% of the 12.3ms needed for transient simulations of the audio signal.
While the transfer characteristic approach has inaccuracy associated with DN value spacing algorithms, simulation of audio sine wave operation has a very similar inaccuracy related to the choice of audio frequency. Reproducing an audio sine wave with a fixed PWM frequency corresponds to sampling the transfer characteristic at a finite number of points spaced linearly in time. E.g. playing back one period of a 5kHz audio signal at 400kHz switching frequency provides 80 data points. Because of the repetitive nature of a sine wave, half of these points are repetitions of points already simulated, and do not contribute any additional accuracy. The data set thus contains 40 unique data points, and the sine wave shape causes a high density of data points at large duty cycle values and a low density around idle. While the straightforward approach has the advantage that these 40 data points are always within the range of the audio signal, regardless of amplitude, the lower resolution around idle is likely to impact accuracy of e.g. the THD contribution related to dead time at medium signal amplitudes.

6. Summary

An indirect performance simulation method for Class D amplifiers has been presented. Like most simulations, it possesses basic trade offs between CPU time and accuracy, but it is easily more efficient than transient simulation of sine wave amplification. The method is based on the assumption that the transfer characteristic of the amplifier is time invariant. This is true for open-loop Class D amplifier output stages if distortion related to finite PSU impedance and temperature modulation is disregarded. For amplifiers with feedback, the approach can only be applied with the feedback loop opened, but this can still be useful for assessing linearity of the feed-forward path.

7. References

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