

Analog Input Buffer Architectures

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1. Introduction

There are many considerations that must be taken into account when designing and implementing an analog input buffer. These include negligible noise contribution, input biasing, isolation from switched capacitor currents, maintaining a low output impedance so as not to cause distortion, and providing anti-alias filtering appropriate for the modulator sampling rate.

This application note provides several filter topologies that address the above concerns. The following analog input buffers have been divided into four categories: fully differential, single-ended to differential, single-ended with dedicated reference pins for each channel, and single-ended with a common, or shared, reference.

2. Fully Differential Analog Input Buffer

2.1 Applicable Converters

A fully differential analog input buffer is ideal for use with the following Cirrus Logic audio converters:

- CS5361
- CS5381
- CS4272
- CS42528/26/18/16
- CS42428/26/18/16

2.2 Introduction to Differential Signals

A differential signal can be defined as two nodes that have equal but opposite signals around a fixed point (called the common mode level). The two signal nodes are typically referred to as positive and negative (or non-inverting and inverting), as shown in the following example of a differential sine wave:

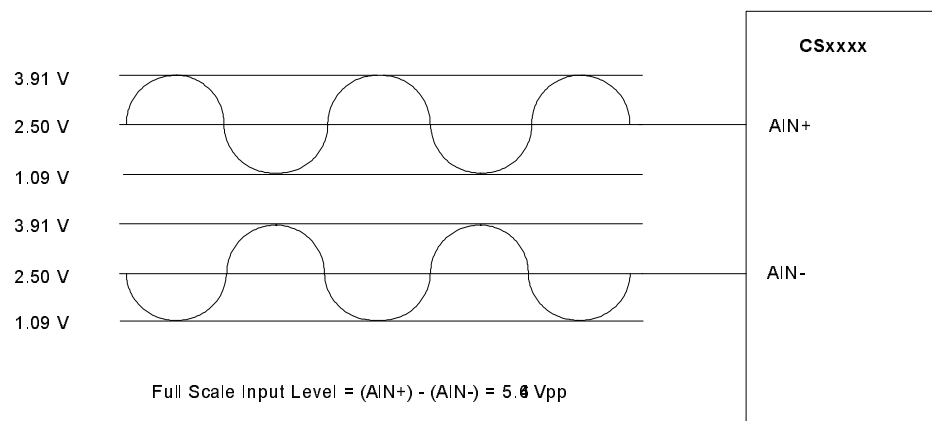


Figure 1. Example of a Differential Signal

In the above example, the full scale input voltage is 5.64 Vpp (differentially), with each leg swinging 2.82 Vpp. Please note that the full scale input voltage level may vary from part to part. Also, the common mode level (which in the above example is 2.5 0V) can also vary depending on the converter.

2.3 Recommended Filter Topology

Figure 2 shows a fully differential analog input buffer. This buffer provides proper biasing, isolation from the switched capacitor currents, low output impedance, and anti-alias filtering. The noise contribution of this buffer is determined primarily by the noise floor of the op-amp.

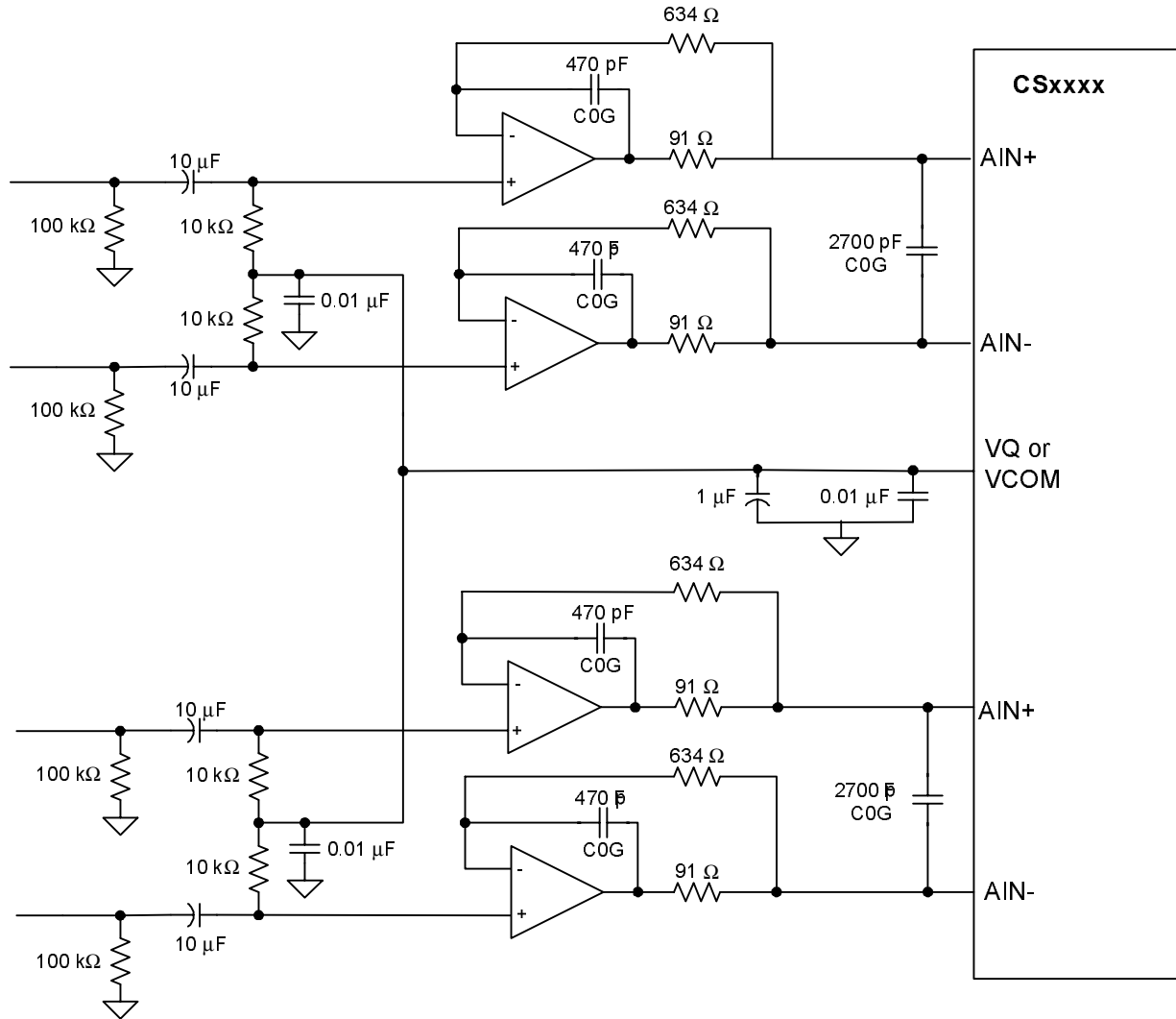


Figure 2. Fully Differential Input Buffer

2.4 Overview of the Filter Topology

2.4.1 High Pass Filter and DC Biasing

The first stage of the buffer forms a high pass filter and provides the proper biasing to the positive terminals of the op-amps. The high pass filter is formed from the combination of the AC-coupling capacitor along with the resistor to the bias voltage reference (VQ or VCOM, depending on the naming convention). The 3 dB corner of the high pass filter can be calculated as follows:

$$F_c = \frac{1}{2\pi RC}$$

where: R is the value of the resistor (in Ohms)

C is the value of the capacitor (in Farads)

In the input buffer shown in Figure 2, $R = 10\text{ k}\Omega$ and $C = 10\text{ }\mu\text{F}$. This places the 3 dB corner at approximately 1.59 Hz. Typically, this corner should be at least one decade below the bandwidth of interest in order to prevent a significant droop in the frequency response.

The proper DC biasing (common mode level) is set via the on-chip reference (VQ or VCOM). In the input buffer shown above, the bias is set through a $10\text{ k}\Omega$ resistor. Please note that this resistor value has several implications. Since the input impedance into the op-amp is extremely high, the effective input impedance into the analog input buffer will be determined by the value of the resistor to the bias voltage in parallel with the $100\text{ k}\Omega$ shunt resistor. In the input buffer shown above, the input impedance is approximately $9\text{ k}\Omega$. Ideally, the larger this input impedance the better. However, in the input buffer shown in Figure 2, the AC-coupling capacitor will initially be charged up via the on-chip reference (VQ or VCOM). This charge up time is dependent on the size of the AC-coupling capacitor and the amount of series resistance to the reference voltage supply. The reference pin (VQ or VCOM) has an associated output impedance that must also be considered when calculating the charge up time. The time constant can be calculated as follows:

$$\tau = RC$$

where R = the amount of resistance between the AC-coupling capacitor and reference voltage (in Ohms)

C = the value of capacitance of the AC-coupling capacitor (in Farads)

In the input buffer shown in Figure 2, $R = 35\text{ k}\Omega$ (assuming a $25\text{ k}\Omega$ output impedance on the reference pin), and $C = 10\text{ }\mu\text{F}$. This produces a time constant of 0.35 s. This would indicate that the capacitor will charge up to within 99% of the final DC value in approximately 1.75 s (which is 5 time constants). The $100\text{ k}\Omega$ resistors to ground on the input node allow a DC path to charge the AC-coupling capacitors, regardless of whether or not there is an input signal source present.

2.4.2 Op Amp Circuitry and Anti-Aliasing Capacitor

The op-amp topology used in the input buffer shown in Figure 2 addresses two issues. First, it provides an extremely low output impedance and therefore minimizes the amount of distortion presented to the converter's internal sampling circuits. By placing the $91\text{ }\Omega$ resistor in the feedback loop, its resistance is divided by the open-loop gain of the op-amp, providing a sub-ohm output impedance. Secondly, this op-amp topology provides a low pass filter. Using the recommended values, this filter remains flat throughout the audio passband and provides approximately 20 dB of rejection at the modulator sampling rate (where the converter is susceptible to aliasing). The characteristics of this low pass filter can be changed by adjusting the values of the resistors and capacitors in the feedback loop. However, it is important to maintain a flat frequency response throughout the passband of interest and to provide reasonable attenuation at the input sampling rate of the converter. Also, low value resistors should be used to minimize the addition of resistor thermal noise.

Figure 2 implements a common mode capacitor between the positive and negative nodes of the differential inputs. This capacitor is commonly referred to as the anti-aliasing capacitor, and performs several functions. The value of the capacitor affects the overall low pass filter response and the amount of attenuation at the modulator sampling rate. This capacitor also acts as a charge reservoir for the internal sampling capacitors. Since this capacitor is located in the signal path, it is very important not to use capacitors with a large voltage coefficient (such as general purpose ceramics) since they can degrade signal linearity.

3. Single-Ended to Differential Input Buffer

3.1 Applicable Converters

A single-ended to differential analog input buffer is ideal for use with the following Cirrus Logic audio converters:

- CS5361
- CS4272
- CS42528/26/18/16
- CS42428/26/18/16

3.2 Introduction

A single-ended signal consists of only one signal line and hence requires only one input pin. Single-ended inputs typically require less input buffer components, but also have several disadvantages. First, at a given voltage level, a single-ended input cannot produce as much signal swing as a differential signal, hence reducing the dynamic range. Also, single-ended inputs are more prone to errors caused by DC offsets and coupled-noise.

3.3 Recommended Filter Topology

Figure 3 shows a single-ended to differential analog input buffer. This buffer provides proper biasing, isolation from the switched capacitor currents, low output impedance, and anti-alias filtering. The second op-amp stage is set up in an inverting configuration to produce the negative node of the differential input. In the input buffer shown below, the second stage has unity gain, and the single-ended input level will effectively be doubled when presented differentially to the converter. For example, a 2V_{pp} single-ended input will provide a 4V_{pp} differential input to the converter.

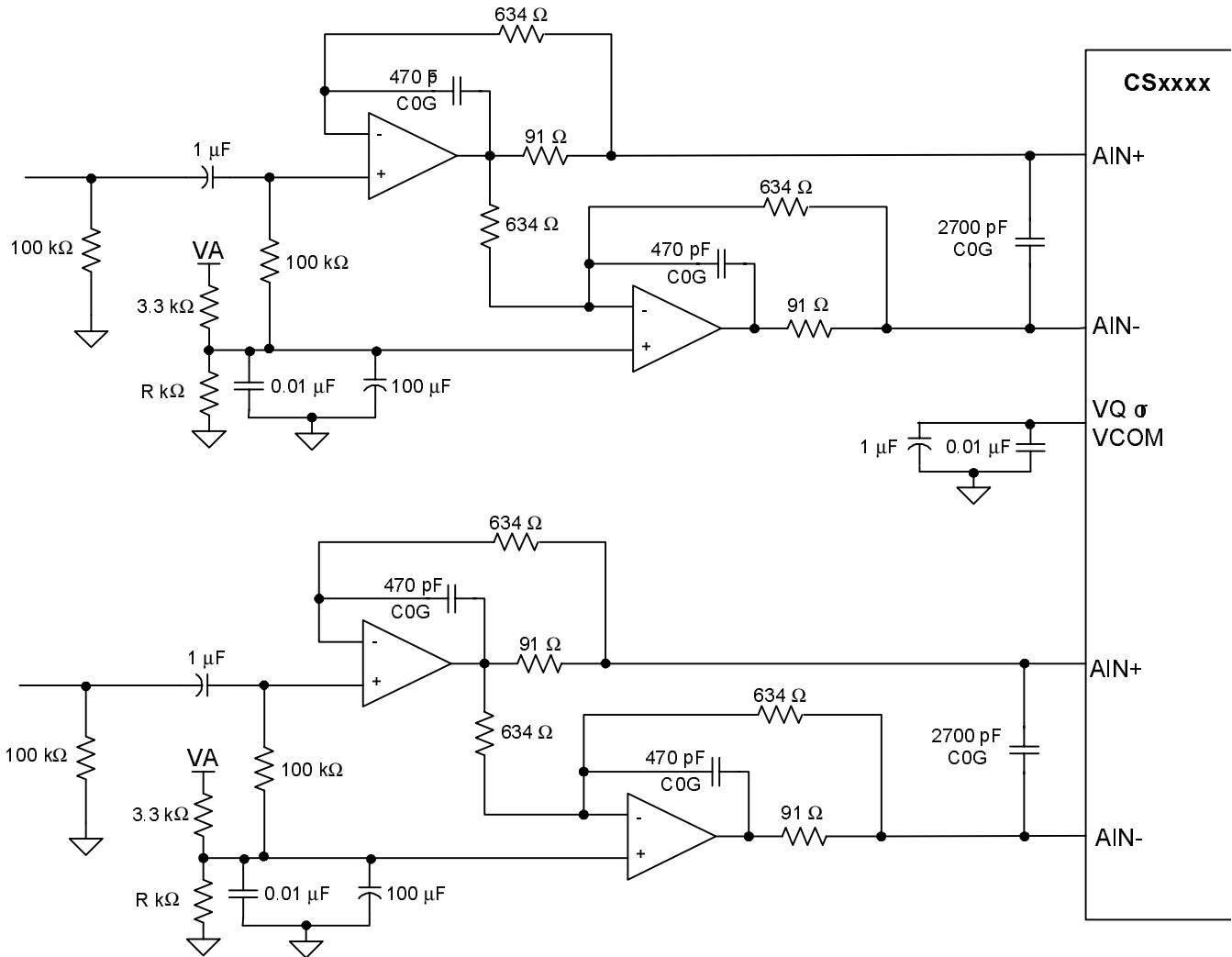


Figure 3. Single-Ended to Differential Input Buffer

3.4 Overview of the Filter Topology

3.4.1 High Pass Filter and DC Biasing

The first stage of the buffer forms a high pass filter and provides the proper biasing to the positive terminals of the op-amps. The value of the resistors denoted as “R” will vary depending on the optimal DC bias for the given converter. Typically this is around half of the VA voltage supply. The high pass filter is formed from the combination of the AC-coupling capacitor along with the resistor that connects the positive terminal of the op-amp to the DC bias voltage. The 3dB corner of the high pass filter can be calculated as follows:

$$F_c = \frac{1}{2\pi R_{EQ} C}$$

where: R_{EQ} is the value of the equivalent resistance (in Ohms)

C is the value of the capacitor (in Farads)

In the input buffer shown in Figure 3, $R_{EQ} = 100 \text{ k}\Omega$ and $C = 1.0 \text{ }\mu\text{F}$. This places the 3 dB corner at approximately 1.59 Hz. Typically, this corner should be at least one decade below the bandwidth of interest in order to prevent a significant droop in the frequency response.

Since the input impedance into the op-amp is extremely high, the effective input impedance into the analog input buffer will be determined by the value of the resistor to the bias voltage in parallel with the 100 k Ω shunt resistor. In the input buffer shown above, the input impedance is approximately 50 k Ω . Ideally, the larger this input impedance the better. However, in the input buffer shown in Figure 3, the AC-coupling capacitor will initially be charged up via the resistor divider on VA. This charge up time is dependent on the size of the AC-coupling capacitor and the amount of series resistance to the reference voltage supply. The time constant can be calculated as follows:

$$\tau = R_s C$$

where R_s = the amount of resistance between the AC-coupling capacitor and reference voltage (in Ohms)

C = the value of capacitance of the AC-coupling capacitor (in Farads)

In the input buffer shown in Figure 3, $R_s \approx 100 \text{ k}\Omega$, and $C = 1.0 \text{ }\mu\text{F}$. This produces a time constant of 0.1 s. This would indicate that the capacitor will charge up to within 99% of the final DC value in approximately 0.5 s (which is 5 time constants). The 100 k Ω resistors to ground on the input nodes allow a DC path to charge the AC-coupling capacitors, regardless of whether or not there is an input signal source present.

3.4.2 Op Amp Circuitry and Anti-Aliasing Capacitor

The op-amp topology used in the input buffer shown in Figure 3 addresses two issues. First, it provides an extremely low output impedance and therefore minimizes the amount of distortion presented to the converter's internal sampling circuits. By placing the 91 Ω resistor in the feedback loop, its resistance is divided by the open-loop gain of the op-amp, providing a sub-ohm output impedance. Secondly, this op-amp topology provides a low pass filter. Using the recommended values, this filter remains flat throughout the audio passband and provides approximately 20 dB of rejection at the modulator sampling rate (where the converter is susceptible to aliasing). The characteristics of this low pass filter can be changed by adjusting the values of the resistors and capacitors in the feedback loop. However, it is important to maintain a flat frequency response throughout the passband of interest and to provide reasonable attenuation at the input sampling rate of the converter. Also, low value resistors should be used to minimize the addition of resistor thermal noise.

Figure 3 implements a common mode capacitor between the positive and negative nodes of the converter's differential inputs. This capacitor is commonly referred to as the anti-aliasing capacitor, and performs several functions. The value of the capacitor affects the overall low pass filter response and the amount of attenuation at the modulator sampling rate. This capacitor also acts as a charge reservoir for the internal sampling capacitors. Since this capacitor is located in the signal path, it is very important not to use

capacitors with a large voltage coefficient (such as general purpose ceramics) since they can degrade signal linearity.

4. Single-Ended Input Buffer with Dedicated Reference Pins

4.1 Applicable Converters

A single-ended analog input buffer with dedicated reference pins is ideal for use with the following Cirrus Logic audio converters:

- CS5351
- CS4271
- CS42528/26/18/16 (Note: Full performance will not be realized with a single-ended implementation.)
- CS42428/26/18/16 (Note: Full performance will not be realized with a single-ended implementation.)

4.2 Introduction

A single-ended signal consists of only one signal line and hence requires only one input pin. Some converters have a dedicated reference pin for each channel, as well as an on-chip reference. These pins are typically labeled VQx. Please check the datasheet for the particular converter to determine the naming convention of the VQx pins.

4.3 Recommended Filter Topology #1

Figure 4 shows a single-ended analog input buffer with dedicated reference pins. This filter implements one op-amp per channel, and uses a third op-amp to properly bias the analog inputs and independent channel reference pins. This buffer provides proper biasing, isolation from the switched capacitor currents, low output impedance, and anti-alias filtering.

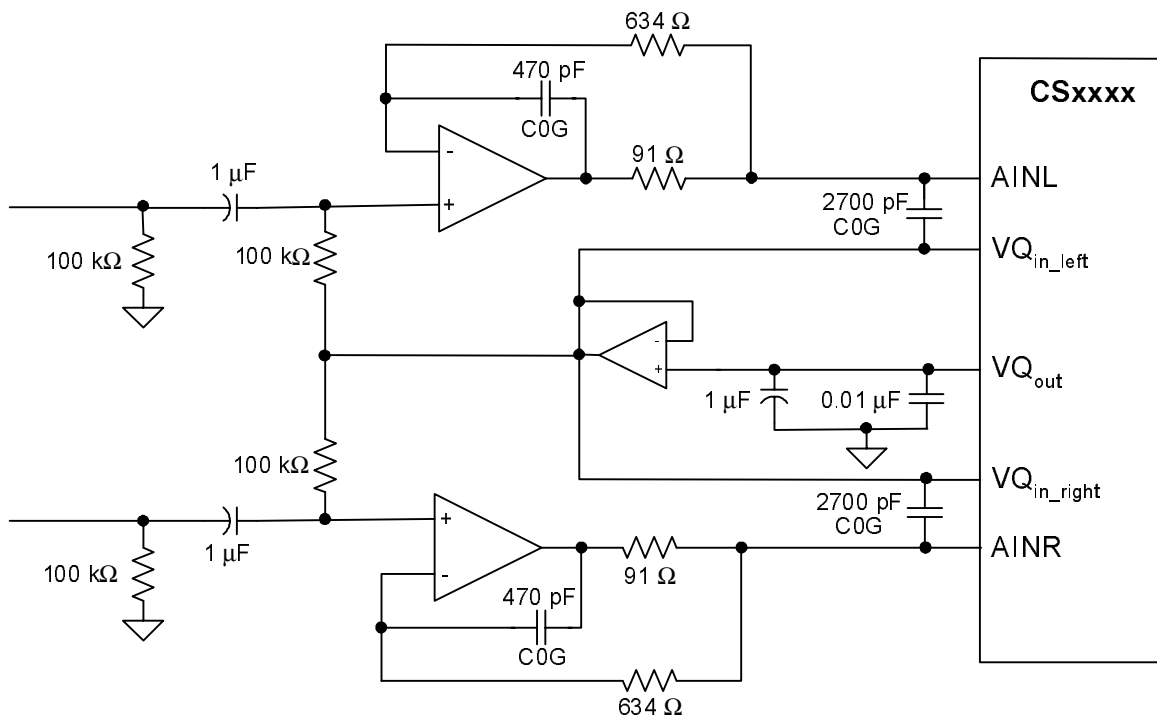


Figure 4. Single-Ended Input Buffer with Dedicated Reference Pins (Example #1)

4.4 Overview of Filter Topology #1

4.4.1 High Pass Filter and DC Biasing

The first stage of the buffer forms a high pass filter from the combination of the AC-coupling capacitor along with the resistor that connects the positive terminal of the op-amp in the input signal path to the DC bias voltage. The 3 dB corner of the high pass filter can be calculated as follows:

$$F_c = \frac{1}{2\pi RC}$$

where: R is the value of the resistor (in Ohms)

C is the value of the capacitor (in Farads)

In the input buffer shown in Figure 4, $R = 100 \text{ k}\Omega$ and $C = 1.0 \text{ }\mu\text{F}$. This places the 3 dB corner at approximately 1.59 Hz. Typically, this corner should be at least one decade below the bandwidth of interest in order to prevent a significant droop in the frequency response.

Since the input impedance into the op-amp is extremely high, the effective input impedance into the analog input buffer will be determined by the value of the resistors to the bias voltage in parallel with the $100 \text{ k}\Omega$ shunt resistors. In the input buffer shown above, the input impedance is approximately $50 \text{ k}\Omega$. Ideally, the larger this input impedance the better. However, in the input buffer shown in Figure 4, the AC-coupling capacitor will initially be charged up via the op-amp connected to the on-chip voltage reference. This charge up time is dependent on the size of the AC-coupling capacitor and the amount of series resistance to the DC-biasing op-amp. The time constant can be calculated as follows:

$$\tau = RC$$

where R = the amount of resistance between the AC-coupling capacitor and the DC-biasing op-amp (in Ohms)

C = the value of capacitance of the AC-coupling capacitor (in Farads)

In the input buffer shown in Figure 4, $R = 100 \text{ k}\Omega$, and $C = 1.0 \text{ }\mu\text{F}$. This produces a time constant of 0.1 s. This would indicate that the capacitor will charge up to within 99% of the final DC value in approximately 0.5 s (which is 5 time constants). The $100 \text{ k}\Omega$ resistors to ground on the input node allow a DC path to charge the AC-coupling capacitors, regardless of whether or not there is an input signal source present.

4.4.2 Op Amp Circuitry and Anti-Aliasing Capacitor

The op-amp topology used in the input buffer shown in Figure 4 addresses two issues. First, it provides an extremely low output impedance and therefore minimizes the amount of distortion presented to the converter's internal sampling circuits. By placing the $91 \text{ }\Omega$ resistor in the feedback loop, its resistance is divided by the open-loop gain of the op-amp, providing a sub-ohm output impedance. Secondly, this op-amp topology provides a low pass filter. Using the recommended values, this filter remains flat throughout the audio passband and provides approximately 20 dB of rejection at the modulator sampling rate (where the converter is susceptible to aliasing). The characteristics of this low pass filter can be changed by adjusting the values of the resistors and capacitors in the feedback loop. However, it is important to maintain a flat frequency response throughout the passband of interest and to provide reasonable attenuation at

the input sampling rate of the converter. Also, low value resistors should be used to minimize the addition of resistor thermal noise.

Figure 4 implements a common mode capacitor between the analog input and the associated reference voltage pin on each channel of the converter. This capacitor is commonly referred to as the anti-aliasing capacitor, and performs several functions. The value of the capacitor affects the overall low pass filter response and the amount of attenuation at the input sample rate of the converter. This capacitor also acts as a charge reservoir for the internal sampling capacitors. Since this capacitor is located in the signal path, it is very important not to use capacitors with a large voltage coefficient (such as general purpose ceramics) since they can degrade signal linearity.

4.5 Recommended Filter Topology #2

Figure 5 shows a single-ended analog input buffer with dedicated reference pins. This filter implements one op-amp per channel, and uses passive components to properly bias the analog inputs and independent channel reference pins. This buffer provides proper biasing, isolation from the switched capacitor currents, low output impedance, and anti-alias filtering.

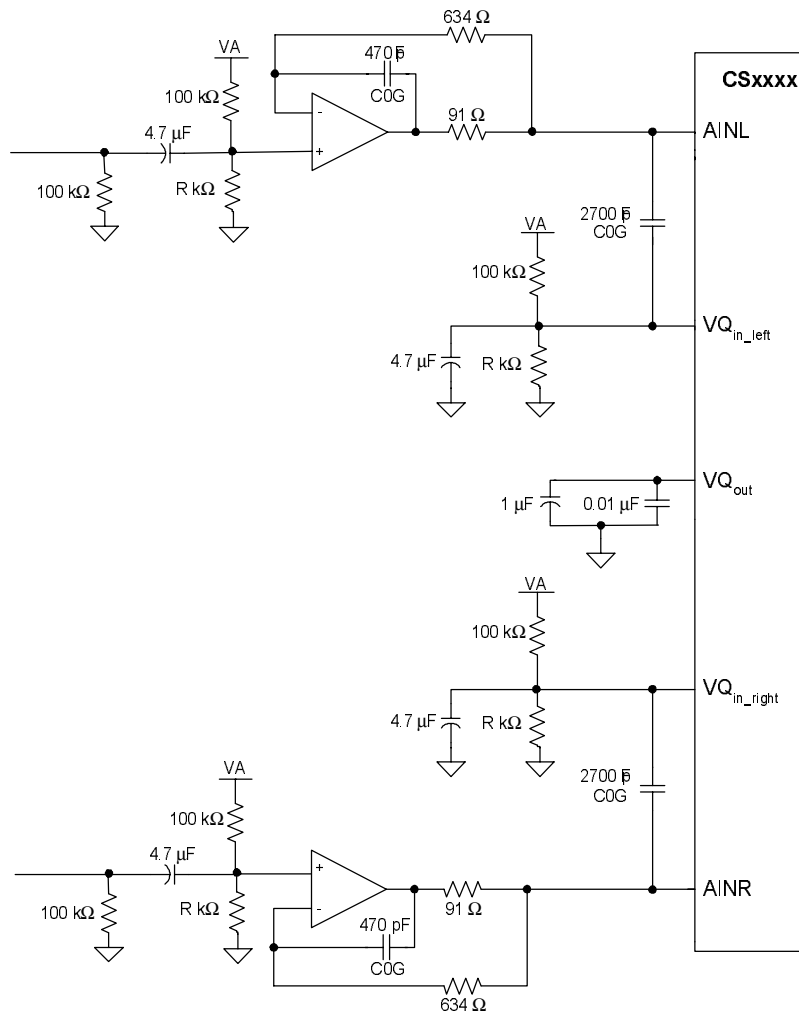


Figure 5. Single-Ended Input Buffer with Dedicated Reference Pins (Example #2)

4.6 Overview of Filter Topology #2

4.6.1 High Pass Filter and DC Biasing

The first stage of the buffer forms a high pass filter from the combination of the AC-coupling capacitor along with the resistor divider that biases the positive terminal of the op-amp to the proper DC bias voltage. The value of the resistors denoted as “R” will vary depending on the optimal DC bias for the given converter. Typically this is around half of the VA voltage supply. A high pass filter is also formed from the resistor divider and capacitor to ground on the reference voltage pin of each channel. The 3dB corner of the high pass filter can be calculated as follows:

$$F_c = \frac{1}{2\pi R_{EQ} C}$$

where: R_{EQ} is the value of the resistor divider in parallel (in Ohms)

C is the value of the capacitor (in Farads)

In the input buffer shown in Figure 5, $R_{EQ} \approx 50 \text{ k}\Omega$ ($100 \text{ k}\Omega \parallel R \text{ k}\Omega$) and $C = 4.7 \text{ }\mu\text{F}$. This places the 3 dB corner at approximately 0.68 Hz. Typically, this corner should be at least one decade below the bandwidth of interest in order to prevent a significant droop in the frequency response.

Since the input impedance into the op-amp is extremely high, the effective input impedance into the analog input buffer will be determined by the parallel combination of the resistors in the biasing divider in parallel with the $100 \text{ k}\Omega$ shunt resistor. In the input buffer shown above, the input impedance is approximately $33 \text{ k}\Omega$. Ideally, the larger this input impedance the better. However, in the input buffer shown in Figure 5, the AC-coupling capacitor will initially be charged up via the resistor divider. This charge up time is dependent on the size of the AC-coupling capacitor and the amount of resistance to the VA voltage supply. The time constant can be calculated as follows:

$$\tau = R_{EQ} C$$

where R_{EQ} = the amount of resistance between the AC-coupling capacitor and the voltage supply (in Ohms)

C = the value of capacitance of the AC-coupling capacitor (in Farads)

In the input buffer shown in Figure 5, $R_{EQ} \approx 50 \text{ k}\Omega$ ($100 \text{ k}\Omega \parallel R \text{ k}\Omega$), and $C = 4.7 \text{ }\mu\text{F}$. This produces a time constant of approximately 0.24 s. This would indicate that the capacitor will charge up to within 99% of the final DC value in approximately 1.2 s (which is 5 time constants). The $10 \text{ k}\Omega$ resistors to ground on the input node allow a DC path to charge the AC-coupling capacitor, regardless of whether or not there is an input signal source present.

4.6.2 Op Amp Circuitry and Anti-Aliasing Capacitor

The op-amp topology used in the input buffer shown in Figure 5 addresses two issues. First, it provides an extremely low output impedance and therefore minimizes the amount of distortion presented to the converters internal sampling circuits. By placing the $91 \text{ }\Omega$ resistor in the feedback loop, its resistance is divided by the open-loop gain of the op-amp, providing a sub-ohm output impedance. Secondly, this op-amp topology provides a low pass filter. Using the recommended values, this filter remains flat throughout the audio passband and provides approximately 20dB of rejection at the modulator sampling rate (where

the converter is susceptible to aliasing). The characteristics of this low pass filter can be changed by adjusting the values of the resistors and capacitors in the feedback loop. However, it is important to maintain a flat frequency response throughout the passband of interest and to provide reasonable attenuation at the modulator sampling rate of the converter. Also, low value resistors should be used to minimize the addition of resistor thermal noise.

Figure 5 implements a common mode capacitor between the analog input and the associated reference voltage pin on each channel of the converter. This capacitor is commonly referred to as the anti-aliasing capacitor, and performs several functions. The value of the capacitor affects the overall low pass filter response and the amount of attenuation at the input sample rate of the converter. This capacitor also acts as a charge reservoir for the internal sampling capacitors. Since this capacitor is located in the signal path, it is very important not to use capacitors with a large voltage coefficient (such as general purpose ceramics) since they can degrade signal linearity.

4.7 Recommended Filter Topology #3

Figure 6 shows a single-ended analog input buffer with dedicated reference pins. This filter implements one op-amp per channel, and uses a third op-amp to properly bias the independent channel reference pins. This input buffer topology offers some unique advantages. First, the analog inputs to the op-amps do not need to be AC-coupled (although they can be), which allows the input impedance of the buffer to be set without regard to any charge up times. This can also be advantageous if the op-amps are restricted to limited supply rails of ± 5 V. In this case, it is optimal to have an input referenced to ground in order to prevent the op-amp from clipping. Secondly, this input buffer topology allows for some signal gain, as determined by the resistor R_g . Finally, this buffer provides proper biasing, isolation from the switched capacitor currents, and anti-alias filtering. On disadvantage of this topology is the large AC-coupling capacitor directly on the input sampling node. The ESR of the capacitor will increase distortion, especially at low frequencies where the ESR of the capacitor is generally much greater.

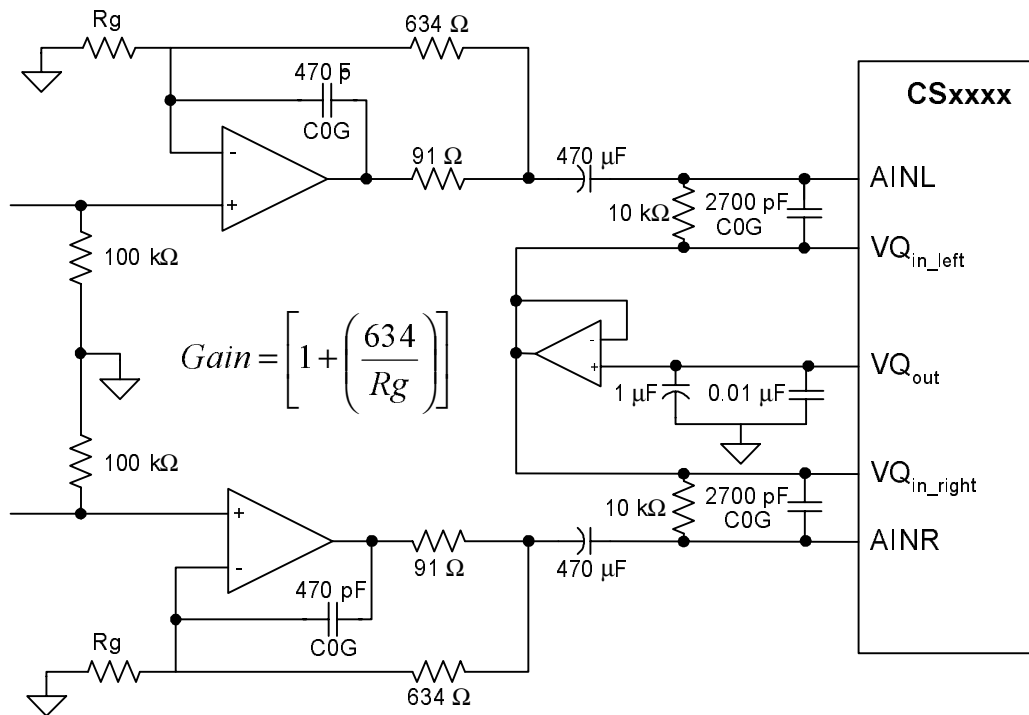


Figure 6. Single-Ended Input Buffer with Dedicated Reference Pins (Example #3)

4.8 Overview of Filter Topology #3

4.8.1 Op Amp Circuitry

The op-amp topology used in the input buffer shown in Figure 6 addresses two issues. First, it provides an extremely low output impedance and therefore minimizes the amount of distortion presented to the converter's internal sampling circuits. By placing the 91 Ω resistor in the feedback loop, its resistance is divided by the open-loop gain of the op-amp, providing a sub-ohm output impedance (not including the ESR of the AC-coupling capacitor). Secondly, this op-amp topology provides a low pass filter. Using the recommended values, this filter remains flat throughout the audio passband and provides approximately 20 dB of rejection at the modulator sampling rate (where the converter is susceptible to aliasing). The characteristics of this low pass filter can be changed by adjusting the values of the resistors and capacitors in the feedback loop. However, it is important to maintain a flat frequency response throughout the passband of interest and to provide reasonable attenuation at the input sampling rate of the converter. Also, low value resistors should be used to minimize the addition of resistor thermal noise.

4.8.2 High Pass Filter and DC Biasing

The outputs of the op-amps are AC-coupled to the converter, with the converter inputs being biased to the proper voltage level through a 10 k Ω resistor from the DC-biasing op-amp. The AC-coupling capacitor and resistor from the biasing op-amp form a high pass filter. The 3 dB corner of the high pass filter can be calculated as follows:

$$F_c = \frac{1}{2\pi RC}$$

where: R is the value of the resistor to the biasing op-amp (in Ohms)

C is the value of the AC-coupling capacitor (in Farads)

In the input buffer shown in Figure 6, $R = 10$ k Ω and $C = 470$ μ F. This places the 3 dB corner at approximately 0.03 Hz. Typically, this corner should be at least one decade below the bandwidth of interest in order to prevent a significant droop in the frequency response. The value of the AC-coupling capacitor must be large in order to prevent the DC resistance of the capacitor from degrading signal linearity. Please note that with 470 μ F aluminum electrolytic capacitors, distortion will begin to increase at input frequencies below 100 Hz.

In Figure 6, the AC-coupling capacitor will initially be charged up via the op-amp connected to the on-chip voltage reference. This charge up time is dependent on the size of the AC-coupling capacitor and the amount of series resistance to the op-amp. The time constant can be calculated as follows:

$$\tau = RC$$

where R = the amount of resistance between the AC-coupling capacitor and the op-amp (in Ohms)

C = the value of capacitance of the AC-coupling capacitor (in Farads)

In the input buffer shown in Figure 6, $R = 10$ k Ω , and $C = 470$ μ F. This produces a time constant of approximately 4.7 s. This would indicate that the capacitor will charge up to within 99% of the final DC value in approximately 23.5 s (which is 5 time constants).

4.8.3 Anti-Aliasing Capacitor

Figure 6 implements a common mode capacitor between the analog input and the associated reference voltage pin on each channel of the converter. This capacitor is commonly referred to as the anti-aliasing capacitor, and performs several functions. The value of the capacitor affects the overall low pass filter response and the amount of attenuation at the modulator sampling rate. This capacitor also acts as a charge reservoir for the internal sampling capacitors. Since this capacitor is located in the signal path, it is very important not to use capacitors with a large voltage coefficient (such as general purpose ceramics) since they can degrade signal linearity.

5. Single-Ended Input Buffer with a Common Reference Pin

5.1 Applicable Converters

A single-ended analog input buffer with a common reference pin is ideal for use with the following Cirrus Logic audio converters:

- CS5340
- CS5341
- CS5342
- CS42406

5.2 Introduction

A single-ended signal consists of only one signal line and hence requires only one input pin. Single-ended inputs typically require less input buffer components, but also have several disadvantages. First, at a given voltage level, a single-ended input cannot produce as much signal swing as a differential signal, hence reducing the dynamic range. Also, single-ended inputs are more prone to errors caused by DC offsets and coupled-noise.

5.3 Recommended Filter Topology

Figure 7 shows a single-ended analog input buffer. This buffer provides proper biasing, isolation from the switched capacitor currents, low output impedance, and anti-alias filtering.

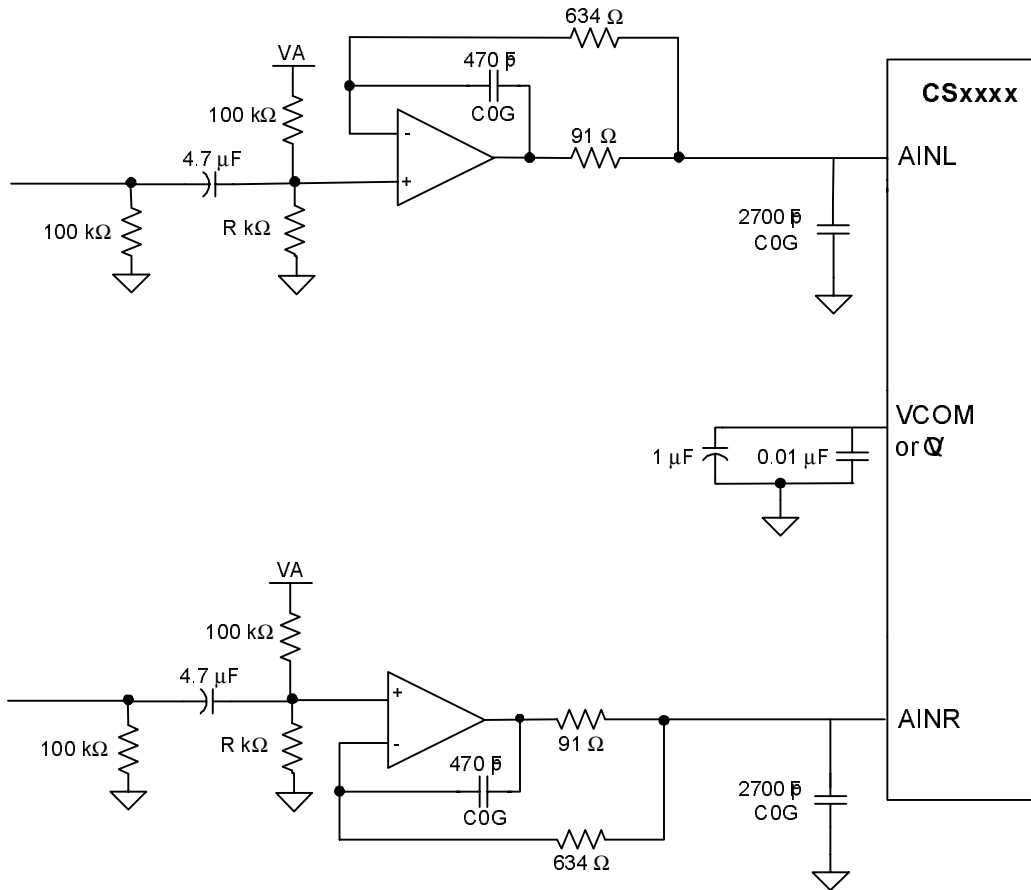


Figure 7. Single Ended Input Buffer with a Common Reference Pin

5.4 Overview of Filter Topology

5.4.1 High Pass Filter and DC Biasing

The first stage of the buffer forms a high pass filter from the combination of the AC-coupling capacitor along with the resistor divider that biases the positive terminal of the op-amps to the proper DC bias voltage. The value of the resistors denoted as “R” will vary depending on the optimal DC bias for the given converter. Typically this is around half of the VA voltage supply. Please refer to the converter datasheet for the recommended input bias voltage. The 3dB corner of the high pass filter can be calculated as follows:

$$F_c = \frac{1}{2\pi R_{EQ} C}$$

where: R_{EQ} is the value of the resistor divider in parallel (in Ohms)

C is the value of the AC-coupling capacitor (in Farads)

In the input buffer shown in Figure 7, $R_{EQ} \approx 50 \text{ k}\Omega$ ($100 \text{ k}\Omega \parallel R \text{ k}\Omega$) and $C = 4.7 \text{ }\mu\text{F}$. This places the 3 dB corner at approximately 0.68 Hz. Typically, this corner should be at least one decade below the bandwidth of interest in order to prevent a significant droop in the frequency response.

Since the input impedance into the op-amp is extremely high, the effective input impedance into the analog input buffer will be determined by the parallel combination of the resistors in the divider in parallel with the $100 \text{ k}\Omega$ shunt resistor. In the input buffer shown above, the input impedance is approximately $33 \text{ k}\Omega$. Ideally, the larger this input impedance the better. However, in the input buffer shown in Figure 7, the AC-coupling capacitor will initially be charged up via the resistor divider. This charge up time is dependent on the size of the AC-coupling capacitor and the amount of resistance to the VA voltage supply. The time constant can be calculated as follows:

$$\tau = R_{EQ} C$$

where R_{EQ} = the amount of resistance between the AC-coupling capacitor and the voltage supply (in Ohms)

C = the value of capacitance of the AC-coupling capacitor (in Farads)

In the input buffer shown in Figure 7, $R_{EQ} \approx 50 \text{ k}\Omega$ ($100 \text{ k}\Omega \parallel R \text{ k}\Omega$), and $C = 4.7 \text{ }\mu\text{F}$. This produces a time constant of approximately 0.24 s. This would indicate that the capacitor will charge up to within 99% of the final DC value in approximately 1.2 s (which is 5 time constants). The $100 \text{ k}\Omega$ resistors to ground on the input nodes allow a DC path to charge the AC-coupling capacitor, regardless of whether or not there is an input signal source present.

5.4.2 Op Amp Circuitry and Anti-Aliasing Capacitor

The op-amp topology used in the input buffer shown in Figure 7 addresses two issues. First, it provides an extremely low output impedance and therefore minimizes the amount of distortion presented to the converter's internal sampling circuits. By placing the $91 \text{ }\Omega$ resistor in the feedback loop, its resistance is divided by the open-loop gain of the op-amp, providing a sub-ohm output impedance. Secondly, this op-amp topology provides a low pass filter. Using the recommended values, this filter remains flat throughout the audio passband and provides approximately 20 dB of rejection at the modulator sampling rate (where the converter is susceptible to aliasing). The characteristics of this low pass filter can be changed by adjusting the values of the resistors and capacitors in the feedback loop. However, it is important to maintain a flat frequency response throughout the passband of interest and to provide reasonable attenuation at the input sampling rate of the converter. Also, low value resistors should be used to minimize the addition of resistor thermal noise.

Figure 7 implements a capacitor from the analog input to ground on each channel of the converter. This capacitor is commonly referred to as the anti-aliasing capacitor, and performs several functions. The value of the capacitor affects the overall low pass filter response and the amount of attenuation at the modulator sampling rate. This capacitor also acts as a charge reservoir for the internal sampling capacitors. Since this capacitor is located in the signal path, it is very important not to use capacitors with a large voltage coefficient (such as general purpose ceramics) since they can degrade signal linearity.

Contacting Cirrus Logic Support

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