21 October, 1983

Digital Delay Engineering Memo
Models: D1280 & D640

The D1280 and the D640 digital delays are the same design with the exception of the number of memory IC's used and the clock circuitry. The topic of this memo is encoder/decoder quantising errors and associated problems. This discussion applies to both products, the D1280 and the D640.

ADA employs an adaptive syllabic companded delta slope modulation technique for its encoder and decoder. The minimum sampling rate is 204.8kHz, while the maximum is 2.048mHz. Because of the wide sweep range, the encoder/decoder integrator time constants could not be optimized at either extremes of their sampling frequencies. The trade-off resulted in low frequency distortion at high sampling rates, and slew-rate and harmonic distortion at low sampling rates. The trade-off seemed acceptable for most music applications, however, in critical applications the distortion may be unacceptable. One solution to the problem of slew-rate distortion above 3kHz would be to keep the minimum sampling rate at 256Hz -- or better yet 320kHz. The maximum delay times would be 1024ms and 820ms. Trimmers T4 and T5 adjust the maximum and minimum clock frequency of the front panel potentiometer labelled "MULTIPLIER"

Another change would involve the pre-emphasis/de-emphasis circuity around the encoder/decoder. Removing C33 and C44 would decrease the amplitude of the input signal above 3kHz and thus decrease the slew-rate distortion. The trade-off would be a slight increase in "hiss" at the output of the delay line.

Further circuit changes are more complex and involve changing time constants in the encoder/decoder integrators. Any change made here to increase performance of one parameter always decreases performance in another area. The delicate balance present in the stock design was arrived at through many hours of listening tests. But those daring enough could try lowering the values of C7, C8, C14, and C15 to perhaps 820pf. All parts must be matched to 2%. Do not attempt to change the values of the input resistors (R17, R18, R34, and R35) because changing them would upset the stability of the decoder and hence the transient response of the circuit.

I hope that this memo answers some of your questions above our delay lines.

Sincerely,

David Tarnowski, chief engineer