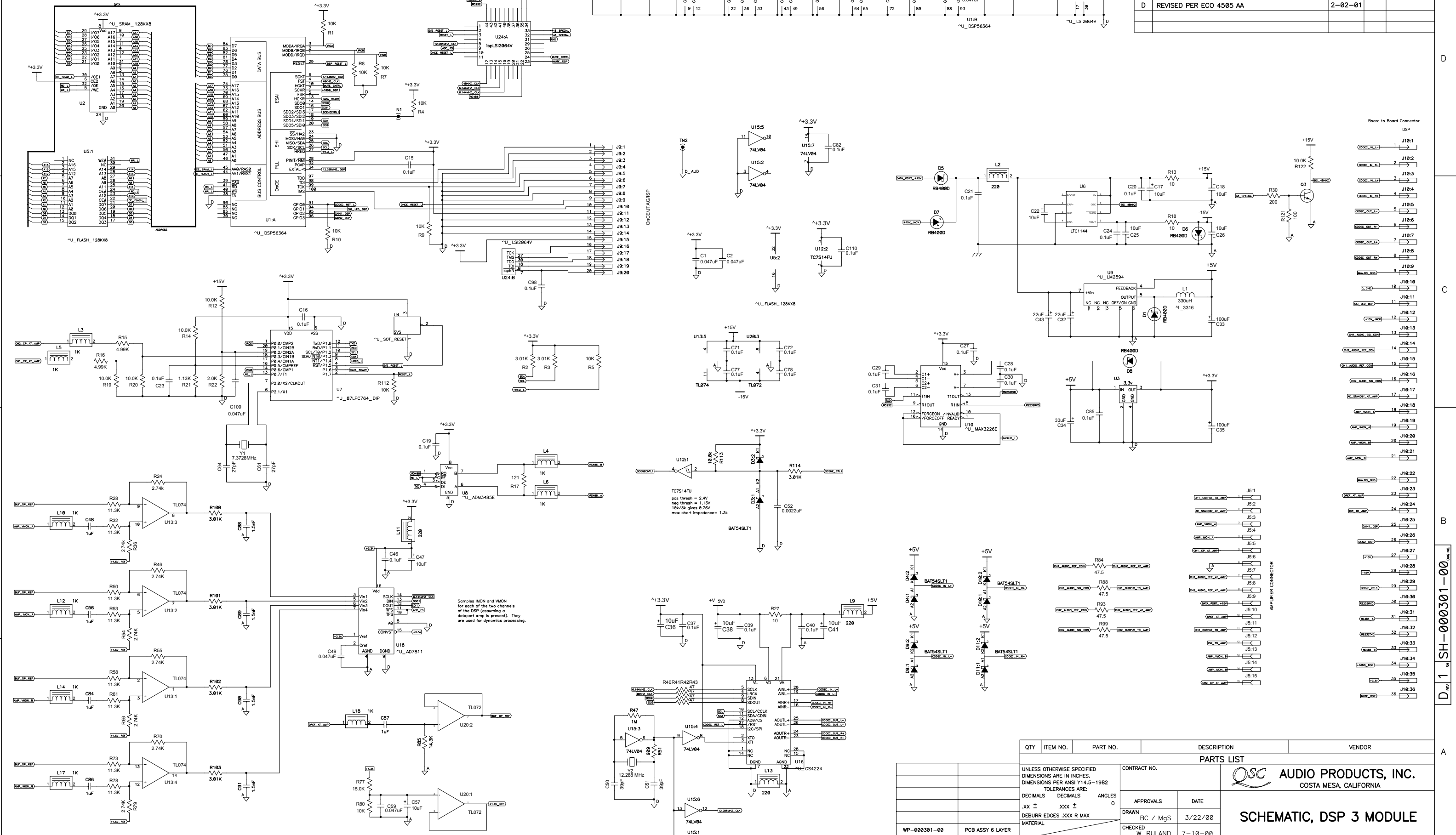


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REVISION				
REV	DESCRIPTION	EFF. DATE	CHK	APPROVED/DATE
A	PRODUCTION RELEASE PER ECO 4323 MP	7-19-00	DD	8-08-00
B	REVISED PER ECO 4366 AA	9-08-00	DD	9-08-00
C	REVISED PER ECO 4489 AA	1-05-01	DD	12-04-00
D	REVISED PER ECO 4505 AA	2-02-01		



THIS DRAWING USED IN CONJUNCTION WITH PCB FILE PC-000301-00

NOTES: UNLESS OTHERWISE SPECIFIED

QTY	ITEM NO.	PART NO.	DESCRIPTION	VENDOR										
PARTS LIST														
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. DIMENSIONS PER ANSI Y14.5-1982 TOLERANCES ARE:			<table border="1"> <tr> <td>APPROVALS</td> <td>DATE</td> </tr> <tr> <td>DRAWN BC / MgS</td> <td>3/22/00</td> </tr> <tr> <td>CHECKED W. RULAND</td> <td>7-10-00</td> </tr> <tr> <td>ISSUED D. DELARM</td> <td>8-08-00</td> </tr> <tr> <td>CAD SEED FILE NO.</td> <td></td> </tr> </table>		APPROVALS	DATE	DRAWN BC / MgS	3/22/00	CHECKED W. RULAND	7-10-00	ISSUED D. DELARM	8-08-00	CAD SEED FILE NO.	
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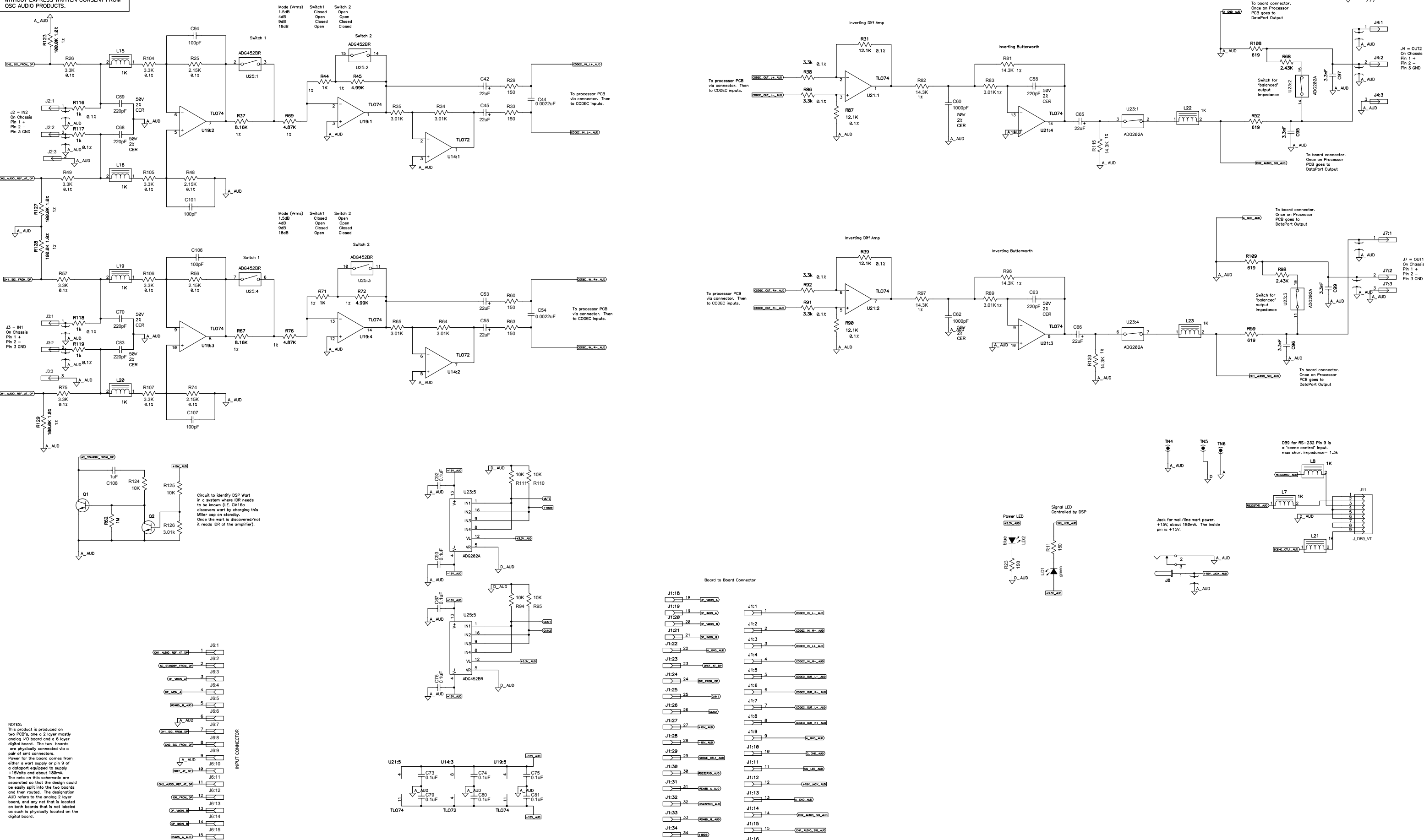
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NOTES:
This product is produced on two PCB's, one a 2 layer mostly analog I/O board and a 6 layer digital board. The two boards are physically connected via a pair of smt connectors.
Power for the board comes from either a wort supply or pin 9 of a dataport equipped to supply +15volts and about 180mA.
The nets on this schematic are separated so that the design could be easily split into the two boards and then routed. The designation AUD refers to the analog 2 layer board, and any net that is located on both boards that is not labeled as such is physically located on the digital board.

NOTES: UNLESS OTHERWISE SPECIFIED

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