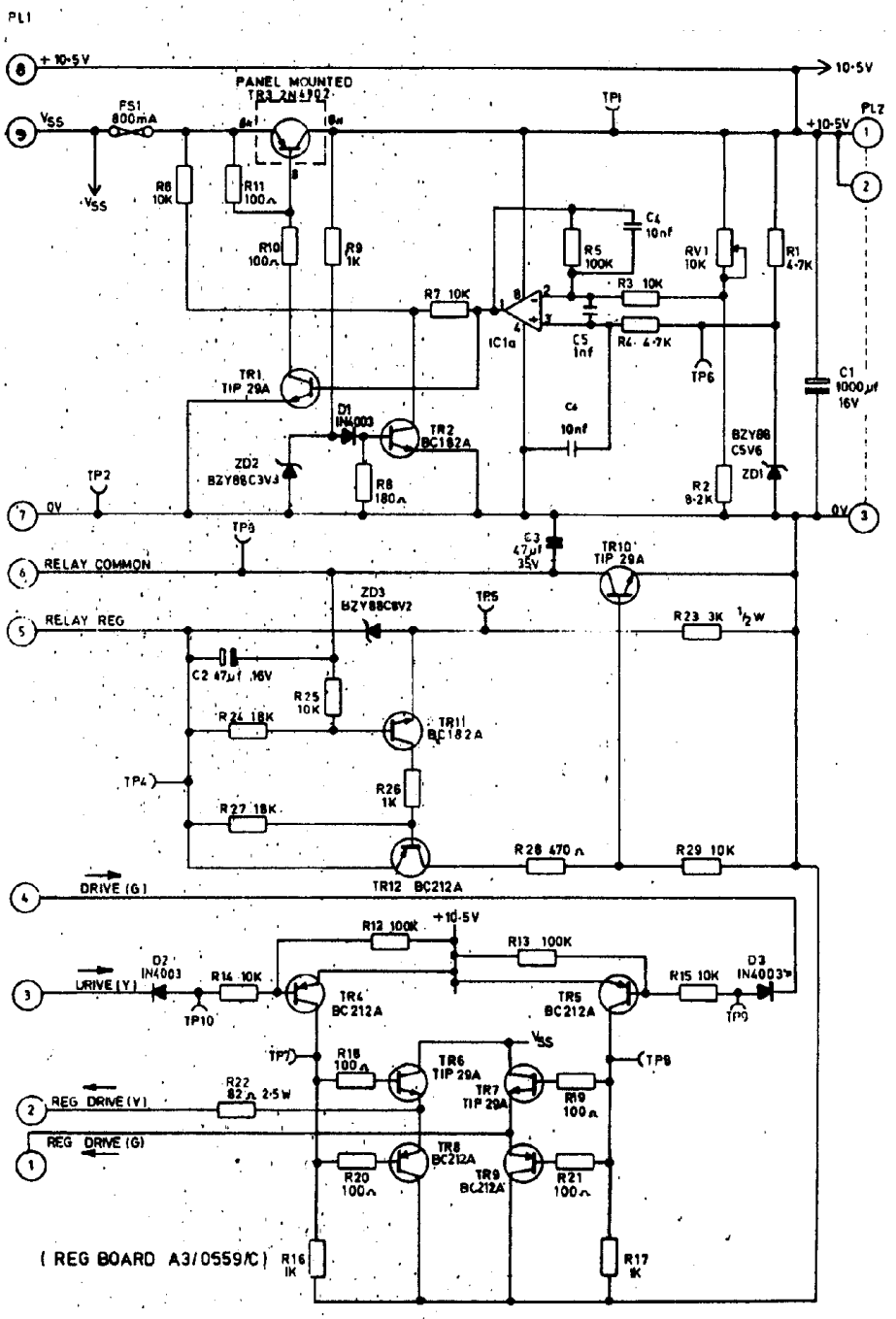
Regulator Board



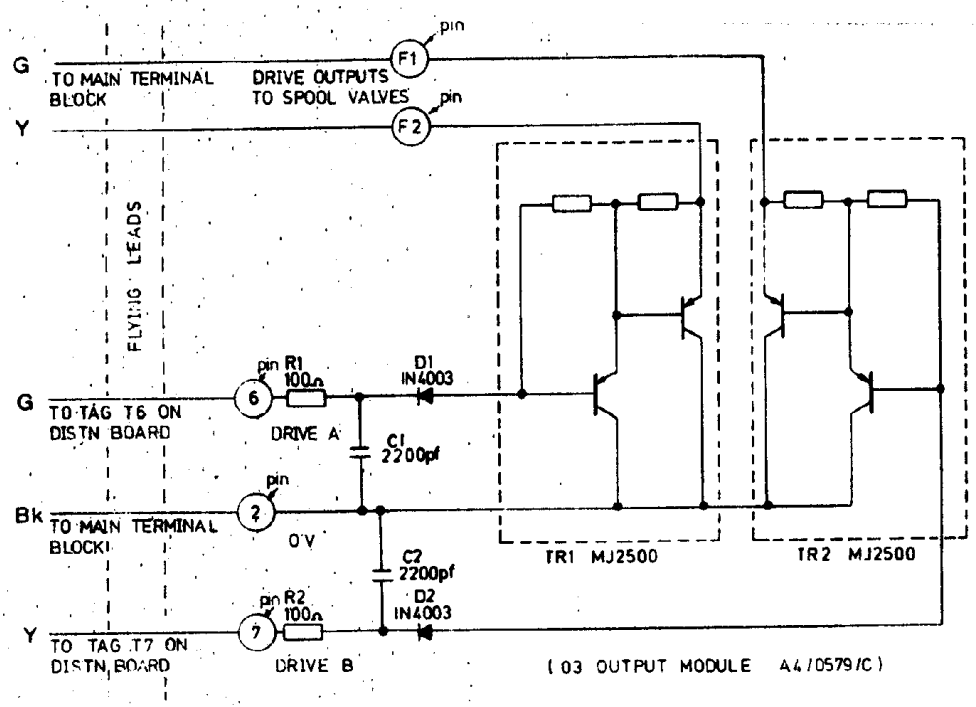
The regulator PCB consists of three independent regulator circuits:-

(1) +10.5v stabilised line, which is the basic voltage reference for the system and appears at PL1/8 and in plug PL2/1&2. The level is set by potentiometer RV1.

(2) +12v rough regulation for relays RLA and RLB on the distribution board. This appears at PL1/5 and 6.

(3) +8.5v supply for the 504 servo motor. The drive inputs originate from the 701 control unit and appear at PL1-3 and PL1-4. These are normally high (at ship's supply) but one or the other goes low in the drive mode. TR4 and TR5 covert the signals to 10.5v for drive, and 0v for no drive, and these appear at PL1/ 1&2.

Output Module 03



The 03 Output Module assembly consists of a PCB mounted on a heatsink chassis. It is used to drive hydraulic spool valves.

The drive inputs enter the board on PIN 6 and flying lead (drive A) and PIN 7 and flying lead (Drive B). When these inputs are positive the darlington transistors TR1 and TR2 are turned off and no energisation takes place via flying lead outputs F1 and F2. When either one or other drive input (PIN 6 or PIN 7 and flying leads) is taken low (to 0V) the appropriate darlington transistor is turned on causing current to flow from negative rail (PIN 2 and flying lead) through the transistor and relevant output energising one of the two spool valves.

The return path is via terminal E10, which is high only when the 701 is switched to DRIVE.
Thus for Phasing A :-
Port Spool Valve connects between terminal F2 and E10
Starboard Spool Valve connects between terminal F1 and E10.
Reverse connections for Phasing B.

Output Module 07

The 600/7 drive board assembly consists of a PCB mounted to a heatsink chassis. It is used to drive the coils of heavy duty relays and solenoids.

Refer to Circuit Diagram A3/0574/C

The drive command inputs enter the board at PIN 6 and flying lead (DRIVE A IN) and PIN 7 and flying lead DRIVE B IN). These are generated by the 701 control unit. Each channel is identical and operation of one channel only will be described in detail. The circuit references in parenthesis refer to the opposite channel.

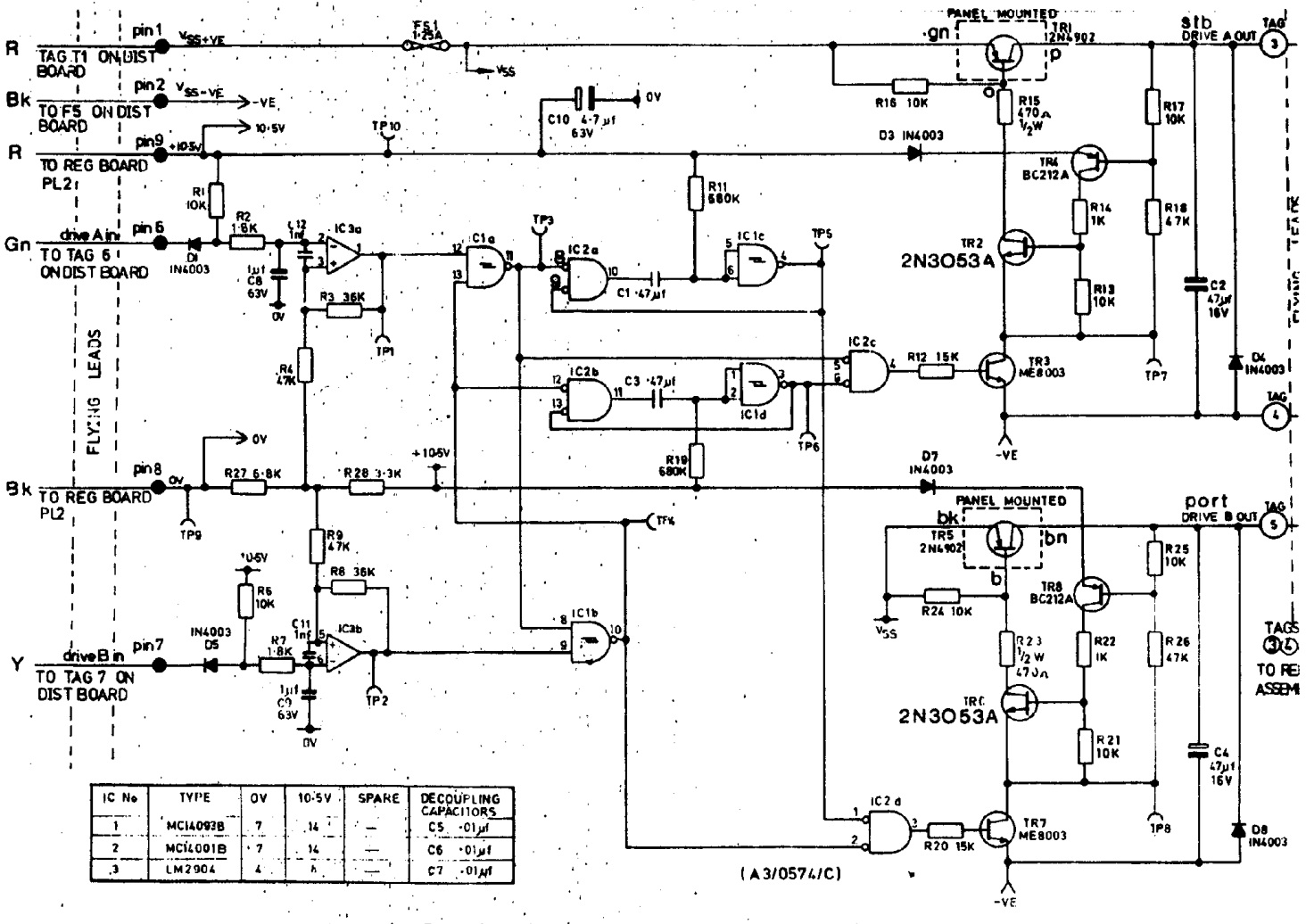
An input network shapes the 701 drive output to a CMOS compatible level and prevents switching transients from the 701 causing mistriggering of the drive output.

Diode D1 (D5) and resistor R1 (R6) limit the input high level (12 - 40V) to the system regulated supply of +10.5V. R2 and C8 (R7, C9) form a simple low pass filter which effectively filters high frequency parasitic pulses. IC3a (IC3b) is an inverting op-amp schmitt trigger which triggers at 8.5V when the inverting input is positive going and at +3V when the inverting input is negative going. Integrated circuits IC1a and IC1b are cross-coupled NAND schmitt triggers. The schmitt action shapes the output from the previous stage and by being cross coupled both channels are prevented from being activated simultaneously. Consider both inputs "off". With DRIVE A IN (PIN 6 flying leads), positive input pin 12 of IC1a is low, forcing IC1a output high and enabling input 8 of IC1b. Similarly with DRIVE B IN (PIN 7 and flying lead) positive input pin 13 of IC1a is also enabled.

When DRIVE A IN (PIN 6 and flying lead) goes low (i.e. a-drive command) pin 12 of IC1a goes high and provided DRIVE B IN is still positive the output of IC1a goes low. This low disables IC1b blocking drive command signals on channel B. Similarly, the output of IC1b goes low disabling IC1a when DRIVE A IN is positive and DRIVE B IN is low.

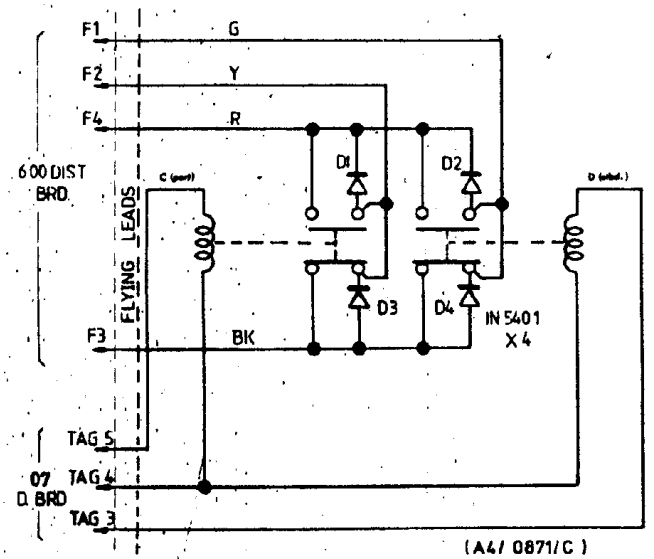
IC2a, IC1c, C1, R11 and IC2b, IC1d, C3, R19 form two monostables whose outputs are normally low enabling one input of IC2c and IC2d. When the output of IC1a (IC1b) goes low the other input of IC2c (IC2d) is enabled, forcing the output of IC2c (IC2d) high and switching on TR3 (TR7). When the drive command ceases and the output of IC1a(IC1b) goes high, monostable IC2a/C1/R11/IC1c (IC2b/C3/R19/IC1d) is fired and the output of IC1c (IC1d) goes high for approximately 200 mS disabling IC2d (IC2c) and preventing the other channel from switching on for this time period. This prolongs the life of the relay contacts.

When TR3 (TR7) is switched on by the output of IC2c (IC2d) going high, a 0V reference is applied to the output regulating circuitry. At the instance of "switch-on" TR4 (TR8) is switched hard on causing TR2 (TR6) and in turn TR1 (TR5) to start to conduct. When TR1 (TR5) begins conduction the base of TR4 (TR8) rises to Vref on D3 (D7), causing the transistor to conduct less. This then has the effect of reducing conduction in TR2 (TR6), which in turn causes TR1 (TR5) to begin to turn off. An equilibrium point is reached regulating the output at approximately +12v.



IC No	TYPE	0V	10·5V	SPARE	DECOUPLING CAPACITORS
1	MC14093B	7	14	—	C5 ·01µf
2	MC14001B	7	14	—	C6 ·01µf
3	LM2904	4	11	—	C7 ·01µf

Output Module 07 - Drive Board Circuit



Output Module 07 - Solenoid Circuit