CMOS Circuits

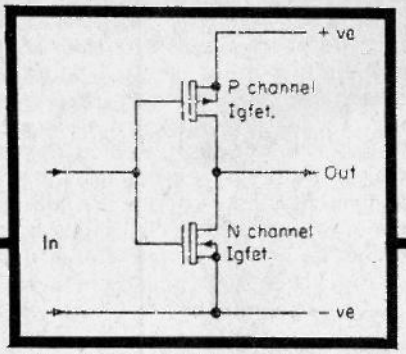

Fig. 1 Basic CMOS inverter circuit.

CMOS circuits to tickle your imagination and clutter every flat space, by R.A. Penfold.

ALTHOUGH CMOS ICs are a range of digital devices they are suitable for a range of applications which is far more diverse than one might expect. In fact, there can be little doubt that these ICs are the most useful range of digital devices for the average amateur user, and are perhaps even the most useful range of ICs of any type.

When CMOS devices were first introduced in the early 1970s they were much more expensive than their alternatives in other logic families. This is not the case these days and they are now about the cheapest ICs available. The more simple of the devices in the CMOS range cost less than many ordinary transistors, and on a cost basis these ICs are just about unbeatable.

Earlier families of digital devices suffer from three main disadvantages which limit their usefulness to the amateur. They require relatively high supply currents (about 20 mA for a simple quad gate IC), supply voltages are rather critical (5 V ± 10% for TTL devices for instance), and input impedances are usually rather low, often being only in the region of a few hundred ohms.

CMOS devices do not have any of these disadan tages. They require only very modest supply currents, and even some quite complex devices, such as the 4046 low frequency phase locked loop will operate at supply currents of less than 1mA. Simple gates, when they are in a static condition, use virtually no power at all.

The supply voltage range over which a CMOS device will operate depends upon the suffix given after the type number. The devices usually supplied to amateur users, and specified for the projects in this book, have an 'AE' suffix. The 'A' of the suffix denotes that the unit has an operating voltage range of 3 to 15 V and the 'E' indicates that it is contained in a standard DIL plastic encapsulation.

Input impedances of CMOS ICs are extremely high indeed, being something in the order of 1,000,000 Megohms. For all practical purposes they can be regarded as having an infinite input impedance, and are voltage rather than current operated devices.

TOUCH SWITCH

Touch switches seem to have become quite popular these days and although this is probably mainly due to their novelty value rather than any practical advantage, they do have certain practical advantages over more conventional forms of switch. Probably the main one in most applications is that they can be designed to have no moving parts to wear out. This makes them as reliable and hard wearing as the main (electronic) part of the equipment they are controlling.

The circuit diagram of a simple touch switch using a CMOS bistable circuit is shown in Fig. 3. This will provide on/off switching for any piece of 9 volt battery operated equipment which does not have a current consumption of more than 100 mA (the maximum operating current for the 2N3905 transistor).

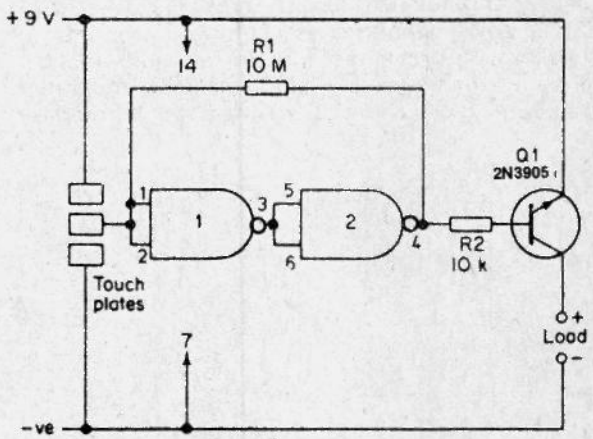

Fig. 2 The touch switch circuit.

CMOS ICs are ideal for use in this particular application since they can easily provide the necessary very high input impedances, and they also consume no significant current when they are not driving a load. The current consumption of this circuit in the off state is very low, being actually less than 1 micro-amp. There is subsequently no significant battery drain when the equipment is turned off, and the battery life should not be significantly less than if a mechanical switch were used.

The circuit operates in the following manner. When the power is initially connected to the device the output of the bistable will go into the high condition. Q1 is cut off and no power is applied to the load.

It is possible to alter the state of the bistable by touching the lower set of touch contacts. The resistance of the operators skin then takes the input of the bistable low, and the output of the bistable will then also go low. A base current is then applied to Q1 which is biased into saturation and virtually the full supply rail potential is supplied to the load.

The unit can be switched off again by touching the upper set of touch contacts. The input of the bistable is then connected to the positive supply by way of the skin resistance of the operator's finger, and in consequence

both the input and output of the bistable take up the high condition. Q1 is therefore cut off once again, with no significant current being supplied to the load.

R1 provides the necessary latching action by holding the input in whatever state it was in when the finger of the user is removed from the touch contacts. If necessary, the sensitivity of the circuit can be boosted by raising the value of R1. Resistors having values of more than 10 Megohms are not readily available, and so an increased value for R1 can only be obtained by adding two or more resistors in series to make up the required value.

R2 is needed in order to prevent Q1 from passing an excessive base current. It also limits this current to an economical level. If the unit is being used to control a fairly high current level. If the unit is being used to control a fairly high current load, say 25 mA or more, it is necessary to reduce the value of R2 to 1 k.

CRYSTAL OSCILLATOR

Crystal oscillators have been used since the early days of entertainment broadcasting whenever a highly stable RF oscillator is required. They are probably used more now than at any time in the past, and apart from use in crystal calibration oscillators and similar radio applications they are often used in digital clocks and other digital equipment where they generate a stable timebase signal.

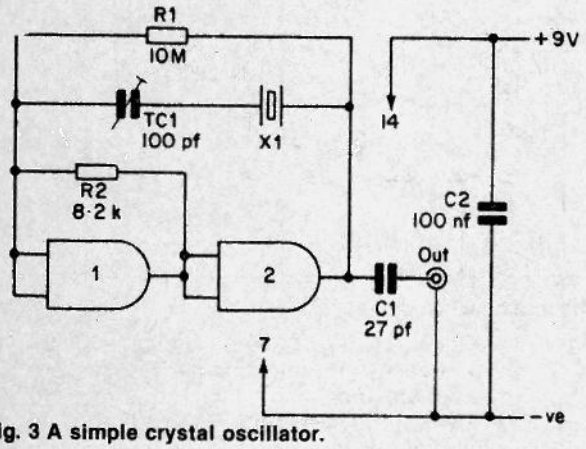

Fig. 3 A simple crystal oscillator.

CMOS ICs can be used as the active devices in good quality crystal oscillators having operating frequencies up to about 10 MHz or so Fig. 3 shows the circuit diagram of a simple CMOS crystal oscillator which uses a couple of inverters.

The two inverters are used to provide an amplifier which has its input and output of the amplifier via TC1, and at the series resonant frequency of the crystal (where it has a very low impedance) positive feedback will be applied to the circuit and it will oscillator.

VC1 enables the oscillation frequency of the circuit to be finely trimmed to the nominal frequency of the crystal. If this feature is not required VC1 can be omitted, with the crystal then being connected in parallel with R1.

At first sight R1 may appear to perform no useful function, but it was found to be necessary to add this as otherwise the oscillator often failed to start when power was applied to the circuit. C1 is the output DC blocking capacitor and C2 is a supply decoupling capacitor.

This circuit seems to operate satisfactorily over a wide range of frequencies with the component values shown, and the prototype oscillated properly with any crystal having a frequency from a few tens of kHz to many MHz.

CAPACITANCE METER

Most multimeters are equipped to measure wide ranges of voltage, current, and resistance, but few, if any, are capable of capacitance measurements. As a result of this, most electronics enthusiasts are unable to undertake capacitance measurements. and this must lead to many useable capacitors being discarded simply because their identification markings have become erased. Some means of testing capacitors is also very useful when one is engaged on servicing faulty equipment.

A capacitance meter is therefore a very useful piece of equipment to have in the workshop. A simple capacitance meter can be based on an astable and a monostable multivibrator, and it is possible to make one using a single CMOS IC as the only active device. The circuit diagram of such a unit is shown in Fig. 4 and this uses a single 4001 IC.

Gates 1 and 2 are connected as the astable circuit and gates 3 and 4 form the monostable multivibrator. The astable operates at a frequency of about 100 Hz, and its output is fed to the trigger input of the monostable. Thus

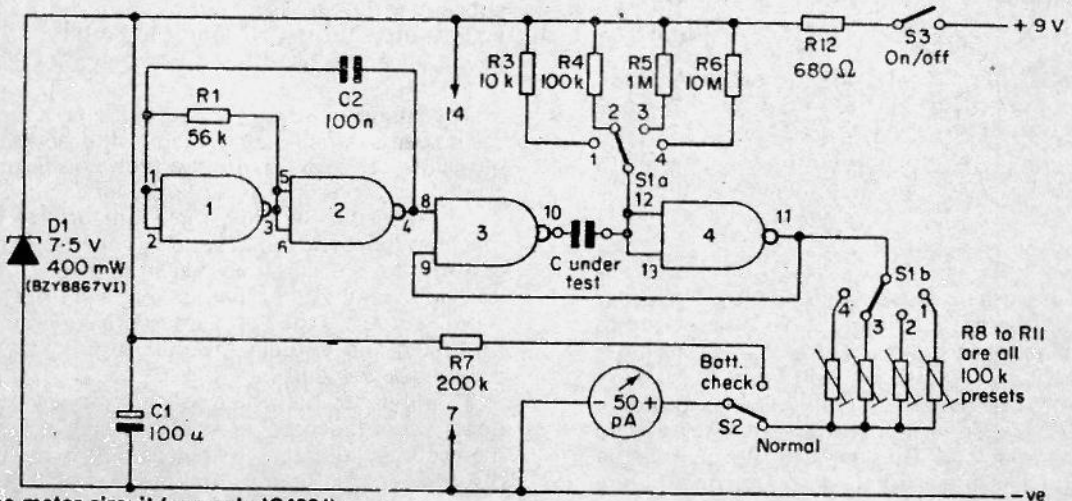

Fig. 4 Capacitance meter circuit (use only IC4001).

one hundred times per second the monostable will produce an output pulse. The length of this output pulse is determined by the values of the timing components, and the timing capacitor under test. The timing resistor is one of the four resistors, R3 to R6, and is whichever one is switched into circuit by S1.

By using four timing resistors the unit is able to provide four measuring ranges. These are as follows:

Range 1	0 to 500 nF
Range 2	0 to 50 nF
Range 3	0 to 5 nF
Range 4	0 to 500 pF

The unit thus covers most normal amateur requirements. The circuit values have been chosen so that the monostable acts as a pulse shortener. For instance, with the unit switched to Range 1 and a 500 nF test capacitor in circuit, the output pulse from the monostable will only be about half the length of the trigger pulse from the astable. Lower values of test capacitance will produce an even shorter monostable pulse length.

A voltmeter circuit consisting of M1 and one of the set of four preset resistors (R8 to R11) is connected at the output of the monostable. Each time the output of the monostable goes high, a pulse of current will be fed to the meter. A constant string of pulses are generated when a test capacitor is connected to the unit, and the meter will respond to the average output voltage.

On Range 2 the timing resistor is ten times the value of that used on Range 1. Only one-tenth of the previous test capacity is therefore needed to produce an identical meter reading. For example, 500 nF was needed to produce FSD of the meter on Range 1 whereas only 50 nF will be needed on Range 2. In practice this is not quite the case since the tolerances of the timing resistors will prevent such a precise relationship from being obtained. In order to ensure that good accuracy is obtained on all four ranges, a different preset resistor for each range is provided in the meter circuit. This enables each range to be calibrated against a close tolerance capacitor.

An alternative approach is to use 1% tolerance components for R3 to R6, and a single calibration preset. The unit would then only need to be calibrated on one range, with good accuracy being automatically obtained on the other three ranges.

A simple battery check facility is incorporated in the circuit, and this merely consists of S2 and R7. When S2 is in the position shown, the circuit functions normally. The meter is connected across the stabilised supply rail when S2 is in the other position. It is connected via R2 which converts the meter into a 0 to 10 V voltmeter. This can be used to monitor the supply potential and when it falls below its nominal level of 7.5 V, this indicates that a new battery is required.

Calibrating the unit is quite straightforward, and four

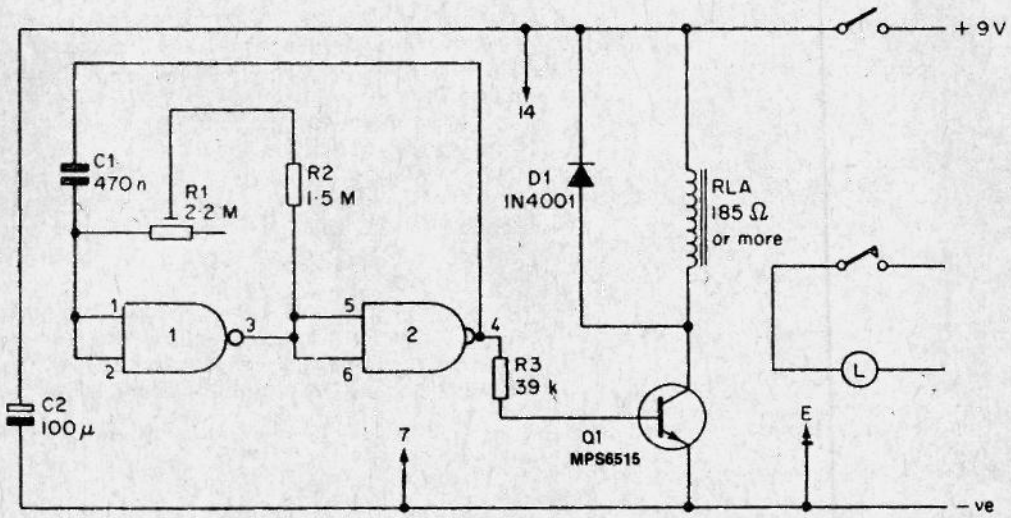

Fig. 5 Christmas tree lamps flasher.

With a 500 nF capacitor in circuit, R9 is adjusted to produce FSD of the meter. If, for instance, a 100 nF capacitor is connected in place of the 500 nF one, the length of the output pulses will only be one-fifth of the previous duration. The rate at which the monostable is triggered is the same, and so the pulses still occur at the same frequency. Therefore, the average voltage across the meter circuit will only be one-fifth of its original level and the meter will read one-fifth FSD.

It will be apparent from this that there is a linear relationship between the meter reading and the value of the test capacitor. The unit thus functions very effectively as a linear reading capacitance meter.

close tolerance capacitors are required for this. For example, a 470 nF 2% capacitor could be used to calibrate Range 1. With this connected across the test terminals and the unit set for normal operation on Range 1, R10 would be adjusted for a reading of 47 on the meter.

It is best not to use a calibration capacitor which has a value corresponding to less than half FSD of the range being calibrated, as this will result in inferior accuracy being obtained. It is advisable to initially adjust all the preset resistors for maximum resistance before commencing calibration of the unit.

FLASHER

Several useful gadgets can be made by using a multivibrator to drive a relay, and a popular example is a Christmas Tree Lights Flasher. This will provide a much more regular flashing rate than can be obtained by using a bi-metal flashing bulb, and the flashing rate can also be made variable. The circuit diagram of this device appears in Fig. 5.

The two inverters are connected as a low frequency astable circuit, and the operating frequency of this is variable over a range of about 0.5 to 1.5 Hz by means of R1. The output of inverter 2 drives common emitter amplifier Q1 via R3. R3 is a current limiting resistor.

Q1 has the relay coil as its collector load, and the relay will be energised when the output of inverter 2 is high. The relay will be of when the output of inverter 2 is low A single set of relay contacts (either normally closed or normally open ones) are used to control the lights. These will therefore switch on and off at a rate determined by the setting of R1.

D1 is a protective diode, and this is needed to protect the circuit against the high reverse voltage which is developed across the relay coil as the power to the circuit is switched off. This voltage is generated by the magnetic lines of force quickly decaying and cutting through the relay coil. Because of the speed at which this magnetic force dies away, quite a high voltage can be produced, but it is at a high impedance. D1, in effect, shorts out this voltage and is protected against passing an excessive current by the high source resistance of the signal. D1 should not be omitted from the circuit as this voltage spike is quite capable of destroying both the IC and Q1.

Schmitt trigger. The trigger circuit then provides a base current to a high gain Darlington pair using Q1 and Q2. Q2 is a power transistor which is capable of handling the relatively high current drawn by a parking light. S1 enables the light to be turned on indpendently of the automatic circuitry.

In this circuit the current consumption of the device is of secondary importance since it will be powered from a high capacity car battery. However, it is obviously desirable to have the lamp switching cleanly from one state to the other. Perhaps less obviously it is necessary for the circuit to avoid intermediate output states in order to illiminate the possibility of damage to Q2 due to overheating.

This could occur if Q2 was partially switched on with about half the supply voltage being present at its collector, as it would then have to dissipate several watts of power. This could be overcome by using a large amount of heatsinking for Q2, but it is probably better to use a trigger circuit, as Q2 can then only rest in the hard on or fully off state. The dissipation in either case can only be low, as when it is turned hard on very little voltage is produced across it, and when it is turned hard off it passes no significant current. It will dissipate a significant amount of power when it is turned on, and if a high current lamp is being controlled a certain amount of heatsinking will be necessary, but this will only need to be minimal. In all the light switches just described it is possible to adjust the circuit by means of RV1 to produce a switching threshold at almost any required light intensity.

ELECTRONIC EGG TIMER

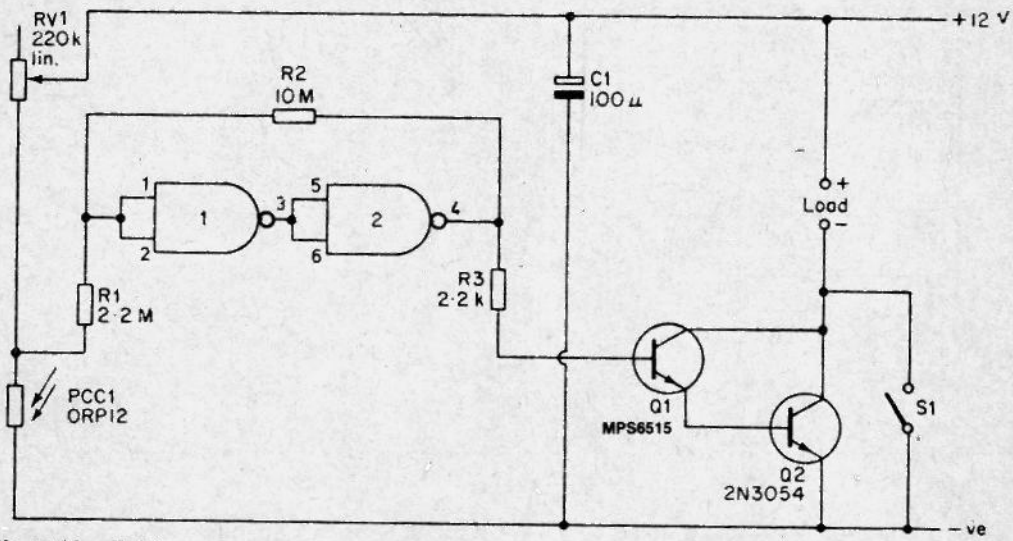

Fig. 6 An automatic parking light.

AUTOMATIC PARKING LIGHT

In applications where a light switch is to be used to operate a low voltage DC load it is usually possible to use a relayless circuit. An automatic parking light for a car is one such example, and a suitable circuit is shown in Fig. 6.

Here the circuit is triggered when the light level falls below a level which causes the voltage at the junction of RV1 and PCC1 to exceed the trigger voltage of the

Simple timers which provide an audible output at the end of a variable timing period are always interesting. Such circuits are limited to a maximum timing interval of only about 10 seconds, because using a longer time constant would result in the tone generator being turned on only gradually, which would obviously not be satisfactory.

The timer circuit shown in Fig. 7 uses an R—C timing network and an astable multivibrator tone

generator. The multivibrator itself is controlled via a control voltage which is fed to one input of gate 4. This terminal is normally low and the astable circuit is muted. The output of gates is also normally low with Q1 being cut off and passing no current. This is very important, as if it were normally high, Q1 would be biased on and there would be a very high static current consumption.

Gates 2 and 3 are used as the Schmitt trigger, and this has its input fed from an inverter which in turn has its input fed from the R—C timing network. C1 is the capacitive part of the timing network and R1 — RV1 are the reistive part.

immediately go high. This turns on the multivibrator and the audible alarm tone is produced from the speaker.

When the unit is switched off, S1a discharges C1 and the unit is then ready to start another timing period when it is switched on once again. RV1 enables the length of the timing interval to be varied from less than 30 seconds to more than 6 minutes, and the unit is thus suitable for use as an egg timer. or indeed for a multitude of uses in the house. A timer of this type can be much more useful than one might imagine.

A dial calibrated in minutes should be marked around the control knob of RV1, and there is unfortunately no

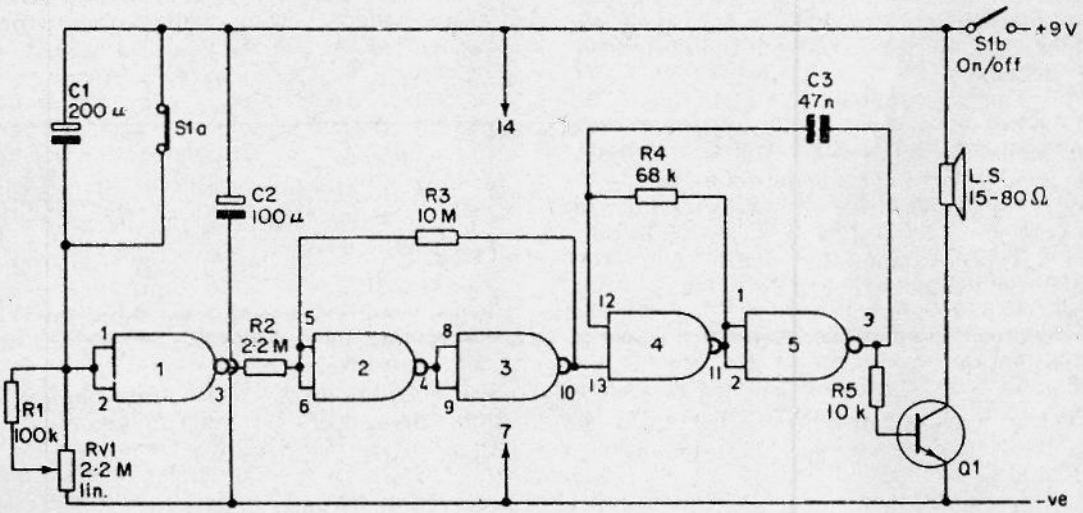

Fig. 7 Electronic eggtimer circuit (use 4011 only).

ELECTRONIC GAME

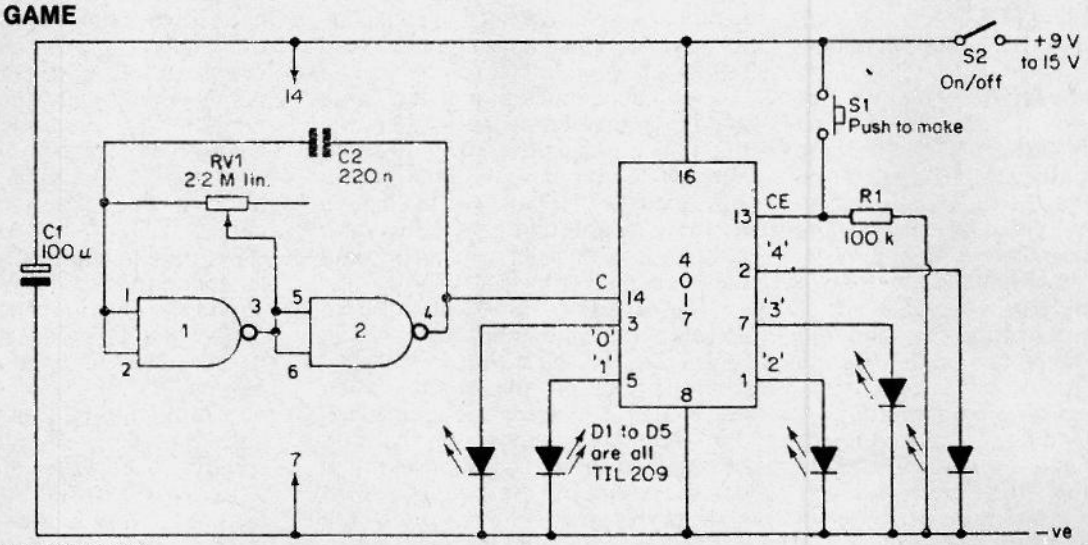

Fig. 8 Simple electronic game.

S1a opens when the on/off s with (S1b) is closed and this starts the timing interval. C1 begins to charge up through RV1 and R1 and eventually the voltage across R1 and RV1 will fall to the transfer voltage of gate 1. When this happens, the output voltage of gate 1 will gradually begin to rise. After a short while its output voltage will reach the trigger voltage of the Schmitt trigger circuit, and the output of inverter 3 will

quick way of doing this. It is a matter of finding all the calibration points using a process of trial and error.

Note that this circuit can only be built using a 4011 IC, as gate 4 must be a NAND type. In actual fact it requires two ICs, since five gates are employed in the circuit and only four are contained in each 4011 IC. The diagram above shows that the 4017 IC has ten outputs are utilised in the circuit of Fig. 9 which shows

how the device can be used as the basis of a simple electronic game. It also demonstrates the properties of the 4017 IC.

The two inverters are used in an astable multivibrator, and the operating frequency of this can be varied from less than 1 Hz to over 100 Hz by means of RV1. The output of the multivibrator is used to drive the clock input of the 4017.

The clock enable terminal of the 4017 is connected to ground through R1, and so when S2 is closed and power is applied to the circuit, the 4017 will start to operate. The first input cycle will cause pin 3 (the 'O' output) to go high, and the first LED will light up. At the commencement of the next clock input cycle pin 3 will return to the low state and pin 5 (the '1' output) will go high for one complete input cycle. Then pin 5 goes low and pin 1 goes high, and so on until all the LEDs have turned on in sequence.

There is then a pause during which none of the LEDs come on, and this is the period during which the unconnected outputs go high. When all five of these outputs have gone high the cycle starts once again from the beginning, with the five LEDs turning on in sequence followed by a break.

In practice the LEDs are mounted in a row along the front panel of the unit, and the idea of the game is to stop the sequence when the middle LED (D3) is on. The sequence is stopped simply by pressing S1 which is a push to make non-locking push button switch. When this is operated it takes the clock enable input high, and this blocks the clock signal and holds the 4017 in whatever state it was in when at the instant S1 was closed.

The circuit is reset ready for a new round by releasing S1. The sequence then continues from where it left off. The speed at which the circuit operates, and therefore the degree of difficulty, is controlled by the setting given to RV1. The circuit may appear to be one that tests the reaction speed of the competitor, but it is really more a test of co-ordination and anticipation.

It is possible to use the circuit from a 9 volt supply, but the LED display will not be very bright and it is better to use a supply voltage of about 12 to 15 volts.

ETI

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Continued from page 40

multi-element crossovers were not necessary, and as a result only a few components are used in the Keesonic models. The overcomes the problems of low efficiency and loss of signal detail.

The Keesonic Kolt is engineered for restricted listening areas, and measures only 238 x 133 x 165 mm, weighs less than 4 kg, and will handle 60W.

The major British companies, of course, manufacture their own drivers and have formulated various synthetic materials. These range from Bextrene thermo-plastic cones to polyester weave domes for the high frequency drivers. B and W introduced in its Series 80 mid-range head assembly a special type of glass reinforced concrete, and the outer head casing is moulded in rigid polystyrene.

Designers have paid great attention to overloading, which can result in distortion and even damage to the speaker, and the world's first automatic overload protection system was incorporated in the B and W 801 Studio Reference Monitor. The company's DM12 model has an even more refined version in the form of APOC, which stands for audio powered overload circuit.

Steady State And Transient

KEF has its S-Stop - steady state and transient overload protection -system, which is fitted to the KEF Reference Model 101.

For 25 years the QUAD, electrostatic has been regarded by many audiophiles as the standard by which other loudspeakers are judged. It thus is a major event when QUAD's designer, Peter Walker, and his colleagues introduce a new model based on the same principle.

The concept of a relatively large and light membrane acting directly upon the air, and driven over its entire surface in a controlled manner, is very attractive. In fact, work was done on the concept long before Rice and Kellogg invented the familiar moving coil loudspeaker in 1925-26.

QUAD's new ESL-63 stems from 18 years of development work. Given the acronym FRED - full range electrostatic doublet - this dipole source has benefits in terms of room position and stereo perception. The ratio of direct to reflected sound is much greater with a dipole source, which gives better localisation of the stereo image, and its sound dispersion pattern is substantially figure-of-eight.

Concentric Rings

The centre diaphragm of the ESL-63 consists of about half a square metre of suspended thin plastic sheeting, with a special coating, and on each side of it a set of electrolstatic plates. The central "disc" is fed directly with high voltage audio, and concentric rings receive the audio signals through a system of electronic time delays, which lengthen according to each segment's distance from the centre. The two areas furthest from the centre are fed from a normal capacitive delay, so that they have only the frequency dependent characteristic necessary to improve response and phase linearity.

The base stand contains the electronics required to supply the 5 kV polarisation voltage, audio currents and complex protection circuitry.

From an auditory standpoint, the listener cannot ascribe the source of sound to the loudspeakers, and a stereo pair creates an illusion of depth as well as width in the sound picture.

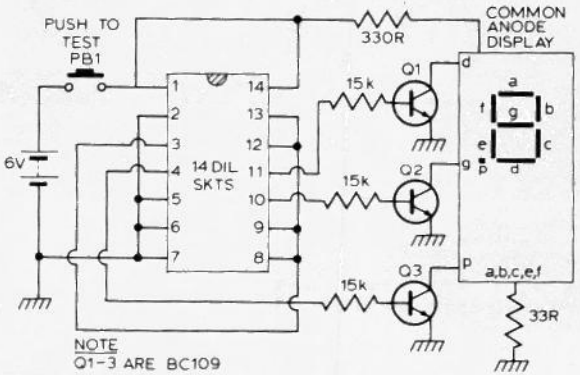
Although the ESL-63 may not be able to produce sounds loud enough for the rock music enthusiast, this latest QUAD design offers a fidelity for the listener in the home that has to be heard to be believed. In fact, the sound quality is of such a standard that all source - broadcast, disc or tape - imperfections are very evident. (16D981/JS)

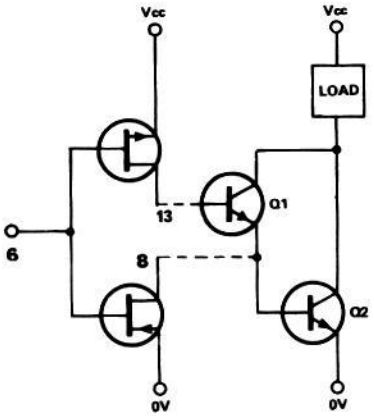
ETI

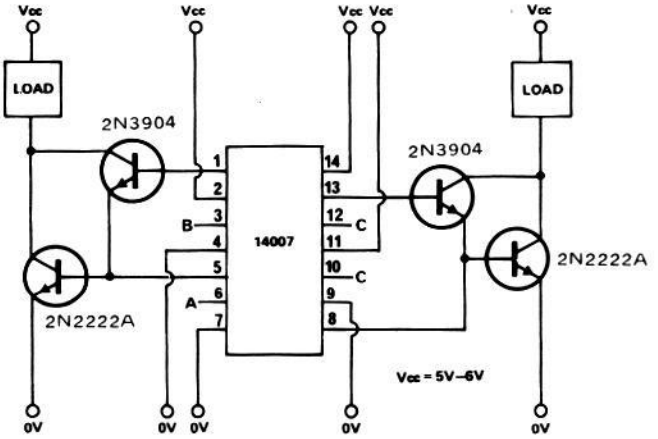
CMOS Gate Identifier

C. Ching

This circuit can be used to distinguish four types of dual input gates — AND, OR, NAND, NOR — it is also a quick method of checking IC function. If an AND gate is inserted into the socket, an A appears on the LED. An O denotes an OR gate. The decimal point is used to denote inverted function, i.e. .A is an NAND gate.







Darlington Drivers

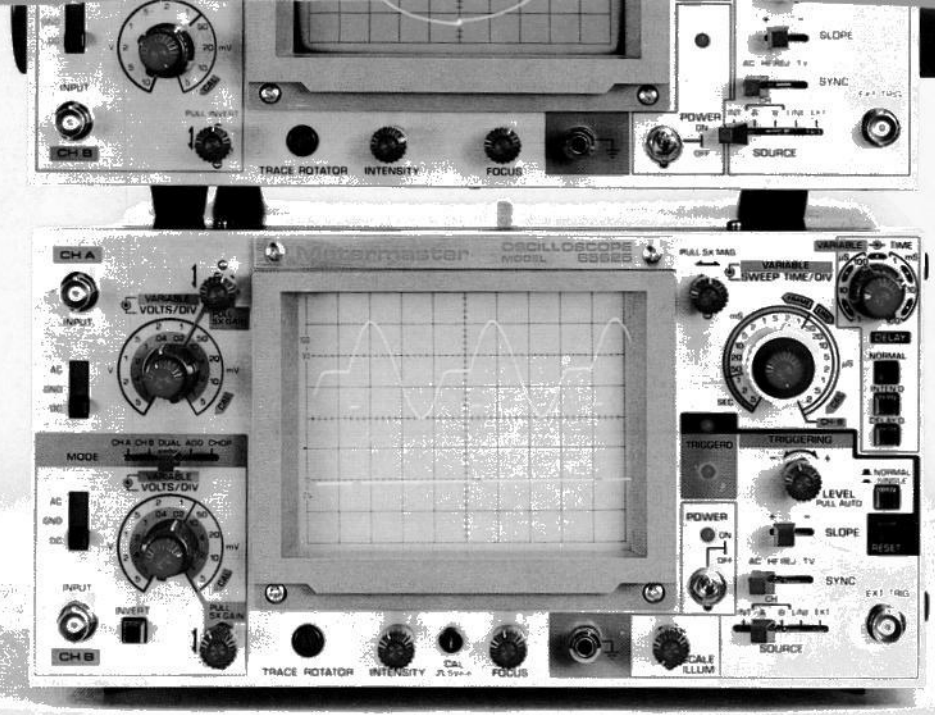
C. J. Ramey

This circuit offers a very efficient way of driving a pair of transistors in Darlington configuration from CMOS. The circuit at right shows how two loads of up to 1A may be driven from a single 14007 chip with no external resistors. Using a 2N3055 in place of the 2N2222A will enable loads of up to 3A to be driven at voltages limited only by the Vceo of the transistors.

The circuit at left shows the internal circuit of one section of the 14007. A high on pin 6 switches the lower CMOS transistor on, holding Q2 off and sinking the leakage current of Q1. A low on pin 6 drives Q1 and switches the lower CMOS transistor off and the upper CMOS transistor on.

The result is fast switch off at low cost and efficient switch on.

A bonus is the inverter between pins 10 and 12. Note: Vcc should be 5-6 V to prevent excessive current being drawn from the CMOS chip.



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Use a TRIPLE-THREAT IC

How a CD4040's 12 flip-flops can be used to make a frequency divider, counter, or meter

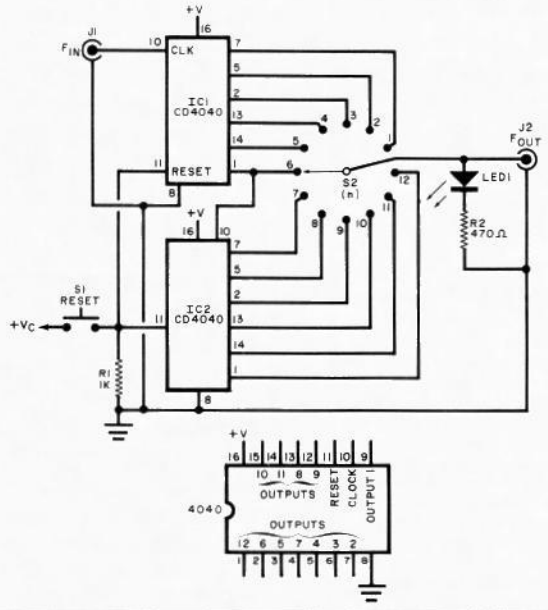
By Sami A. Shakir

A MAJOR advantage in using state-of-the-art semiconductors is that a number of transistors and several conventional ICs often can be replaced by a single IC. A case in point is the CD4040 CMOS 12-stage ripple binary up-counter. This versatile IC can be used to make a low-cost frequency divider, long-term counter or even a simple frequency meter. In this article, we'll discuss how you can go about doing all three inexpensively and with minimum parts count.

Technical Details. All 12 of the CD4040's cascaded flip-flops are capable of being reset to zero by applying a high (+V) at the RESET input. For normal counting however, the RESET input is held low.

If an input signal is applied to the clock input, each stage will divide the frequency of the signal by 2, the last stage dividing the frequency by 2^{12} (4096). Cascading two counters as shown provides 24 stages that each divide by two, for a grand total of 16,777,216 divisions. In general, stage *n* will divide the input by 2^n, where *n* is the stage number.

Maximum input frequency to the circuit depends upon supply voltage. For example, with 5-, 10-, and 12-volt supplies, maximum input signals are about 4, 10, and 12 MHz, respectively. Since the 4040 is a CMOS device, it has the advantage of low power consumption, wide 1-to-15-volt power supply range and high noise immunity.



PARTS LIST

IC1,IC2—CD4040 12-stage counter
LED1—Any light-emitting diode
J1,J2—Miniature open-circuit phone jack
R1—1-kilohm, ¼-W resistor
R2—470-ohm, ¼-W resistor
S1—Spst normally open pushbutton switch (Radio Shack 275-1547)
S2—Single-pole, 12-position (or 24-position) nonshorting rotary switch (Radio Shack 275-1385 or similar)

Possible Applications. The circuit shown here can be used as a frequency divider, timer, and simple form of frequency meter as follows:

Frequency Divider. Twelve-position switch *S2* permits a selection of every other counting stage. In this configuration, each position permits division by 4 of the input frequency. Thus, for any selected position of *S2*, the circuit will divide the input frequency by 4^n, where *n* is the number of the switch position selected. Of course, a 24-pole switch can be substituted to obtain *every* divide-by capability of the two-chip circuit. In the frequency-divider mode, any signal within the maximum range of the IC can be divided down as desired. One possible application of the frequency-divider mode is to allow an r-f generator to cover the audio range. If an accurate oscillator is used as the input, you will end up with a precision audio source.

Timer. If the power line-frequency of 60 (or 50) Hz is used as the input signal, the circuit can be used as a timer that can be reset using *S1*. A 60-Hz input has a period of 0.016667 second (16.667 ms), which means the first stage will change state every 0.01667 second, the second stage will double this time, and so on to the last stage, which changes state every 139,809.57 seconds (1.618 days). Since the selected

position of *S2* will be high after 4^n (0.01667) seconds, *LED1* will turn on to indicate that the output is high. This high can then be used to control other circuits, the only precaution here being that the input voltage of the circuit being controlled must be about equal to the supply voltage for the timer circuit.

Frequency Meter. This mode is just the reverse of the timer mode, because here the input frequency is not known. If we assume the period of the input signal is T, the first stage will change state every $2 \times T$ seconds and, hence, will come back to its state after $4 \times T$ seconds. Therefore, any position of *S2* will yield a period of $4^n \times T$ (*n* being the switch selected). The output is monitored by *LED1*. Hence a period is measured from the time the LED turns off until it turns on again. If you use a stop watch or wristwatch to measure the period, you can calculate the unknown frequency from $f = 4^n/T$, where T is the time measured, for position *n*, to turn off *LED1* and then turn it on again.

Frequency measurement accuracy depends upon time-measurement accuracy. Consequently, accuracy is greater for large values of T since the percentage error due to human reflexes in the measuring process decreases. You should choose the highest possible position for *S2* for greatest accuracy. However, to avoid making the measurement process a lengthy one, an optimum choice for *S2* is the position in which an extinguish/turn-on period is a few seconds. (Note: If the input signal level is low, a suitable amplifier should be used to increase it to where it will reliably drive the circuit.)

Construction. Since the circuit has so few components, perforated-board construction can be conveniently used. Selector switch *S2*'s positions can be numbered from 0 to 11 (or 0-23 if you substitute a 24-position switch as described above). Any LED with the appropriate current-limiting resistor (*R1*) can be used to monitor the output. The board can be installed in almost any metallic or plastic box. Finally, any 3-to-15-volt source can be used to supply power to the circuit. ◇

Into Linear ICs

part 8

To sleep, perchance to dream; Ay, there's the transistor (just under your shoe). The final hour upon the stage for Into Linear IC's, by Ian Sinclair.

ONE TYPE OF IC we haven't mentioned so far, mainly because it's used so much more for digital circuits than for linear types, is the CMOS IC. The letters CMOS mean Complementary Metal Oxide Silicon; the complementary part of the title means that some of the silicon is P-type and other parts N-type, and the metal-oxide part of the name indicates that the currents through the silicon are controlled by the voltage of bits of metal which are separated from the silicon by the insulator silicon oxide. A CMOS IC is an IC made from field-effect transistors, rather than the familiar junction (or bipolar) transistors, and for some purposes these ICs can provide features which can't be equalled by the more common types of bipolar ICs.

Two features of CMOS ICs are valuable in linear circuits. One is the very high input resistance which can be obtained, and the other is the use of these circuits as resistors which change value as the voltage bias changes. Before we look at some practical circuits, though, a warning is needed. Because of the very high input resistance, a CMOS input cannot discharge the voltages caused by electrostatic charging. Your body can be charged to several thousand volts by simply walking over a dry nylon carpet, and such a voltage applied across two pins of a CMOS IC from your fingers will destroy the IC completely. A bipolar IC such as the 741 is unaffected because its input resistance is low enough to discharge the voltage harmlessly. CMOS ICs should be kept in the holders in which they are supplied, and connected into the circuit only after all the other components are in place. Many constructors prefer always to use CMOS ICs in holders rather than soldering into place. Certainly if these ICs are soldered in, a grounded iron must be used, and the other components must be connected in place first. When several CMOS devices are on one IC, then no inputs must ever be left unconnected. In the diagrams which follow, the unused inputs are grounded by wire links which must be in place before the IC is plugged in, and which must not be removed while the CMOS IC is in place. Similarly, the IC must never be plugged in or out while the supply voltage is switched on, and the pins of the IC must never be touched; you soon develop the habit of holding the body of the IC and transferring it from its wrapping to the board or back again without letting the pins come into contact with anything else.

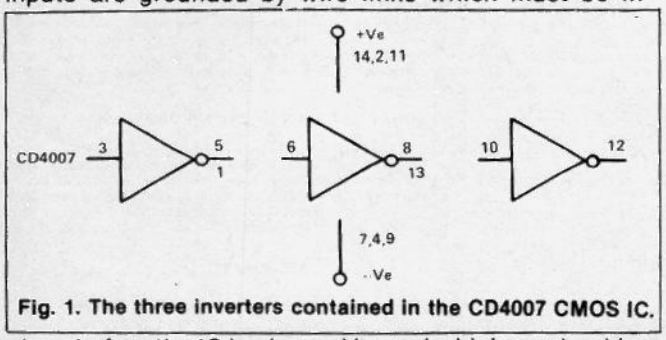


Fig. 1. The three inverters contained in the CD4007 CMOS IC.

The CD4007 is a versatile circuit which consists of three pairs of complementary MOSFETs inside one package, with enough separate connections to allow the unit to be used for a variety of purposes. The most useful connection for linear circuits is as three separate inverters, as shown in Fig. 1. These can each be used as common-drain amplifiers, as shown in Fig. 2 making use of the very high input resistance and the fact that no bias is needed.

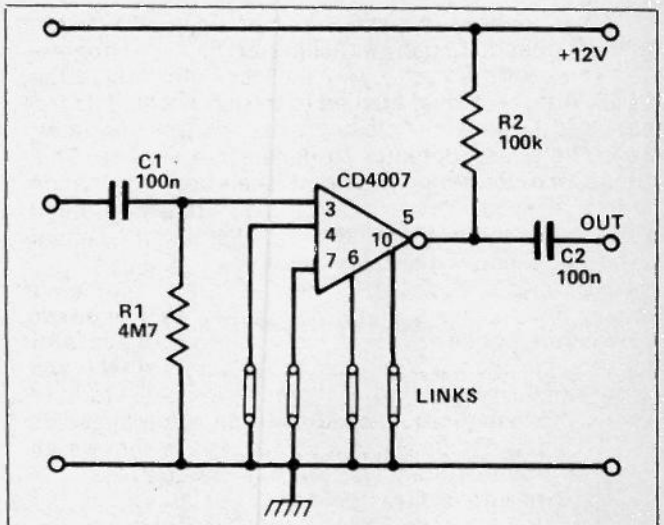


Fig. 2. Using one section of the CD4007 as an inverting amplifier.

Phase-Locked Loops

The phase-locked loop is a type of IC which is rather more specialised than the ones we've looked at earlier in this series, but it's a circuit which is nowadays used to such an extent that we can't ignore it. The block diagram of a phase-locked loop (PLL) is shown in Fig. 3; it consists of an oscillator whose frequency can be controlled by a steady (DC) voltage, along with a phase comparator (or phase-sensitive detector). The phase comparator does pretty well what its name suggests — it compares the phase of two signals and gives an output whose amplitude and sign depends on the phase difference. Let's make that a bit clearer. Suppose we have two inputs A and B to a phase-sensitive detector, and we have sine-wave signals of the same frequency at each input. We can arrange the detector so that if the phase of the signal at A is earlier than the phase of the signal at B, the output of the detector is a positive DC voltage whose size depends on the amount of the phase difference, perhaps 200 mV for every 20° of phase difference.

Removing the constraints of C-MOS bilateral switches

by W. Chomik and A. J. Cousin
Department of Electrical Engineering, University of Toronto, Canada

Two major limitations imposed on the popular complementary-metal-oxide-semiconductor 4016 switch may be overcome with this circuit. As well as allowing the signal magnitude to exceed the power-supply voltage, it enables unipolar control signals to switch bipolar input signals. Only a second switch and an inverter need be added to a standard circuit to remove these operating constraints on the signal-handling gate.

Usually, the signal voltage to be passed through a single switch must be limited to between $V_{DD}+0.7$ volt and $V_{SS}-0.7$ v, where V_{DD} is the positive supply (drain) voltage and V_{SS} is the minus supply (source) voltage. Otherwise, the signal voltage will cause the forward biasing of the diode between the substrate and channel of one MOS field-effect transistor, and the gate may be destroyed.

This problem might arise if the power-supply value applied to some active element in a circuit happened to lie outside the voltage range that could be applied to the switch ($V_{DD}-V_{SS}$), dictating that the gate must be protected from input and control signals that saturate to the supply level.

Furthermore, many circuits, especially those containing operational amplifiers, use bipolar supplies. The resulting signals to be processed are likely to be bipolar as well. Yet the channel-voltage constraints inherent in the design of the 4016 (that is, the fact that the logic 0 control voltage, V_{SS}, must be at or below the most negative signal voltage, and the logic 1 control voltage, V_{DD}, must be at or above the most positive signal voltage) means that bipolar supplies and control signals must also be applied to the switch if these bipolar signals are to be passed. Unfortunately, too, many systems use digital control signals that are unipolar, and so logic-level shifters are needed also, to make this signal symmetrical with respect to ground.

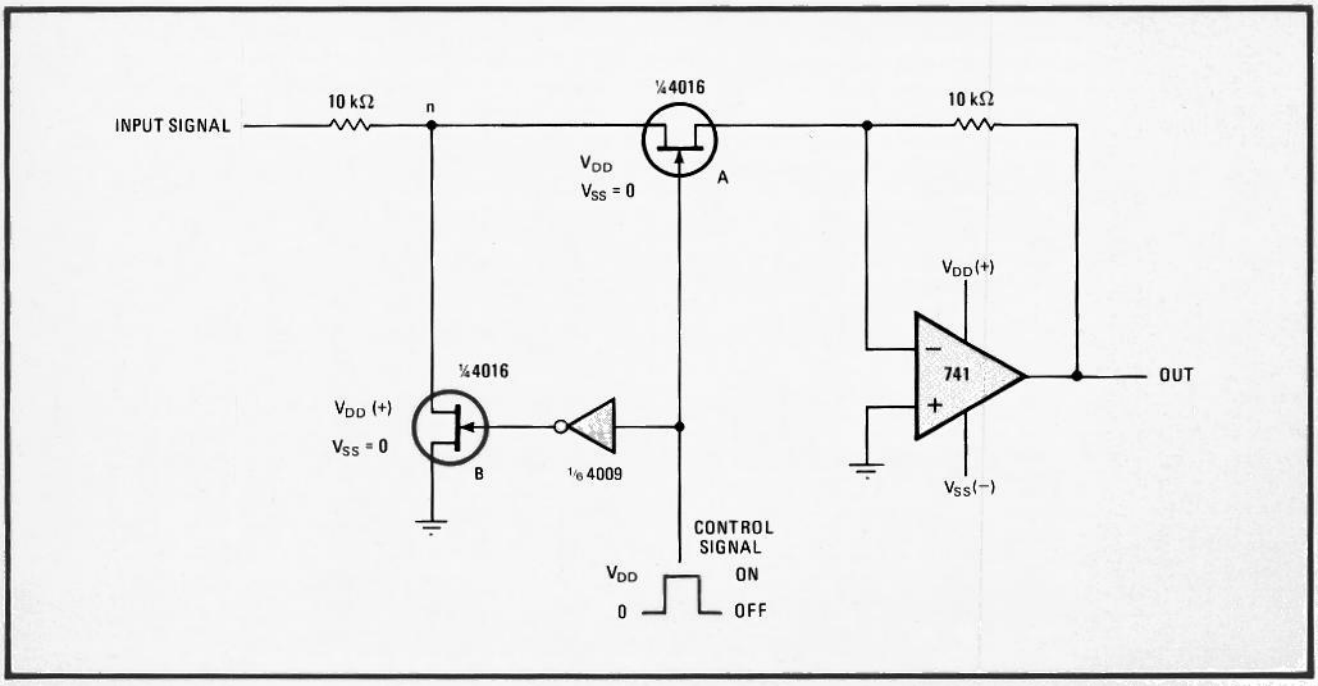
With the addition of a second bilateral switch and an inverter to a standard op-amp circuit, as shown, the signal-handling switch can operate from a single power supply and be driven by unipolar logic at the control input in order to pass bipolar signals. Moreover, the signal can lie outside the $V_{DD}-V_{SS}$ limit of the switches.

The channel voltage of both switches is set by fixing their drain potentials at the virtual ground of the op amp or to circuit ground, depending on which switch is on. Because the virtual ground never strays from true ground by more than a few millivolts, the switches will be protected from burn out, as their channel-voltage limit will never be exceeded.

When switch A is on and switch B is off, node n will be essentially at ground potential. When B is on and A is off, the signal is removed from the op amp's input, but node n will still be at ground (through B), and the same channel-voltage conditions will prevail.

Note that the actual input voltage to the gate at node n will never drop more than a few millivolts below the minimum control voltage, even if the input signal is negative. Thus, the gate's channel-voltage constraint is always met. □

No limitations. Inverter and gate B enable switching of bipolar input signals by unipolar control signals at gate A and also allow magnitude of input to exceed gate's supply voltage. Node n is held near to ground at all times, so that channel-voltage limit of gate is never exceeded. Magnitude of signal at node n never exceeds control-signal potential, enabling gate to switch properly.



THE VERSATILE 4007

Need a versatile CMOS building block for a one-of-a-kind application? Then the 4007 is for you. Find out how to use it here.

RAY MARSTON

THE 4007 IS THE SIMPLEST IC IN THE CMOS line. It contains just two pairs of complementary MOSFET's and a CMOS inverter. However, each element is independently accessible, so the elements can be combined in a great variety of ways. In fact, the 4007 is sometimes known as the "design-it-yourself" CMOS IC, as it can function as a digital inverter, a NAND or a NOR gate, or an analog switch. It can also function as a linear device.

Therefore, not only is the 4007 the simplest CMOS IC, but it is also the most versatile. And that makes it an ideal device for demonstrating the principles by which CMOS devices operate to students, technicians, and engineers. In this article we'll examine the 4007 from both theoretical and practical points of view, and we'll include many circuits that you can use as-is in your next design.

Basic digital operation

The guts of the 4007 are shown in Fig. 1. All MOSFET's in the 4007 are enhancement-mode devices; Q1, Q3, and Q5 are p-channel, and Q2, Q4, and Q6 are n-channel types. The drains and sources of MOSFET's Q1–Q4 are independent; the drain of Q6 is connected to the drain of Q5, so those two MOSFET's compose the inverter mentioned above. Each pair of transistors is protected by a network like the one shown in Fig. 2.

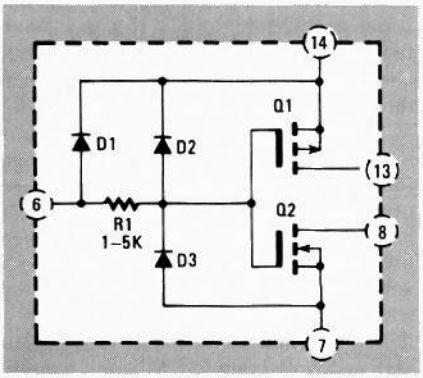


FIG. 2—INPUT PROTECTION CIRCUITRY R1,D1–D3) of each pair of MOSFET's is shown here.

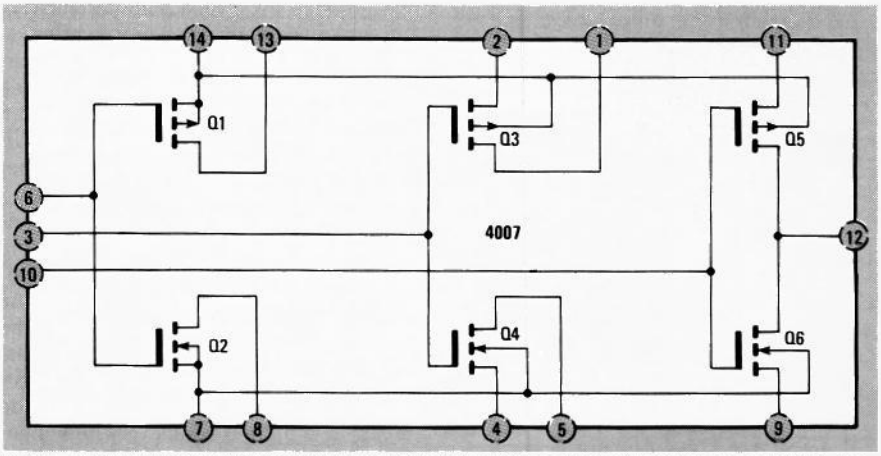


FIG. 1—THE 4007 IS COMPOSED OF three pairs of complementary enhancement-mode MOSFET's.

As you recall, the term *CMOS* is an acronym for *C*omplementary *M*etal *O*xide *S*emiconductor; it is fair to say that most CMOS IC's are designed around CMOS devices like those that compose the 4007. Therefore it is worthwhile to get a good understanding of how those elements work. Let's look first at their digital characteristics; later we'll examine them in light of their analog capabilities.

The two fundamental characteristics of a MOSFET are as follows. First, the gate, or input terminal, of a MOSFET has a near-infinite impedance. Second, the magnitude of the voltage applied to the gate controls the magnitude of drain-to-source current flow.

In an enhancement-mode *n*-channel MOSFET the drain-to-source circuit is a high impedance when the gate is at the same potential as the source. However, that impedance decreases as the potential applied to the gate becomes positive with respect to the source. So an n-channel MOSFET can be used as a digital inverter by wiring it as shown in Fig. 3-*a*. With a low applied to its input the MOSFET is cut off, so the output goes high. With a high applied to its input the MOSFET saturates, so the output goes low.

In a *p*-channel enhancement-mode MOSFET the drain-to-source circuit is also a high impedance when the gate is at the same potential as the source. But, unlike the n-channel device, that impedance decreases as the potential applied to the gate becomes *negative* with respect to the source. So a p-channel MOSFET can be used as a digital inverter by wiring it as shown in Fig. 3-*b*.

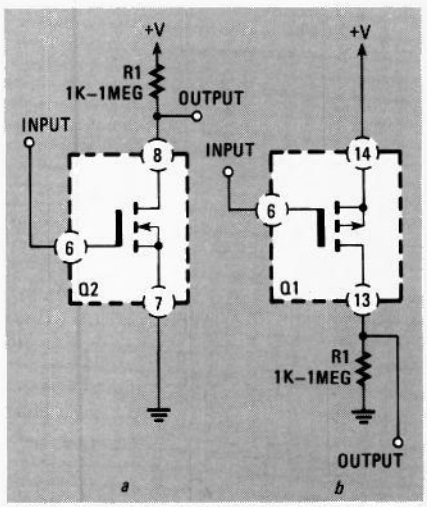


FIG. 3—A DIGITAL INVERTER can be built from either an n-(*a*) or a p-channel MOSFET (*b*).

In both n- and p-channel inverters, the amount of current that flows through the device is limited by the value of R1. And both circuits draw a finite quiescent current in the on state. However, quiescent current drain can be reduced to almost zero by connecting a pair of complementary MOSFET's as shown in Fig. 4.

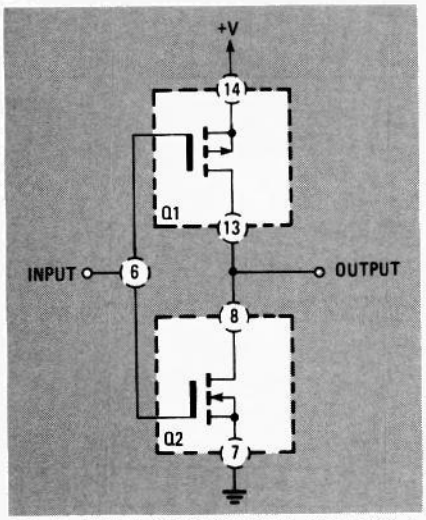


FIG. 4—THE STANDARD CMOS INVERTER is built from two stacked MOSFET's.

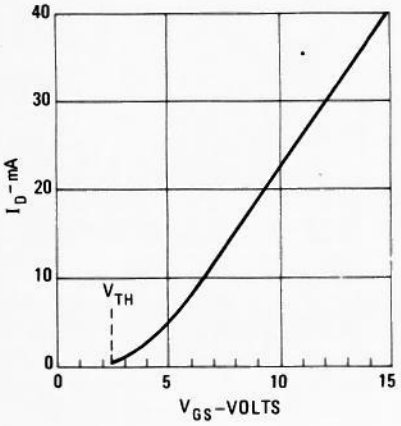


FIG. 5—THE N-CHANNEL MOSFET conducts almost no current until V_{GS} exceeds about 2 volts.

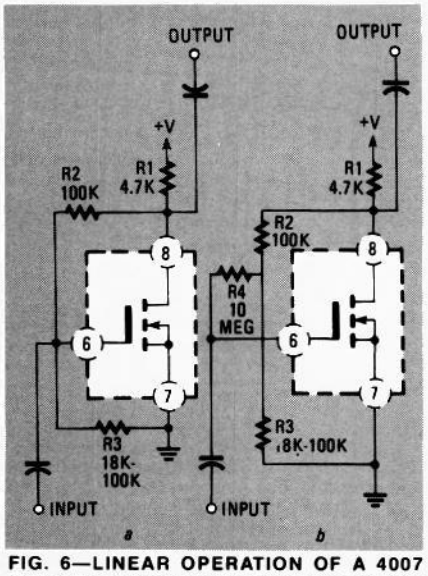


FIG. 6—LINEAR OPERATION OF A 4007 MOSFET requires simple biasing (*a*); very high input impedance is achieved by the addition of R4 (*b*).

In that configuration, which is standard for many CMOS inverters and buffers, with a low applied to the input, Q1 is on, so the output is high. However, Q2 is off, so no quiescent current can flow. With a high applied to the input, Q2 is on, so the output is low. In that case Q1 is off, so quiescent current flow is still nil. Of course, there is no requirement that the MOSFET's be operated solely in the digital mode; let's find out how they can be used otherwise.

Basic linear operation

To understand the operation of CMOS circuitry, it is essential to understand the linear characteristics of the basic MOSFET. Figure 5 shows the typical gate-voltage (V_{GS}) to drain-current (I_D) curve of an n-channel enhancement-mode MOSFET. Note that negligible drain current flows until the gate votage rises to a threshold value, V_{TH}, of about 1.5 to 2.5 volts. After that point, however, drain current increases almost linearly with further increases in gate voltage.

Figure 6-*a* shows how to connect an n-channel MOSFET as a linear inverting amplifier. Resistor R1 is the drain load, and R2 and R3 bias the gate so that the device operates in the linear range. The value of R3 must be selected to give the desired quiescent drain current; it normally ranges from 18–100K. To provide the linear amplifier with a very high input impedance, wire a 10-megohm resistor (R4) as shown in Fig. 6-*b*.

Figure 7 shows typical VI characteristics of an n-channel MOSFET at various fixed values of V_{GS}. To understand that graph, imagine that, for each curve, V_{GS} is fixed at V_{DD}, but that V_{DS} can be varied by altering the value of the drain-load resistor. The graph can then be divided into two characteristic regions, as indicated by the dotted line: the ohmic region and the pinch-off region.

For each curve shown in Fig. 7, the beginning of the pinch-off region—the point where the dashed line crosses the solid line—is called the pinch-off voltage, or V_P, which is the value of V_{DS} above which I_D increases little, if at all, for further increases in V_{DS}.

When the MOSFET is in the pinch-off region and V_{DS} is more than 50% of V_{GS}, the drain functions as a constant-current source. The amount of current that flows is controlled by V_{GS}. A low value of V_{GS} gives a low current flow, and a high value of V_{GS} gives a high current flow. Those saturated constant-current characteristics protect CMOS devices from short-circuit failure and also determine operating speed at various supply voltages. Both current-drive and operating speed increase in proportion to the supply voltage.

When the MOSFET is in the ohmic region and V_{DS} is less than 50% of V_{GS}, the drain functions as a voltage-controlled resistance. That resistance increases approximately as the square of V_{GS}.

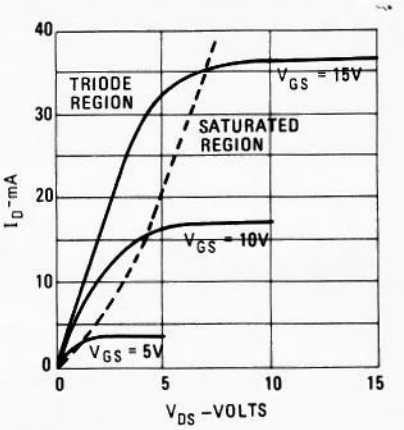


FIG. 7—AN N-CHANNEL MOSFET operates linearly in the ohmic region above the dashed line and digitally in the pinch-off region below the dashed line.

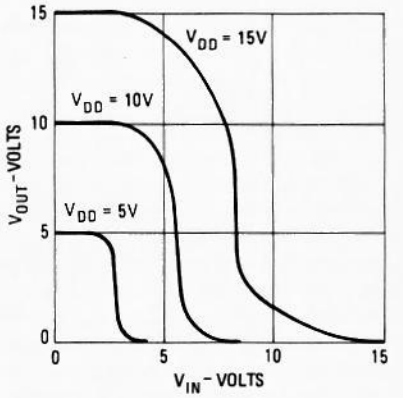


FIG. 8—VOLTAGE-TRANSFER characteristic of the CMOS inverter (Fig. 4) reveals that, for inputs near ground and V_{DD}, output changes very little.

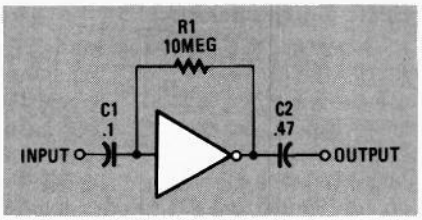


FIG. 9—LINEAR OPERATION of the inverter (Fig. 4) is possible, as shown here.

Figure 8 shows typical voltage-transfer characteristics of the standard CMOS inverter at different supply voltages. Note that when V_{DD} is 15 volts, the output voltage changes a very small amount when the input voltage is near either zero or V_{DD}. However, when the input voltage is biased at roughly $V_{DD}/2$, a small change in input voltage produces a large change in output voltage. Typically, the inverter has a voltage gain of about 30 db when used with a 15-volt supply, and 40 db at 5 volts. Figure 9 shows how to connect the CMOS inverter for use as a linear amplifier; the circuit has a bandwidth of 710 kHz at 5 volts, and 2.5 Mhz at 15 volts.

We can wire three simple CMOS inverters (like the one shown in Fig. 4) in series

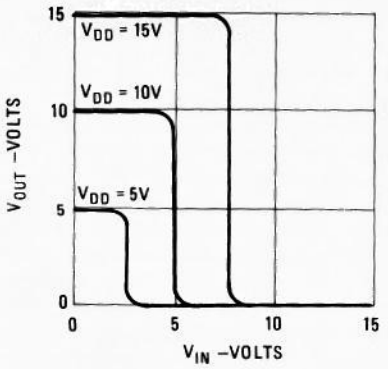


FIG. 10—VOLTAGE-TRANSFER characteristic of a B-series CMOS inverter is similar to that of the simple inverter.

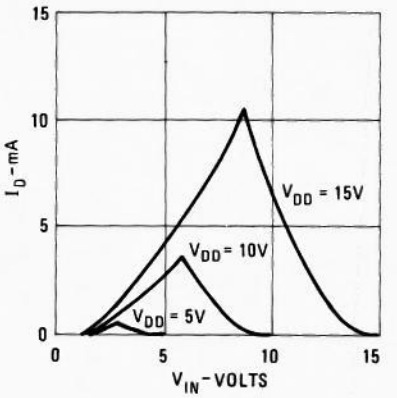


FIG. 11—DRAIN CURRENT of the simple inverter peaks at an input voltage just over $V_{DD}/2$.

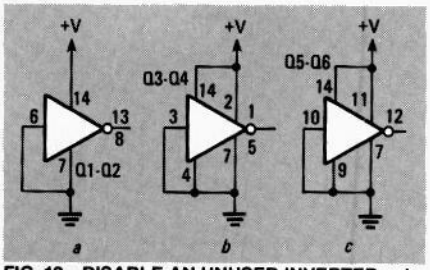


FIG. 12—DISABLE AN UNUSED INVERTER pair as shown here; Q1 and Q2 are disabled as in *a*; Q3 and Q4 as in *b*; Q5 and Q6 as in *c*.

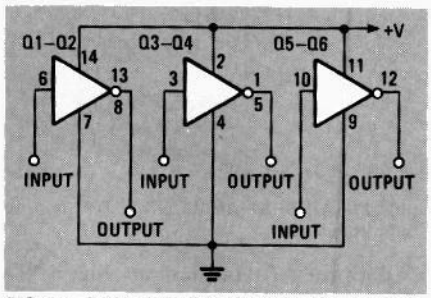


FIG. 13—EACH PAIR OF TRANSISTORS may be used independently as an inverter.

to obtain the direct equivalent of a modern "buffered" B-series inverter, which has the overall voltage transfer curve shown in Fig. 10. A B-series inverter typically gives about 70 db of linear voltage gain, but it tends to be quite unstable when used in the linear mode.

To finish up our discussion of basic operation, take a look at Fig. 11. Shown there is the drain-current transfer characteristics of the simple (non-buffered) CMOS inverter. Note that drain current is zero when input voltage is zero or V_{DD}. However, in the middle range, current rises to a maximum value when the input is at approximately $V_{DD}/2$, at which point both MOSFET's are on. That on current can be reduced by wiring resistors in series with the source of each MOSFET. We'll use that technique in the "micropower" circuits discussed below.

Basic rules

There are a few basic rules to follow in order to use the 4007 successfully. First, you must ensure that all unused elements of the devices are disabled. A pair of MOSFET's can be disabled by connecting them as an inverter and grounding their inputs. As shown in Fig. 12-*a*, to disable the Q1-Q2 pair, just ground pin 6. To disable the other pairs, in addition to grounding the inputs, the sources and drains must be connected to ground and +V as shown in Fig. 12-*b* and Fig. 12-*c*.

In use, the input terminals must not be allowed to rise above V_{DD} (the supply voltage) or below ground. To use an n-channel MOSFET, the source must be tied to ground, either directly or through a current-limiting resistor. To use a p-channel MOSFET, the source must be tied to V_{DD}, either directly or through a current-limiting resistor.

Digital circuits

A single 4007 can be configured as three independent inverters, as shown in Fig. 13. In that figure, and in others that follow, we won't necessarily show all details of how to wire the circuit under discussion. Also, multiple pin connections that terminate in a single function will be shown as in Fig. 13. For example, the output of the Q1-Q2 inverter in that figure is obtained by connecting pins 13 and 8 together.

Figure 14 shows how to connect the 4007 as one inverting and one non-inverting buffer. In the non-inverting circuit, the Q1-Q2 and Q3-Q4 inverters are simply wired in series to provide two stages of inversion—which provides a non-inverting buffer.

The maximum source (load-driving) and sink (load-absorbing) currents of a simple CMOS inverter are about 10—20 mA when either output MOSFET is fully on. To increase that sink current, several n-channel MOSFET's can be connected in parallel in the output stage. Figure 15 shows how to configure the 4007 as a high sink-current inverter. Similarly, Fig. 16 shows how to configure the IC as a high

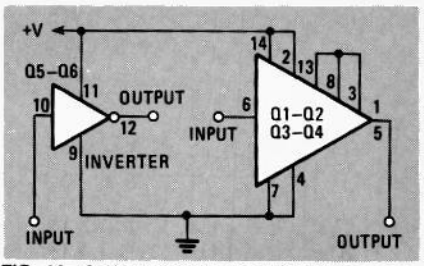


FIG. 14—A NON-INVERTING BUFFER is composed of two inverters connected in series (Q1–Q4). The other inverter (Q5 and Q6) can be used independently.

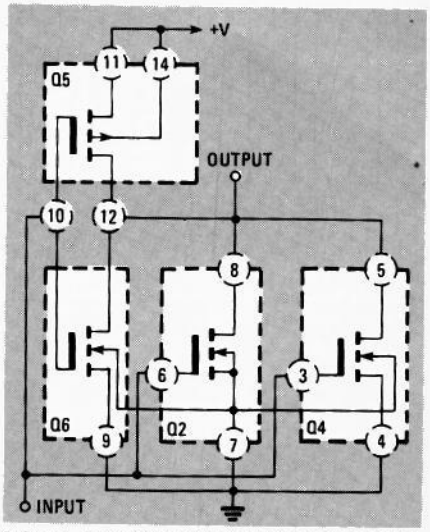


FIG. 15—SINK CURRENT may be increased by connecting the n-channel MOSFET's in parallel.

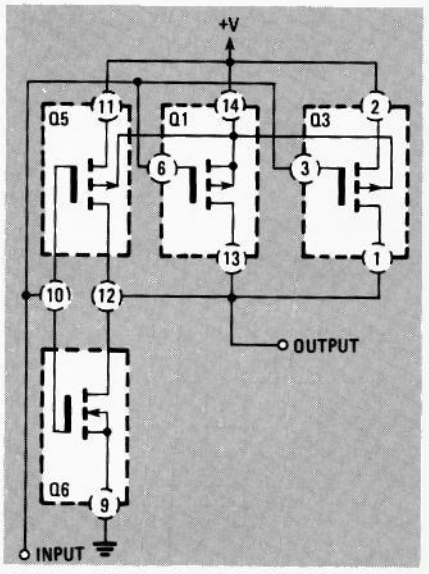


FIG. 16—SOURCE CURRENT MAY BE INCREASED by connecting the p-channel MOSFET's in parallel.

source-current inverter. Last, Fig. 17 shows how to connect all the elements of a 4007 in parallel to produce a single inverter that will both sink and source three times the current of a standard inverter.

Logic circuits

The 4007 is well-suited for demonstrating the basic principles of CMOS logic

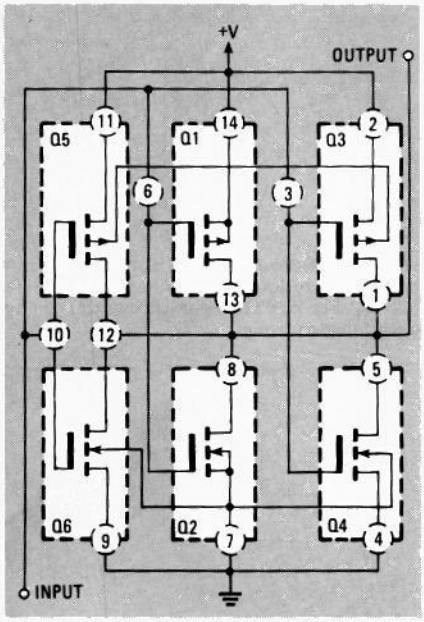


FIG. 17—BOTH SINK AND SOURCE CURRENT may be increased by connecting all transistors of each type in parallel.

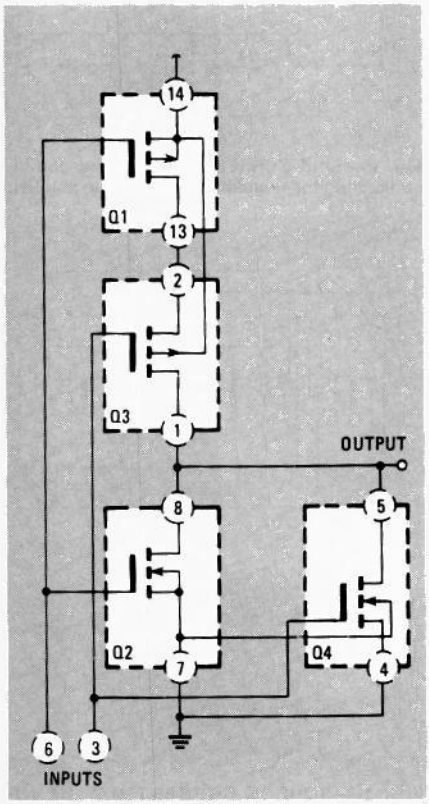


FIG. 18—A TWO-INPUT NOR GATE can be built from a 4007.

gates. Figure 18 shows how to configure the 4007 as a 2-input NOR gate. In that circuit two n-channel MOSFET's are wired in parallel so that either can pull the output to ground with a high input. Also, two p-channel MOSFET's are wired in series so that, with low inputs, both must turn on to pull the output high. Figure 19 shows how to wire up a 3-input NOR gate; it is composed of three series- and three parallel-connected MOSFET's, and its principle of operation is the same as the 2-input circuit. Figure 20 shows how to configure the 4007 as a 2-input NAND gate. When both inputs are high, Q2 and Q4 both turn on, so the output goes low. Otherwise Q1 or Q3 pull the output high.

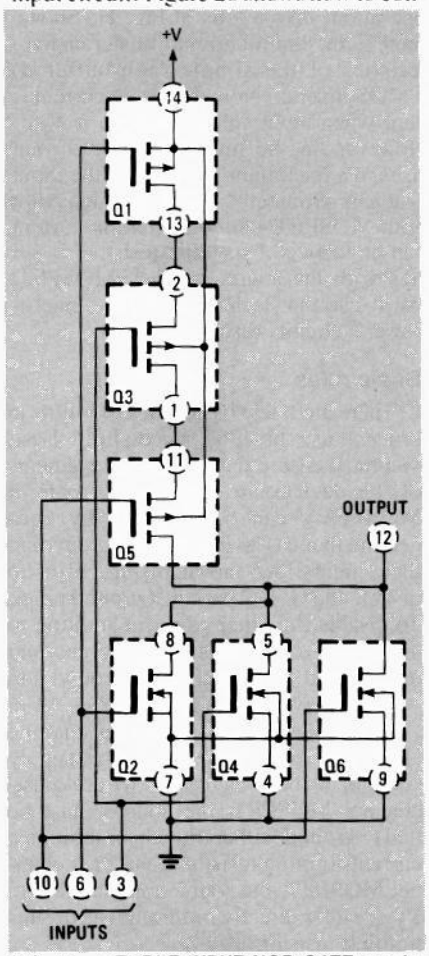


FIG. 19—A THREE-INPUT NOR GATE can be built from a 4007.

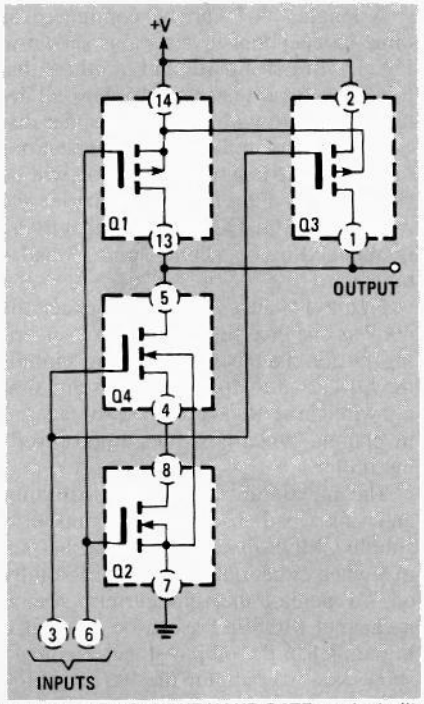


FIG. 20—A TWO-INPUT NAND GATE can be built from a 4007.

An important element of many digital circuits is called an analog switch. It is an electronically-controlled SPST, SPDT, or other switch. The principle of the SPST type is shown in Fig. 21-*a*. When the CONTROL input is high, signals can flow between points X and Y unimpeded. When that input is low, no signal can flow.

The 4007 analog switch has a near-infinite off resistance and an on resistance of about 600 ohms. It can handle signals between zero volts and the positive supply voltage. And since the gate is bilateral, terminals X and Y can function as either input or output.

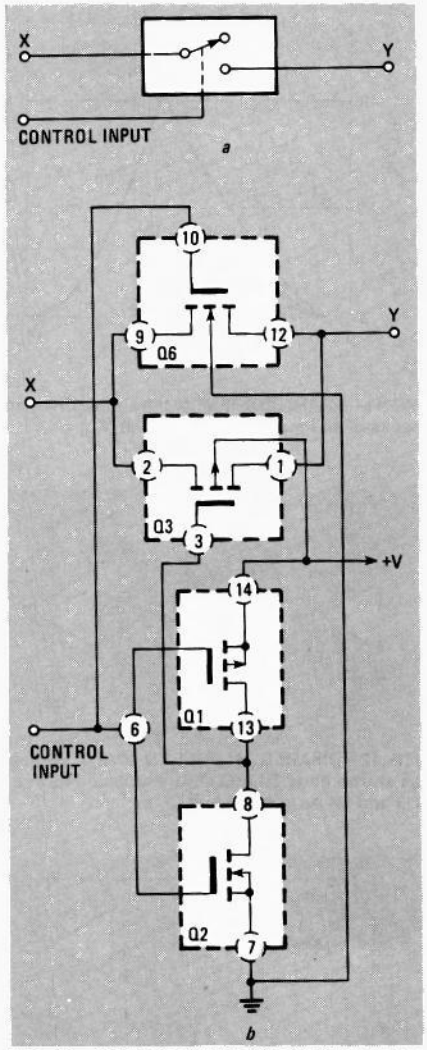


FIG. 21—AN SPST ANALOG SWITCH can be built from a 4007.

Circuitry to implement the SPST switch is shown in Fig. 21-*b*. An n-channel and a p-channel MOSFET are wired in parallel (source-to-source and drain-to-drain), but their gate signals are applied out of phase by means of the Q1-Q2 inverter. To turn the Q3-Q6 pair of transistors on, Q6's gate must be high, and Q3's gate

low; to turn the switch off, the opposite conditions must be present.

An SPDT analog switch is shown in Fig. 22-*a*; circuitry which accomplishes that function is shown in Fig. 22-*b*. Here two transmission elements are connected in parallel, but their control voltages are applied out of phase, so that one switch opens when the other closes, and vice versa.

We saw earlier that the 4007 can also be used in a linear mode; now let's look at how to do that, and at the sort of performance we can expect from a linearly-operated 4007.

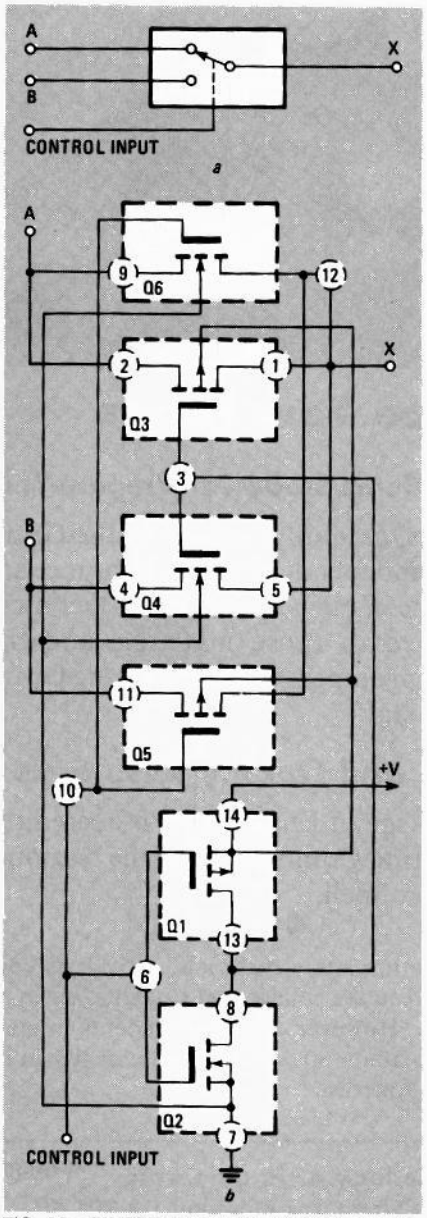


FIG. 22—AN SPDT ANALOG SWITCH can be built from a 4007.

Linear circuits

Figure 23 shows how voltage gain and frequency response vary according to supply voltage. The curves shown in that figure assume that the 4007 is driving a high-impedance (10 megohm), low-capacitance (15 pF) scope probe. The output impedance of the open-loop amplifier typically varies from 3K (at 15 volts) to 5K (at 10 volts) to 22K (at 5 volts). The product of the output impedance and the ouput load capacitance determines the circuit's bandwidth. Increasing either load capacitance or output impedance decreases bandwidth.

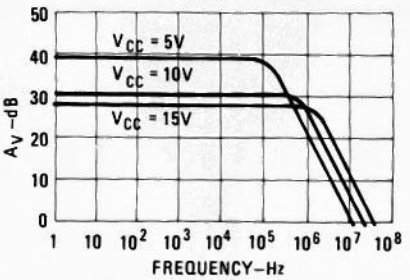


FIG. 23—FREQUENCY RESPONSE and voltage gain of a linear-mode CMOS amplifier is dependent partially on supply voltage.

As you can see in the voltage transfer curve back in Fig. 8, the distortion characteristics of the CMOS linear amplifier are not particularly impressive. Linearity is good for small-amplitude signals, but distortion increases progressively as the output swing approaches the upper and lower limits of the power supply.

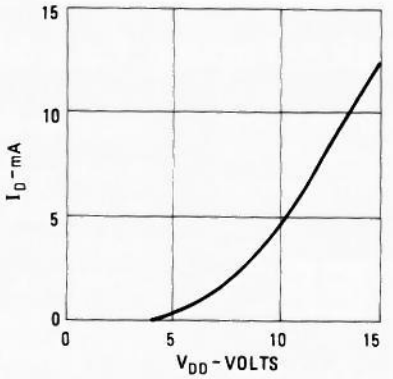


FIG. 24—VERY LITTLE CURRENT FLOWS until V_{DD} exceeds 5 volts.

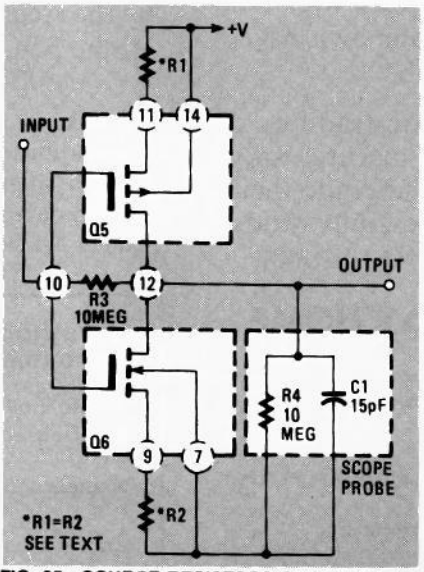


FIG. 25—SOURCE RESISTORS R1 AND R2 decrease current consumption drastically.

TABLE 1—
LINEAR-MODE PERFORMANCE

R1/R2	I_D	A_V	Bandwidth
0	12.5mA	20	2.7 MHz
100Ω	8.2mA	20	1.5 MHz
560Ω	3.9mA	25	300 kHz
1K	2.5mA	30	150 kHz
5.6K	600μA	40	25 kHz
10K	370μA	40	15 kHz
100K	40μA	30	2 kHz
1MEG	4μA	10	1 kHz

Figure 24 shows the typical drain-current versus supply-voltage charcteristic of the basic CMOS linear amplifier. Note that supply current typically varies from 0.5 mA at 5 volts to 12.5 mA at 15 volts.

As we mentioned above, in many applications, the quiescent supply current of a 4007 CMOS amplifier often can be reduced (at the expense of reduced bandwidth) by wiring external resistors in series with the source terminals of the two MOSFET's. In Fig. 25 we show how a micropower circuit would be configured.

It is important to understand that the source resistors increase the output impedance of the amplifier; output impedance is roughly equal to the product of R1 and A_V. That impedance, and the resistance and the capacitance of the load affect the circuit's gain and bandwidth.

Table 1 shows how supply current, voltage gain, and bandwidth vary with the value of those source resistors. As you can see, with 10K source resistors, bandwidth is about 15 kHz. However, by increasing load capacitance to 50 pF, bandwidth decreases to about 4 kHz; by reducing capacitance to 5 pF, bandwidth increases to 45 kHz. Similarly, reducing the resistive load from 10 megohms to 10 kilohms causes voltage gain to fall to unity. The conclusion is that, to obtain significant gain, load resistance must be large relative to the amplifier's output impedance.

An unbiased 4007 inverter has an input capacitance of about 5 pF and an input resistance near infinity. So, if the output of the circuit in Fig. 25 is fed directly to the input of another 4007 stage, the overall voltage gain will be about 30 dB, and the bandwidth will be about 3 kHz. Those values will be obtained when R1 has a value of 1 megohm. For extremely low current drain (.4 μA!), R1 could be increased to 10 megohms.

Now you can see why we said that the 4007 is the most versatile CMOS IC. With the ideas we've presented here, you should have no trouble thinking of many more applications for the 4007. **R-E**

4066B Circuits

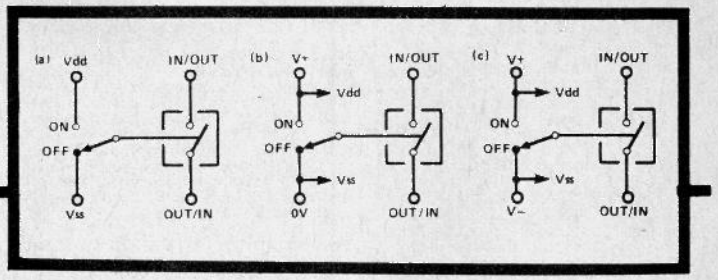


Fig. 2 (a) The basic bilateral switch is turned off by taking the control terminal to V_{SS} and turned on by taking the control to V_{DD}. (b) In digital switching applications, V_{DD} is V+ and V_{SS} is 0V. (c) In analogue switching applications where a split power supply is used, V_{DD} must go to V+ and V_{DD} to V−.

The CMOS family contains many useful ICs, and this month, Ray Marston takes an in-depth look at the 4066B quad bilateral switch.

THE 4066B CMOS IC is described in the manufacturer's literature as a 'quad bilateral switch', a pretty fair description since the device contains four independed electronic switches, each capable of passing signals in either direction and being controlled (turned on or off) by a single high-impedance terminal. The switches have a very high off impedance, an on impedance of about 90R, and can be used to switch both analogue and digital signals. The ICs typically cost a mere 50 cents each, not bad for four independent SPST switches.

Basic 4066B Circuits

Fig. 1 shows the outline and pin notations of the 4066B quad bilateral switch, which can be used with any supply voltage in the range 3 to 18V. Note that, since the switches are of the bilateral type, either switch terminal can be used as the input or output.

Fig. 2a shows the basic way of using the bilateral switch; the switch can be turned off (open circuit) by taking the control terminal to V_{SS} or turned on by taking

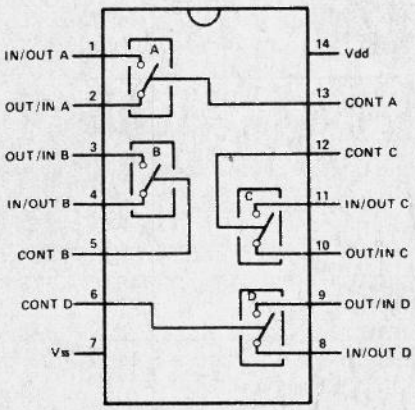


Fig. 1 Outline and pin notations of the 4066B quad bilateral switch.

the control terminal to V_{DD}. In digital switching applications (Fig. 2b) the IC can be used with a single-ended supply, with V_{SS} at 0V and V_{DD} at the desired positive supply. In analogue switching applications (Fig. 2c), a split power supply (either true or effective) must be used, with the positive rail to V_{DD} and the negative to V_{SS}; in this case, of course, the maximum supply limits are restricted to ±9V. Typically, the bilateral switch introduces less than 0.5% of signal distortion when used in the analogue mode.

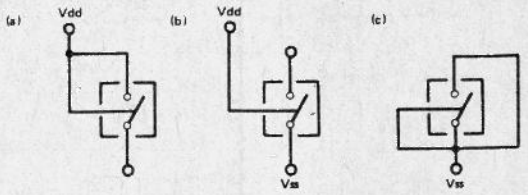


Fig. 3 Unused bilateral switches must be disabled, either by taking the control terminal to V_{DD} and one of the switch terminals to V_{DD} (a) or V_{SS} (b), or by taking all three terminals to V_{SS}.

Certain simple precautions must be observed when using the 4066B. First, the switch signals must in no circumstances be allowed to rise above the V_{DD} voltage or fall below the V_{SS} voltage. Each unused switch in the 4066B package must be disabled (see Fig. 3) either by taking its control terminal to V_{DD} or V_{SS} (as most convenient), or by taking all three terminals to V_{SS}.

Fig. 4 shows how the 4066B can be used to implement the four basic switching functions of SPST, SPDT, DPST and DPDT. Fig. 4a shows the SPST connections, which we have already discussed. The SPDT function is implemented by wiring an inverter stage (a 4001 or 4011, etc) between the IC1a and IC1b control terminals as shown. The DPST switch (Fig. 4c) is simply two SPST switches sharing a common control terminal, and the DPDT switch (Fig. 4d) is two SPDT switches sharing a common inverter stage in the control line.

Note that the basic switching functions of Fig. 4 can be expanded or combined in any desired way by simply adding extra switches/4066B-packages, as appropriate. Thus, a 10-pole double-throw switch can, for example, be made by using five of the Fig. 4d circuits and joining their control inputs together.

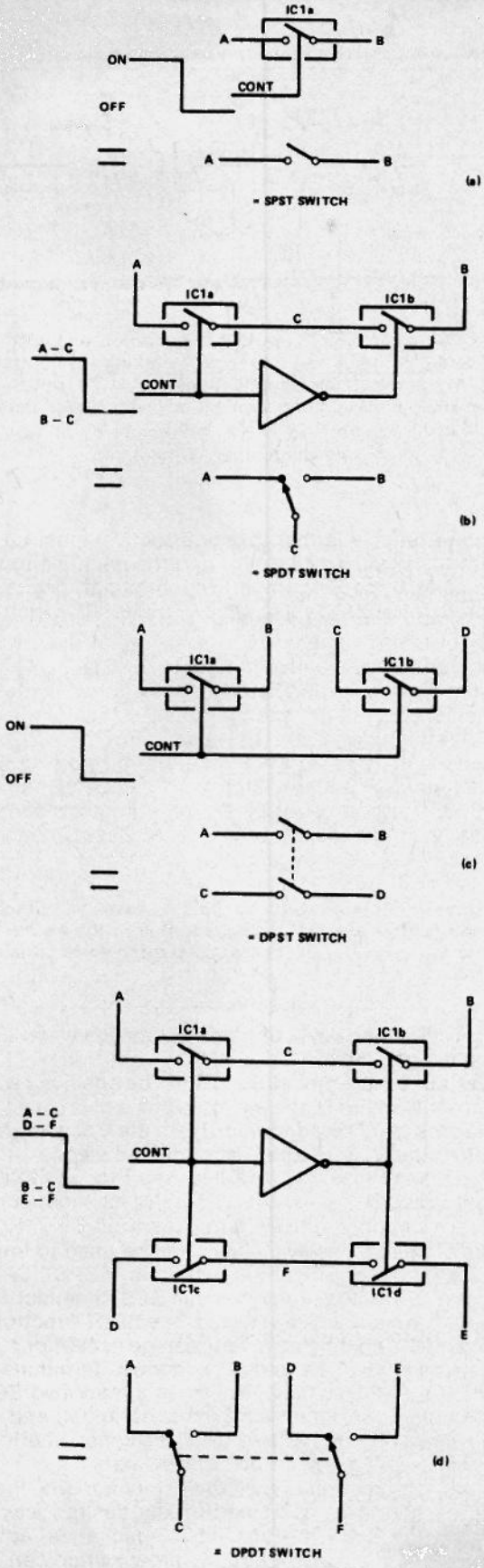


Fig. 4 Using the 4066B to implement the four basic switching functions.

Six Latching Circuits

Fig. 5 shows how a 4066B switch can be used as a simple but very useful push button activated latch; the LED is merely used to indicate the state of the latch and can be replaced with a short circuit if preferred. Circuit operation is easily understood.

Suppose initially that the latch is off (switch open). In this case the output, and hence the control bias applied via R2, will be zero, so the switch will maintain its off state. If PB1 is now momentarily closed the control voltage will go high and turn the switch on, thus driving the output high and maintaining the control drive high (switch on) once PB1 is released. This new state will be maintained until PB2 is closed, at which point the switch will latch into the off state again. R1 is used in the circuit to ensure that a supply short will not occur if both buttons are pressed at the same time; with R1 in the position shown, the switch will turn off if both buttons are pressed at once; if R1 is moved to the low side of PB2, the switch will turn on if both buttons are pressed at once.

The Fig. 5 circuit has a couple of interesting characteristics. First, the control bias resistor can be given any desired value up to practical limits. Fig. 6, for example, shows how the value can be increased to 10M to make a latching touch switch that can be activated by placing a finger across the upper or lower set of touch contacts. R1 and C1 are used to suppress hum signals and ensure positive switching.

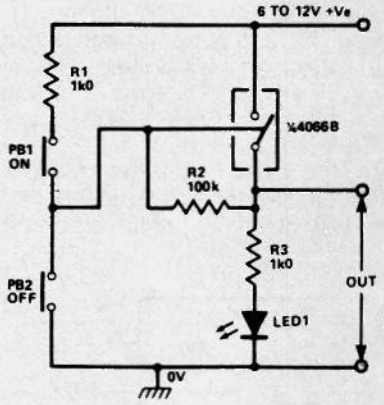


Fig. 5 Push-button latch using the 4066B.

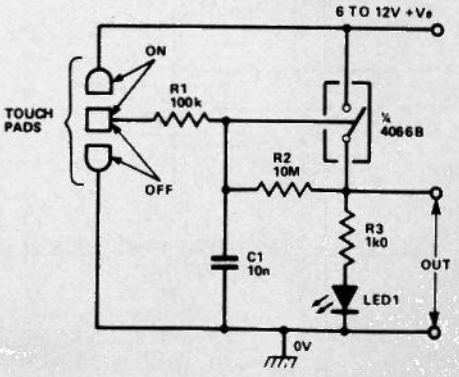


Fig. 6 A latching touch-switch.

Another useful feature is that, since the on resistance of the switch is only 90 R or so, the voltage loss across the switch can be quite low (90 mV at 1 mA): in practice, the on current should be limited to 10 mA maximum. Fig. 7 shows how this low-loss effect can be exploited to make a push-button power switch that can be used to connect or disconnect the power supply to a piece of electronic equipment (amplifier, test gear, etc).

When the switch is off, Q1 is cut off and the circuit consumes a typical standby current of less than 1 uA. When the switch is on, Q1 acts as a voltage follower with its base tied to the positive line via IC1a, so the output voltage is high. The actual voltage drop between the output and the supply is equal to the IC1a drop plus the base-emitter drop of Q1 and typically ranges from 600 to 800 mV. The available output current depends on the gain and current rating of Q1, but currents of a few hundred milliamps are readily available from a single transistor.

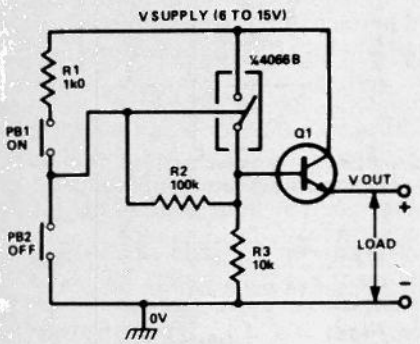


Fig. 7 This push-button activated power switch can be used to replace a conventional slide or toggle switch.

A slightly more efficient version of the push-button power switch is shown in Fig. 8. In this case the load is wired between the collector of Q1 and the positive supply rail. The voltage drop in this circuit is determined only by the saturation characteristics of Q1 and may typically be in the range 200 to 600 mV.

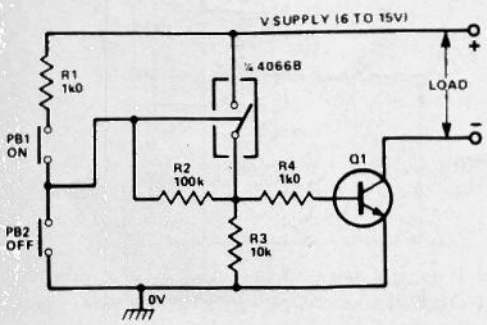


Fig. 8 An alternative version of the push-button power switch.

Fig. 9 shows how the above circuit can be modified for use as a 'close-to-activate' burglar, panic or fire alarm, in which Q1 output feeds directly to a heavy duty 'alarm' relay which, in turn, actuates an external bell or siren. Any number of normally-open sensors/switches can be wired in parallel in the 'PB' positions. The circuit consumes only a microamp or so when in the 'ready' or off mode.

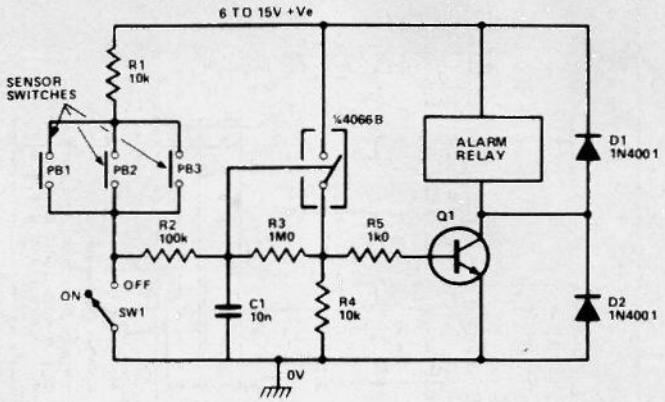


Fig. 9 A close-to-activate burglar/panic/fire alarm.

Finally, Fig. 10 shows how a pair of 4066B switches can be used to make a break-to-activate burglar alarm in which any number of normally-closed sensor switches can be wired in series and which typically consumes a standby current of only 1 uA or so. Here, if any of the switches open, the control terminals of IC1a and IC1b are pulled high by R1 and cause both switches to close; IC1a then shorts out R1, ensuring that the switches will not turn off again when the sensor switches close. Simultaneously IC1b activates the alarm relay via Q1. Note that, once this alarm circuit has been activated, it can only be turned off again by resetting the sensor switches and momentarily breaking the supply connections via SW1.

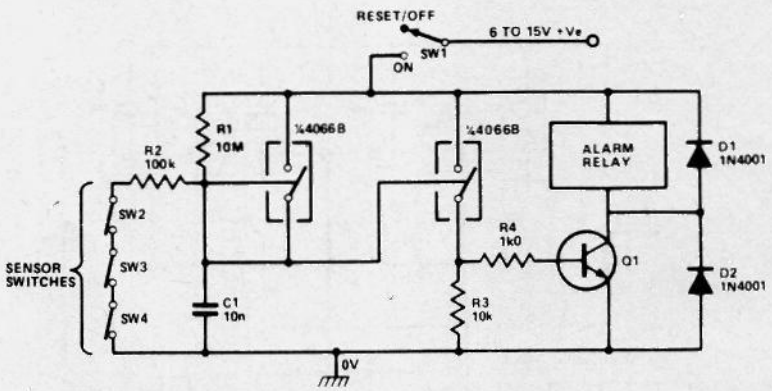
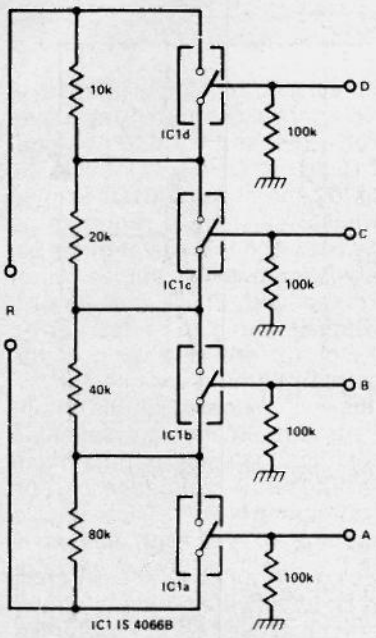


Fig. 10 A break-to-activate burglar alarm.

Digital Control

The 4066B can be used to digitally control or vary resistance, capacitance, impedance, amplifier gain or oscillator frequency in any desired number of discrete steps. Fig. 11 shows how the four switches of a single 4066B can be used to vary the effective value of a resistance in 16 digitally-controlled steps of 10K each.



A	B	C	D	R
0	0	0	0	150k
0	0	0	1	140k
0	0	1	0	130k
0	0	1	1	120k
0	1	0	0	110k
0	1	0	1	100k
0	1	1	0	90k
0	1	1	1	80k
1	0	0	0	70k
1	0	0	1	60k
1	0	1	0	50k
1	0	1	1	40k
1	1	0	0	30k
1	1	0	1	20k
1	1	1	0	10k
1	1	1	1	0

Fig. 11 This circuit gives 16-step digital control of resistance. R can be varied from zero to 150k in steps of 10k.

In practice, of course, the step magnitudes can be given any desired value (determined by the value of the smallest resistor) so long as the four resistors are kept in the ratio 1-2-4-8.

Fig. 12 shows how four switches can be used to make a digitally-controlled capacitor that can be varied in sixteen steps of 1n0 each.

Note that in the Fig. 11 and 12 circuits the resistor/capacitor values can be controlled by operating the 4066B switches manually, or automatically using simple logic networks, microprocessors, up/down counters, and so on.

The circuits of Figs. 11 and 12 can be combined in a variety of ways to make digitally-controlled impedance and filter networks. Fig. 13, for example, shows three different ways of using the circuits to make a digitally-controlled first-order low pass filter.

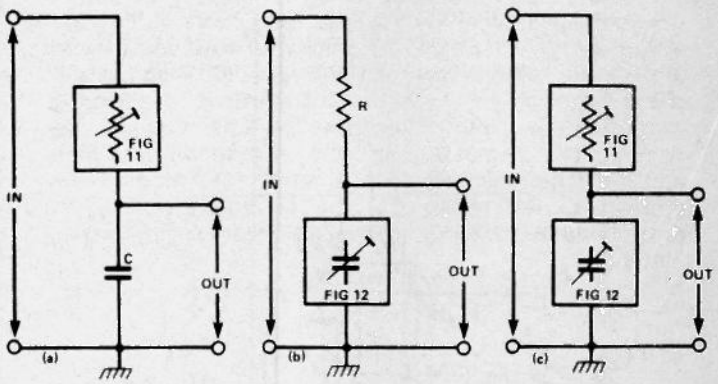
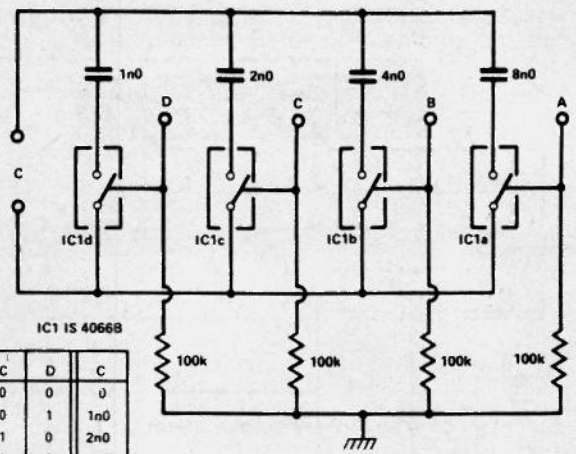


Fig. 13 Three ways of using the circuits of Fig. 11 and Fig. 12 to make a digitally-controlled first-order low pass filter.

Digital control of amplifier gain can be obtained by hooking the 'resistance' circuit of Fig. 11 into the feedback or input path of a standard op-amp inverting circuit, as shown in Figs. 14 and 15. The gain of such a circuit is equal to R_F/R_{IN}, where R_F is the feedback resistance and R_{IN} is the input resistance. Thus, in the Fig. 14 circuit, where the controlled resistance is in the feedback loop, the gain can be varied from zero to unity in 16 discrete steps of 'one fifteenth' each, ie giving a sequence of 0, 1/15, 2/15, 3/15, ..., 14/15, 15/15.



A	B	C	D	C
0	0	0	0	0
0	0	0	1	1n0
0	0	1	0	2n0
0	0	1	1	3n0
0	1	0	0	4n0
0	1	0	1	5n0
0	1	1	0	6n0
0	1	1	1	7n0
1	0	0	0	8n0
1	0	0	1	9n0
1	0	1	0	10n
1	0	1	1	11n
1	1	0	0	12n
1	1	0	1	13n
1	1	1	0	14n
1	1	1	1	15n

Fig. 12 A similar circuit to that of Fig. 11 gives 16-step digital control of capacitance. C can be varied from zero to 15n in steps of 1n0.

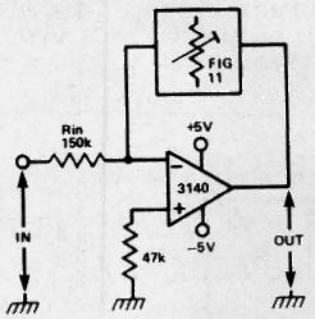


Fig. 14 Digital control of gain using the Fig. 11 circuit. The gain can be varied between zero and unity in 16 steps.

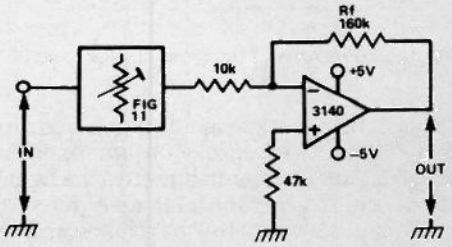


Fig. 15 This application of the Fig. 11 circuit gives digital control of gain between unity and X16 in 16 steps.

In the Fig. 15 circuit, where the controlled resistance is in the input path, the gain can be varied from unity to X16 in 16 steps, giving a gain sequence of 1,2,3,4,5,6. . . . Note that in both of these circuits, the op-amp uses a split power supply so the 4066B control voltage must switch between the negative and positive supply rails.

Fig. 16 shows how the Fig. 11 circuit can be used to digitally control the frequency of an oscillator in 16 discrete steps. In this example the circuit is that of a 555 astable, but the general control principle can be applied equally well to many other types of oscillator circuit.

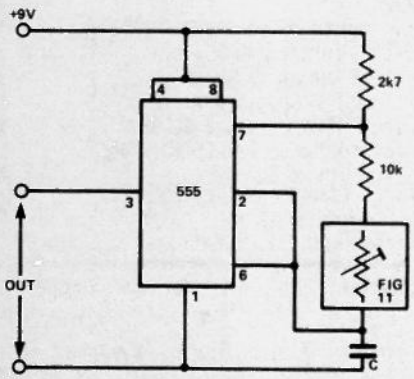


Fig. 16 Digital control of the frequency of a 555 astable. The frequency can be varied in 16 steps.

Fig. 17 shows how a trio of 4066B switches can be used to implement digital control of the decade range selection of 555 astable. Here, only one of the switches must be turned on at any time. Naturally, the circuits of Figs. 16 and 17 can be combined to form a wide-range oscillator that can be digitally controlled by a computer, for example.

Synthesized Multi-Gang Pots

The synthesizing principle is quite simple and is illustrated in Fig. 18, which shows the circuit of a synthesized four-gang 10k-100k rheostat for use at signal frequencies up to about 15 kHz.

Here, the 555 is used to generate a 50 kHz (nominal) rectangular waveform whose mark/space ratio can be varied from 11:1 to 1:11 by RV1, and this waveform is used to control the switching of the 4066B stages. All of the 4066B switches are fed with the same control waveform, and each switch is wired in series with a range resistor (RA, RB, etc), to form one gang of the 'rheostat' between the pairs of terminals, as shown.

Remembering that the switching rate of this circuit is very fast (50 kHz) relative to the rheostat's maximum signal frequency (15 kHz), it can be seen that the mean or effective value of the 'rheostat' resistance can be varied with mark/space ratio control RV1. Thus, if IC2a is closed for 90% and open for 10% of each dury cycle (mark/space ratio of 9:1), the apparent (mean) value of the resistance will be 10% greater than RA, i.e., 10k. If the duty cycle is reduced to 50%, the apparent RA value will double, to 18k2. If the duty cycle is further decreased, so that IC2a is closed for only 10% of each duty cycle (mark/space ratio 1:9), the apparent value of RA will increase by a decade, to 91k. Thus, the apparent resistance of each 'gang' of the 'rheostat' can be varied by RV1.

There are some important point to note about the Fig. 18 circuit. First, the circuit can be given any desired number of 'gangs' by simply adding an appropriate number of switch stages and range resistors. Since all switches are controlled by the same mark/space ratio waveform, perfect tracking is automatically assured. Individual gangs can be given different ranges, without affecting the tracking, by giving them different range resistor values. The sweep range and the log of the rheostat can be changed by changing the characteristics of the mark/space ratio generator.

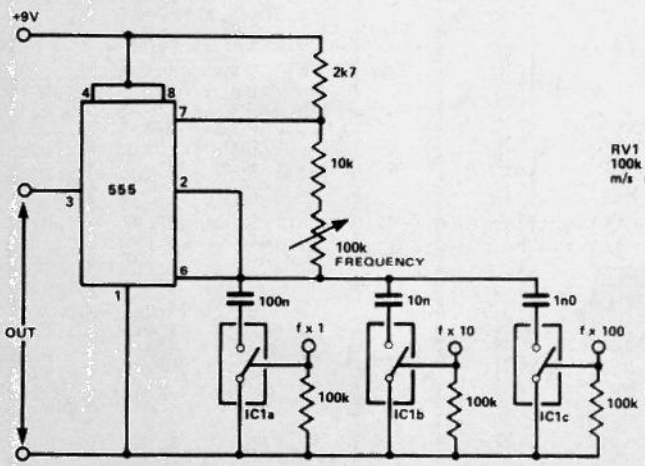


Fig. 17 Digital control of decade range switching of a 555 astable.

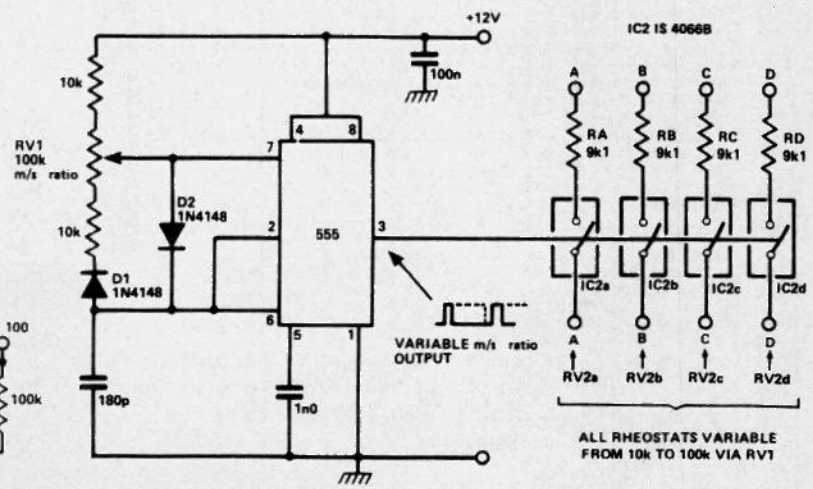
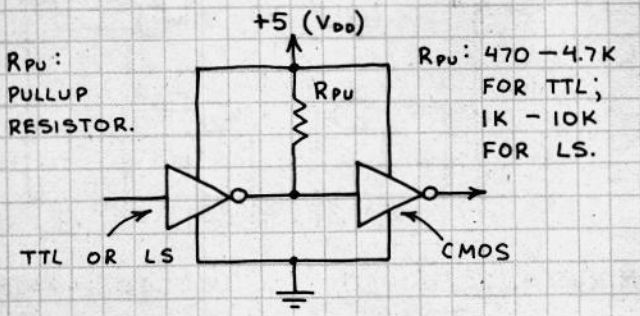
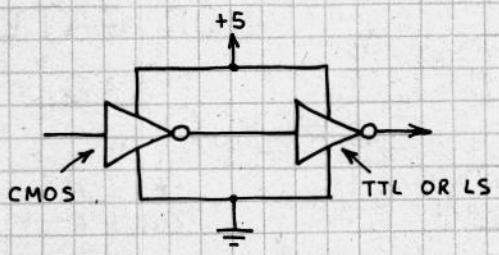


Fig. 18 Synthesized precision four-gang rheostat.

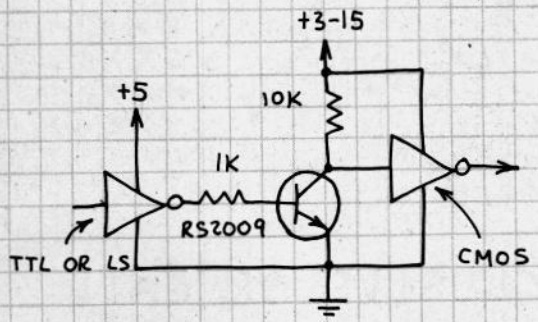
INTERFACING CMOS

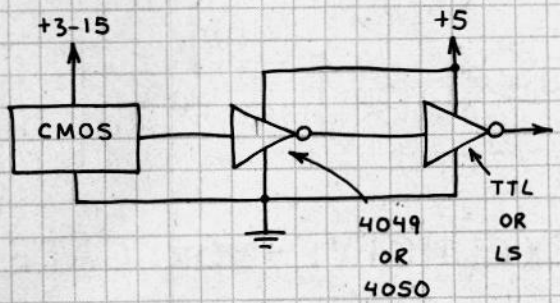
1. IF SUPPLY VOLTAGES ARE EQUAL:





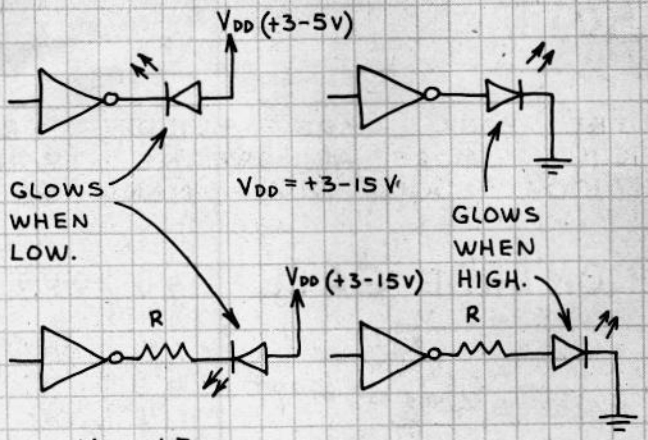
2. DIFFERENT SUPPLY VOLTAGES:





NOTE THAT CMOS MUST BE POWERED BY AT LEAST 5 VOLTS WHEN CMOS IS INTERFACED WITH TTL. OTHERWISE THE CMOS INPUT WILL EXCEED V_{DD}.

3. CMOS LED DRIVERS:

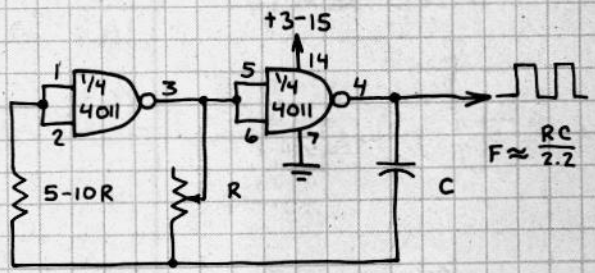


$$R = \frac{V_{DD} - 1.7}{.01}$$ (FOR 10 mA LED CURRENT)

USE 1000 OHMS FOR MOST APPLICATIONS.

CMOS LOGIC CLOCK

MANY CIRCUITS IN THIS SECTION REQUIRE A SOURCE OF PULSES. HERE'S A SIMPLE CMOS CLOCK:



TYPICAL VALUES: R = 100K, C = 0.01 – 0.1 μF

OK TO USE 4049 ... BUT MUCH MORE CURRENT WILL BE REQUIRED.

CMOS TROUBLESHOOTING

1. DO <u>ALL</u> INPUTS GO SOMEWHERE?

2. ARE <u>ALL</u> IC PINS INSERTED INTO THE BOARD OR SOCKET?

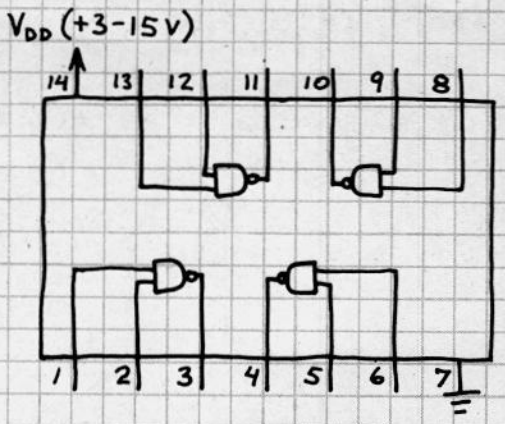
3. IS THE IC <u>HOT</u>? IF SO, SEE 1-2 ABOVE AND MAKE SURE THE OUTPUT IS NOT OVERLOADED.

4. DOES THE CIRCUIT OBEY <u>ALL</u> CMOS OPERATING REQUIREMENTS?

5. HAVE YOU FORGOTTEN A CONNECTION?

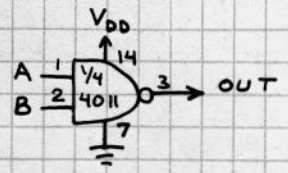
QUAD NAND GATE
4011

THE BASIC CMOS BUILDING BLOCK CHIP. MORE APPLICATIONS THAN TTL 7400/74LS00 QUAD NAND GATE.



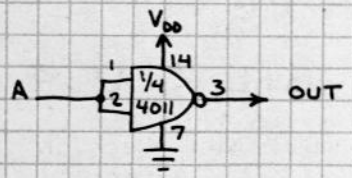
IMPORTANT: CONNECT ALL UNUSED INPUTS TO PIN 7 OR 14!

CONTROL GATE



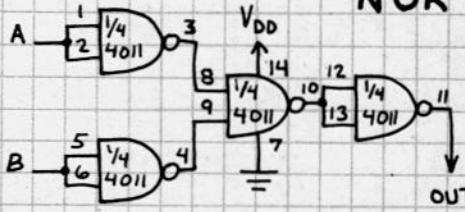
A	B	OUT
L	L	H
L	H	H
H	L	H
H	H	L

INVERTER



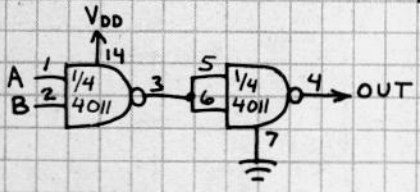
A	OUT
L	H
H	L

NOR GATE



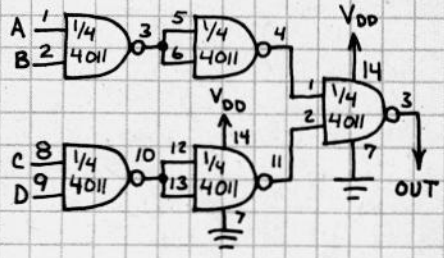
A	B	OUT
L	L	H
L	H	L
H	L	L
H	H	L

AND GATE



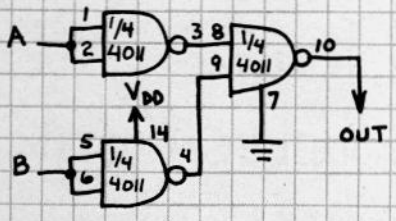
A	B	OUT
L	L	L
L	H	L
H	L	L
H	H	H

4-INPUT NAND GATE



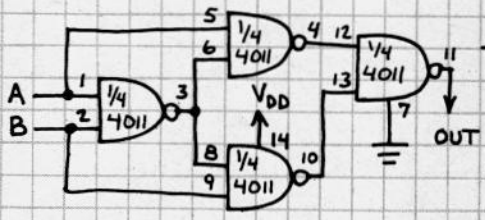
A	B	C	D	OUT
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

OR GATE



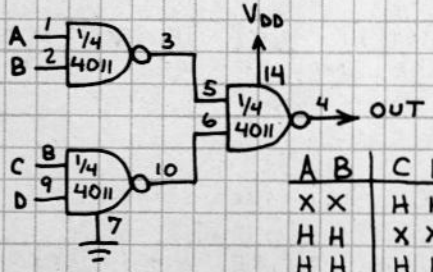
A	B	OUT
L	L	L
L	H	H
H	L	H
H	H	H

EXCLUSIVE-OR GATE



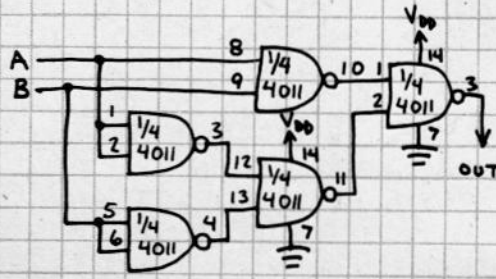
A	B	OUT
L	L	L
L	H	H
H	L	H
H	H	L

AND-OR GATE



A	B	C	D	OUT
X	X	H	H	H
H	H	X	X	H
H	H	H	H	H

EXCLUSIVE-NOR GATE



A	B	OUT
L	L	H
L	H	L
H	L	L
H	H	H