AUTOMOTIVE IC-DESIGN

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Abstract

The design of integrated circuits for automotive applications has to face multiple challenges, such as high voltage capability, robustness in a wide temperature range, good electromagnetic compability, protection against short-circuit and overvoltage conditions, and predictable behaviour also in case of missing supply voltages.
This paper presents some analog circuit examples to deal with the mentioned circumstances without loosing functional performance.

1. Introduction

Today's suppliers of automotive electronics prefer a system-on-a-chip approach to achieve the ever increasing reliability requirements. Smart Power technologies make it possible to combine logic, analog functions and multiple power output stages on one chip. Special design efforts are necessary for the analog circuits to obtain function and accuracy under tough conditions, caused by the high power dissipation, which directly implies very high chip temperatures. Other than wireless, consumer or desktop applications, automotive electronics have to withstand operating temperatures in the range of -40°C to 175°C and even more for a short time in short-current or broken-load conditions. Another challenge is the handling of disturbant electric pulses occuring randomly during operation. These pulses are caused by the switching of the various actuators distributed along the electric power net of the car or by the actuators themselves. They must not lead to malfunction or destruction of the integrated circuit, but they are often the root cause for activating parasitics.

2. Technology

Integrated circuits for automotive applications require power technologies which can withstand 60V, can handle high currents of up to 50A and are reliable over a wide temperature range.
Two kinds of technologies are used to fulfill these requirements:

J. H. Huijsing et al. (eds.), Analog Circuit Design, 137-151.

2.1 Self-isolation Smart Technology with vertical current flow

This kind of power semiconductor technology is based on the CMOS self-isolation approach. To minimize Rds(on) for a given chip area, the n-channel DMOS power device is vertical, using the backside metallization of the chip as a drain connection. This enables very low on-state resistances in the milli-Ohm range and consequently is very well suited for switching high currents in automotive applications. As shown in Fig. 2.1 the drain connection is equal to the substrate of the chip and, therefore, always has to be connected to the positive supply voltage. This leads to the restriction that multi-channel switches are only possible in common-drain (high-side) configuration. Analog and logic circuits can be integrated on the same chip by using the low-voltage CMOS and the high-voltage lateral MOS devices.

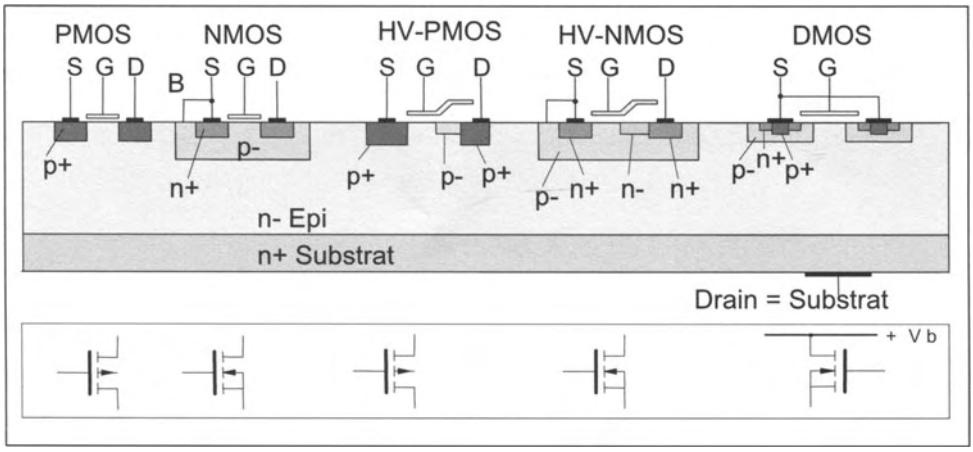

Fig. 2.1: Cross section of vertical Smart Technology

2.2 Junction isolated Smart Power Technology (SPT)

The junction-isolation approach enables the integration of CMOS, bipolar and power-DMOS on one chip, therefore, this type of technology is known as BCD (bipolar-CMOS-DMOS) [1,7]. The cross- section of some devices is shown in Fig. 2.2. Each device is placed within an n-well terminated by the highly n-doped buried layer and n-sinker. The isolation among the n-wells by p^+-areas allows for the implementation of several devices working independently on a chip. Therefore this technology allows to integrate a system solution on one chip with multifold low-side or high-side outputs or even power stages in bridge configuration including all circuits for analog diagnostics and protection and logic circuits.

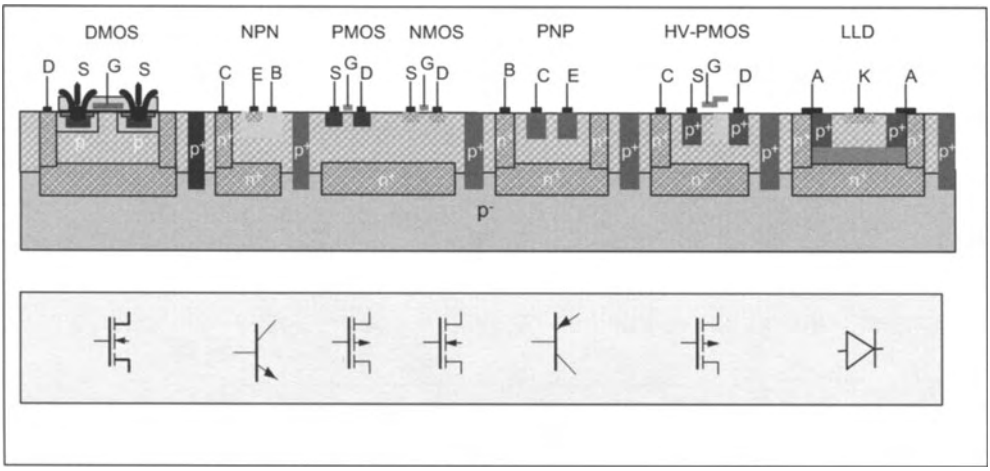

Fig. 2.2: Cross section of some devices of an SPT technology

3. Robust design of a bandgap reference circuit

As mentioned before, in BCD semiconductor technologies the devices sharing one substrate are isolated from each other by reverse-biased p-n-junctions. Reverse bias is usually established by connecting the p-doped substrate to the most negative supply voltage, which often is equal to ground. Under normal operating conditions, the parasitic interaction among the devices via the substrate is minimized this way. There are, however, situations where the isolation is degraded or partly lost. Two examples are very high operating temperatures (>150°C) and the presence of minority carriers in the substrate. In the automotive environment, both occur frequently and consequent degradation of performance or loss of functionality have to be avoided by a robust design.
In this section, the implications of very high operating temperatures and minority-carrier injection are discussed. Possible ways to deal with the issue are presented and a robust bandgap reference circuit is shown as a design example.

3.1. High Temperature Operation

The automotive operating temperature ranges from -40°C to 150°C. At these temperatures, junction leakage currents are small compared to the operating bias currents and usually do not limit the overall performance. There are, however, requirements for an extended temperature range of up to 175°C during operation and more than 200°C during fault conditions such as overload (short circuit). Junction leakage currents rise exponentially with temperature and can, at

T>150°C, exceed the operating bias currents by far. The leakage currents can be expressed as

$$I_S = qA\left[\frac{D_p}{L_p}\frac{1}{N_D} + \frac{D_n}{L_n}\frac{1}{N_A}\right]n_i^2 + qA\frac{w}{\tau_0}n_i^2 \qquad (1)$$

with q being the electron charge, A the junction area, D_p and D_n the diffusion constants, L_p and L_n the diffusion lengths, N_D and N_A the doping levels, n_i the intrinsic carrier density, w the junction width, and τ_0 the effective lifetime of the minority carriers in the depletion region.

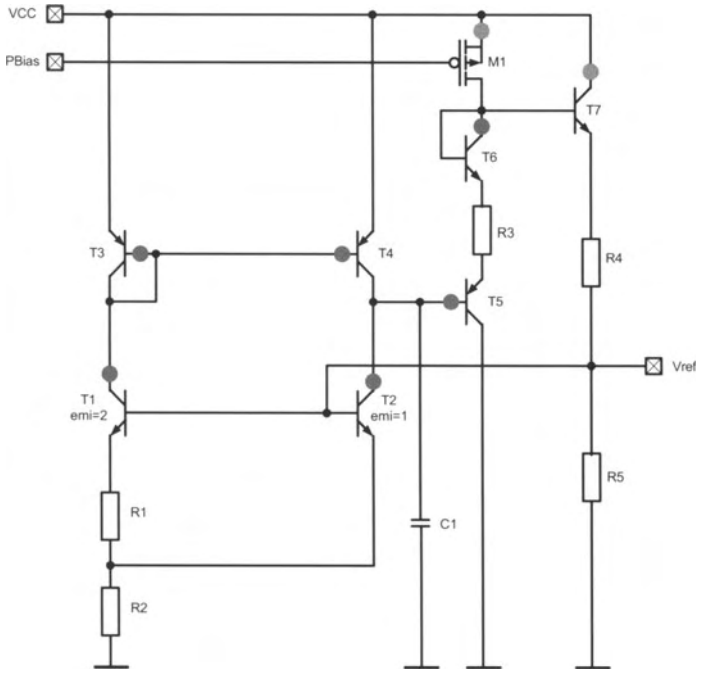

Fig. 3.1: Brokaw cell with substrate junctions (red circles)

From equation (1), it is obvious that leakage currents are proportional to the junction area A and that higher doping levels lead to lower leakage currents. Therefore, the junctions isolating the devices from the substrate are the ones with the highest leakage currents due to their large area and to the low doping level of the substrate [3]. This can be exploited in circuit design by avoiding substrate junctions in the critical signal path and biasing those junctions from low-impedance sources. As shown in the example in Fig. 3.1, some commonly

used circuits do not follow this rule and therefore in high-temperature design new circuit topologies have to be used [9]. The red circles in Fig. 3.1 mark nodes associated with n-epi wells which are driven from high-impedance sources. Clearly parasitic currents at those nodes will degrade the circuit's performance. A measurement result of the reference voltage obtained from a circuit with the topology of Fig. 3.1 is shown in Fig. 3.2. At temperatures above approximately 150°C, a deviation from the expected 2nd order characteristic can be observed and at T>180°C, the influence of leakage currents gets dominant and leads to malfunction above 200°C.

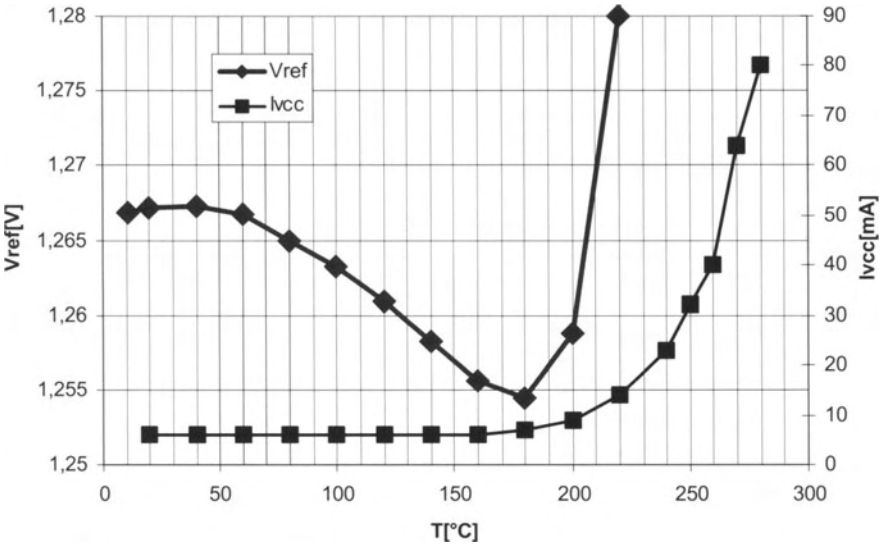

Fig. 3.2: Standard bandgap reference circuit performance and total current consumption

3.2. Minority Carrier Injection

The presence of minority carriers in the substrate is a well known problem in BCD semiconductor technologies and a major cause for redesign [7, 8]. Minority carriers, i.e. electrons when a p-type substrate is used, are injected into the substrate when the n-epi well of a device gets forward-biased in respect to the substrate. Subsequently, these electrons diffuse over large distances (in the order of the die size) and are partially swept across reverse-biased epi-substrate junctions of other devices in the same substrate. There, they impose parasitic currents which are highly dependent on doping levels, temperature, amount of injection, and layout and therefore are hard to predict.
The nodes where parasitic currents caused by minority carrier injection have to be expected are the n-epi wells of each device. These are exactly the same nodes

where the largest high-temperature junction leakage currents will be observed (see section 3.1).
From this, it can be concluded that a circuit topology which is designed for high-temperature operation will also be inherently robust against parasitic currents caused by minority carriers in the substrate and vice versa.

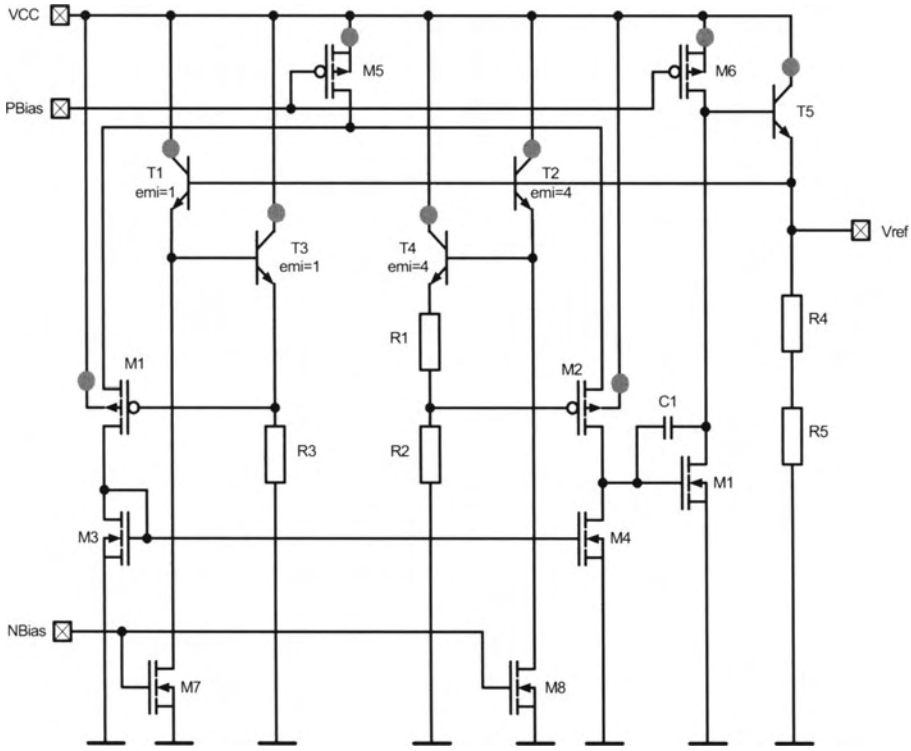

Fig. 3.3: Robust bandgap reference – simplified schematic

Fig. 3.3 shows an example of a bandgap reference circuit which has been designed in order to avoid parasitic currents in the control loop. This is achieved mainly by supplying all nodes associated with n-epi wells (green circles in Fig. 3.3) from low-impedance sources such as the voltage supplies. This is in accordance with the design rule derived in section 3.1. The circuit uses a series connection of two base-emitter junctions of n-p-n transistors which, in turn, are connected in series with a dVBE generator. This way, a stable reference voltage of 2.4V is achieved according to the bandgap reference principle [10]. A simple CMOS opamp is used to close the control loop and to establish equal voltages at the gates of M1 and M2. Due to the stacking of two base-emitter junctions, the

ratio of R2/R1 can be kept low. Therefore, the offset of the CMOS opamp has less influence on the output voltage.
Measurement results of the robust bandgap reference circuit are presented in Fig. 3.4. The scale of the voltage has been chosen so that the upper and lower limit in the graph correspond to the average reference voltage ±1%. As can be seen, the reference voltage is accurate within a fraction of one percent in a temperature range of up to 295°C (which was the limit of the measurement equipment). The total current consumption of the chip is also shown to emphasize the effect of junction leakage currents.
Tests have also been carried out to demonstrate the immunity against minority carrier injection. A large epi-substrate junction of a power-DMOS transistor has been forward-biased to inject a large amount of electrons into the substrate. As expected, no influence on the reference voltage could be detected until the injected current reached excessive levels and the power-DMOS was destroyed.

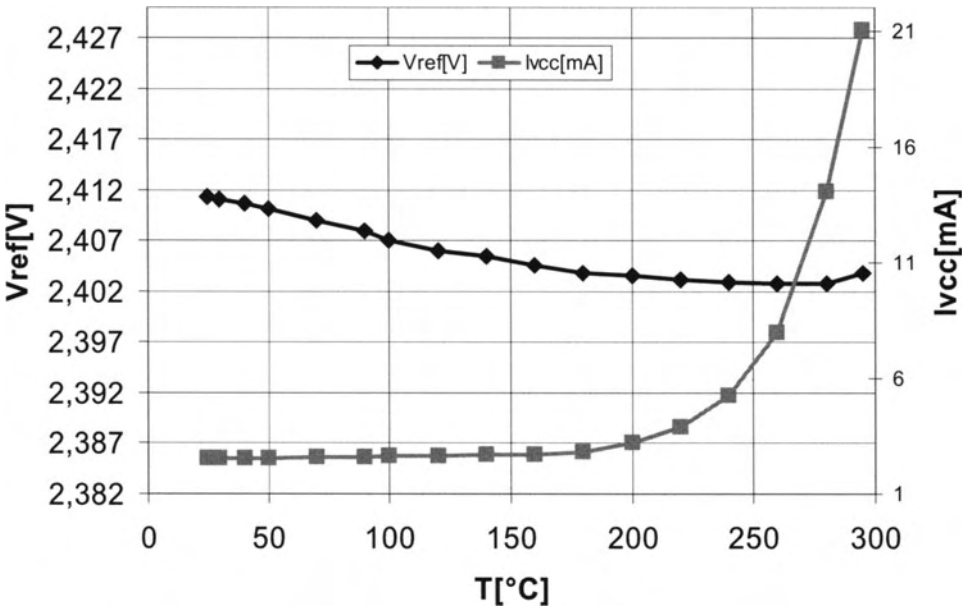

Fig. 3.4: Robust bandgap reference – measurement result

4. Failsafe warning-lamp driver circuit

The typical configuration of an automotive system chip with a warning-lamp output is shown in Fig. 4.1. It includes power outputs to drive the application specific loads and analog diagnostic circuits which are responsible for testing

the internal circuits and the external components. All diagnostic information is combined and activates an output which drives a lamp. This warning lamp is situated in the dashboard of the car. It is switched on for a short time when the car is started and then - if everything is okay - it is switched off. In case of any error in the system, this warning lamp is switched on again and the car driver gets the information that, e.g., the airbag or the ABS system do not work properly.

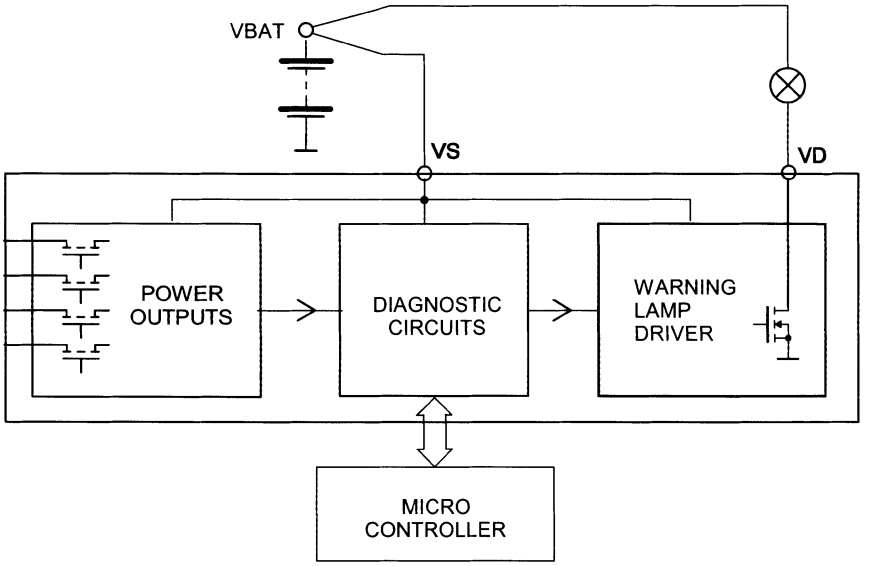

Fig. 4.1: Block diagram of a smart-power system chip

The definition: "In case of an error the lamp has to be switched on" includes also the failure mode that the supply line is disconnected. Loosing the battery connection VS of the module should result in an activated lamp. How to consider this requirement in designing a driver circuit is described in detail below.

A block diagram of the lamp driver circuit is shown in Fig. 4.2. Under normal supply voltage conditions, the load RL is fed by the voltage VBAT, whereas the logic and the gate driver circuits are supplied by VS. Now we assume the following error condition: The voltage VS is missing, but the voltage VBAT exists. In that case, the lamp should be switched on. This would report the error condition of the missing VS because all errors are reported by switching on the lamp - normally by the logic circuit. But the logic circuit is now missing its supply voltage! To achieve the desired function, the gate voltage has to be

captured from VBAT via the load. It would be no problem if the DMOS was switched off. But the switched-on DMOS does not provide a sufficient voltage VD at its drain to supply the circuits. The target is to develop a gate-driver circuit which can manage this condition. This is done in two essential steps: Firstly, a charge pump is used to multiply the low voltage VD to an adequate level. And secondly, a regulation circuit controls the saturation voltage VD in such a way that it will not drop below a minimum value which is the required operation voltage of the charge pump. Additionally, the design of the overload protection circuit has to accept a low-voltage VD as a supply voltage.

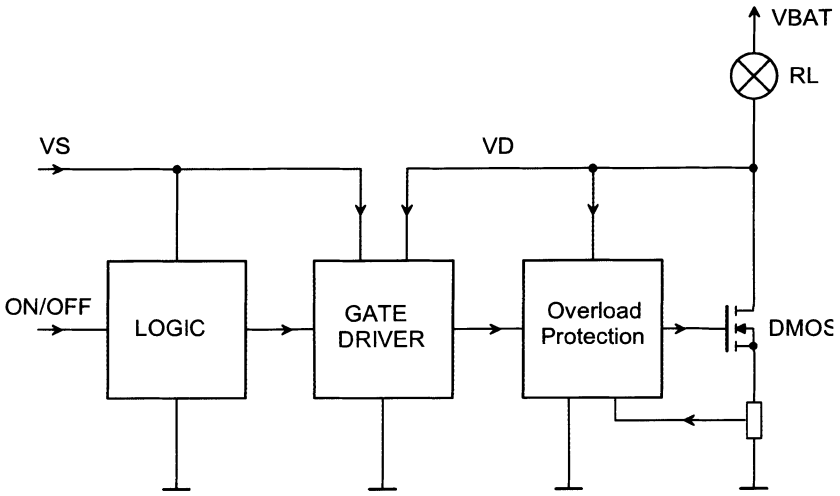

Fig. 4.2: Block diagram of the lamp driver circuit

A more detailed circuit diagram is shown in Fig. 4.3. The gate voltage of the DMOS is supplied either via VS or via VCP, which is the output voltage of the charge pump. The input voltage of the charge pump is supplied by VD, the drain voltage of the power DMOS. A bias circuit consisting of the devices Q1 to Q4 generates a stabilized current IB which is mirrored to supply the charge pump and the regulation circuit. To keep the bias circuit operating, the voltage VD should not drop below two base-emitter voltages (VBE). The control loop is described below. The DMOS gate is charged by the current I8 and discharged by the current I10. The discharging current is cut off by means of Q10 so that the DMOS will remain switched on. If the drain voltage VD decreases, a point will be reached where the current I2 becomes zero. Then the current I9 and, correspondingly, I10 will increase. This leads to a state where I8 is equal to I10 as a stable operating point. The large gate capacitance of the DMOS acts as a sufficient loop compensation of this control circuit. The final potential of VD is defined by the voltage drops of M11 and Q9. In practice, this amounts to about

2V, which is high enough to feed the bias circuit and the charge pump. On the other hand, it is low enough to be accepted as a drain-to-source voltage drop of the DMOS.

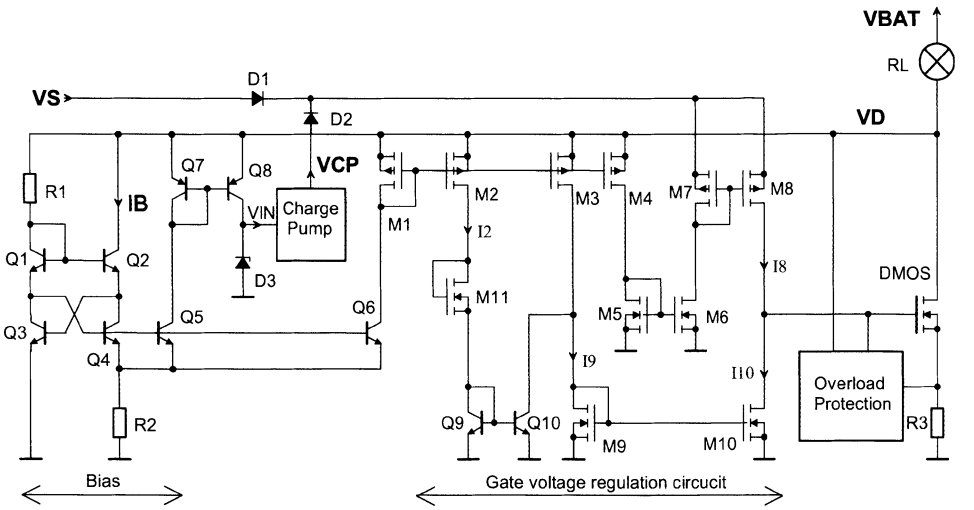

Fig. 4.3: Circuit diagram of the lamp driver circuit

The charge pump circuit is shown in Fig. 4.4. To achieve the required gate voltage, a multi-stage design was chosen. The five inverter stages are directly connected in a feedback loop to form a ring oscillator, therefore, no additional oscillator is necessary.

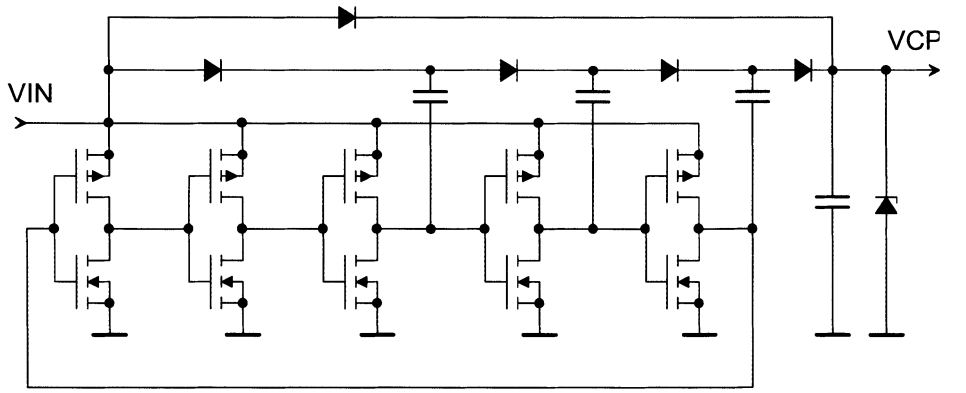

Fig. 4.4: Charge pump circuit

The overload protection circuit is shown in Fig. 4.5. It provides current limiting and temperature protection of the DMOS. The circuit is supplied directly from the drain voltage of the output power transistor and does not need any additional supply voltage or reference voltage. The bias generator is similar to the one shown in Fig. 4.3.

The current I2 depends on ΔVBE and R2, where ΔVBE is given by comparing Q1 + Q4 with Q2 + Q3:

$\Delta VBE = Vt \cdot [\ \ln(AreaQ1) + \ln(AreaQ4) - \ln(AreaQ2) - \ln(AreaQ3)\ ]$,

$Vt = kT/q$ depends on the absolute temperature T, thus the bias circuit is actually a so-called PTAT source. This means that the current is proportional to the absolute temperature. Adding the current mirror Q7, Q11 and the devices R4, Q14 completes the circuit to a temperature shut-off block. The voltage drop across R4 is increasing with temperature. Compared to the decreasing VBE characteristic of the bipolar device Q14, this results in a well defined temperature shut-off point.

The second task of the circuit is current limitation. The current threshold is defined by the ΔVBE of Q15 and Q16, compared to the voltage drop at R3. The shunt resistor R3 is part of the metal interconnect layer. This leads to a first-order temperature compensation of the current threshold.

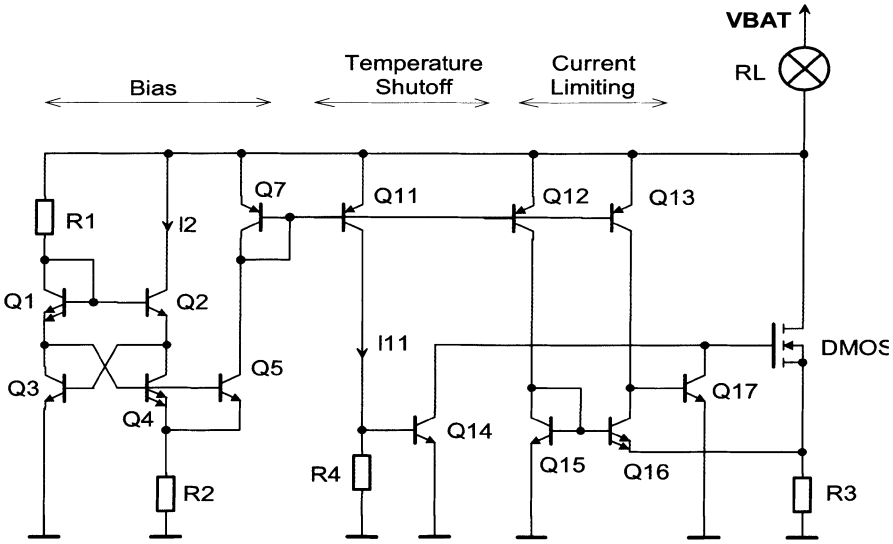

Fig. 4.5: Overload protection circuit

5. Temperature sensor for very high temperature thresholds

Thermal protection of smart power circuits requires a temperature sensor. The temperature threshold has to be low enough to protect the device in case of any overload like a short circuit or an overvoltage pulse. On the other hand, the temperature threshold should be sufficiently high so that the sensor is never activated under any possible operating conditions including highest ambient temperature and overvoltage. The required temperature threshold depends on the position of the temperature sensor in relation to the hot spot of the power-DMOS [2]. It is typically in the range of 175°C to 200°C if the sensor is situated at the edge of the power device. But for some applications, as e.g. power ICs for activating airbag firing, the worst- case operating conditions can lead to very fast heating of the DMOS, which results in hot spot temperatures of above 250°C. To allow this high temperature for operation and, on the other hand, to protect the device against thermal destruction, the temperature sensor should be situated close to the hot spot in the center of the power device. This requires temperature sensors which can reliably be adjusted in a temperature range of 250°C and higher.
For accurate temperature sensing, it is convenient to use a bipolar transistor and to compare the characteristic of the base emitter voltage with a constant reference voltage, which is generated e.g. from a bandgap reference [6], see Fig. 5.1.

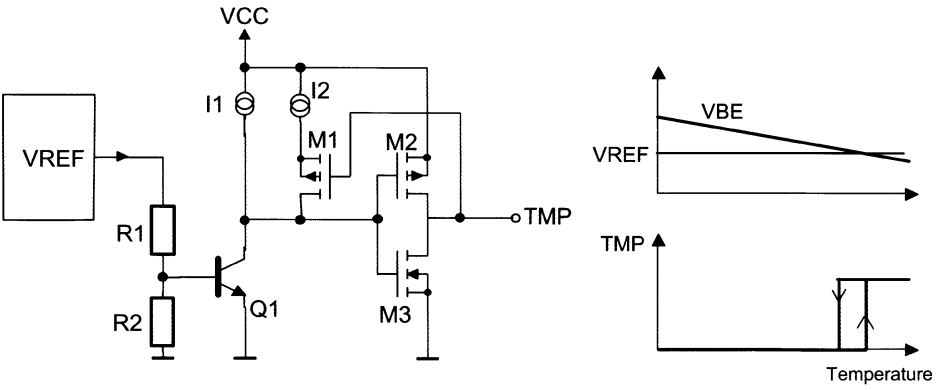

Fig. 5.1: Temperature sensor with hysteresis

The problem of a bipolar device in the very high temperature range is the increase of junction leakage currents from collector to substrate and collector to base at high temperatures. A measurement of the VBE voltage of an n-p-n transistor over temperature is shown in Fig. 5.2. The measured data shows that

the linear behavior of the VBE of approximately -2mV/K is valid in a wide temperature range up to 250°C but drops down in the higher temperature range if the bipolar n-p-n is driven by a constant collector current. By forcing a constant emitter current to the transistor, it would be possible to extend the useful range of the VBE voltage for temperature measurement.

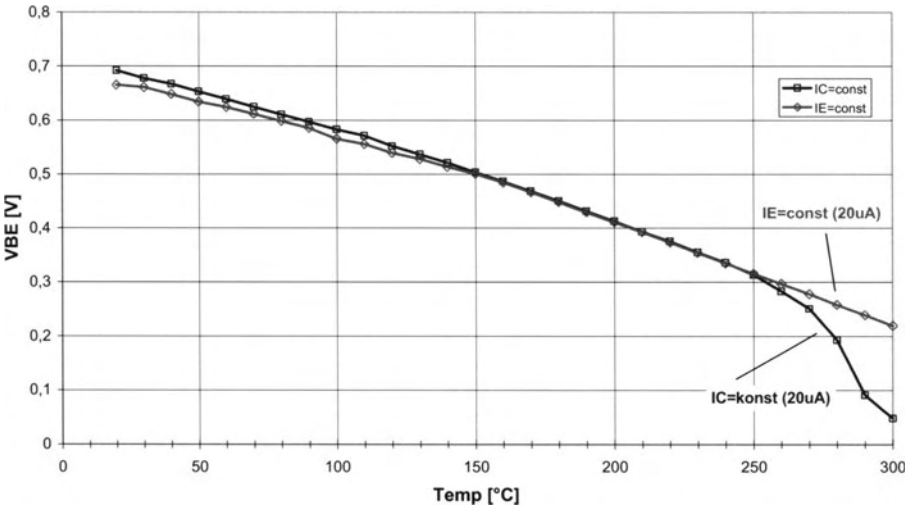

Fig. 5.2: Measured data of base-emitter voltage vs. temperature

If a simple temperature sensor circuit as shown in Fig. 5.1 is used in an extended temperature range, the leakage current will lead to a wrong threshold for the over-temperature detection. Fig. 5.3 shows an improved circuit where the leakage current of the bipolar temperature sensor T1 is compensated with the help of a second transistor T2 which is deactivated by a shorted BE diode and situated close to the sensor to have the same temperature as the sensor and subsequently to have the same leakage current. The PMOS current mirror M2, M3 compensates this leakage current by feeding the same amount of current into the collector of the sensor. An additional current mirror T3,T4 sinks the additional current due to high temperature from the base of the sensor. This concept has proven to work reliably up to 300°C and allows for extending the usable range of bipolar sensors for power switches with very high power densities.

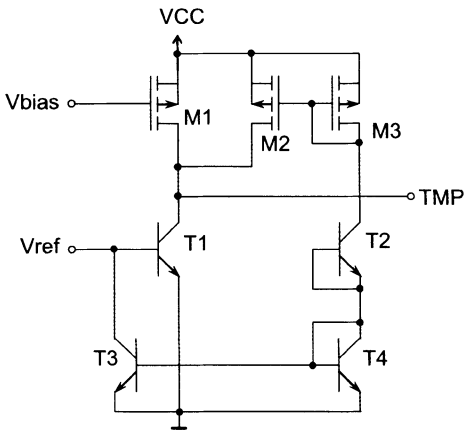

Fig. 5.3: Temperature sensor with full leakage current compensation

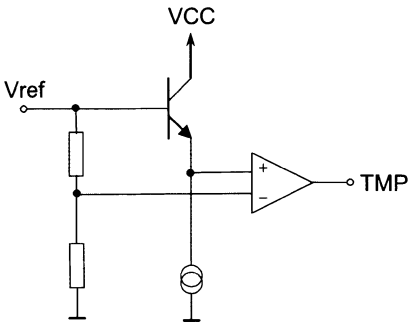

Fig. 5.4: Temperature sensor with collector at supply line t

Another concept for an improved temperature sensor circuit is shown in Fig. 5.4. Here the collector of the sense-transistor is directly connected to a power supply line which is able to deliver the leakage current without an additional compensation device. Comparison of the base-emitter voltage with the reference voltage is performed by an MOS comparator.

6. Conclusions

Analog circuits, which are part of smart power circuits for automotive applications, have to withstand tough requirements. A selection of circuits which deals with the problem of very high temperatures, substrate injection problems caused by reverse-current conditions, and a solution for functionality without supply voltage are presented. Modern smart power technologies offer all analog and digital
components necessary to integrate system solutions, including the power stages on one chip. Robustness of analog design in this surrounding will be one key factor for success of extended smart- power system integration in the future.

7. References

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