COS/MOS digital ICs

COS/MOS is a development of bipolar IC technology and an offspring of the MOS (Metal Oxide Semiconductor).
It started with the MOSFET being developed from the universally known junction FET (Field Effect Transistor). The former distinguish themselves from the latter by their isolated gate. The result of this gate isolation is a particularly high gate resistance. A drawback is that a static charge can build up on such a gate when the transistor is not connected in a circuit. This charge usually causes the immediate destruction of a MOSFET because the extremely thin isolating layer breaks down. So the handling of MOSFETs calls for special precautions. This also applies to COS/MOS ICs in which MOSFETs are integrated.

The integration is such that P+ and N- channel transistors are used alternately. Furthermore the switching circuits are integrated symmetrically. The latter two characteristics form the basis for the term COS (COmplementary Symmetry). Thus COS/MOS can be briefly described as complementary symmetrical MOSFET integration. A simple example of a COS/MOS IC construction is given in figure A. Here the dark-shaded area represents the n- (polarized) substrate. The diagonally-hatched area is the metal oxide film on which the electrical contacts are made. These contacts are drawn in deep black. Below the isolating layer at the electrical contact interruptions are the p- and n- layers. The layers are so integrated that the result is a complementary MOSFET pair as shown in figure B. Corresponding to the labelling of figure A, we have the following labelling in figure B: 'S' for sources, 'G' for gates and 'D' for common drain.

As can be seen from figure A the integration of an N- channel MOSFET is of a simpler construction than a P-channel. The latter requires an extra p- layer separating the substrate from the two n- layers which lie between the drain and G2 (= gate 2) and the junction between G2 and S2 (= source 2), respectively.

Of course, the integration of even the simplest COS/MOS IC is slightly more complex than figure B suggests. Even a common 2-input NAND gate consists of no less than four integrated MOSFETs.
Like MOSFETs, every COS/MOS IC must be handled with due care because the inputs (gates) are isolated with respect to the rest of the integrated circuit. Normally the input impedance of a gate is $10^{12}\ \Omega$. As a result a static charge can easily build up if such an IC is kept in a plastic box, for instance. The human body too, is often statically charged. Touching the inputs with a finger can be sufficient to destroy the COS/MOS IC. Therefore the IC[illegible]re packed in a kind of expanded [illegible]ic containing a highly conductive substance. The connecting pins of the IC are pressed into the expanded plastic.
To give the inputs some measure of protection, manufacturers often provide COS/MOS IC inputs with an inbuilt protection circuit. These circuits are not shown in the circuit diagrams of the ICs.
Figure C is an example of an input circuit of a COS/MOS inverter. As can be seen in this figure, the circuit consists of a P- and an N- channel MOSFET. In reality the input circuit is as shown in figure D. Here we see that each gate input protection circuit comprises one resistor and three diodes. The diodes D_4 to D_8 are usually formed in the diffusion process. The gate input protection, however, is added as an extra (a resistor of about 500 Ω plus three diodes).
In figure D the diode D_3 has a breakdown voltage of about 25 V. The breakdown voltage of the diodes D_1 and D_2 is about 50 V.