Micropower Circuits Using the LM4250 Programmable Op Amp

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Application Note 71
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INTRODUCTION

The LM4250 is a highly versatile monolithic operational amplifier. A single external programming resistor determines the quiescent power dissipation, input offset and bias currents, slew rate, gain-bandwidth product, and input noise characteristics of the amplifier. Since the device is in effect a different op amp for each externally programmed set current, it is possible to use a single stock item for a variety of circuit functions in a system.

This paper describes the circuit operation of the LM4250, various methods of biasing the device, frequency response considerations, and some circuit applications exercising the unique characteristics of the LM4250.

CIRCUIT DESCRIPTION LM4250

The LM4250 has two special features when compared with other monolithic operational amplifiers. One is the ability to externally set the bias current levels of the amplifiers, and the other is the use of PNP transistors as the differential input pair.

Referring to *Figure 1*, Q_1 and Q_2 are high current gain lateral PNPs connected as a differential pair. R_1 and R_2 provide emitter degeneration for greater stability at high bias currents. Q_3 and Q_4 are used as active loads for Q_1 and Q_2 to provide high gain and also form a current inverter to provide the maximum drive for the single ended output into Q_5. Q_5 is an emitter follower which prevents loading of the input stage by the succeeding amplifier stage.

One advantage of this lateral PNP input stage is a common mode swing to within 200 mV of the negative supply. This feature is especially useful in single supply operation with signals referred to ground. Another advantage is the almost constant input bias current over a wide temperature range. The input resistance R_{IN} is approximately equal to 2β (R_E + r_e) where β is the current gain, r_e is the emitter resistance of one of the input lateral PNPs, and R_E is the resistance of one of the 10 kΩ emitter resistor. Using a DC beta of 100 and the normal temperature dependent expression for r_e gives:

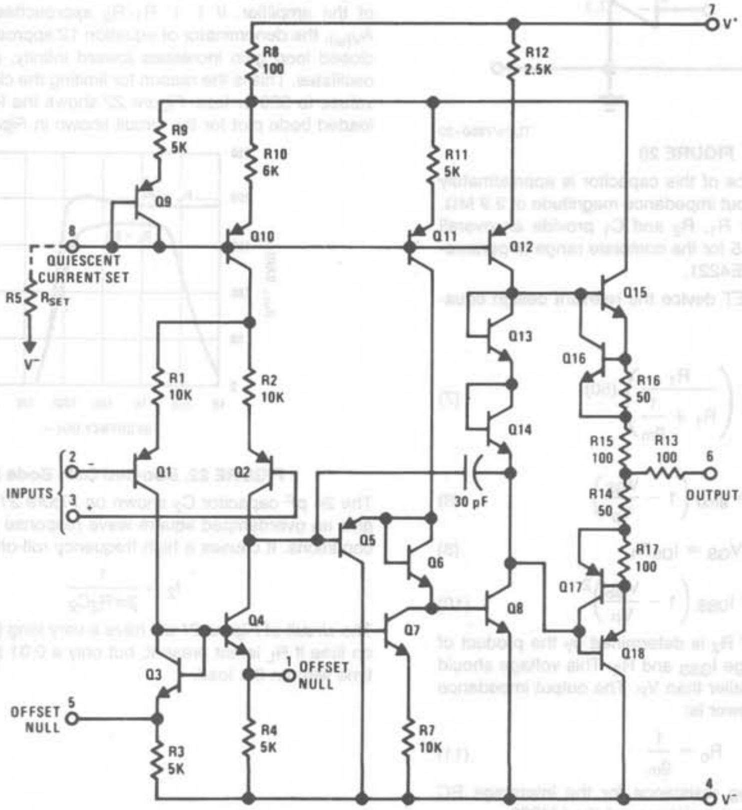

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FIGURE 1. LM4250 Schematic Diagram

$$R_{IN} \approx 2\ M\Omega + 2\frac{kT}{qI_B} \quad (1)$$

where I_B is input bias current. At room temperature this formula becomes:

$$R_{IN} \approx 2\ M\Omega + \frac{52\ mV}{I_B} \quad (2)$$

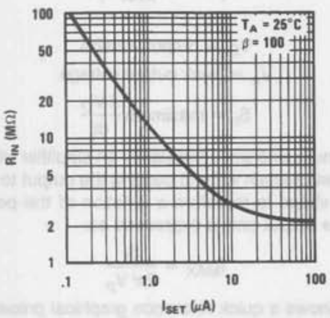

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FIGURE 2. Input Resistance vs I_{SET}

Figure 2 gives a typical plot of R_{IN} vs I_{set} derived from the above equation.

Continuing with the circuit description, Q_6 level shifts downward to the base of Q_8 which is the second stage amplifier. Q_8 is run as a common emitter amplifier with a current source load (Q_{12}) to provide maximum gain. The output of Q_8 drives the class B complementary output stage composed of Q_{15} and Q_{18}.

The bias current levels in the LM4250 are set by the amount of current (I_{set}) drawn out of Pin 8. The constant current sources Q_{10}, Q_{11}, and Q_{12} are controlled by the amount of I_{set} current through the diode connected transistor Q_9 and resistor R_9. The constant collector current from Q_{10} biases the differential input stage. Therefore, the level Q_{10} is set at will control such amplifier characteristics as input bias current, input resistance, and amplifier slew rate. Current source Q_{11} biases Q_5 and Q_6. The current ratio between Q_5 and Q_6 is controlled by constant current sink Q_7. Current source Q_{12} sets the currents in diodes Q_{13} and Q_{14} which bias the output stage to the verge of conduction thereby eliminating the dead zone in the class B output. Q_{12} also acts as the load for Q_8 and limits the drive current to Q_{15}. The output current limiting is provided by Q_{16} and Q_{17} and their associated resistors R_{16} and R_{17}. When enough current is drawn from the output, Q_{16} turns on and limits the base drive of Q_{15}. Similarly Q_{17} turns on when the LM4250 attempts to sink too much current, limiting the base drive of Q_{18} and therefore output current. Frequency compensation is provided by the 30 pF capacitor across the second stage amplifier, Q_8, of the LM4250. This provides a 6 dB per octave rolloff of the open loop gain.

BIAS CURRENT SETTING PROCEDURE

The single set resistor shown in *Figure 3a* offers the most straightforward method of biasing the LM4250. When the set resistor is connected from Pin 8 to ground the resistance value for a given set current is:

$$R_{SET} = \frac{V^+ - 0.5}{I_{SET}} \quad (3)$$

The 0.5 volts shown in Equation 3 is the voltage drop of the master bias current diode connected transistor on the integrated circuit chip. In applications where the regulation of the V^+ supply with respect to the V^- supply (as in the case of tracking regulators) is better than the V^+ supply with respect to ground the set resistor should be connected from Pin 8 to V^-. R_{SET} is then:

$$R_{SET} = \frac{V^+ + |V^-| - 0.5}{I_{SET}} \quad (4)$$

The transistor and resistor scheme shown in *Figure 3b* allows one to switch the amplifier off without disturbing the main V^+ and V^- power supply connections. Attaching C_1 across the circuit prevents any switching transient from appearing at the amplifier output. The dual scheme shown in *Figure 3c* has a constant set current flowing through R_{S1} and a variable current through R_{S2}. Transistor Q_2 acts as an emitter follower current sink whose value depends on the control voltage V_c on the base. This circuit provides a method of varying the amplifier's characteristics over a limited range while the amplifier is in operation. The FET circuit shown in *Figure 3d* covers the full range of set currents in response to as little as a 0.5V gate potential change on a low pinch-off voltage FET such as the 2N3687. The limit resistor prevents excessive current flow out of the LM4250 when the FET is fully turned on.

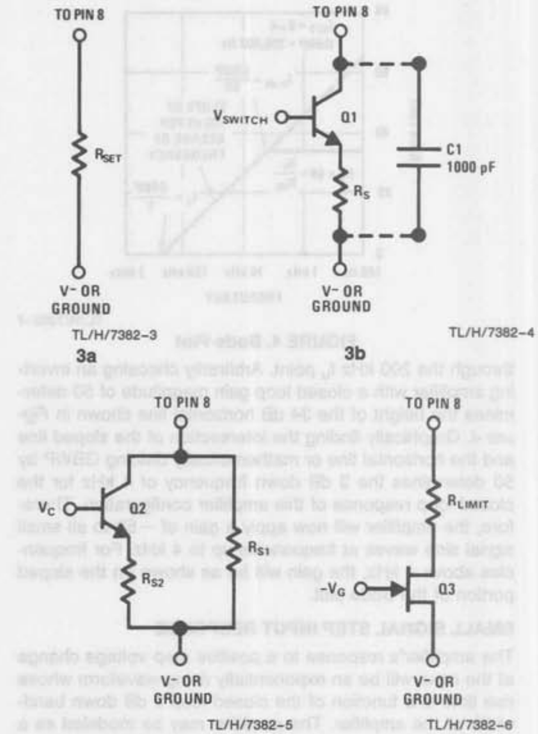

FIGURE 3. Biasing Schemes

FREQUENCY RESPONSE OF A PROGRAMMABLE OP AMP

This section provides a method of determining the sine and step voltage response of a programmable op amp. Both the sine and step voltage responses of an amplifier are modified when the rate of change of the output voltage reaches the slew rate limit of the amplifier. The following analysis develops the Bode plot as well as the small signal and slew rate limited responses of an amplifier to these two basic categories of waveforms.

SMALL SIGNAL SINE WAVE RESPONSE

The key to constructing the Bode plot for a programmable op amp is to find the gain bandwidth product, GBWP, for a given set current. Quiescent power drain, input bias current, or slew rate considerations usually dictate the desired set current. The data sheet curve relating GBWP to set current provides the value of GBWP which when divided by one yields the unity gain crossover of f_u. Assuming a set current of 6 μA gives a GBWP of 200,000 Hz and therefore an f_u of 200 kHz for the example shown in *Figure 4*. Since the device has a single dominant pole, the rolloff slope is -20 dB of gain per decade of frequency (-6 dB/octave). The dotted line shown on *Figure 4* has this slope and passes

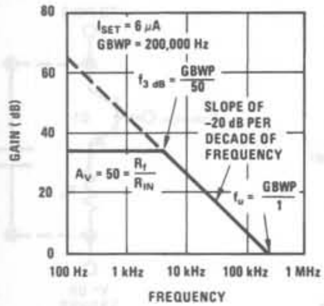

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FIGURE 4. Bode Plot

through the 200 kHz f_u point. Arbitrarily choosing an inverting amplifier with a closed loop gain magnitude of 50 determines the height of the 34 dB horizontal line shown in *Figure 4*. Graphically finding the intersection of the sloped line and the horizontal line or mathematically dividing GBWP by 50 determines the 3 dB down frequency of 4 kHz for the closed loop response of this amplifier configuration. Therefore, the amplifier will now apply a gain of -50 to all small signal sine waves at frequencies up to 4 kHz. For frequencies above 4 kHz, the gain will be as shown on the sloped portion of the Bode plot.

SMALL SIGNAL STEP INPUT RESPONSE

The amplifier's response to a positive step voltage change at the input will be an exponentially rising waveform whose rise time is a function of the closed loop 3 dB down bandwidth of the amplifier. The amplifier may be modeled as a single pole low pass filter followed by a gain of 50 wideband amplifier. From basic filter theory*, the 10% to 90% rise time of a single pole low pass filter is:

$$t_r = \frac{0.35}{f_{3\ dB}} \tag{5}$$

For the example shown in *Figure 4* the 4 kHz 3 dB down frequency would give a rise time of 87.5 μs.

SLEW RATE LIMITED LARGE SIGNAL RESPONSE

The final consideration, which determines the upper speed limitation on the previous two types of signal responses, is the amplifier slew rate. The slew rate of an amplifier is the maximum rate of change of the output signal which the amplifier is capable of delivering. In the case of sinosoidal signals, the maximum rate of change occurs at the zero crossing and may be derived as follows:

*See reference.

$$V_O = V_p \sin 2\pi f t \tag{6}$$

$$\frac{d V_O}{d t} = 2\pi f V_p \cos 2\pi f t \tag{7}$$

$$\left.\frac{d V_O}{d t}\right|_{t = o} = 2\pi f V_p \tag{8}$$

$$S_r = 2\pi f_{MAX} V_P \tag{9}$$

where:

V_O = output voltage

V_p = peak output voltage

$S_r = \text{maximum} \dfrac{d V_O}{dt}$

The maximum sine wave frequency an amplifier with a given slew rate will sustain without causing the output to take on a triangular shape is therefore a function of the peak amplitude of the output and is expressed as:

$$f_{MAX} = \frac{S_r}{2\pi V_p} \tag{10}$$

Figure 5 shows a quick reference graphical presentation of this formula with the area below any V_{peak} line representing an undistorted small signal sine wave response for a given frequency and amplifier slew rate and the area above the V_{peak} line representing a distorted sine wave response due to slew rate limiting for a sine wave with the given V_{peak}.

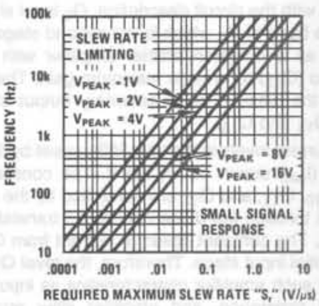

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FIGURE 5. Frequency vs Slew Rate Limit vs Peak Output Voltage

Large signal step voltage changes at the output will have a rise time as shown in equation 5 until a signal with a rate of output voltage change equal to the slew rate of the amplifier occurs. At this point the output will become a ramp function with a slope equal to S_r. This action occurs when:

$$S_r \leq \frac{V_{step}}{t_r} \tag{11}$$

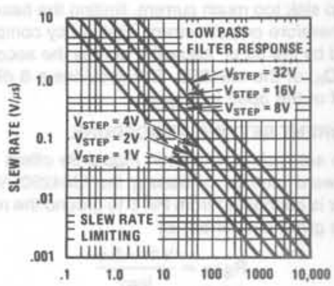

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FIGURE 6. Slew Rate vs Rise Time vs Step Voltage

Figure 6 graphically expresses this formula and shows the maximum amplitude of undistorted step voltage for a given slew rate and rise time. The area above each step voltage line represents the undistorted low pass filter type response mode of the amplifier. If the intersection of the rise time and slew rate values of a particular amplifier configuration falls below the expected step voltage amplitude line, the rise time will be determined by the slew rate of the amplifier. The rise time will then be equal to the amplitude of the step divided by the slew rate S_r.

FULL POWER BANDWIDTH

The full power bandwidth often found on amplifier specification sheets is the range of frequencies from zero to the frequency found at the intersection on *Figure 5* of the maximum rated output voltage and the slew rate S_r of the amplifier. Mathematically this is:

$$f_{\text{full power}} = \frac{S_r}{2\pi V_{\text{rated}}} \quad (12)$$

The full power bandwidth of a programmable amplifier such as the LM4250 varies with the master bias set current.

The above analysis of sine wave and step voltage amplifier responses applies for all single dominant pole op amps such as the LM101A, LM1107, LM108A, LM112, LM118, and LM741 as well as the LM4250 programmable op amp.

500 MANO-WATT X10 AMPLIFIER

The X10 inverting amplifier shown in *Figure 7* demonstrates the low power capability of the LM4250 at extremely low values of supply voltage and set current. The circuit draws 260 nA from the +1.0V supply of which 50 nA flows through the 12 MΩ set resistor. The current into the −1.0V supply is only 210 nA since the set resistor is tied to ground rather than V^-. Total quiescent power dissipation is:

$$P_D = (260\ \text{nA})\ (1\text{V}) + (210\ \text{nA})\ (1\text{V}) \quad (13)$$

$$P_D = 470\ \text{nW} \quad (14)$$

The slew rate determined from the data sheet typical performance curve is 1 V/ms for a .05 μA set current. Samples of actual values observed were 1.2 V/ms for the negative slew rate and 0.85 V/ms for the positive slew rate. This difference occurs due to the non-symmetry in the current sources used for charging and discharging the internal 30 pF compensation capacitor.

The 3 dB down (gain of −7.07) frequency observed for this configuration was approximately 300 Hz which agrees fairly closely with the 3.5 kHz GBWP divided by 10 taken from an extrapolation of the data sheet typical GBWP versus set current curve.

Peak-to-peak output voltage swing into a 100 kΩ load is 0.7V or ±0.35V peak. An increase in supply voltage to ±1.35V such as delivered by a pair of mercury cells directly increases the output swing by ±0.35V to 1.4V peak-to-peak. Although this increases the power dissipation to approximately 1 μW per battery, a power drain of 15 μW or less will not affect the shelf life of a mercury cell.

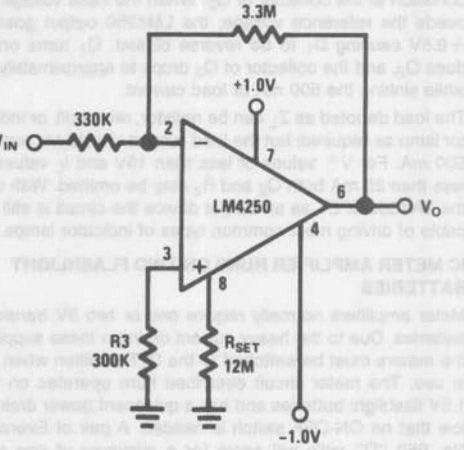

FIGURE 7. 500 nW x 10 Amplifier

MICRO-POWER MONITOR WITH HIGH CURRENT SWITCH

Figure 8 shows the combination of a micro-power comparator and a high current switch run from a separate supply. This circuit provides a method of continuously monitoring an input voltage while dissipating only 100 μW of power and still being capable of switching a 500 mA load if the input exceeds a given value. The reference voltage can be any value between +8.5V and −8.5V. With a minimum gain of approximately 100,000 the comparator can resolve input voltage differences down into the 0.2 mV region.

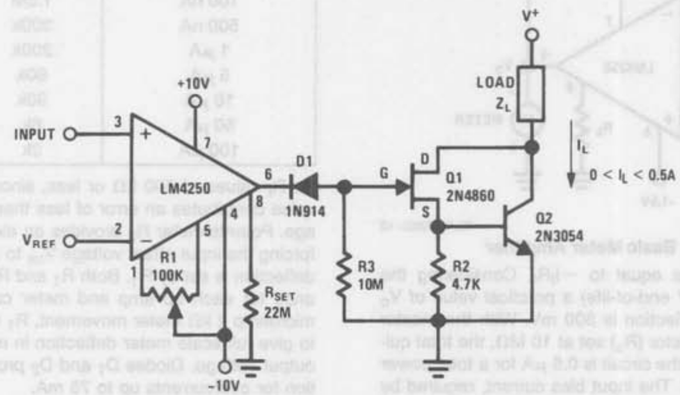

FIGURE 8. μ−Power Comparator with High Current Switch

offset nulling capability for high accuracy applications. When the input voltage is less than the reference voltage, the output of the LM4250 is at approximately −9.5V causing diode D_1 to conduct. The gate of Q_1 is held at −8.8V by the voltage developed across R_3. With a large negative voltage on the gate of Q_1 it turns off and removes the base drive from Q_2. This results in a high voltage or open switch condition at the collector of Q_2. When the input voltage exceeds the reference voltage, the LM4250 output goes to +9.5V causing D_1 to be reverse biased. Q_1 turns on as does Q_2, and the collector of Q_2 drops to approximately 1V while sinking the 500 mA of load current.

The load denoted as Z_L can be resistor, relay coil, or indicator lamp as required; but the load current should not exceed 500 mA. For V^+ values of less than 15V and I_L values of less than 25 mA both Q_2 and R_2 may be omitted. With only the 2N4860 JFET as an output device the circuit is still capable of driving most common types of indicator lamps.

IC METER AMPLIFIER RUNS ON TWO FLASHLIGHT BATTERIES

Meter amplifiers normally require one or two 9V transistor batteries. Due to the heavy current drain on these supplies, the meters must be switched to the OFF position when not in use. The meter circuit described here operates on two 1.5V flashlight batteries and has a quiescent power drain so low that no ON-OFF switch is needed. A pair of Eveready No. 950 "D" cells will serve for a minimum of one year without replacement. As a DC ammeter, the circuit will provide current ranges as low as 100 nA full-scale.

The basic meter amplifier circuit shown in *Figure 9* is a current-to-voltage converter. Negative feedback around the amplifier insures that currents I_{IN} and I_f are always equal, and the high gain of the op amp insures that the input voltage between Pins 2 and 3 is in the microvolt region. Output

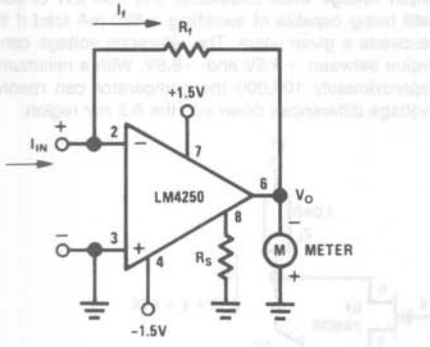

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FIGURE 9. Basic Meter Amplifier

voltage V_o is therefore equal to $-I_fR_f$. Considering the ±1.5V sources (±1.2V end-of-life) a practical value of V_o for full scale meter deflection is 300 mV. With the master bias-current setting resistor (R_s) set at 10 MΩ, the total quiescent current drain of the circuit is 0.6 μA for a total power supply drain of 1.8 μW. The input bias current, required by the amplifier at this low level of quiescent current, is in the range of 600 pA.

nulling for minimum offset voltage. Resistor R'_f (equal in value to R_f for measurements of less than 1 μA) insures that the input bias currents for the two input terminals of the amplifier do not contribute significantly to an output error voltage. The output voltage V_o for the differential current-to-voltage converter is equal to $-2\,I_fR_f$ since the floating input current I_{IN} must flow through R_f and R'_f. R'_f may be omitted

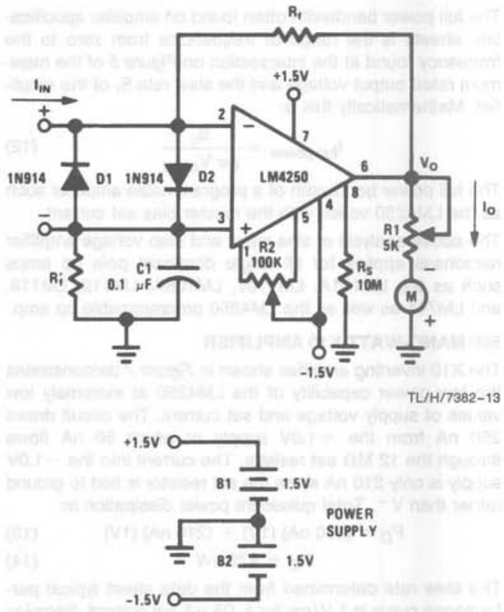

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FIGURE 10. Complete Meter Amplifier

Resistance Values for DC Nano and Micro Ammeter

I FULL SCALE	R_f [Ω]	R'_f [Ω]
100 nA	1.5M	1.5M
500 nA	300k	300k
1 μA	300k	0
5 μA	60k	0
10 μA	30k	0
50 μA	6k	0
100 μA	3k	0

for R_f values of 500 kΩ or less, since a resistance of this value contributes an error of less than 0.1% in output voltage. Potentiometer R_2 provides an electrical meter zero by forcing the input offset voltage V_{os} to zero. Full scale meter deflection is set by R_1. Both R_1 and R_2 only need to be set once for each op amp and meter combination. For a 50 microamp 2 kΩ meter movement, R_1 should be about 4 kΩ to give full scale meter deflection in response to a 300 mV output voltage. Diodes D_1 and D_2 provide full input protection for overcurrents up to 75 mA.

With an R_f resistor value of 1.5M the circuit in *Figure 10* becomes a nanommeter with a full scale reading capability of 100 nA. Reducing R_f to 3 kΩ in steps, as shown in *Figure 10* increases the full scale deflection to 100 μA, the maximum for this circuit configuration. The voltage drop across the two input terminals is equal to the output voltage V_o divided by the open loop gain. Assuming an open loop gain of 10,000 gives an input voltage drop of 30 μV or less.

CIRCUIT FOR HIGHER CURRENT READINGS

For DC current readings higher than 100 μA, the inverting amplifier configuration shown in *Figure 11* provides the required gain. Resistor R_A develops a voltage drop in response to input current I_A. This voltage is amplified by a factor equal to the ratio of R_f/R_B. R_B must be sufficiently larger than R_A, so as not to load the input signal. *Figure 11* also shows the proper values of R_A, R_B and R_f for full scale meter deflections of from 1 mA to 10A.

Resistance Values for DC Ammeter

I FULL SCALE	R_A [Ω]	R_B [Ω]	R_f [Ω]
1 mA	3.0	3k	300k
10 mA	.3	3k	300k
100 mA	.3	30k	300k
1A	.03	30k	300k
10A	.03	30k	30k

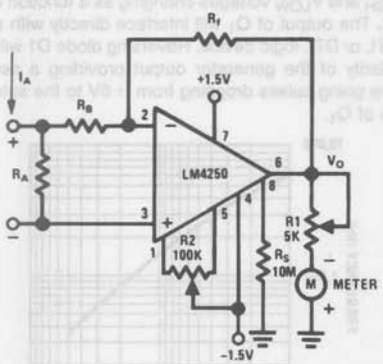

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FIGURE 11. Ammeter

A 10 mV TO 100V FULL-SCALE VOLTMETER

A resistor inserted in series with one of the input leads of the basic meter amplifier converts it to a wide range voltmeter circuit, as shown in *Figure 12*. This inverting amplifier has a gain varying from −30 for the 10 mV full scale range to −0.003 for the 100V full scale range. *Figure 12* also lists the proper values of R_V, R_f, and R'_f for each range. Diodes D_1 and D_2 provide complete amplifier protection for input overvoltages as high as 500V on the 10 mV range, but if overvoltages of this magnitude are expected under continuous operation, the power rating of R_V should be adjusted accordingly.

Resistance Values for a DC Voltmeter

V FULL SCALE	R_V [Ω]	R_f [Ω]	R'_f [Ω]
10 mV	100k	1.5M	1.5M
100 mV	1M	1.5M	1.5M
1V	10M	1.M	1.5M
10V	10M	300k	0
100V	10M	30k	0

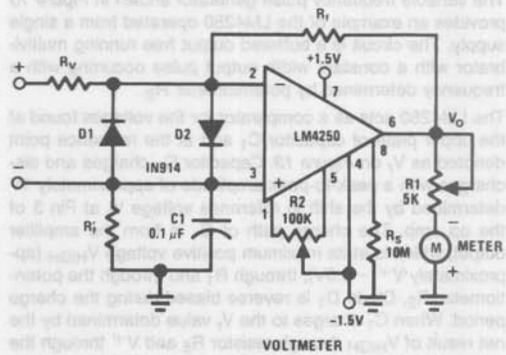

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FIGURE 12. Voltmeter

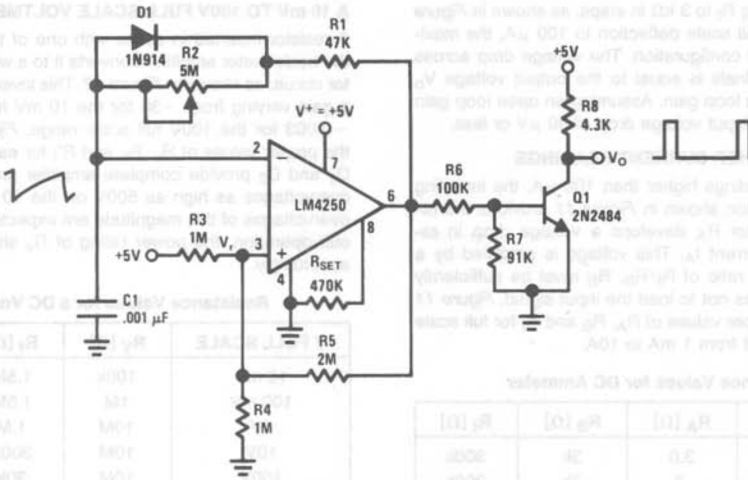


FIGURE 13. Pulse Generator

LOW FREQUENCY PULSE GENERATOR USING A SINGLE +5V SUPPLY

The variable frequency pulse generator shown in *Figure 13* provides an example of the LM4250 operated from a single supply. The circuit is a buffered output free running multivibrator with a constant width output pulse occurring with a frequency determined by potentiometer R_2.

The LM4250 acts as a comparator for the voltages found at the upper plate of capacitor C_1 and at the reference point denoted as V_r on *Figure 13*. Capacitor C_1 charges and discharges with a peak-to-peak amplitude of approximately 1V determined by the shift in reference voltage V_r at Pin 3 of the op amp. The charge path of C_1 is from the amplifier output, which is at its maximum positive voltage V_{HIGH} (approximately $V^+ - 0.5V$), through R_1 and through the potentiometer R_2. Diode D_1 is reverse biased during the charge period. When C_1 charges to the V_r value determined by the net result of V_{HIGH} through resistor R_5 and V^+ through the voltage divider made up of resistors R_3 and R_4 the amplifier swings to its lower limit of approximately 0.5V causing C_1 to begin discharging. The discharge path is through the forward biased diode D_1, through resistor R_1, and into Pin 6 of the op amp. Since the impedance in the discharge path does not vary for R_2 settings of from 3 kΩ to 5 MΩ, the output pulse maintains a constant pulse width of 41 µs ±1.5 µs over this range of potentiometer settings. *Figure 14* shows the output pulse frequency variation from 6 kHz down to 360 Hz as R_2 places from 100 kΩ up to 5 MΩ of additional resistance in the charge path of C_1. Setting R_2 to zero ohms will short out diode D_1 and cause a symmetrical square wave output at a frequency of 10 kHz. Increasing the value of C_1 will lower the range of frequencies available in response to the R_2 variation shown on *Figure 14*. Electrolytic capacitors may be used for the larger values of C_1 since it has only positive voltages applied to it.

The output buffer Q_1 presents a constant load to the op amp output thereby preventing frequency variations caused by V_{HIGH} and V_{LOW} voltages changing as a function of load current. The output of Q_1 will interface directly with a standard TTL or DTL logic device. Reversing diode D1 will invert the polarity of the generator output providing a series of negative going pulses dropping from +5V to the saturation voltage of Q_1.

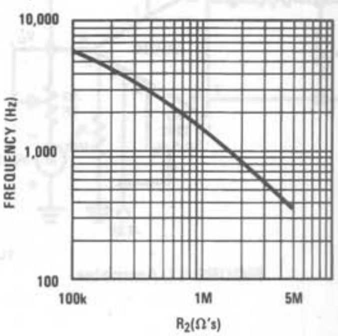
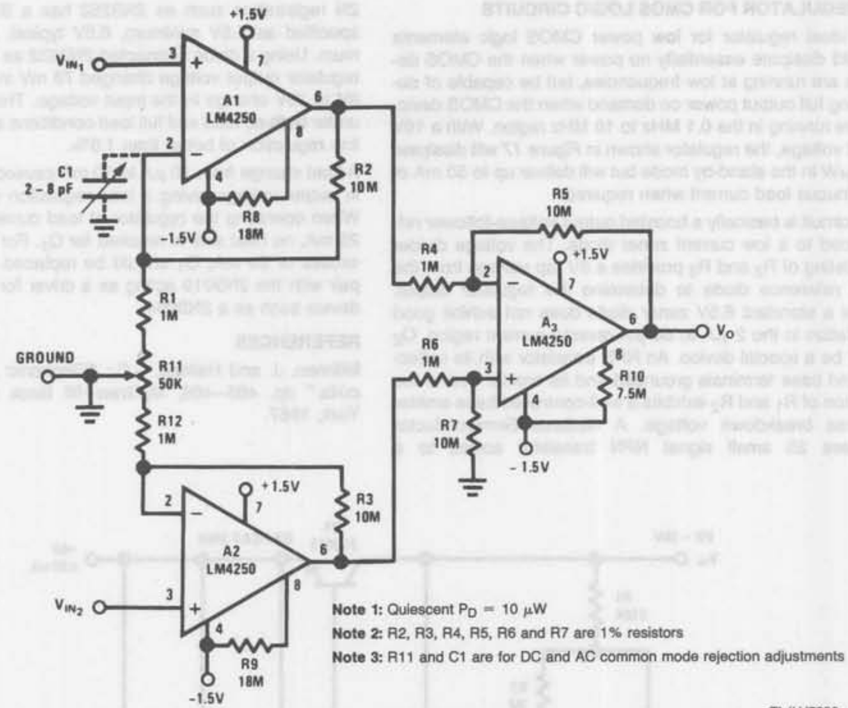


FIGURE 14. Pulse Frequency vs R_2

The change in output frequency as a function of supply voltage is less than ±4% for a V^+ change of from 4V to 10V. This stability of frequency versus supply voltage is due to the fact that the reference voltage V_r and the drive voltage for the capacitor are both direct functions of V^+.

The power dissipation of the free running multivibrator is 300 µW and the power dissipation of the buffer circuit is approximately 5.8 mW.



Note 1: Quiescent P_D = 10 μW

Note 2: R2, R3, R4, R5, R6 and R7 are 1% resistors

Note 3: R11 and C1 are for DC and AC common mode rejection adjustments

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FIGURE 15. × 100 Instrumentation Amplifier

X100 INSTRUMENTATION AMPLIFIER

The instrumentation amplifier circuit shown in *Figure 15* has a full differential input center tapped to ground. With the bias current set at approximately 0.1 μA, the impedance looking into either V_{IN_1} or V_{IN_2} is 100 MΩ with respect to ground, and the input bias current at either terminal is 0.2 nA. The two non-inverting input stages A_1 and A_2 apply a gain of 10 to the input signal, and the differential output stage applies an additional gain of −10 for a net amplifier gain of −100:

$$V_O = -100(V_{IN_1} - V_{IN2}). \qquad (15)$$

The entire circuit can run from two 1.5V batteries connected directly (no power switch) to the V^+ and V^- terminals. With a total current drain of 2.8 μA the quiescent power dissipation of the circuit is 8.4 μW. This is low enough to have no significant effect on the shelf life of most batteries.

Potentiometer R_{11} provides a means for matching the gains of A_1 and A_2 to achieve maximum DC common mode rejection ratio CMRR. With R_{11} adjusted to its null point for DC common mode rejection the small AC CMRR trimmer capacitor C_1 will normally give an additional 10 to 20 dB of CMRR over the operating frequency range. Since C_1 actually balances wiring capacitance rather than amplifier frequency characteristics, it may be necessary to attach it to Pin 2 of either A_1 or A_2 as required. *Figure 16* shows the variation of CMRR (referred to the input) with frequency for this configuration. Since the circuit applies a gain of 100 or 40 dB to an input signal, the actual observed rejection ratio is the difference between the CMRR curve and A_V curve. For example, a 60 Hz common mode signal will be attenuated by 67 dB minus 40 db or 27 dB for an actual rejection ratio of V_{IN}/V_O equal to 22.4.

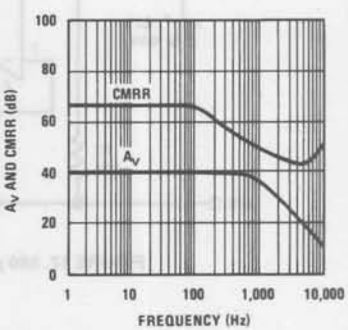

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FIGURE 16. A_V and CMRR vs Frequency

The maximum peak-to-peak output signal into a 100 kΩ load resistor is approximately 1.8V. With no input signal, the noise seen at the output is approximately 0.8 mV_{RMS} or 8 μV_{RMS} referred to the input. When doing power dissipation measurements on this circuit, it should be kept in mind that even a 1 MΩ oscilloscope probe placed between +1.5V and −1.5V will more than double the power drawn from the batteries.

5V REGULATOR FOR CMOS LOGIC CIRCUITS

The ideal regulator for low power CMOS logic elements should dissipate essentially no power when the CMOS devices are running at low frequencies, but be capable of delivering full output power on demand when the CMOS devices are running in the 0.1 MHz to 10 MHz region. With a 10V input voltage, the regulator shown in *Figure 17* will dissipate 350 μW in the stand-by mode but will deliver up to 50 mA of continuous load current when required.

The circuit is basically a boosted output voltage-follower referenced to a low current zener diode. The voltage divider consisting of R_2 and R_3 provides a 5V tap voltage from the 6.5V reference diode to determine the regulator output. Since a standard 6.5V zener diode does not exhibit good regulation in the 2 μA to 60 μA reverse current region, Q_2 must be a special device. An NPN transistor with its collector and base terminals grounded and its emitter tied to the junction of R_1 and R_2 exhibits a well-controlled base emitter reverse breakdown voltage. A National Semiconductor process 25 small signal NPN transistor sorted to a 2N registration such as 2N3252 has a BV_{EBO} at 10 μA specified as 5.5V minimum, 6.5V typical, and 7.0V maximum. Using a diode connected 2N3252 as a reference, the regulator output voltage changed 78 mV in response to an 8V to 36V change in the input voltage. This test was done under both no load and full load conditions and represents a line regulation of better than 1.6%.

A load change from 10 μA to 50 mA caused a 1 mV change in output voltage giving a load regulation value of 0.05%. When operating the regulator at load currents of less than 25 mA, no heat sink is required for Q_1. For load currents in excess of 50 mA, Q_1 should be replaced by a Darlington pair with the 2N3019 acting as a driver for a higher power device such as a 2N3054.

REFERENCES

Millman, J. and Halkias, C.C.: *"Electronic Device and Circuits,"* pp. 465–466, McGraw-Hill Book Company, New York, 1967.

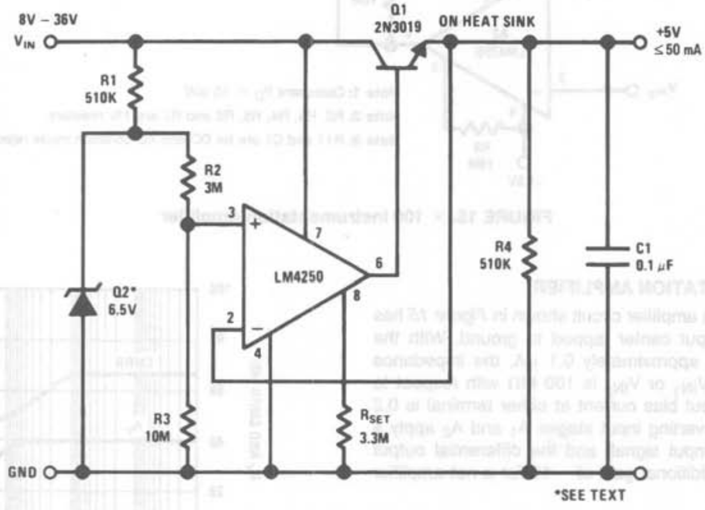

FIGURE 17. 350 μW Quiescent Drain 5 Volt Regulator