Understanding the 567 Tone Decoder

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Synchronization of the horizontal and vertical sweep in television receivers and transmitted sync pulses were the first wide-spread uses of phase-locked loops back in the 1940s. Such circuits carried the names "Synchro-Lock" and "Synchro-Guide." Since that time, the phase-locked loop is an extremely versatile circuit that is used for frequency comparison and synchronization, frequency multiplication and division, frequency-to-voltage conversion (FM demodulation), frequency shifting and AM demodulation. The basic phase-locked loop circuit consists of an analog multiplier, a low-pass filter, and a voltage controlled oscillator. The ability to insert various components into the feedback loop before or after the VCO gives it the versatility of a variety of circuit applications as previously mentioned. The phase-locked loop circuit that is quite versatile in terms of circuit applications is the 567 Tone Decoder IC. This phase-locked loop circuit is capable of responding to a specific tone of a constant input frequency within its bandwidth. Basically, the 567 is a circuit capable of detecting a frequency that is equal to its free running or center frequency and locking on to that frequency.

In the following paragraphs the design, construction and circuit applications will be explored. At the end of the discussion, an experiment will be described in a step-by-step procedure so that the theory can best be comprehended by the reader through the use of hands-on experimentation.

Chip Construction and Configuration

As mentioned in the introduction, the 567 device is a phase-locked loop system designed specifically to respond to a given tone of constant input frequency within its bandwidth. The bandwidth is a percentage of the constant input frequency and is expressed in a mathematical equation which will be defined later. The 567 phase-locked loop chip contains a phase detector, two driver amplifiers, a quadrature phase detector, and a current controlled oscillator. Upon the IC detecting an input signal, if the signal level at the lock frequency is sufficiently high, the driver amplifier turns on providing load drive capability up to 200 mA. When an "inband" tone is present above the required minimum level, the 567 chip will provide an output whose voltage level depends upon the circuit supply voltage. The output signal is provided by an uncommitted transistor incorporated into the driver amplifier (pin 8) of the IC. When the transistor saturates due to an inband signal present at pin 3, its collector voltage is less than 1 volt (typically 0.6 volts) providing an output drive capability up to 200 mA. Figure 1. illustrates the block diagram of the 567 Tone Decoder phase-locked loop IC.

Resistor R_1 should be between 2KΩ and 20KΩ for best temperature stability. The capacitor C_2 is the low-pass element for the chip. Capacitor C_3 value is generally non-critical because it sets the band edge of the low-pass filter portion of the chip. Besides setting the band edge of the low-pass filter, the C_3 capacitor attenuates frequencies outside the detection band to eliminate spurious outputs. If C_3 is too small, frequencies just outside the detection band will switch the output stage on and off at the beat frequency or the output may pulse on and off during the turn on transient. If C_3 is too large in value, turn on and turn off of the output stage will be delayed until the voltage on C_3 passes the threshold voltage.

Design Equations and Limitations

The following equations are used in identifying design parameters which dictate the circuit performance of the 567 PLL IC.

Center Frequency is approximately equal to:

$f_o \approx 1.1 / R_1C_1$

where R_1 should be between 2kΩ and 20KΩ.

$C_2 = V_{in} / (1070/BW)^2$ in μF).

where $v_{in} \approx$ 100 MV. (input Volts V_{in})

BW (Bandwidth) is approximately equal to:

BW ≈ 1070 SQR(V_{in} / f_0C_2) in which BW is a % of f_0. Note: SQR means square root.

Design Example:

Design a Guitar Tuning Aid to decode an 82.4 Hz ("E" note) using a 567 Tone Decoder Chip. Input signal level is 100mV.

Solution:

Picking C_1 to be 4.7 µF, R_1 equals:

$R_1 = 1.1 / f_0C_1$

$= 1.1 / (82.4 \times 4.7\mu F)$

$= 2.8K\Omega$, use a 2.7KΩ resistor.

$C_2 = (V_{in} / f_0) \times (1070 / 12\%)^2$

$= (100\ mV / 82.4\ Hz) \times (1070 / 12\%)^2$

$= 9.65\ \mu F$, use a 10 µF capacitor.

C_3 equals 2 x C_2 which equals:

2 x 9.65 = 19.3µF, use a 22 µF capacitor.

Figure 2 is the completed circuit for a Guitar Tuning Aid.

Design Limitations

As discussed previously, the value of R_1 should be between 2KΩ and 20KΩ for best temperature stability. The 567 IC has an input decoding range of 0.1 Hz through 500KHz. The value of C_3 shouldn't be too small or too large where the output will not switch on and off at the beat frequency or the output switching will be delayed until the voltage on C_3 passes the threshold voltage respectively. Due to the high switching speeds (20nS) associated with the 567 operation, care should be taken in lead routing. Lead lengths should be kept to a minimum. Another factor which must be considered is the effect of load energization on the power supply. For example, an incandescent lamp or dc motor typically draws 10 times the rated current at turn on. This can cause supply voltage fluctuations which could, for example, shift the detection band of narrow band systems sufficiently to cause momentary loss of lock. The result is a low frequency oscillation into and out of lock. Such effects can be prevented by supplying heavy load currents from a separate supply.

Applications

Although there are numerous applications in which the 567 Tone Decoder IC can be used, the two most popular ones are a Tone Decoder and a Frequency Indicator.

The Touch Tone™ application of the 567 is used for decoding Dual Tone, Multiple Frequency (DTMF) signals. These DTMF or Touch Tone signals are coded in tone pairs using two of seven possible tones or numbers 0 through 9, and the symbols # (pound) and * (star). The listing in Table 1 shows the audio frequencies used in the system. The basic decoder circuit for a single digit or symbol is shown in Figure 3. Note in the circuit that two 567 decoders are needed to represent the number 9. A low tone of 852 Hz and a high tone of 1477 Hz are required for correct tone detection. When the Touch Tone signal corresponding to the number is detected at the input of the circuit, the output of both decoders will be at logic 0 signifying both PLLs are locked. The output of the NOR Gate will be at logic 1. If the NOR Gate's output is at logic 0, this represents the number 9 input was initiated by the user. If you have not already guessed it, this circuit describes how a Touch Tone telephone keypad functions. To create a partial telephone keypad, a circuit consisting of 12 NOR Gates and 7 PLLs would be required. Figure 4 illustrates such a system.

The construction of a low cost frequency indicator is a novel application for the 567 IC shown in Figure 5. The decoder labelled (A) is set approximately 6% above the desired frequency, while the other decoder labelled (B) is set 6% below. If the input frequency is within 13% of the desired frequency, either lamp No. 1 or lamp No. 2 will come on. If both are on, then the frequency is within 1% of the desired frequency.

A Demonstration of the 567 Circuit Operation Through Experimentation

Objective

The objective of this experiment is to demonstrate the operation of the 567 phase-locked loop Tone Decoder IC.

1. Wire the circuit shown in the schematic diagram of Figure 6. Apply power to the circuit and adjust the frequency generator for 60Hz output signal with a 2 volt peak-to-peak signal level. The LED should not be lit at this time.
2. Slowly decrease the input frequency until the LED lights, and record this frequency:
   f_1 = _____ Hz
3. Slowly continue to increase the input frequency until the LED goes out and record this frequency:
   f_2 = _____ Hz
4. Set the input frequency at about 40 Hz. Slowly increase the input frequency until the LED lights and record this frequency:
   f_3 = _____ Hz
5. Slowly decrease the input frequency until the LED goes out and record this frequency:
   f_4 = _____ Hz
6. Now set the input frequency at approximately 40Hz and measure the frequency at pin 5 of the 567 integrated circuit, which is the vco free running frequency, f_0. Record your result:
   f_0 = _____ Hz

From the measurements of Steps 2 through 6, you have determined the range of frequencies for which the 567 tone decoder will lock. Decreasing frequencies will occur at f_1 and will stay locked until the input frequency reaches f_2. On increasing frequencies, lock will occur at f_3 and will stay locked until the input frequency equals f_4. The **free running frequency** f_0 is determined by the 18KΩ resistor (R_1) and the 1µF capacitor (C_1) according to the approximate equation: $f_0 \approx 1.1 / R_1C_1$ which is about 61 Hz. Within 10%, this should agree with the values just determined. The % bandwidth is found from: % bandwidth (BW) = $(f_2\text{-}f_4/f_0) \times 100$.

From your results, compute the % bandwidth and record your result:

% BW = _____

For the 567 Tone Decoder, the % BW is typically 14%. The frequency range, f_2 - f_4 is the **lock range** of the decoder phase-locked loop, and is sometimes referred to as the **bandwidth**. The fre-

quency range, $f_3 - f_1$ is the **loop capture range** and is never greater than the lock range.

7. From the values you determined in Steps 3, 4, and 5, compute the lock range (f_2-f_4) and the capture range (f_3-f_1) for this 567 Tone Decoder circuit and record your results:
lock range = _____
Hz, capture range = _____ hz

GLOSSARY of TERMS

Center Frequency (f_0) - The free running frequency of the current controlled oscillator (CCO) in the absence of an input signal.

Detection Bandwidth (BW) - The frequency range, centered about f_0, within which an input signal above the threshold voltage (typically 20mV rms) will cause a logical zero state on the output. The detection bandwidth corresponds to the loop capture range.

Largest Detection Bandwidth - The largest frequency range within which an input signal above the threshold voltage will cause a logical zero state on the output. The maximum detection bandwidth corresponds to the loop lock range.

Detection Bandskew - A measure of how well the largest detection band is centered about center frequency, f_0. The skew is defined as the $(f_{max}+f_{min=0}) / f_0$ where f_{max} and f_{min} are the frequencies corresponding to the edges of the detection band. The skew can be to zero if necessary by means of an optional adjustment. ❐

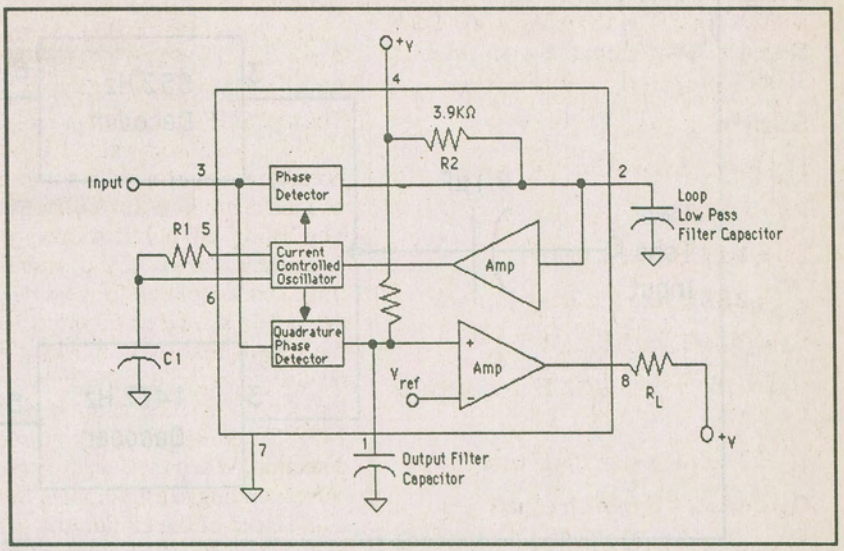

Figure 1.
Block Diagram Of The 567 Tone Decoder Phase Locked Loop

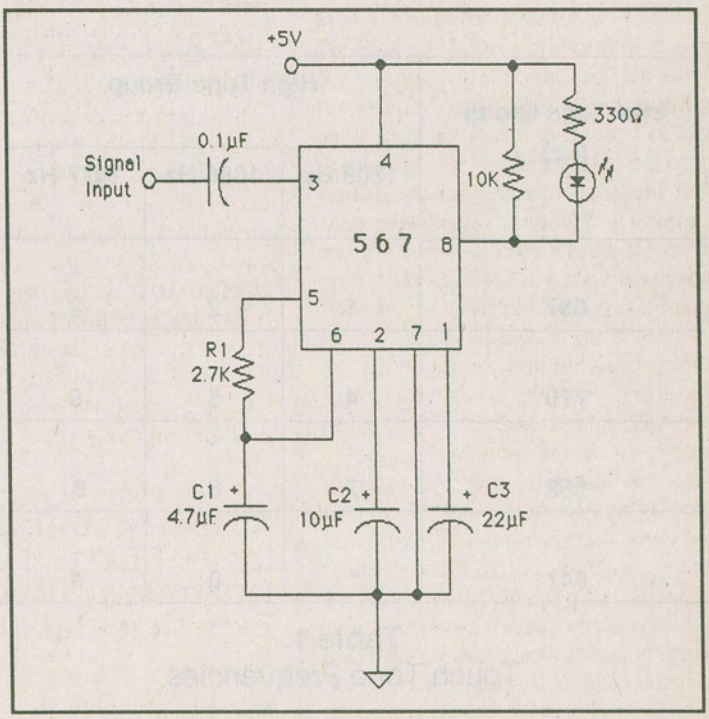

Figure 2.
An Electronic Guitar Tuning Aid Using The 567

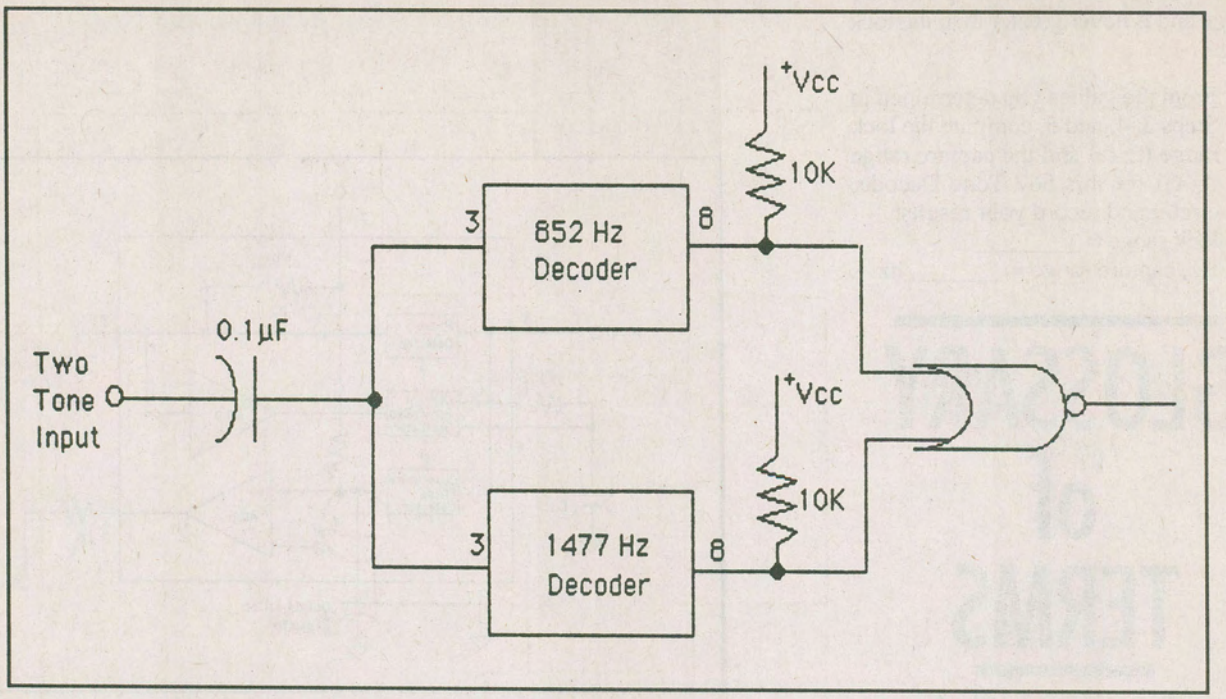

Figure 3.
Touch-Tone Decoder For The Number 9

Low Tone Group (Hz)	High Tone Group		
	1209 Hz	1336 Hz	1477 Hz
697	1	2	3
770	4	5	6
852	7	8	9
941	*	0	#

Table 1.
Touch Tone Frequencies

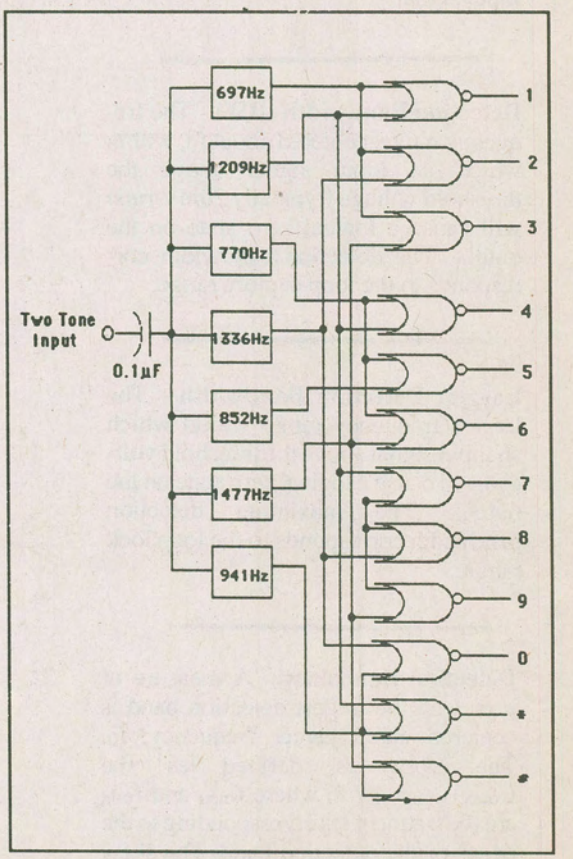

Figure 4.
A 12 Digit Touch-Tone Decoder Circuit

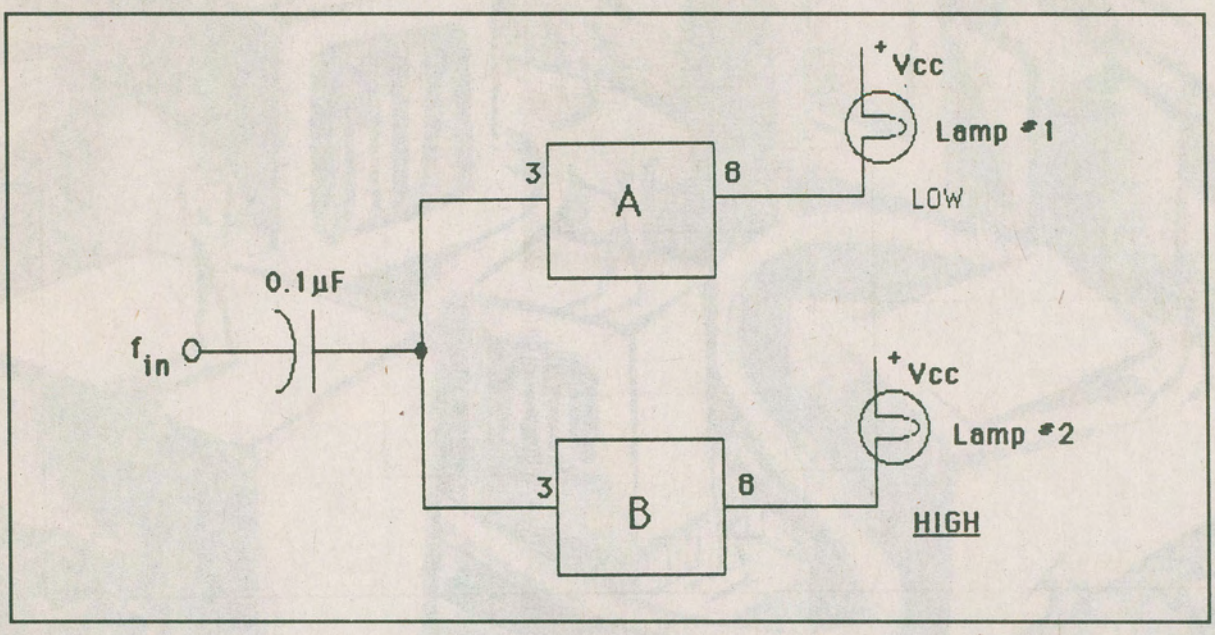

Figure 5.
A Simple Frequency Indicator

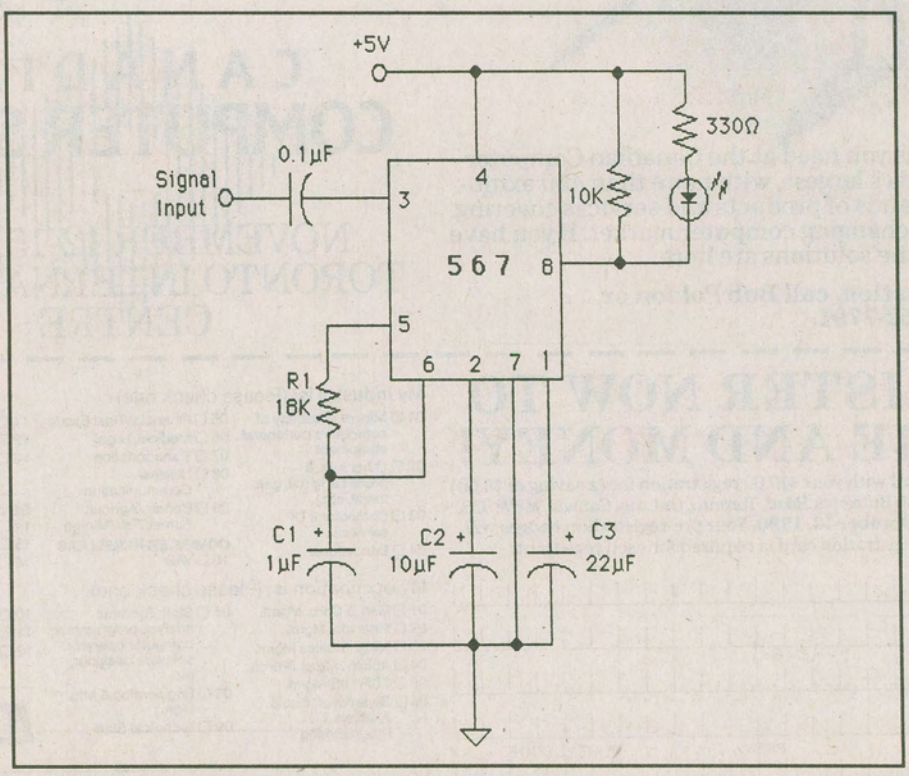

Figure 6.
A 567 Phase-Locked Loop Tone Decoder