Basic Design Considerations

Solid-state devices are small but versatile units that can perform a great variety of control functions in electronic equipment. Like other electron devices, they have the ability to control almost instantly the movement of charges of electricity. They are used as rectifiers, detectors, amplifiers, oscillators, electronic switches, mixers, and modulators.

In addition, solid-state devices have many important advantages over other types of electron devices. They are very small and light in weight. They have no filaments or heaters, and therefore require no heating power or warm-up time. They consume very little power. They are solid in construction, extremely rugged, free from microphonics, and can be made impervious to many severe environmental conditions.

SEMICONDUCTOR MATERIALS

Unlike some electron devices, which depend on the flow of electric charges through a vacuum or a gas, solid-state devices make use of the flow of current in a solid. In general, all materials may be classified into three major categories—conductors, semiconductors, and insulators—depending upon their ability to conduct an electric current. As the name indicates, a semiconductor material has poorer conductivity than a conductor, but better conductivity than an insulator.

The material most often used in semiconductor devices is silicon. Germanium has higher electrical conductivity (less resistance to current flow) than silicon, and has been used in the past in many low- and medium-power diodes and transistors. Silicon is more suitable for higher power devices than germanium. One reason is that it can be used at much higher temperatures. In general, silicon is preferred over germanium because silicon processing techniques yield more economical devices. As a result, silicon has superseded germanium in almost every type of application, including the small-signal area.

Resistivity

The ability of a material to conduct current (conductivity) is directly proportional to the number of free (loosely held) electrons in the material. Good conductors, such as silver, copper, and aluminum, have large numbers of free electrons; their resistivities are of the order of a few millionths of an ohm-centimeter. Insulators such as glass, rubber, and mica, which have very few loosely held electrons, have resistivities as high as several million ohm-centimeters.

Semiconductor materials lie in the range between these two extremes, as shown in Fig. 1. Pure germanium has a resistivity of 60 ohm-centimeters. Pure silicon has a considerably higher resistivity, in the order of 60,000 ohm-centimeters. As used in solid-state devices, however, these materials contain carefully controlled amounts of certain impurities which reduce their resistivity from a low of less than one to greater than 50 ohm-centimeters at room temperature (this resistivity decreases rapidly as the temperature rises).

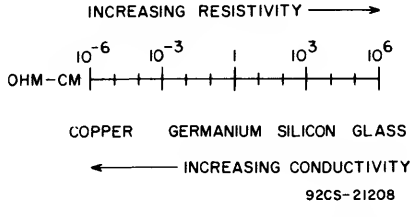

Fig. 1 - Resistivity of typical conductor, semiconductor, and insulator.

Impurities

Carefully prepared semiconductor materials have a crystal structure. In this type of structure, which is called a lattice, the outer or valence electrons of individual atoms are tightly bound to the electrons of adjacent atoms in electron-pair bonds, as shown in Fig. 2. Because such a structure has no loosely held

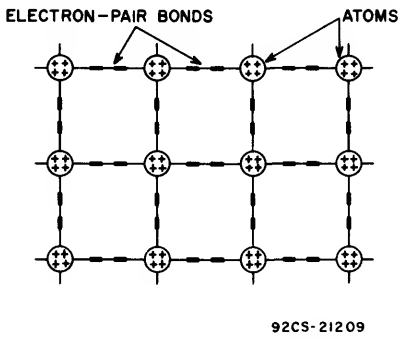

Fig. 2 - Crystal lattice structure.

electrons, semiconductor materials are normally poor conductors. One way to separate the electron-pair bonds and provide free electrons for electrical conduction would be to apply high temperature or strong electric fields to the material.

Another way to alter the lattice structure and thereby obtain free electrons, however, is to add small amounts of other elements having a different atomic structure. By the addition of almost infinitesimal amounts of such other elements, called **impurities**, the basic electrical properties of pure semiconductor materials can be modified and controlled. The ratio of impurity to the semiconductor material is usually extremely small, in the order of one part in ten million.

When the impurity elements are added to the semiconductor material, impurity atoms take the place of semiconductor atoms in the lattice structure.

When the impurity atom has one more valence electron than the semiconductor atom, this extra electron cannot form an electron-pair bond because no adjacent valence electron is available. The excess electron is then held very loosely by the atom, as shown in Fig. 3, and requires only slight excitation to break away. Consequently, the presence of such excess electrons makes the material a better conductor, i.e., its resistance to current flow is reduced.

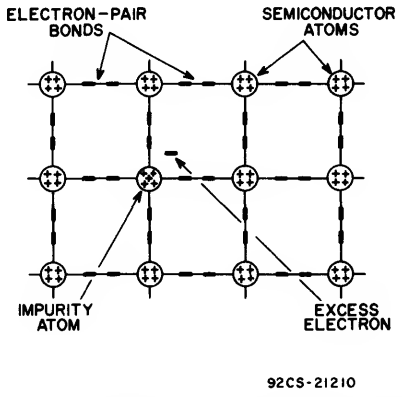

Fig. 3 - Lattice structure of n-type material.

Impurity elements which are added to silicon crystals to provide excess electrons include phosphorus, arsenic, and antimony. When these elements are introduced, the resulting material is called **n-type** because the excess free electrons have a negative charge. (It should be noted, however, that the negative charge of the electrons is balanced by an equivalent positive charge in the center of the impurity atoms. Therefore, the net electrical charge of the semiconductor material is not changed.)

A different effect is produced when an impurity atom having one less valence electron than the semiconductor atom is substituted in the lattice structure. As a result, a vacancy or **hole** exists in the lattice, as shown in Fig. 4. An

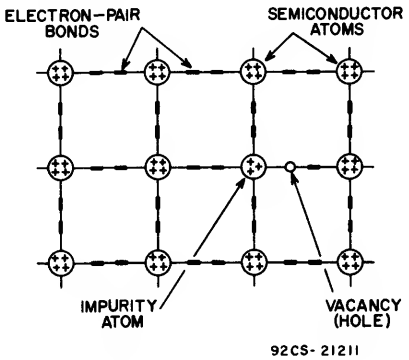

Fig. 4 - Lattice structure of p-type material.

electron from an adjacent electron-pair bond may then absorb enough energy to break its bond and move through the lattice to fill the hole. As in the case of excess electrons, the presence of holes encourages the flow of electrons in the semiconductor material;

consequently, the conductivity is increased and the resistivity is reduced.

The vacancy or hole in the crystal structure is considered to have a positive electrical charge because it represents the absence of an electron. (Again, however, the net charge of the crystal is unchanged.) Semiconductor material which contains these holes or positive charges is called **p-type** material. P-type materials are formed by the addition of boron, aluminum, gallium, or indium.

Although the difference in the chemical composition of n-type and p-type materials is slight, the differences in the electrical characteristics of the two types are substantial, and are very important in the operation of semiconductor devices.

JUNCTIONS

When n-type and p-type materials are joined together, as shown in Fig. 5, an unusual but

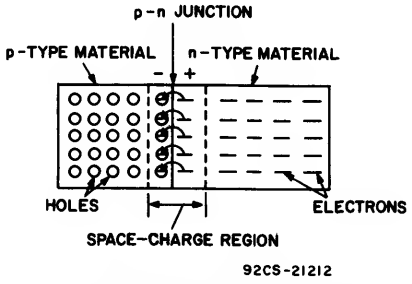

Fig. 5 - Interaction of holes and electrons at p-n junction.

very important phenomenon occurs at the interface where the two materials meet (called the **p-n junction**). An interaction takes place between the two types of material at the junction as a result of the holes in one material and the excess electrons in the other.

When a p-n junction is formed, some of the free electrons from the n-type material diffuse across the junction and recombine with holes in the lattice structure of the p-type material; similarly, some of the holes in the p-type material diffuse across the junction and recombine with free electrons in the lattice structure of the n-type material. This interaction or diffusion is brought into equilibrium by a small space-charge region (sometimes called the **transition region** or **depletion layer**). The p-type material thus acquires a slight negative charge and the n-type material acquires a slight positive charge.

Thermal energy causes charge carriers (electrons and holes) to diffuse from one side of the p-n junction to the other side; this flow of charge carriers is called **diffusion current**. As a result of the diffusion process, however, a potential gradient builds up across the space-charge region. This potential gradient can be represented, as shown in Fig. 6, by an imaginary battery connected across the p-n junction. (The battery symbol is used merely to illustrate internal effects; the potential it represents is not directly measurable.) The

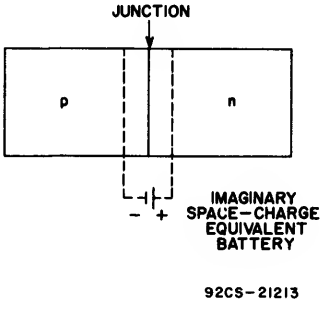

Fig. 6 - Potential gradient across space-charge region.

potential gradient causes a flow of charge carriers, referred to as **drift current**, in the opposite direction to the diffusion current. Under equilibrium conditions, the diffusion current is exactly balanced by the drift current so that the net current across the p-n junction is zero. In other words, when no external current or voltage is applied to the p-n junction, the potential gradient forms an **energy barrier** that prevents further diffusion of charge carriers across the junction. In effect, electrons from the n-type material that tend to diffuse across the junction are repelled by the slight negative charge induced in the p-type material by the potential gradient, and holes from the p-type material are repelled by the slight positive charge induced in the n-type material. The potential gradient (or energy barrier, as it is sometimes called), therefore, prevents total interaction between the two types of materials, and thus preserves the differences in their characteristics.

Current Flow

When an external battery is connected across a p-n junction, the amount of current flow is determined by the polarity of the

applied voltage and its effect on the space-charge region. In Fig. 7(a), the positive terminal of the battery is connected to the n-type material and the negative terminal to the p-type material. In this arrangement, the free electrons in the n-type material are attracted toward the positive terminal of the battery and away from the junction. At the same time, holes from the p-type material are attracted toward the negative terminal of the battery and away from the junction. As a result, the space-charge region at the junction becomes effectively wider, and the potential gradient increases until it approaches the potential of the external battery. Current flow is then extremely small because no voltage difference (electric field) exists across either the p-type or the n-type region. Under these conditions, the p-n junction is said to be **reverse-biased**.

In Fig. 7(b), the positive terminal of the external battery is connected to the p-type material and the negative terminal to the n-type material. In this arrangement, electrons in the p-type material near the positive terminal of the battery break their electron-pair bonds and enter the battery, creating new holes. At the same time, electrons from the negative terminal of the battery enter the n-type material and diffuse toward the junction. As a result, the space-charge region becomes effectively narrower, and the energy barrier decreases to an insignificant value. Excess electrons from the n-type material can then penetrate the space-charge region, flow across the junction, and move by way of the holes in the p-type material toward the positive terminal of the battery. This electron flow continues as long as the external voltage is applied. Under these conditions, the junction is said to be **forward-biased**.

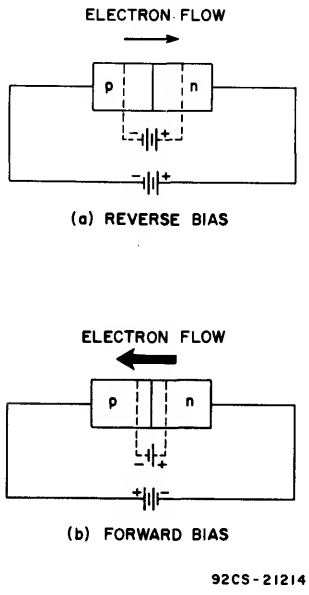

Fig. 7 - Electron current flow in biased p-n junctions.

The generalized voltage-current characteristic for a p-n junction in Fig. 8 shows both the reverse-bias and forward-bias regions. In the

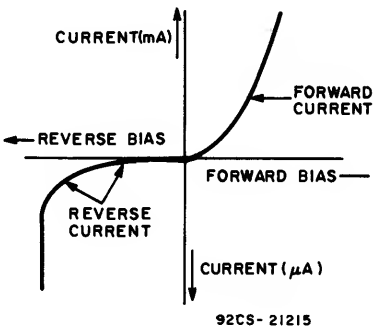

Fig. 8 - Voltage-current characteristic for a p-n junction.

forward-bias region, current rises rapidly as the voltage is increased and is relatively high. Current in the reverse-bias region is usually much lower. Excessive voltage (bias) in either direction is avoided in normal applications because excessive currents and the resulting high temperatures may permanently damage the solid-state device.

TRANSISTOR STRUCTURES

Fig. 7 shows that a p-n junction biased in the reverse direction is equivalent to a high-resistance element (low current for a given applied voltage), while a junction biased in the forward direction is equivalent to a low-resistance element (high current for a given applied voltage). Because the power developed by a given current is greater in a high-resistance element than in a low-resistance element ($P=I^2R$), power gain can be obtained in a structure containing two such resistance elements if the current flow is not materially reduced. A device containing two p-n junctions biased in opposite directions can operate in this fashion. The resulting device is called a transistor.

Such a two-junction device is shown in Figs. 9 and 10. The thick end layers are made of the same type of material (n-type in this case), and are separated by a very thin layer of the opposite type of material (p-type in the device shown). The three regions of the device are called the **emitter**, the **base**, and the **collector**, as shown in Fig. 10. By means of the external batteries, the left-hand (n-p) junction is biased in the forward direction to provide a low-resistance input circuit, and the right-hand (p-n) junction is biased in the reverse direction to provide a high-resistance output circuit.

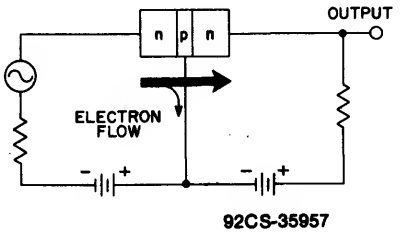

Fig. 9 - N-P-N structure biased for power gain.

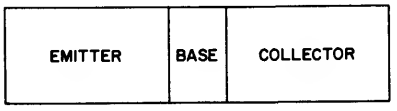

Fig. 10 - Functional diagram of transistor structure.

Electrons flow easily from the left-hand n-type region to the center p-type region as a result of the forward biasing. Most of these electrons diffuse through the thin p-type region, however, and are attracted by the positive potential of the external battery across the right-hand junction. In practical devices, approximately 95 to 99.5 per cent of the electron current reaches the right-hand n-type region. This high percentage of current penetration provides power gain in the high-resistance output circuit and is the basis for transistor amplification capability.

The operation of p-n-p devices is similar to that shown for the n-p-n device, except that the bias-voltage polarities are reversed, and electron-current flow is in the opposite direction. (In general, discussions of semiconductor theory assume that the "holes" in semiconductor material constitute the main charge carriers in p-n-p devices, and discuss "hole currents" for these devices and "electron currents" for n-p-n devices. The direction of hole current flow is considered to be the same as that of conventional current flow, which is assumed to travel through a circuit in a direction from the positive terminal of the external battery back to its negative terminal. This direction is opposite from that of electron flow, which travels from a negative to a positive terminal.)

Different symbols are used for n-p-n and p-n-p transistors to show the difference in the direction of current flow in the two types of devices. In the n-p-n transistor shown in Fig. 11(a), electrons flow from the emitter to the collector. In the p-n-p transistor shown in Fig. 11(b), electrons flow from the collector to the emitter. In other words, the direction of electron current is always opposite to that of the arrow on the emitter lead. The arrow indicates the direction of "conventional current flow" in the circuit.

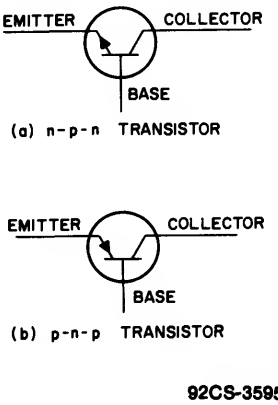

Fig. 11 - Schematic symbols for transistors.

The transistor can be used for a wide variety of control functions, including amplification, oscillation, switching, and frequency conversion. Power-transistor characteristics and ratings are discussed in the following pages.

The ultimate aim of all transistor fabrication techniques is the construction of two parallel p-n junctions with controlled spacing between the junctions and controlled impurity levels on both sides of each junction. A variety of structures and geometries have been developed in the course of transistor evolution.

In power transistors, structure refers to the junction depth, the concentration and profile of the impurities (doping), and the spacings of the various layers of the device. Geometry refers to the topography of the transistor. These factors and the method of assembly of the semiconductor pellet into the over-all transistor package have an important bearing on the types of applications in which a power transistor can be used to optimum advantage. The proper choices of trade-offs among these factors determine the gain, frequency, voltage, current, and dissipation capabilities of power transistors.

Various structures have been developed to provide different electrical, thermal, or cost properties, with each having certain advantages or compromises to offer. Table I lists the principal structures available for silicon power transistors, together with some of the advantages and disadvantages of each type. A brief description of each type of structure follows.

Table I—Types of Structures for Silicon Power Transistors

Structure	Advantages	Disadvantages
Hometaxial-base	Electrically rugged, low cost, good voltage rating	Low speed, low upper-voltage limit (150-200 V)
Double-diffused mesa	High speed	High saturation resistance
Double-diffused planar	Uniformity of device characteristics, high speed, low leakage	High saturation resistance
Triple-diffused	High speed, low saturation resistance	Moderate cost, moderate leakage
Triple-diffused planar	Very low leakage, high speed, low saturation resistance	Higher cost
Double-diffused epitaxial mesa	High speed, low saturation resistance	Moderate cost, moderate leakage, less rugged
Double-diffused epitaxial planar	High speed, low leakage, low saturation resistance	High cost, less rugged
Epitaxial-base mesa	High current-carrying capability, moderate speed, low saturation resistance	Low voltage, moderate leakage
Multiple-epitaxial-base mesa	Good current-handling capability, moderate speed, low saturation resistance, electronically rugged, high voltage	Moderate cost
Double-diffused multiple-epitaxial mesa	High speed, electronically rugged, low saturation resistance, high collector-junction voltage ratings	Moderate cost, moderate leakage
Darlington (double-epitaxial, single-diffused)	Moderate speed, high gain, high input impedance	High saturation resistance

Hometaxial-Base Transistors

Hometaxial-base transistors start with a wafer of moderately-high-resistivity silicon on which are deposited several thin layers of impurities. Then, under controlled temperature and ambient conditions, the impurities are driven deep into both sides of the silicon wafer. Early in the diffusion, the process is interrupted briefly, and a "mesa" or raised portion is selectively etched to define the emitter geometry. The process is complete when the deep diffused junctions are separated by a moderately wide (about 1 mil) base region. Fig. 12 shows a typical cross section of a completed single-diffused hometaxial transistor.

Double-Diffused Transistors

Double-diffused transistors start with a relatively high-resistivity silicon wafer on which a base dopant impurity is deposited. This dopant is then diffused to a shallow depth. Then, an oxide (S_iO_2) is selectively etched to define regions where an emitter impurity is to be deposited and diffused. The oxide acts as an effective mask against the diffusion of most of the usual impurity elements, such as boron or phosphorus. The emitter diffuses more rapidly than the base and, therefore, provides a means to narrow the base width until the desired electrical properties are obtained. The more rapid emitter diffusion results from a much higher impurity level, which enhances the diffusion coefficient as compared to that of the base diffusion. Fig. 13 shows a cross section of a typical double-diffused transistor.

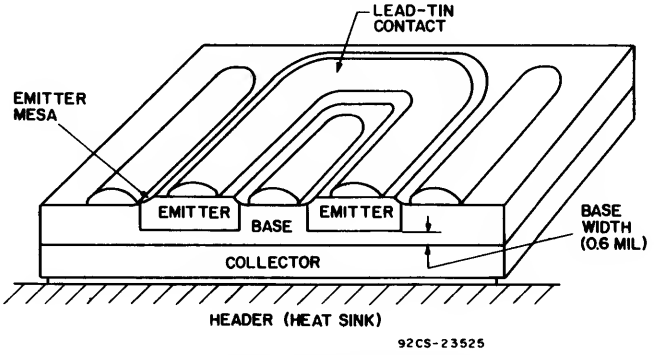

Fig. 12 - Hometaxial-base (single-diffused) transistor structure.

The chief advantages of the hometaxial-base transistors are good voltage ratings and excellent electronic ruggedness that permit these transistors to withstand repeated high-energy power pulses. Both advantages result from the very deep graded junctions and the wide base region. The graded junction provides a benefit of either higher voltage ratings with good saturation resistances, or much lower saturation resistances at a given voltage. The electronic ruggedness arises from the moderately wide, undiffused (homogeneous) base region which allows injected charge carriers to fan out and thereby reduce charge-carrier density at the collector junction where heating effects predominate. Another advantage is that the manufacturing cost per unit of power-handling capability is relatively low, primarily as a result of large-batch processing.

Hometaxial-base transistors have a relatively low switching-speed limit because of the moderately wide base spacing, and a low upper voltage limit of about 150 to 200 volts because of punch-through limitations.

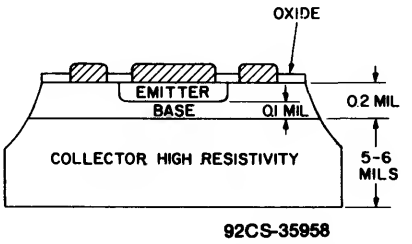

Fig. 13 - Double-diffused transistor structure.

The double-diffused structure differs from other designs in that the high-resistivity side of the collector-base junction is on the collector side; therefore, the collector voltage can be designed almost independent of the base width. The advantage of the double-diffused transistor is that very narrow non-homogeneous

or graded base widths are employed; the frequency responses of these devices, therefore, are orders of magnitude greater than those of earlier types of transistors. Double-diffused transistors, however, have a very high collector saturation resistance and relatively fragile junctions because of the thick high-resistivity collector and narrow graded base width.

Double-Diffused Planar Transistors

The double-diffused planar transistor is essentially identical to the double-diffused type with one modification in the manufacturing process. As shown in Fig. 14 the

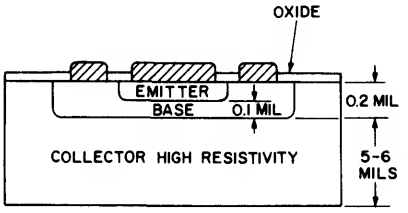

Fig. 14 - Double-diffused planar transistor structure.

collector-base junction terminates under a protective oxide layer at the surface of the silicon wafer instead of at the side. This requires one additional masking step for the base impurity. An oxide similar to the emitter masking step is also used for this mask.

The double-diffused planar transistor features drastically reduced collector leakage currents and better uniformity of device characteristics. The double-diffused planar structure allows the transistor to come very close to the low theoretical limit for silicon junction leakage current.

The disadvantages are similar to those of the double-diffused transistor, in that the double-diffused planar type has a very high collector saturation resistance and relatively fragile junctions. The double-diffused planar transistor has a collector voltage 10 to 20 per cent lower than that of mesa types with the same junction design.

Triple-Diffused Transistors

The triple-diffused structure is essentially identical to the double-diffused design except that a third diffusion is performed. The third diffusion, on the opposite side of the silicon wafer, eliminates the major disadvantage of the double-diffused design—high saturation resistance. In the triple-diffused transistor the wafer of silicon is coated with a dopant, followed by a controlled diffusion. Fig. 15 shows a typical cross section of a triple-diffused transistor.

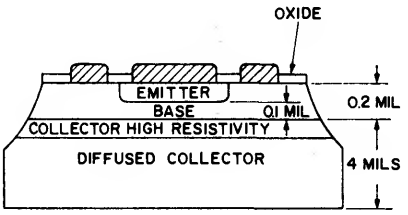

Fig. 15 - Triple-diffused transistor structure.

The principal advantage of the triple-diffused structure is that it has low saturation resistance which is of crucial importance in power transistor applications. The saturated switching speeds of this type of transistor are faster than those of the double-diffused design. Both advantages are a result of the thinning down of the high-resistivity section while the bulk of the collector is heavily doped and highly conductive. This technique, however, results in relatively fragile junctions.

Triple-Diffused Planar Transistors

The triple-diffused planar transistor, which is similar in structure to the triple-diffused transistor, incorporates a planar collector, as shown in Fig. 16. Critical cross sections of

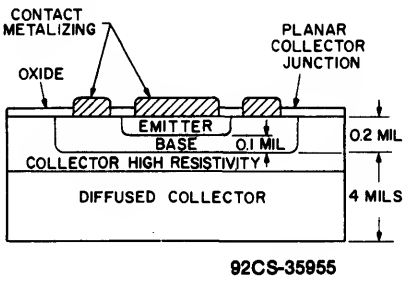

Fig. 16 - Triple-diffused planar transistor structure.

different stages of the manufacturing processes are shown in Fig. 17.

The principal advantages of the triple-diffused planar transistor are very low leakage

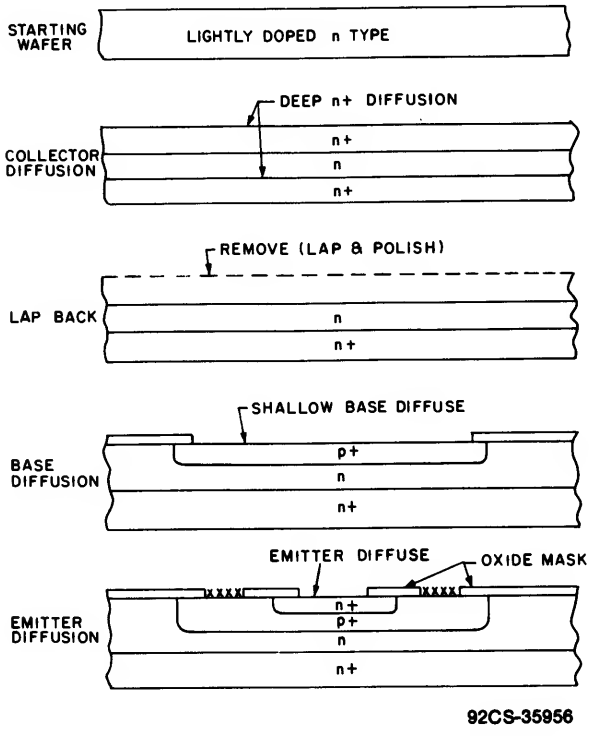

Fig. 17 - Processing steps in the manufacture of a triple-diffused planar transistor.

current, high-speed operation, and low saturation resistance. The main disadvantage is that the cost of manufacturing is higher than that of non-planar devices.

Double-Diffused Epitaxial Transistors

The double-diffused epitaxial structure is similar in appearance to the triple-diffused design, except that the diffused collector region is replaced by a heavily doped homogeneous layer referred to as the epitaxial substrate. Because of the difference in doping between the double-diffused epitaxial and triple-diffused structures, some improvements in switching speeds and saturation resistance can be realized. The double-diffused structure, however, has a somewhat poorer reverse "energy profile", so that its capability to withstand inductive or capacitive energy pulses is reduced.

Fig. 18 shows a cross section of a typical double-diffused epitaxial transistor, and Fig. 19 shows a planar version of the same kind of transistor.

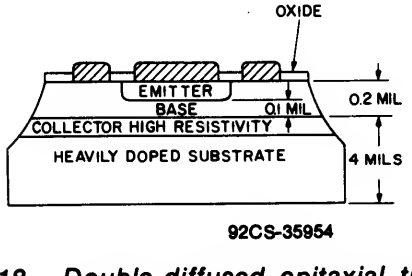

Fig. 18 - Double-diffused epitaxial transistor structure.

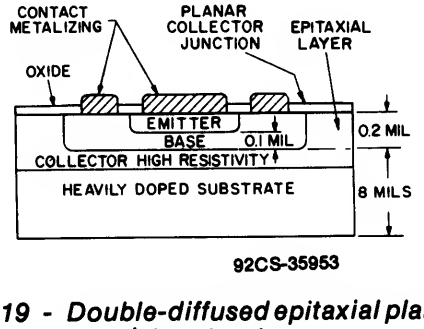

Fig. 19 - Double-diffused epitaxial planar transistor structure.

Epitaxial-Base Transistors

The epitaxial-base structure uses epitaxial layers in the actual formation of the base-collector junction. A single diffusion of the emitter completes this relatively simple design. A layer of impurity (opposite to the substrate impurity) is epitaxially grown on the highly doped substrate. An oxide masking and emitter diffusion into this epitaxial layer completes the construction. Fig. 20 shows a typical cross section of an epitaxial-base power transistor.

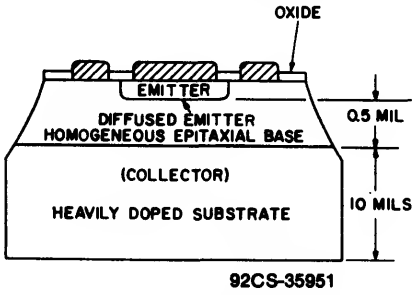

Fig. 20 - Epitaxial-base transistor structure.

The principal advantage of the epitaxial-base structure, compared to the double-diffused designs, is that it is electronically more rugged (able to withstand energy pulses) as a result of the wider and homogeneous base region. In comparison to the hometaxial structure, the epitaxial-base type has significantly higher frequency response and the ability to carry higher currents for an equivalent emitter area.

The disadvantage of the epitaxial-base design is that it is limited by low voltage ratings imposed by the constraint of the abrupt base-collector junction formed between the heavily doped collector substrate and the epitaxially deposited base layer. The low voltage rating also results from the thin base width necessary for adequate current gain which reduces voltage limits because of punch-through effects. The epitaxial-base transistor also suffers from moderate collector leakage-current levels resulting from the abrupt step junctions and mesa construction.

Multiple-Epitaxial-Base Transistors

The multiple-epitaxial-base structure is similar to the epitaxial-base transistor, but has the added feature of a high-resistivity epitaxial layer for the active collector region. The multiple epitaxial-base transistor is fabricated from a heavily doped silicon wafer on which alternate layers of p-n or n-p high-resistivity silicon are epitaxially grown to create a π - ν or a ν - π base-collector junction. An emitter area is then diffused into the structure. Fig. 21 shows the various stages in

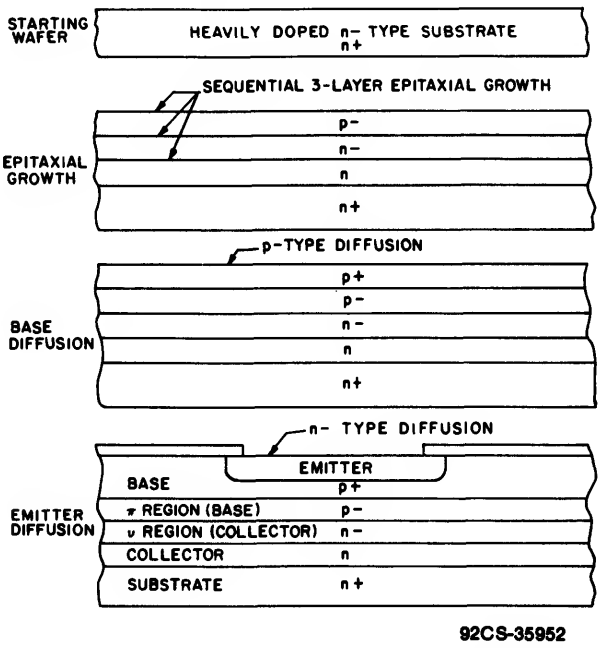

Fig. 21 - Processing steps in the manufacture of a multiple-epitaxial-base transistor.

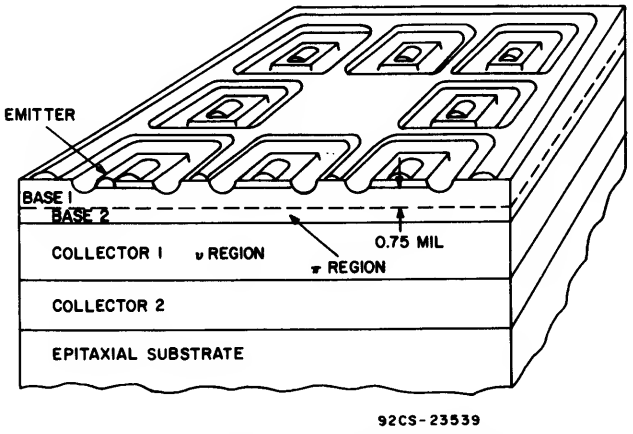

Fig. 22 - Multiple-epitaxial-base transistor structure.

the manufacture of the multiple-epitaxial-base transistor structure, and Fig. 22 shows a typical cross section of this type of device.

The principal advantage of the multiple-epitaxial-base structure is that it has high voltage ratings with good current carrying abilities and excellent power-handling capabilities at high voltages (second breakdown). The higher voltage ratings result because the transistor uses both the base and the collector regions to support the applied collector voltage. The good current-handling characteristic results from the fact that lower collector resistivity can be used for equivalent voltage ratings, as compared to double-diffused epitaxial designs. The lower collector resistivity also minimizes high-current fall-off effects that result from base widening. The excellent second breakdown characteristic results from the moderately wide base width and partial homogeneous base doping, which allows more charge-carrier fan-out (diffusion) and reduced current densities at the collector junction where heating effects predominate.

The principal disadvantage is that the cost of manufacturing the multiple epitaxial-base transistor is relatively high.

Multiple-Epitaxial Double-Diffused Transistors

The multiple epitaxial double-diffused structure is almost identical to the double-diffused epitaxial design, with the exception that multiple epitaxial layers are used in the collector region, instead of a single collector layer. The top collector layer is a thin, high-resistivity layer followed by one or more thin, but more heavily doped, layers. These more heavily doped layers are grown sequentially in an epitaxial reactor system onto a thick, heavily doped silicon substrate wafer. Fig. 23 shows the various stages in manufacture of the multiple epitaxial double-diffused structure, and Fig. 24 shows a typical cross section of the completed transistor.

The advantages of the multiple epitaxial double-diffused structure include those of the double-diffused epitaxial design (high speed and low saturation), as well as the significant advantages of higher collector-junction voltage

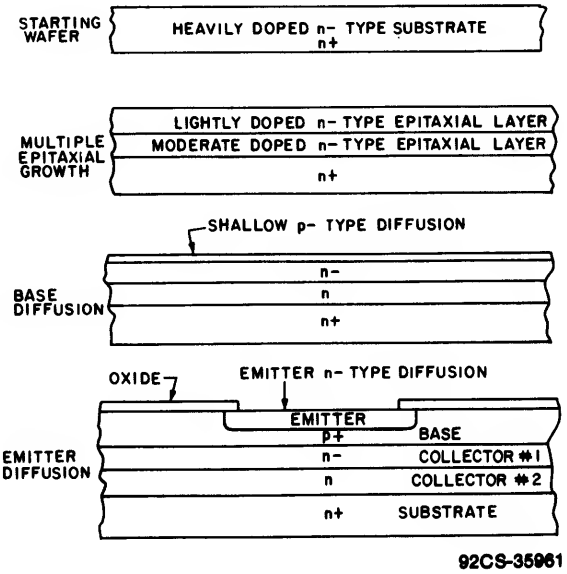

Fig. 23 - Processing steps in the manufacture of a multiple-epitaxial double-diffused transistor.

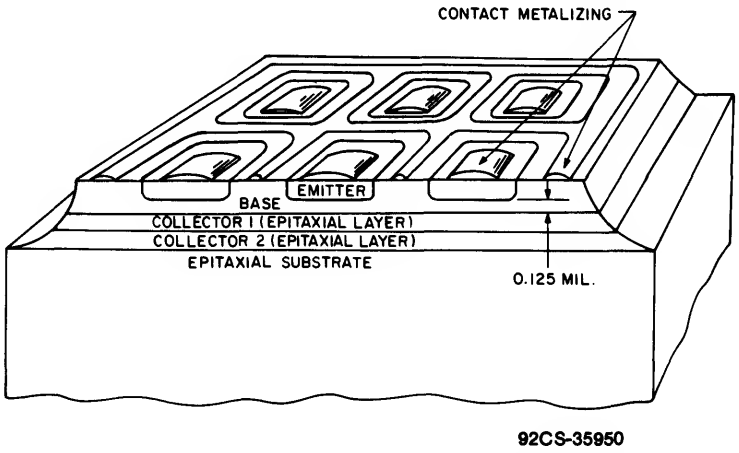

Fig. 24 - Multiple-epitaxial double-diffused transistor structure.

ratings, and increased electrical ruggedness. The electrical ruggedness (supplied by the additional collector layers) becomes even more of a factor during power switching with inductive loads in the 100-to-200-volt range where significant inductive energies (reverse second breakdown) may have to be handled by the transistor.

The disadvantages of the multiple epitaxial double-diffused transistor are the moderate-to-high cost per unit and the moderate leakage in the structure.

GEOMETRIES

The topography of a transistor is referred to as its geometry. This transistor geometry, in conjunction with its structure, establishes most of the fundamental transistor electrical, thermal, and economic properties. Proper geometric design of a transistor allows for many compromises, which may result in a variety of advantages and disadvantages from different structures.

The basic premise for most geometric designs for power transistors is to increase current handling per unit area of device. This condition results in lower-cost designs or, as in high-frequency transistors, higher-speed operation as a result of the smaller device areas.

Power transistor geometries have evolved from the very early inefficient "ring-dot" configurations to the present-day sophisticated "overlay" concepts. Fig. 25 shows some typical geometry milestones in this evolutionary cycle.

The early geometries were characterized by simple shapes, large dimensional tolerances,

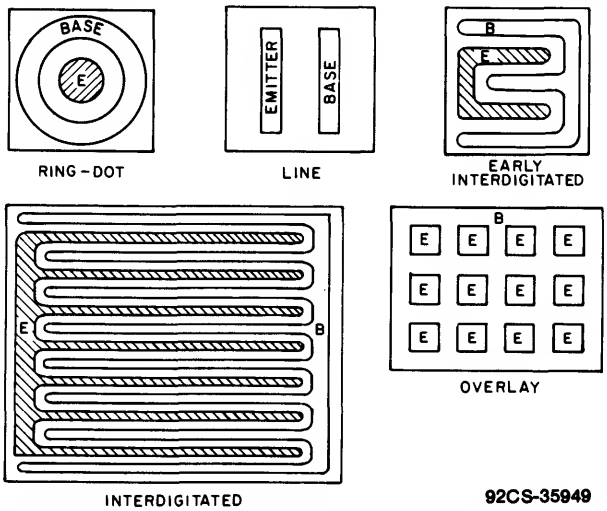

Fig. 25 - Typical geometries in the development of transistors.

and poor utilization of active regions. As the state of the art in fine-line mask making and wafer printing improved, the geometries became more involved, with much finer dimensions.

Certain device structures have constraints on how fine the emitter geometry can be made. Refinement of emitters is governed by the space needed for emitter and collector mesas and by the thickness of oxide masks needed for deep diffusion, as well as by other factors.

SPECIAL PROCESSING TECHNIQUES

Silicon power transistors are now taking on new dimensions in performance. New processing techniques including ion implanted, diffused junctions, polysilicon field shields, glass passivation, moated planar junctions, aluminum-titanium-nickel metallization, and high lifetime wafer processing are some of the advanced technologies that are responsible.

Neutron Doping

The voltage and current performance of a high-voltage transistor is critically dependent on the crystal resistivity in the n-type collector region of the device.

Conventional n-type float-zone crystal-growing techniques tend to produce large variations in doping levels due to the low distribution coefficient of the n-type dopant (phosphorous) and the varying thermal equilibrium conditions at the growth interface.

Phosphorous doping by thermal neutron transmutation is a doping technique in which a flux of thermal neutrons is irradiated on a high-resistivity, undoped single crystal to fractionally transmutate silicon into phosphorous.

The crystal is subsequently annealed to remove radiation-induced defects in the lattice. The technique is cost-effective at low doping levels below $\sim 1 \times 10^{14}/cm^3 (\rho > 50\ \Omega\ cm)$ producing wafers in production quantities with resistivity variations less than 10 per cent.

Ion Implantation

Control of base and collector doping profiles is also an important aspect of transistor processing. The use of ion implantation to achieve precise doping levels for the base and collector diffusion sources has eliminated critical high-temperature chemical-deposition processes, resulting in better yields and tighter parameter distributions. A schematic of a basic ion implant machine is shown in Fig. 26.

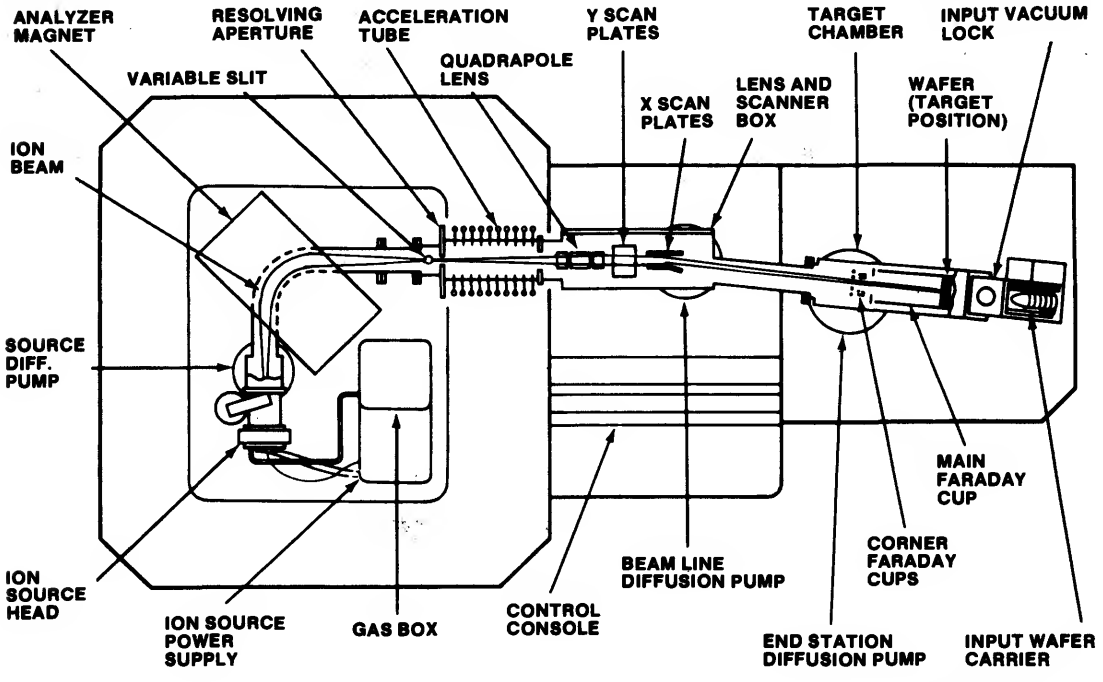

Fig. 26 - Basic ion implantation machine.

The machine provides simple electronic control of the incident beam of doping ions. Mass analysis is used to assure extreme purity of the ion beam. Doping accuracy is better than one per cent compared to about 10 per cent for typical chemical processes. Recently, high current machines have become commercially available, providing sufficient capability for most power device doping.

With the ion-implantation technique, atomic species are ionized, accelerated to high velocities under vacuum by the application of electrostatic fields, and directed against the surface of a target material where they penetrate and come to rest in a shallow layer below the surface.

Diffusion Process

The diffusion process developed for production of high-voltage transistors contains only two diffusion steps as shown in Fig. 27. The ion-implanted base and collector regions are diffused simultaneously from both sides of the wafer. This high-temperature (1300° C) process forms the basic high-voltage diode structure. The ion-implanted emitter, base-contact, and collector-contact regions are then diffused in a second short diffusion step at a moderate temperature (1200° C) producing the complete n-p-n transistor structure. Standard photolithographic and silicon dioxide masking techniques are used to restrict the diffusion to the desired regions.

Surface Electric-Field Control

Once the requirements are met for voltage breakdown capability in bulk silicon, special consideration of the termination of the junction with the silicon surface must be taken because the peak surface electric field that initiates avalanche breakdown is generally significantly lower than the corresponding bulk electric field. Several common methods of reducing surface fields are shown in Fig. 28. While no method is completely successful in eliminating the surface effect, each method is capable of surface breakdown voltage within 90-95 per cent of the bulk capability. For reasons described, the **planar depletion moat** was chosen as the best structure for a passivated high-voltage transistor.

The reverse-bevel technique, shown in Fig. 28(a), is used by most manufacturers of high-voltage transistors. Surface fields are reduced because the field is spread over a larger surface area due to the approximately 30° bevel. One drawback of the technique is that it requires a mechanical grinding step to produce an accurate taper, and mechanical processes are generally expensive in comparison with other semiconductor processes. Hard-glass passivation of the junction is not practical due to the position of the junction, and devices of this type are generally non-passivated. The reverse-bevel technique, however, is proven and has withstood the test of time both in volume production and in device application.

The **planar depletion moat** structure shown in Fig. 28(d) is an excellent method of high-voltage junction termination both from the standpoint of pellet area utilization and the ease of hard-glass passivation. The junction is located in a plane parallel to the top surface of the pellet several mils from the mesa-etch

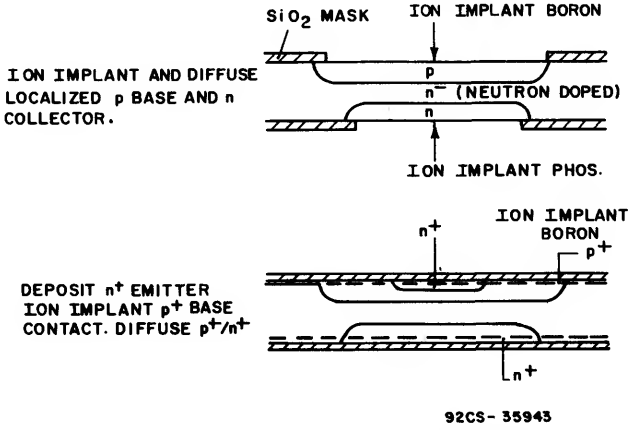

Fig. 27 - Simplified diffusion process.

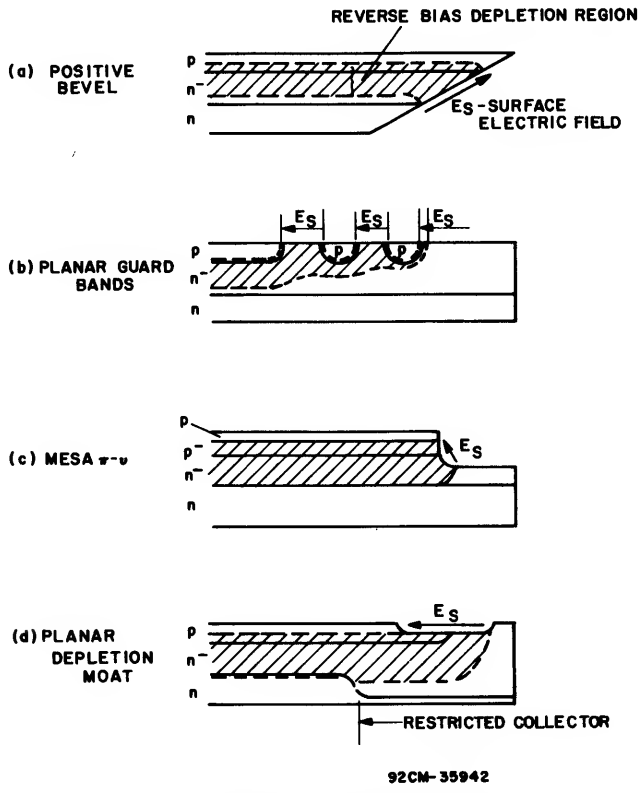

Fig. 28 - Common methods of reducing surface electric fields.

discontinuity. This arrangement minimizes the adverse effects of certain variables in the passivation process such as photoresist adherence, mechanical stresses in the passivation layers, and glass coverage. Near-theoretical breakdown can be achieved with proper etch-depth control.

Glass Passivation

The operating voltage of a solid-state device is generally limited by the surface breakdown voltage and the stability of the surface when the device is subjected to high voltage and high temperature. Bulk silicon can withstand an electric field in the order of 500 volts per mil before breakdown occurs; the surrounding medium and its interface, however, have much lower breakdown potentials. Even when arcing or breakdown of the surface does not occur, high electric fields can cause ionization of atoms or molecules on the surface and migration of ions along the surface.

Ion migration is actually a leakage current that, although of negligible magnitude, results in an accumulation of negative and positive static charges on the pellet surface. These static charges induce opposite-polarity mobile charges beneath the surface within the pellet body. It is the flow of these induced mobile charges within the body of the pellet, rather than the flow of charge on the pellet surface, that actually constitutes the leakage current which is detrimental to a device operated at high voltages and high temperatures. Glass passivation is used to assure maximum surface breakdown voltage and maximum surface stability. The glass protects the surface of the silicon pellet from breakdown or arcing and forms a barrier that prevents migration of ions to the silicon surface. Fig. 29 shows a cross section of a typical glass-passivated transistor pellet.

Sipos/Glass Passivation

In any high-voltage device, fringing electric fields external to the pellet are important in determining performance and reliability. Mobile ionic contaminants on the surface can play havoc with the electrical characteristics causing high leakage, unstable voltage break-

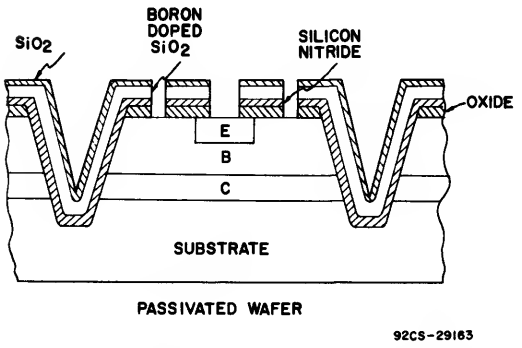

Fig. 29 - Glass-passivated transistor pellet.

down and, in severe cases, complete destruction of the device. This condition is especially true in a non-hermetic environment. To desensitize the junction from external effects, the silicon surface can be passivated with insulating or semi-insulating materials which bond well with the silicon and do not contain mobile contaminants which can be thermally activated at the device's operating temperature.

Passivation of the junction serves another important economic purpose. Because the passivated system hermetically seals the device in chip form, the hard-glass-passivated device can be tested, categorized, and inventoried at the pellet stage, reducing inventory carrying costs and enabling more effective response to varying market conditions.

A multilayer passivation system called SOGO was developed to meet the performance and reliability requirements of high-voltage devices. The basic components of the SOGO system are shown in Fig. 30. The primary passivation layer is a thin film of semi-insulating polycrystalline oxygen doped silicon (Sipos) which is formed by Low Pressure Chemical Vapor Deposition (LPCVD) through the reaction of nitrous oxide (N_2O) and silane (SiH_4).

The use of LPCVD primary passivant is also advantageous from the manufacturing standpoint. High throughput, excellent uniformity and reproducibility are realized with the LPCVD system.

Tri-Metal Metallization

The wide collector region and high lifetime result in large amounts of stored charge which tend to restrict switching performance of high-voltage devices. In order to achieve fast switching and minimize turn-off tails (which lead to high power dissipation in turn-off), RCA high-voltage, high-current transistors use a finely subdivided discrete emitter structure and employ a high-conductivity, solderable Al/Ti/Ni metallization system, shown in Fig. 31, on the emitter-base side of the device with metal-over-oxide capability to access the discrete emitters. In this metal system, a thick layer of aluminum is used to bond to the silicon and silicon dioxide and provide high lateral conductivity, minimizing voltage drops in the base and emitter metal which would tend to create current non-uniformities at high current injection levels. The titanium layer serves as a buffer region preventing the formation of brittle aluminum/nickel intermetallics during the metal alloying process. Solder contact is readily made to the nickel layer. On the collector side of the device a layer of nickel is deposited over a titanium layer to provide a high-conductivity surface for solder mounting to a heat sink. The metal layers are deposited in an electron-gun vacuum evaporator and metal definition is accomplished using photolithographic techniques. A single-step metal etch is employed for ease of manufacturing. This metal system combines the advantages of high conductivity, fine-line geometry, and metal over oxide capability of the aluminum metal system, with the advantages of a rugged nickel-lead solder mounting and clip bonding assembly process.

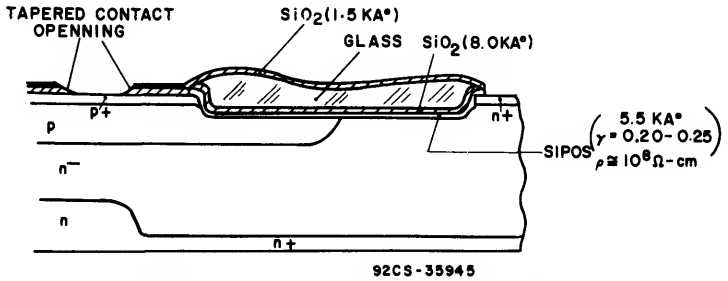

Fig. 30 - Sipos-Oxide-Glass-Oxide (SOGO) passivation system.

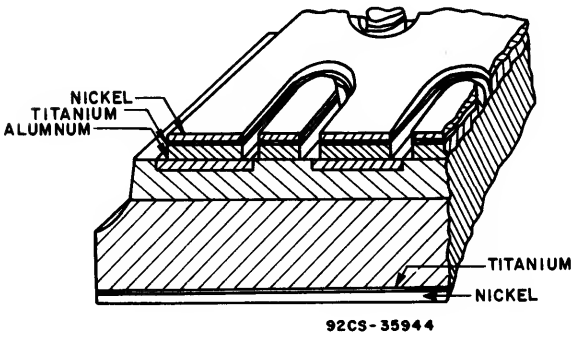

Fig. 31 - Cross section of transistor pellet employing high-conductivity metallization system.

RCA SwitchMax Power Transistors

Many of the special processing techniques described in the previous paragraphs are employed to advantage in the RCA "SwitchMax" series of power-switching transistors. These transistors employ a multiple-layer epitaxial, double-diffused collector structure that is specially designed for high-current, high-speed switching. They are fully characterized for switching applications in off-the-line switching power supplies, converters, and pulse-width-modulated switching regulators.

The RCA SwitchMax transistors feature high voltage capability, fast switching speeds, and high safe-operating-area (SOA) ratings; they are 100 per cent tested for the parameters essential to the design of power-switching circuits. Table II lists the RCA SwitchMax series together with important switching characteristics and voltage and current ratings. As indicated in the table, switching parameters are tested at elevated temperatures ($T_C \geq 100°C$), as well as at room temperature, to provide limit values necessary for worst-case design.

The fine-geometry emitter, together with minimum base and collector sheet resistivities compatible with voltage-breakdown requirements, assures excellent high-current and fast-switching capability. The low collector resistivity and carefully controlled layer thicknesses minimize the fall-off in gain at high currents that results from base-widening effects. A controlled-lifetime process used in the production of the SwitchMax pellets results in higher gain for a given base width and assures stable current gain during operation at elevated temperatures.

The ruggedness of the SwitchMax transistors is enhanced by careful design of the emitter periphery to assure low current density, use of wide base widths so that collector current is spread over more of the pellet area, a special emitter-pad design that provides "dynamic" emitter ballasting during switching, and graded n-type layers for collector ballasting.

The SwitchMax transistors employ the **high-conductivity trimetal metallization** system, previously shown in Fig. 31, that permits a designer to solder-mount pellets and chips for ruggedness and still retain a high-conductivity, fine-geometry metallization pattern. Potential weaknesses in the system are detected by infrared analyses, which enable establishment of optimum patterns to assure uniform base-current distribution over the entire transistor active area. The SwitchMax transistors employ a **unique, proprietary glass-passivation system** (similar to that shown earlier in Fig. 30) that assures low surface leakage, increased voltage capability, and improved high-temperature performance.