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AS POWER-SUPPLY SIZE AND PERFORMANCE DEMANDS INCREASE, SELECTING THE RIGHT SWITCHING DEVICES BECOMES MORE COMPLEX. A STRAIGHTFORWARD METHOD SIMPLIFIES THE SELECTION PROCESS, SPEEDS YOUR DEVELOPMENT, AND HELPS YOU TO OPTIMIZE YOUR DESIGN.

A simple guide to selecting power MOSFETs

Given the wide selection of MOSFETs available now and the shrinking real estate allotted for motherboard power supplies, it's increasingly important to use a dependable, consistent method for selecting the right MOSFET. Such a method can speed development cycles while optimizing application-specific designs.

PC-motherboard and power-supply designers, who frequently go through the power-MOSFET selection process, can benefit from an automated process that uses a spreadsheet. This common tool can significantly reduce the selection time while affording the designer an intimate, step-by-step look at the selection process. Compared with algorithmic programming languages, implementing a selection method in a spreadsheet provides for greater interaction, easy fine-tuning, and simple provisions for building and maintaining a parts database.

To limit the scope of this discussion, consider a MOSFET-selection method for the synchronous buck-converter topology, which suits dc/dc converters for PC motherboards and telecommunications applications. The search for the right MOSFET for a specific application involves minimizing the losses and understanding of how these losses are dependent on the switching frequency, current, duty cycle, and the switching rise and fall times. This information guides the selection tool development.

Once you choose a topology, you can base the MOSFET selection on its position in the circuit and a few device parameters, such as breakdown voltage, current-carrying capability, R_{ON}, and the R_{ON} temperature coefficient. The goal is to minimize conduction and switching and to choose a device with adequate thermal properties.

Examining a typical buck converter reveals how device requirements vary significantly depending on circuit position (**Figure 1**). This circuit takes power from a 12V source and provides an output voltage of 1.5V, resulting in a duty cycle D for Q_1 of 1.5/12=0.125 and 1−D for the synchronous rectifier Q_2. Switching losses dominate the power dissipation in Q_1, owing to its relatively small duty cycle compared with that of Q_2. Q_1's voltage excursion is the source voltage. Although Q_2 must also stand off the full supply voltage, at the beginning of its switching interval, the body diode clamps the filter inductor to ground, so Q_2's excursion is limited to a diode drop. The small duty cycle and large excursion put demands on Q_1's rise- and fall-time performance. Conduction losses, which are a function of R_{ON}, dominate Q_2's power dissipation. Minimizing this ohmic term requires a device with the lowest on-resistance to handle the load current based on cost expectations and efficiency requirements.

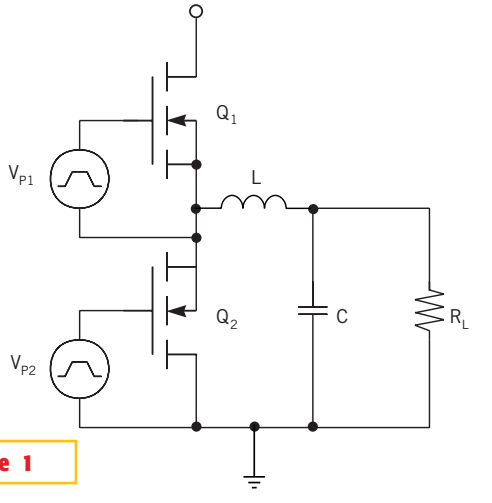

Figure 1

The buck-converter topology uses two n-channel MOSFETs. Q_1 is the switching or control MOSFET, and Q_2 is the synchronous rectifier. L and C comprise the output filter, and R_L is the load resistance.

The spreadsheet includes calculations of static and dynamic losses, the latter of which is the sum of switching and gate-drive losses. To facilitate the dynamic-loss calculations, you need to refer to representative waveforms (**Figure 2**). Prior to switching, the MOSFET's power dissipation derives from conduction losses. The area under the blue triangle depicts the dynamic loss during the switching transition time, which occurs twice per cycle. The total dynamic loss, therefore, is proportional to the switching frequency.

The conduction loss is proportional to the MOS device's on-state channel resistance:

$$P_C(Q_1) = I_{D1}^2 R_{ON1} D,$$

and

$$P_C(Q_2) = I_{D2}^2 R_{ON2}(1-D),$$

where I_D is the drain current, R_{ON} is the channel resistance at the manufacturer's specified nominal ambient temperature, and D is the duty cycle of Q_1.

Charging and discharging the gate capacitance contributes to the switching losses. This loss also depends on the switching frequency:

$$P_G = V_G^2 C_{GS} f,$$

where V_G is the gate-drive voltage, C_{GS} is the gate-source capacitance, and f is the switching frequency.

THE UPS AND DOWNS OF MOSFET SELECTION

The requirements for the control switch, Q_1, and the synchronous rectifier, Q_2, differ. Current, voltage, and power-dissipation ratings are key parameters that determine the suitability of a device for either position. Q_1's power dissipation is given by:

$$P(Q_1) = I_{RMS}^2 R_{ON1} D + f\left[Q_{G1} V_{G1} + \frac{1}{2}(t_r + t_f) I_{RMS} V_S\right]. \quad (1)$$

In **Equation 1**, the first term reflects the conduction loss, and the second term accounts for the dynamic and gate losses. I_{RMS} is the drain current; R_{ON} is the channel resistance; D is the duty cycle; f is the switching frequency; t_r and t_f are the switching rise and fall times, respectively; and V_S is the input source voltage.

Similarly, Q_2's power dissipation is given by:

$$P(Q_2) = I_{RMS}^2 R_{ON2}(1-D) + f\left[Q_{G2} V_{G2} + \frac{1}{2}(t_r + t_f) I_{RMS} V_D\right].$$

As in the previous case, the first term is the conduction loss, and the second term is the switching loss. Note that D is Q_1's duty cycle. The last term, V_D, is the body-diode forward voltage. You can reduce this loss and improve the circuit's switching dynamics by connecting a Schottky diode across Q_2.

With the power dissipation calculated for the two devices, you can calculate the temperature rise from the thermal resistances of the package and heat sink as:

$$\Delta_T = R_\Theta P, \quad (2)$$

where Δ_T is the temperature rise over ambient in degrees Celsius, P is the device's total power dissipation, and R_Θ is the total thermal resistance taken as the sum of the junction-to-case resistance of the FET's package and the heat-sink thermal resistance. There's also a small case-to-heat-sink term, which is often negligible—particularly when you use modern thermal interface materials. The heat sink can be an explicit mechanical device or a pc-board trace with adequate surface area (**Figure 3**).

Although these equations are simple enough to allow a quick check of a given MOSFET's suitability in a specific application, the strong dependency of R_{ON} on the junction temperature somewhat complicates the calculation. A temperature rise of about 80°C causes a 40% increase in the value of R_{ON}. You need to include this behavior in the analysis of the conduction losses to calculate the actual temperature rise.

If you include the R_{ON}'s temperature coefficient in **Equation 1**, you get:

$$P(Q_1) = I_{RMS}^2 R_{ON1}(1+\delta\Delta_T) D + P_D(Q_1),$$

and

$$P(Q_2) = I_{RMS}^2 R_{ON1}(1+\delta\Delta_T)(1-D) + P_D(Q_2),$$

where δ is the temperature coefficient of R_{ON} in °C^{-1}, and P_D is the dynamic loss term, which is independent of R_{ON}.

When you substitute these variables into **Equation 2** and solve for the devices' Δ_Ts, you find that:

$$\Delta_T(Q_1) = \frac{R_\Theta[I_{RMS}^2 R_{ON1} D + P_D(Q_1)]}{1 - R_\Theta I_{RMS}^2 \delta R_{ON1} D}, \quad (3)$$

and

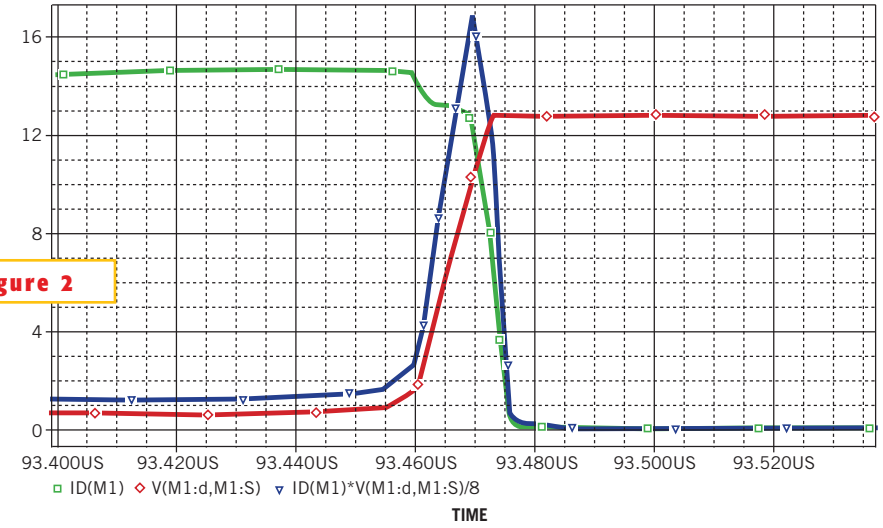

Figure 2

Switching Q_1 results in characteristic waveforms for I_D (green) and V_{DS} (red). The product of these two waveforms gives the instantaneous power dissipation, P_D, (blue).

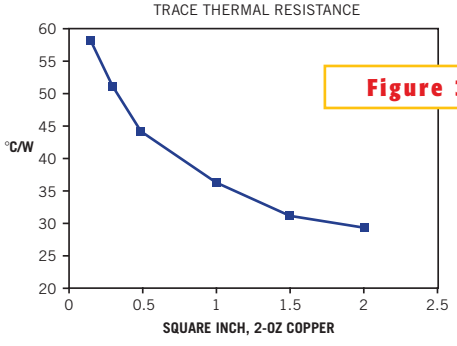

Figure 3

You can express the thermal resistance of a 2-oz copper pc-board trace in degrees Celsius per watt, as a function of the trace area. This thickness of copper is typical of most pc boards.

$$\Delta_T(Q_2) = \frac{R_\Theta[I_{RMS}^2 R_{ON1}(1-D) + P_D(Q_2)]}{1 - R_\Theta I_{RMS}^2 \delta R_{ON1}(1-D)}. \quad (4)$$

Equation 4 provides the junction-temperature rise as a function of the load current and a specific set of MOSFET parameters. A junction temperature of about 105°C is usually a good first cut for commercial applications.

CALCULATING THE DYNAMIC LOSSES

The rise and fall times depend on characteristics of both the MOSFET and your gate-drive circuit. The gate charge, Q_G, is the product of the gate capacitance and the drive voltage, usually given at 4.5V. The gate capacitance combines with the gate drive's output impedance to limit the gate rise and fall times:

$$V_G = V_P\left(1 - e^{\frac{-t}{R_P C_G}}\right),$$

$$\Delta t = -R_P C_G \ln\left(1 - \frac{V_G}{V_P}\right),$$

and

$$t_r = t_f = -R_P \frac{Q_G}{V_P} \ln\left(1 - \frac{V_G}{V_P}\right). \quad (5)$$

In these **equations**, V_G is the equivalent gate voltage, V_P is the gate-drive pulse amplitude, R_P is the gate-drive output impedance, and C_G is the gate capacitance.

The MOSFET is fully on when V_G reaches 99% of V_P. If you substitute this relationship back into **Equation 5**, the rise and fall times reduce to:

$$t_r = t_f \approx 4.6 R_P \frac{Q_G}{V_P}.$$

You can now calculate the total dynamic loss for each device:

$$P_D(Q_1) = f\left[Q_{G1} V_{G1} + \frac{1}{2}(t_r + t_f) I_{RMS} V_S\right],$$

and

$$P_D(Q_2) = f\left[Q_{G2} V_{G2} + \frac{1}{2}(t_r + t_f) I_{RMS} V_D\right],$$

where V_G is the gate drive for the referenced device.

COMPLETING THE DESIGN

Determine the thermal resistance of the heat sink from the manufacturer's data sheet or from the dimensions of the pc-board trace. **Figure 3** shows the pc-board-trace thermal resistance of a single-layer pc board with 2-oz copper, versus a square copper area with the MOSFET located in its center. Depending on the available pc-board area, the copper can act as a heat sink for the MOSFET. It is worth noting that for small devices, increasing the area beyond the 2 square inches will not appreciably lower the thermal resistance.

In a spreadsheet, compile a database of MOSFETs suitable for your application. For the synchronous rectifier, Q_2, the MOSFET must meet the voltage and current requirements of the application. It must also have a sufficiently low R_{ON}, so that the conduction loss is small enough to meet the efficiency target. For this MOSFET, the gate charge plays a secondary role in power dissipation.

For the control device, Q_1, the dynamic or switching losses are the predominant factor, and conduction losses play a secondary role. The MOSFET should meet the voltage and current specification with as low a gate charge as possible to keep the dynamic losses small. Secondarily, seek a device with a moderate R_{ON}.

Solve **equations 3** and **4** for the temperature rise for all the MOSFETs in the database. Then you can select the MOSFET that meets your temperature-rise, package, and price requirements. A spreadsheet sheet that solves **equations 3** and **4** for a selection of MOSFETs allows the simultaneous evaluation of several MOSFETs. By using a spreadsheet this way, you can perform a "what-if" analysis to select the optimum MOSFETs for the application. You can adapt this basic method to other topologies so long as you've gained an understanding of the conduction and switching-loss requirements for each device in your design.□

AUTHOR'S BIOGRAPHY

Alan Elbanhawy is senior staff engineer at Fairchild Semiconductor International. He has more than 30 years experience in power-supply design and R&D management, covering aerospace, military, commercial, and industrial applications. He holds a bachelor of science in electrical engineering.